Multi-Rate Serial Digital Interface Physical Layer IP Core

User's Guide

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Introduction

Serial Digital Interface (SDI) is the most popular raw video link standard used in television broadcast studios and video production facilities. Field Programmable Gate Arrays (FPGAs) with SDI interface capability can be used for acquisition, mixing, storage, editing, processing and format conversion applications. Simpler applications use FPGAs to acquire SDI data from one or more standard definition (SD) or high definition (HD) sources, perform simple processing and retransmit the video data in SDI format. Such applications require an SDI physical layer (PHY) interface and some basic processing blocks such as a color space converter and frame buffer. In more complex applications, the acquired video receives additional processing, such as video format conversion, filtering, scaling, graphics mixing and picture-in-picture display. FPGA devices can also be used as a bridge between SDI video sources and backplane protocols such as PCI Express or Ethernet, with or without any additional video processing.

In an FPGA-based SDI solution, the physical interface portion is often the most challenging part of the solution. This is because the PHY layer includes several device-dependent components such as high speed I/Os (inputs/outputs), serializer/deserializer (SERDES), clock/data recovery, word alignment and timing signal detection logic. Video processing, on the other hand, is algorithmic and is usually achieved using proprietary algorithms developed by in-house teams. The Lattice Multi-Rate SDI PHY Intellectual Property (IP) Core is a complete SDI PHY interface that connects to the high-speed SDI serial data on one side and the formatted parallel data on the other side. It enables faster development of applications for processing, storing and bridging SDI video data. It comprises the high-speed serial I/Os, SERDES, SDI encoder/decoder, word alignment logic, CRC detection and checking logic and rate detection logic.

The interface standards and source formats for SDI are specified in several documents published by the Society of Motion Picture and Television Engineers (SMPTE). The SMPTE standards supported by this IP core are the following:

- **Interface:** SMPTE 259M-2006 [1] (SD) and SMPTE 292M-1998 [2] (HD)
- **SD Source Formats:** SMPTE 125M [3] and SMPTE 267M [4] (13.5 MHz only)
- **HD Source Formats:** SMPTE 260M [5], SMPTE 274M [6], SMPTE 295M [7] and SMPTE 296M [8]

The IP core can automatically scan and lock on to any of the supported video standards and formats. Receiving multiple standards is achieved with the help of an external clock generator that provides SD (27 MHz) or HD (148.5 MHz) rate clocks upon request from the IP core.

Features

- Support for dynamic multi-rate SD-SDI/HD-SDI (SMPTE 259[1] and SMPTE 292[2]) interfaces
- Support for automatic Rx (receive) rate detection and dynamic Tx (transmit) rate selection
- Built-in SERDES programming for multi-rate support
- Support for multiple SD source formats: SMPTE 125M [3] and SMPTE 267M [4] (13.5 MHz only)
- Support for multiple HD source formats: SMPTE 260M [5], SMPTE 274M [6], SMPTE 295M [7] and SMPTE 296M [8]
- Word alignment and timing reference sequence (TRS) detection
- Field vertical blanking (vblank) and horizontal blanking (hblank) identification
- CRC computation, error checking and insertion for HD
- Line number (LN) decoding and encoding for HD

Interface Diagrams

The top-level interface differs largely between configurations where the SERDES is contained inside the IP core and where it exists outside the IP core. The top-level interface diagram for configurations when SERDES is con-

tained inside the IP core and outside the IP core are shown in Figures 1 and 2, respectively. A brief description of the signals is given in Table 1. Note that not all the I/O ports are available for a chosen configuration.

Figure 1. Top-Level Interface for SERDES Inside the IP Core

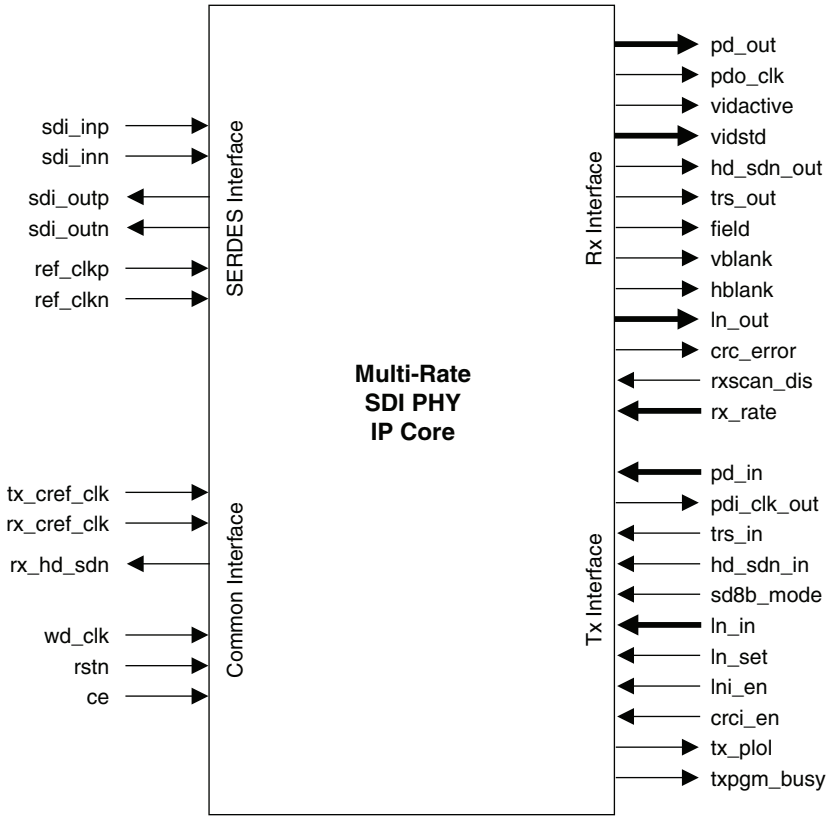
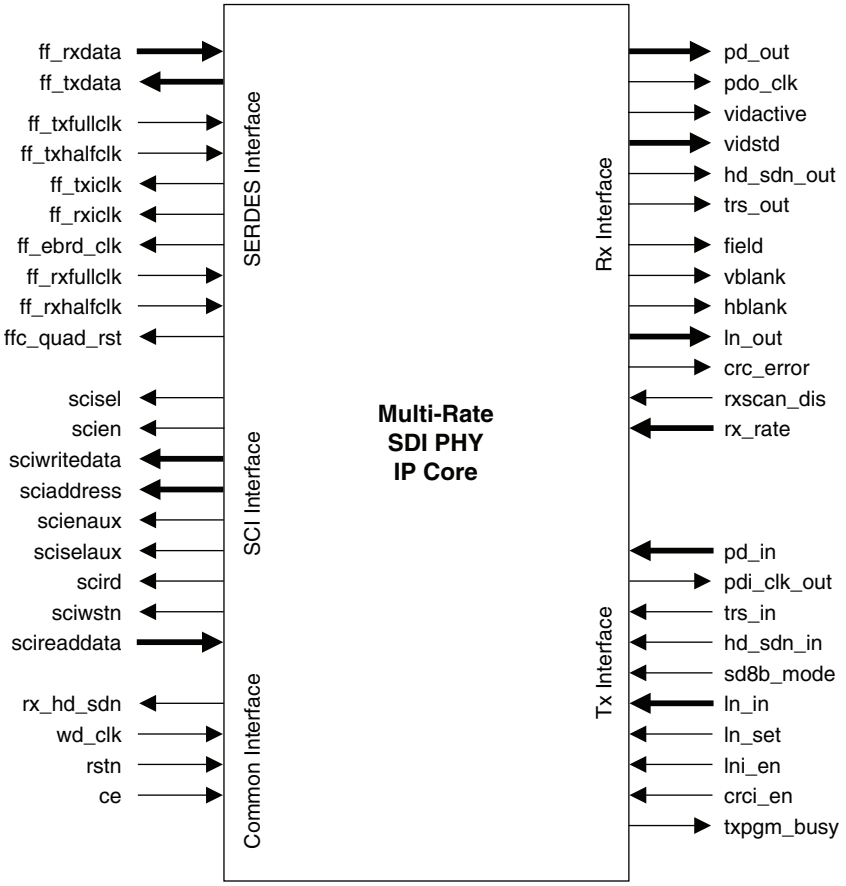


Figure 2. Top-Level Interface for SERDES Outside the IP Core



Video Interface and Source Format Support

This section describes the video interfaces and source formats supported by the Multi-Rate SDI PHY IP Core.

This IP core supports SMPTE 259 and SMPTE 292 interface standards. SMPTE 259 standard is applicable to 4:2:2 video streams defined by SMPTE 125M and SMPTE 267M. These source formats are briefly described below.

1. **SMPTE 125M**: System M- 525 lines and 60 fields based on ITU-R BT.601. The video is transmitted in the form of one luminance (Y) and two color-difference components (scaled versions of R-Y and B-Y). It follows a 4:2:2 family level of ITU-R BT.601 with a nominal luminance sampling at 13.5 MHz allowing for both 8-bit and 10-bit data types.

2. **SMPTE 267M**: System M- 525 lines and 59.94 fields, wide screen, 16x9 aspect ratio, based on ITU-R BT.601. The video is transmitted in the form of one luminance (Y) and two color-difference components (scaled versions of R-Y and B-Y). It follows a 4:2:2 family level of ITU-R BT.601 with a nominal luminance sampling at 13.5 MHz or 18 MHz, allowing for both 8-bit and 10-bit data types.

This IP core supports all of SMPTE 125M and only the 13.5 MHz version of SMPTE 267M.

SMPTE 292 defines a serial data rate of 1.485 Gbps and 1.485/M Gbps, where M=1.001. This interface standard supports four source formats: SMPTE 260M, SMPTE 295M, SMPTE 274M and SMPTE 296M. The parameters for these source formats are given in Appendix A. The IP core works with all these source formats.

Functional Description

This section describes the functionality of the Multi-Rate SDI PHY IP Core.

The top-level view of the IP core is shown in Figure 3.

Figure 3. Top-Level View, Multi-Rate SDI PHY IP Core

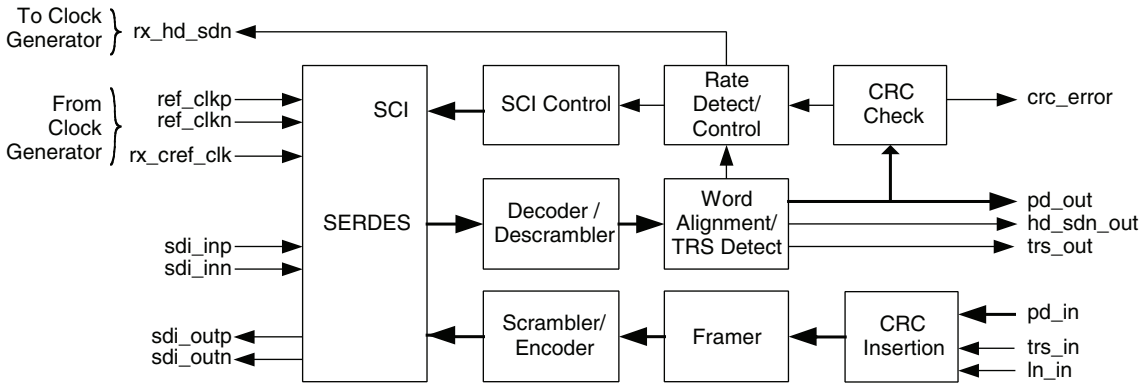


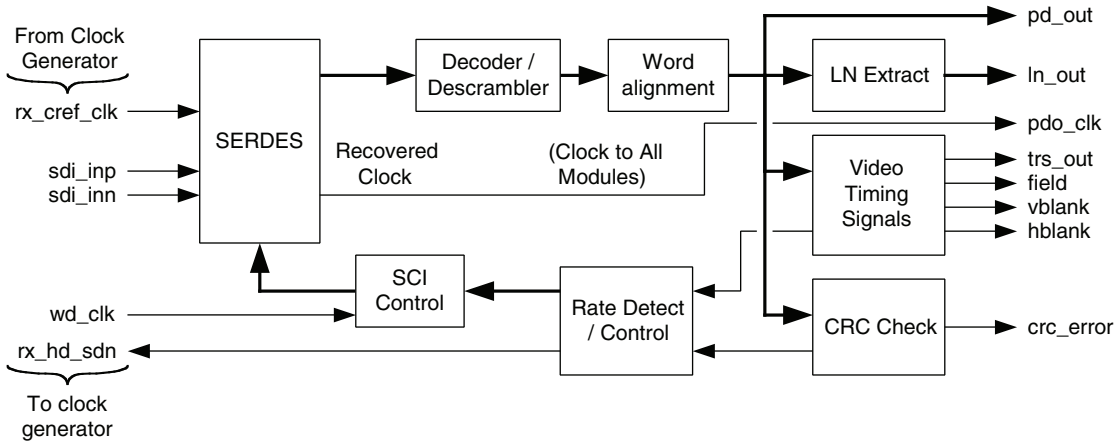
Figure 3 shows the IP core with SERDES instantiated inside. The receive and transmit logic blocks are shown to the right of the SERDES in the top and bottom halves, respectively. It is usually easier to generate and use the IP core with integrated SERDES. The parallel data busses, as well as a host of other signals to and from SERDES, come connected in the IP core. The IP GUI (graphical user interface) allows the user to select the channel number and reference clock source. However, if it is desired to exercise full control over the way SERDES is used in the application, the IP core can be generated without SERDES in it and then connected to SERDES separately.

The Multi-Rate SDI PHY IP Core is capable of receiving any of the video formats specified in the SMPTE 259 and SMPTE 292 interface standards without any manual intervention. The receiver is designed to dynamically support all three video stream rates: SD video at 270 Mbps, HD full frame rate video at 1.485 Gbps and HD fractional frame rate video at 1.4835 Gbps. The multi-rate receiver cyclically scans for each of the video rates until it identifies and locks to the incoming video data. To scan for a video rate, the IP core programs the SERDES and the external reference clock source for that rate and checks for a valid and error free video. If no video is received, or if there are multiple errors in the received data, the receiver goes on to scan for the next rate. The scanning process continues until the receiver "locks" to the incoming video (that is, when the video data reception is valid and error free for a few lines of video data). The receiver programs the SERDES operational frequency band through the SERDES Client Interface (SCI) and issues a clock request command to the external clock generator to switch to the corresponding clock. LatticeECP2M™ SERDES can reliably receive both 1.485 Gbps and 1.4835 Gbps data using any one of the receiver reference clocks (e.g., a 10x reference clock rate of 148.5 MHz). Therefore, the receive reference clock needs to be changed only between 27 MHz and 148.5 MHz for the supported video standards. A detailed description of the multi-rate receiver is given below.

Receiver

A high-level block diagram of the multi-rate SDI receiver is shown in Figure 4. The receive-side logic comprises the SERDES, decoder/descrambler, word alignment, LN extract, TRS detect, CRC extract/check, rate detect/control and SCI control blocks. A description of each of these blocks is given below.

Figure 4. Multi-Rate SDI Receiver, High-Level Block Diagram



SERDES

The LatticeECP2M SERDES is either generated as part of the IP core or separately instantiated and connected to the IP core, depending on the user's choice. The SERDES receiver requires a reference clock that is equal to one-tenth or one-twentieth of the data rate, depending on how it is configured. Refer to Table 1 for the actual data rates and reference clock rates for the supported SD and HD rates. For multi-rate operation, a 10x division factor should be used for both the reference clocks. The reference clock ports can be selected to be the differential inputs (`ref_clkp` and `ref_clkn`) of the SERDES auxiliary channel or the FPGA core reference clock port (`rx_cref_clk`). The IP core assumes that the appropriate reference clock is fed to the SERDES receiver in response to the request from the IP core. It should also be noted that the SERDES receiver is able to receive both the integer frame rate (1.485 Gbps) video as well as fractional frame rate (1.4835 Gbps) video with any one of the HD reference clocks given in the table.

Table 1. Receiver Reference Clocks for Different Video Rates

Standard	Serial Data Rate	Reference Clock	Division Factor
SD	270 Mbps	27 MHz	10x
HD - Integer frame rate	1.485 Gbps	148.5 MHz 74.25 MHz	10x 20x
HD - Fractional frame rate	1.4835 Gbps	148.35 MHz 74.175 MHz	10x 20x

Decoder/Descrambler

Both SMPTE 259 and SMPTE 292 standards define the same scrambling and encoding methods. The polynomials used are given in the Scrambler section of this document. The decoder/descrambler is implemented in the 10-bit or 20-bit parallel path. The input data is first decoded to NRZ and then descrambled following an essentially reverse process of encoding and scrambling operations.

Word Alignment

The deserialized word from the SERDES may not have correctly aligned bit boundaries. The word alignment block determines the degree of misalignment (offset) by looking for the special TRS sequences in the data. TRS is the unique sequence, $3FF_h$, 000_h, 000_h, in a video stream that marks either the end of active video (EAV) or the start of active video (SAV) time instants. Once the offset is determined, the words are realigned using the offset value.

LN Extract

This block is used for HD contents only. In HD frames, the line number is encoded as a two-word sequence and inserted after the XYZ word of the EAV sequence. This block decodes the line number from the LN double words and gives out the line number value on the ports.

Video Timing Signals
Once a TRS is detected during the word alignment processes, the XYZ word following the TRS is decoded by this block. From the XYZ word, the video timing signals field, hblank (horizontal blanking) and vblank (vertical blanking) are determined. XYZ word is also used to determine whether the TRS corresponds to an EAV or a SAV instant.

CRC Check
CRC checking is implemented for HD video streams only. In HD source formats, there are two CRC words per line that contain the CRC value for the previous line. The CRC checker computes the CRC for each line, compares with the received CRC and flags an error if there is a mismatch.

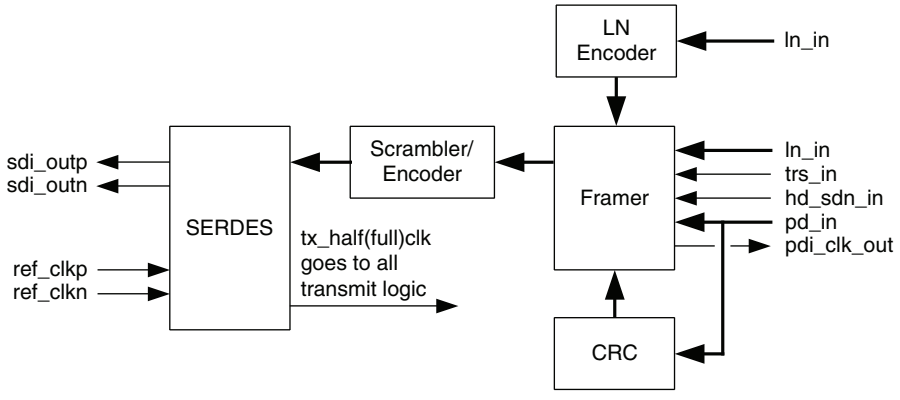
Rate Detect/Select
This module is the heart of the Multi-Rate SDI receiver infrastructure. Rate detection is the process of determining the interface standard and source format of the incoming video stream. Rate detection is done by alternatively setting the receiver in SD and HD modes and checking if the incoming stream matches the set rate. As mentioned earlier, LatticeECP2M SERDES is able to receive both integer and fractional frame rate data using either of the reference clocks for the receiver. Therefore, it is only necessary to apply one of the HD reference clocks to receive any of the HD standards. The Rate Detect module first sets the SERDES frequency band to one of the rates (SD or HD) and requests the corresponding reference clock from the external clock source through the signal rx_hd_sdn. It is assumed that the external clock source immediately responds with the correct clock on rx_cref_clk or ref_clkp/n ports. After the SERDES starts receiving stable data, the timing errors from the TRS detect module and CRC errors are used to determine if the received video corresponds to any of the supported formats. If the incoming video corresponds to one of the supported source formats, the receiver remains locked to this rate. If there are several timing or CRC errors, it indicates that the receiver setting is not conforming to the incoming video rate. The rate detect/select module then sets the receiver for the other rate by programming the SERDES and issuing a command to the external clock source.

The video stream is considered to match the selected clock when the TRS (timing reference signals, EAV and SAV) come in at a specified frequency and the line-based CRC error is within a threshold.

Transmitter

The transmitter supports multi-rate operation catering to most source formats in SMPTE 259 and SMPTE 292. The transmit rate is set through an input port. The transmitter and receiver are independent of each other and can be used for independent video streams. However, when the transmit or receive rate is changed, a quad reset is applied to the SERDES, affecting both the transmitter and the receiver. A high-level block diagram of the transmitter is shown in Figure 5.

Figure 5. Multi-Rate SDI Transmitter, High-Level Block Diagram



The data input to the transmitter is the total video content, including active video, blanking, ANC (ancillary), and TRS words. The CRC and line number words for HD can be used directly from the parallel data input or can be computed by the core and inserted at appropriate places. The transmitter comprises the following logical modules: CRC, Framer, Scrambler/Encoder and SERDES. A brief description of each of these modules is given below.

CRC
The CRC is an optional module that is added if the CRC option is enabled through the IP core GUI. The CRC is computed for the entire active line and the encoded CRC words are embedded at the appropriate places in the next line. Line-based CRC is supported only for HD standards (i.e., when the input `hd_sdn_in` is high). The CRC is computed using the following polynomial equation:

$$CRC\ (X) = X^{18} + X^5 + X^4 + 1$$

LN Encoder
The LN Encoder converts the raw line number value from the input port to two LN words for insertion in the video stream. This module is used only for HD inputs.

Framer
The framer formats the raw data from the `pd_in` input by adding the CRC and line number words at appropriate places. This module is used only for HD inputs.

Scrambler/Encoder
This module performs scrambling and NRZI encoding per the requirements set forth in SMPTE 259 and SPTE 292 standards. The scrambler implements the following equation:

$$G1(x) = x^9 + x^4 + 1$$

The NRZI encoder is defined by the following equation:

$$G2(x) = x + 1$$

SERDES
SERDES is configured for 10-bit parallel output for SD video and 20-bit parallel output for HD video rates. Since this configuration is dynamic, 20 bits are physically available from SERDES. For SD video, only the most significant 10 bits are used and the rest are ignored. The reference clock for the transmit PLL is recommended to be supplied through the auxiliary channel differential reference clock inputs for better jitter performance. The transmit PLL reference clock coming out from the SERDES (`ff_txhalfclk` or `ff_txfullclk`) is used to clock the transmit-side logic. This clock is also provided by the IP core for use as data input.

Parameter Descriptions

The user-configurable parameters for the Multi-Rate SDI PHY IP Core are set from the IP core GUI. GUI dialog boxes for SERDES both inside and outside the IP core are shown in Figures 6 and 7, respectively. Table 2 describes the parameter options available through the IP core GUI.

Figure 6. Multi-Rate SDI PHY IP GUI for SERDES Inside the IP Core

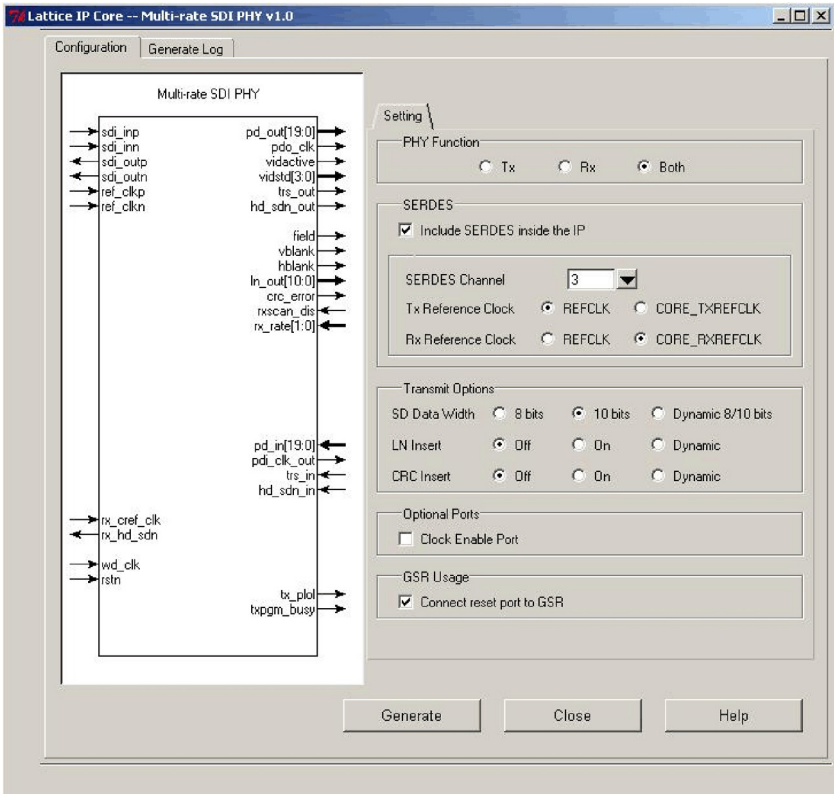


Figure 7. Multi-Rate SDI PHY IP GUI for SERDES Outside the IP Core

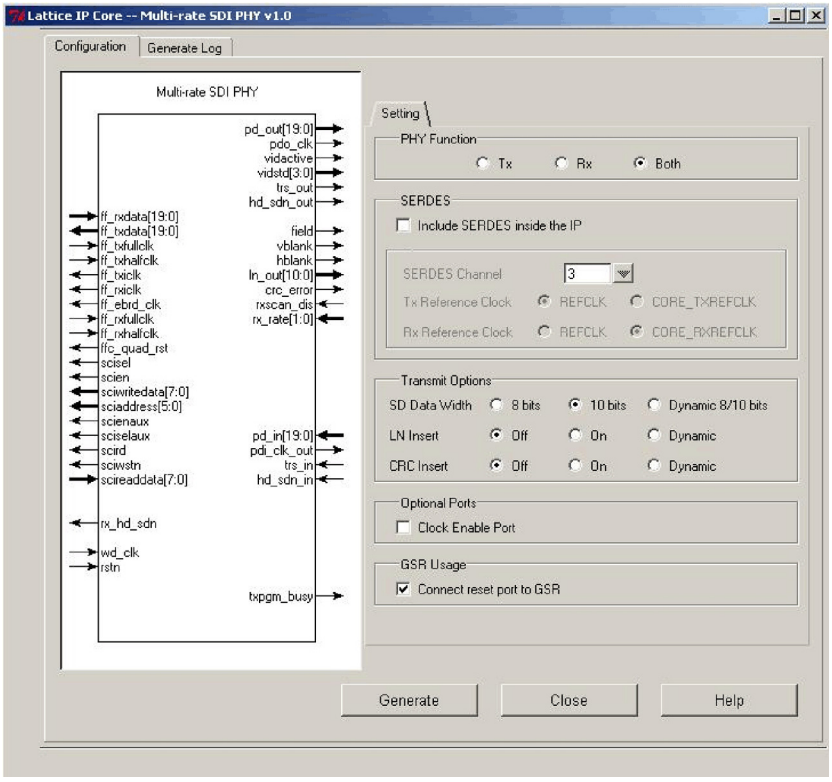


Table 2. Parameter Specifications for the Multi-Rate SDI PHY IP Core

Name	Description	Range/Options	Default
General			
PHY function	Configures the IP core for Tx, Rx or both Tx and Rx functionalities.	{Tx, Rx, Both}	Both
SERDES			
Include SERDES	Configures the SERDES either inside or outside the IP core.	{Yes, No}	Yes
SERDES channel	If SERDES is inside the IP core, this parameter specifies which SERDES channel is to be used.	{0,1,2 or 3}	3
Tx Reference Clock	Tx reference clock selection. The options are differential clock to the SERDES auxiliary channel (REFCLK) and core reference clock from the FPGA fabric (CORE_TXREFCLK). For better jitter performance, the REFCLK option is recommended.	{REFCLK, CORE_TXREFCLK}	REFCLK
Rx Reference Clock	Rx reference clock selection. The options are differential clock to the SERDES auxiliary channel (REFCLK) and core reference clock from the FPGA fabric (CORE_RXREFCLK). Since the reference clock does not largely affect the jitter tolerance, either of the options can be used.	{REFCLK, CORE_RXREFCLK}	CORE_RX REFCLK
Transmit Options			
SD Data Width	Configures the user data width for SD standard video. If this is 10 bits, the data is used directly. If it is 8 bits, the user data drives the most significant 8 bits of the internal data bus and the least significant 2 bits are filled with zeros by the IP core. When the input 8 bits are all ones, then the least significant bits are filled with ones. If configured as dynamic, the 8-bit or 10-bit mode is decided by the input signal sd8b_mode.	{8 bits, 10 bits, dynamic 8/10 bits}	10 bits
LN Insert	Specifies whether the line number information is encoded and inserted in the Tx data. If LN insertion is selected, the core reads the raw line number value from the input port ln_in, encodes to LN words and inserts them at appropriate locations. This is meaningful for HD modes only. If "Dynamic" is selected, the line number insertion or bypass is based on the value of the input signal lni_en. LN words are inserted only when lni_en is high during the time when LN0 and LN1 are placed at pd_in.	{Off, On, Dynamic},	Off
CRC Insert	If this is selected, the core computes the CRC of the incoming line and inserts the CRC information at appropriate places in the line. If the value is "Dynamic", CRC is inserted only when crci_en is high during the time when CR0 and CR1 are placed at the parallel input pd_in. The CRC options do not affect the SD modes.	{Off, On, Dynamic}	Off
Optional Port			
ce	Configures if a clock enable port is required in the IP core. This option must be selected only if required, as the clock enable port increases the resource utilization of the IP core.	{Yes, No}	No
GSR Usage			
Connect reset port to GSR	If this option is checked, the GSR is instantiated and used to route the IP core's rstn input. Using GSR improves the utilization and performance of the IP core. However, if GSR is used, an active input at rstn will reset most of the FPGA components as well. This option must be checked to enable the hardware evaluation capability for this IP core.	{Yes, No}	Yes

Configuring the Multi-Rate SDI PHY IP Core

PHY Function

The IP GUI allows the selection of either receive or transmit or both receive and transmit functionality for the IP core. Even if both functions are available, the receive and transmit logic are totally independent. The transmit and receive rates, however, may be limited by the reference clock and banding requirements imposed by the SERDES quad.

SERDES Options

The SERDES can be inside or outside the IP core. If SERDES is included inside the IP core, the generated IP core instantiates the SERDES with proper settings and connects most of the SERDES I/O ports internally making it easier to use. Advanced users may choose not to include the SERDES inside the IP core. In this case, the SERDES needs to be generated separately from the IPexpress™ GUI and properly connected to the IP core. The SERDES must be generated with the SCI option enabled. The SCI ports of the SERDES must be connected to the corresponding ports in the IP core for proper operation of the IP core. Please refer to the LatticeECP2/M Family Data Sheet or Lattice technical note TN1124, *LatticeECP2/M SERDES/PCS Usage Guide* for details on the usage of SERDES. The ports in the IP core for connecting with SERDES have the same names as the corresponding SERDES ports for easy connectivity.

As the IP core uses 10x for the reference clock multiplication factor, the reference clock frequencies for the three video standards are 27 MHz, 148.5 MHz and 148.35 MHz.

Transmit Options

The parallel input data from the `pd_in` port is used word-for-word for transmission in most cases. If the input is HD, there is an option for the IP core to compute CRC for each input data line and insert that in appropriate places in the transmitted data stream. If the CRC Insert option is disabled (Off), then it is assumed that the incoming data comes with appropriate CRC words in it. There is also an option to dynamically control the insertion or bypass of the CRC fields using an input port.

If it is required to insert line numbers in the format required by the SMPTE 292 standard, the IP core can be set to encode the raw line number information at the input port to the two line number words in the stream. The value at `ln_in` is read into a register whenever the signal `ln_set` is high. The line number value at the register is read when XYZ word is presented at `pd_in`, encoded and inserted after the XYZ word in the transmitted stream. When the dynamic LN insert option is selected, the LN is inserted only if `lni_en` is high during the time when XYZ word is at the input. If the LN insert is on and CRC insert is off, it is the user's responsibility to make sure the CRC check words take into account the encoded LN words also.

If CRC and LN insert functions are not enabled, the `trs_in` signal is not used. For SD inputs, `trs_in` is never used. The SD input data width can be either 8 bits or 10 bits and the parameter `SD Data Width` determines the width. If the data width is 8 bits, they are read from the part input bus `pd_in[9:2]`.

Signal Descriptions

A description of the I/O ports for the Multi-Rate SDI PHY IP Core is provided in Table . The top-level interface diagrams for the IP core are shown in Figures 1 and 2.

Table 3. Top-Level I/O Interface

Port	Bits	I/O	Description
SERDES Interface (SERDES Inside the IP Core)			
`sdi_inp`	1	I	High-speed SDI serial input - positive differential input. This is the serial SDI video stream coming in from the video source or cable equalizer.
`sdi_inn`	1	I	High-speed SDI serial input - negative differential input. This is the serial SDI video stream coming in from the video source or cable equalizer.

Table 3. Top-Level I/O Interface (Continued)

Port	Bits	I/O	Description
sdi_outp	1	O	High-speed SDI serial output - positive differential output. This is the serial SDI video stream going out to a display or video sink.
sdi_outn	1	O	High-speed SDI serial output - negative differential output. This is the serial SDI video stream going out to a display or video sink.
ref_clkp	1	I	Reference clock to the SERDES auxiliary channel - positive differential input. This port is available if either of the parameters Tx Reference Clk or Rx Reference Clk is set to "REFCLK".
ref_clkn	1	I	Reference clock to the SERDES auxiliary channel - negative differential input. This port is available if either of the parameters Tx Reference Clk or Rx Reference Clk is set to "REFCLK".
SERDES Interface (SERDES Outside the IP Core)			
ff_rxdata	20	I	Parallel receive data from the SERDES Rx channel.
ff_txdata	20	O	Parallel transmit data to the SERDES Tx channel.
ff_txfullclk	1	I	Transmit full clock from the SERDES.
ff_txhalfclk	1	I	Transmit half clock from the SERDES.
ff_txiclk	1	O	Clock synchronous with ff_txdata.
ff_rxiclk	1	O	Clock that is used to read out the parallel data from SERDES, ff_rxdata.
ff_ebrd_clk	1	O	Clock input for the elastic buffer read-out of SERDES Rx data.
ff_rxfullclk	1	I	Recovered full clock from the SERDES receive channel CDR.
ff_rxhalfclk	1	I	Recovered half clock from the SERDES receive channel CDR.
ffc_quad_rst	1	O	SERDES quad reset signal.
scisel	1	O	SERDES Client Interface (SCI) ports. Please refer to LatticeECP2M Family Data Sheet for details.
scien	1	O	
sciwritedata	8	O	
sciaddress	6	O	
scienaux	1	O	
sciselaux	1	O	
scird	1	O	
sciwstn	1	O	
scireaddata	8	I	
Common Interface			
tx_cref_clk	1	I	Single-ended transmit reference clock to the SERDES. This port is available only if the parameter Tx Reference Clk is set to "CORE_TXREFCLK".
rx_cref_clk	1	I	Single-ended receive reference clock to the SERDES. This port is available only if the parameter Rx Reference Clk is set to "CORE_RXREFCLK".
rx_hd_sdn	1	O	HD or SD signal sent out to the Rx reference clock generation logic to supply the proper clock for the receiver. If the value is '0', an SD reference clock is requested and if it is '1', a HD reference clock is requested.
wd_clk	1	I	This is a static clock used for watchdog functionality. This clock is primarily used for SCI programming.
rstn	1	I	System-wide asynchronous active-low reset signal. This signal resets the total IP core including the SERDES/PCS Quad.
ce	1	I	Optional clock enable signal. This freezes all the switching operations in the IP core and it is useful for keeping the IP core in a power save mode.
Rx Interface			
pd_out	20	O	Parallel data output. This is the parallel video data output from the receiver. For SD, only the lower 10 bits are valid.
pdo_clk	1	O	Clock output synchronous with the parallel output data, pd_out.

Table 3. Top-Level I/O Interface (Continued)

Port	Bits	I/O	Description
vidactive	1	O	Video active signal. This output signal is high if the receiver is locked to a valid video stream at the input. When the input rxscan_dis goes high, the vidactive signal is frozen at its current state.
vidstd	4	O	Video standard output. This output bus gives out the video source format standard that is identified by the receiver. This signal is valid only when vidactive is high. The video source formats associated with different values of this signal are given in Table 4.
hd_sdn_out	1	O	HD/SD output. This signal indicates if the current output data corresponds to a HD or a SD stream.
trs_out	1	O	Timing reference sequence output. This output is high during the start of the TRS sequence, i.e., during the time 3FFh or FFFFFh is available on pd_out.
field	1	O	Field number. This is the field number information available in the XYZ word. This output transitions immediately after the XYZ word output.
vblank	1	O	Vertical blanking signal. This output transitions immediately after the XYZ word output.
hblank	1	O	Horizontal blanking signal. This output transitions immediately after the XYZ word output.
ln_out	11	O	Line number output. This gives out the line number corresponding to the current parallel data output. This output is valid for HD video only. This output transitions immediately after LN1 word output.
crc_error	1	O	This signal indicates a CRC error has been detected for the current line. This output is valid for HD video only. This output transitions one cycle after CR1 word output.
rxscan_dis	1	I	Rx scan disable input. This signal, when high, disables the receive scanning functionality.
rx_rate	2	I	This input command specifies which rates are scanned for by the receiver. The functionality for different input values are as below:00: multi-rate. Receiver scans for both SD and HD 01 or 10: HD only 11: SD only
Tx Interface			
pd_in	20	I	Parallel data input. This is the parallel video stream data for transmission. For SD input, only the lower 10 bits are read in.
pdi_clk_out	1	O	Output clock from the IP core that can be used to clock in the parallel data at pd_in. This is the same clock that is used for the internal transmit logic.
trs_in	1	I	Timing Reference Signal for the input video stream. This is a one-clock cycle wide pulse that identifies the first word of the TRS in the parallel input data. The trs_in signal is used for the computation of CRC as well as to determine CRC and LN insert instants. This signal is not used for SD or if CRC and LN insertion are disabled for HD.
hd_sdn_in	1	I	HD/SD input. This signal identifies the current input data as a HD or a SD video stream. A transition at this input triggers a reprogramming of the SERDES.
sd8b_mode	1	I	SD 8-bit mode. If this input is high, the incoming data is considered to be 8 bits wide. Only the most significant 8 bits are read from the port. The least significant 2 bits are set to zero for all data except the leading TRS sequence (or ANC identifier). When the 8 most significant 8 bits are 1's, then the least significant 2 bits are made equal to '11'.
ln_in	11	I	Line number input. This input is read in HD mode only. The line number is read when ln_set is high.
ln_set	1	I	Line number set signal. This signal is used as a strobe to read the value at the ln_in port. The line number must be set during or before the LN0 word at the input pd_in.
lni_en	1	I	Line number insert enable. This signal enables insertion of internally encoded line number words after the TRS. If this signal is low during LN0 and LN1 time instants, the line number information contained in the parallel input stream is used unchanged.
crci_en	1	I	CRC insert enable. This signal enables the insertion of the internally computed CRC words after the LN words in the parallel input stream. If this signal is low during CR0 or CR1 instants, the CRC information contained in the parallel input stream is used unchanged.
txpgm_busy	1	O	Transmitter is being programmed and busy. This signal indicates that the transmitter is being programmed and that is not ready to accept input data for transmission. A transmitter programming happens whenever the input hd_sdn_in toggles or at system reset.
tx_plol	1	O	Tx PLL loss-of-lock output from the SERDES. This output is available only when SERDES in inside the IP.

Interfacing with Multi-Rate SDI PHY IP Core

SERDES Inside the IP Core

The ports available in the generated IP core depend on whether the check box "Include SERDES inside the IP" in the IP GUI was checked. If this box was checked, the SERDES is instantiated inside the IP core and several ports of the SERDES are internally connected to the Rx/Tx logic of the IP core. The Tx and Rx reference clocks are brought out as input ports of the IP core. Depending on the selections on `Tx Reference Clock` and `Rx Reference Clock` in the IP GUI, only some of the following ports are available: `ref_clkp`, `ref_clkn`, `tx_cref_clk` and `rx_cref_clk`. When the SERDES is inside the IP core, the serial inputs and outputs are directly available from the IP core.

SERDES Outside the IP Core

If the SERDES is chosen to be outside the IP core, the user must generate SERDES using IPexpress, choosing the SMPTE-292 protocol option and with SCI ports enabled. The SERDES parallel data I/Os, reset, clocks, control and SCI ports need to be connected with the corresponding ports in the IP core.

Common Interface

The reference clock input ports on the IP core depend on the selections made in the IP GUI. The most common scenario is to use REFCLK for Tx and RX_CREFCLK for Rx. In this case, the `rx_cref_clk` input of the IP core is fed from the receive reference clock source. The receiver clock source, whether a programmable video clock generator or clock multiplexer with multiple clock inputs, is controlled by the clock request command `rx_hd_sdn` from the IP core. If `rx_hd_sdn` is high, a HD clock (148.5 or 148.35 MHz) is requested. If it is low, an SD clock (27 MHz) is requested. An independent clock that does not stop or vary during rate changes is required to be connected to the `wd_clk` input port. The frequency of this clock is not very important, as long as it is not higher than 100 MHz. This clock is primarily used to program the SERDES using the SCI interface.

Rx Interface

The parallel output, `pd_out` from the IP core is synchronous with the output clock, `pdo_clk`. The output bus `vidstd` provides the video standard and source format detected by the receiver. The standards for different values of this signal are given in Table 4.

Table 4. Detected Video Standards

Value on vidstd Port	Reference SMPTE Standard	Format[1]	Lines per frame	Words per Active Line[2]	Total Active Lines	Words per Total Line[2]	Frame Rate (Hz)	Fields per Frame	Data Rate Divisor
0	Undefined								
1	260M	A or B	1125	1920	1035	2200	30 or 30/M	2	1 or M
2	Reserved								
3	295M	C	1250	1920	1080	2376	25	2	1
4	274M	D or E	1125	1920	1080	2200	30 or 30/M	2	1 or M
5	Reserved								
6	274M	F	1125	1920	1080	2640	25	2	1
7	274M	G or H	1125	1920	1080	2200	30 or 30/M	1	1 or M
8	Reserved								
9	274M	I	1125	1920	1080	2640	25	1	1
10	274M	J or K	1125	1920	1080	2750	24 or 24/M	1	1 or M
11	Reserved								
12	296M	L or M	750	1280	720	1650	60 or 60/M	1	1 or M
13	Reserved								
14	125M	SD525i	525	1440	486	1716	30	2	1
15	125M	SD625i	625	1440	576	1728	25	2	1

1. As described in SMPTE 292M.
2. Each channel Y Cb/Cr.

As shown in Table 4, the receiver detects both the integer and the fractional frame rates as the same standard. The outputs field, hblank and vblank change state during the time when XYZ word of the TRS sequence is given at the output and they remain in the same state until the next XYZ word instant. The line number output is available only for HD rates. The value at the ln_out output is refreshed when LN1 is at the output and remains the same until the next LN1 instant. The receiver determines the CRC words for Y and C channels from the received data and compares with the corresponding words from the received stream. If there is a mismatch, the signal crc_error is asserted high one cycle after YCR1 is at the output. This signal remains in the same state until the next YCR1 word. The signal rxscan_dis freezes the receiver scanning functionality. The receiver remains set at the same receive rate as long as this signal remains high. The receive scan disable can be used to temporarily disable scanning while the transmitter rate is being changed. The input rx_rate can be used to specify whether the receiver scans for both SD and HD rates or only for one of these rates.

Tx Interface

The parallel data for the transmitter is read at the rising edge of pdi_clk_out. The input trs_in is used for the computation of CRC and for the insertion of CRC and LN, if enabled. If CRC and LN are both disabled, or if the input data is SD, the input trs_in is not used.

The output txpgm_busy goes high whenever there is a transmit rate change and remains high until the transmitter programming is completed and it starts transmitting. When this signal is high, it is recommended to disable receiver scanning functionality. This can be achieved by connecting txpgm_busy to the rxscan_dis input. By doing this, the receiver settings are not disturbed during transmit rate change and when transmitter programming is complete, both receiver and transmitter function normally. It must be noted that whenever the transmitter or the receiver is programmed (when the receiver scans for input rate or when the transmit rate is changed), the SERDES is reset, affecting both receive and transmit functionalities.

Timing Specifications

The top-level timing diagrams for the transmit and receive processes and interface signals are given in the following figures.

Figure 8. Receive-Side Rate Scan and Lock Scheme

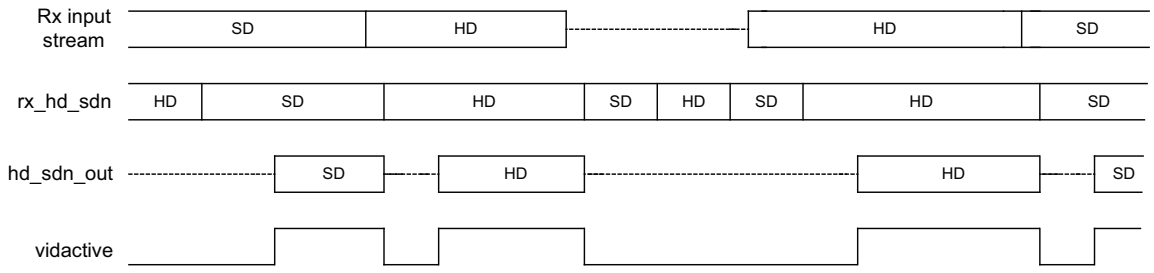


Figure 9. Receive-Side Interface Signals

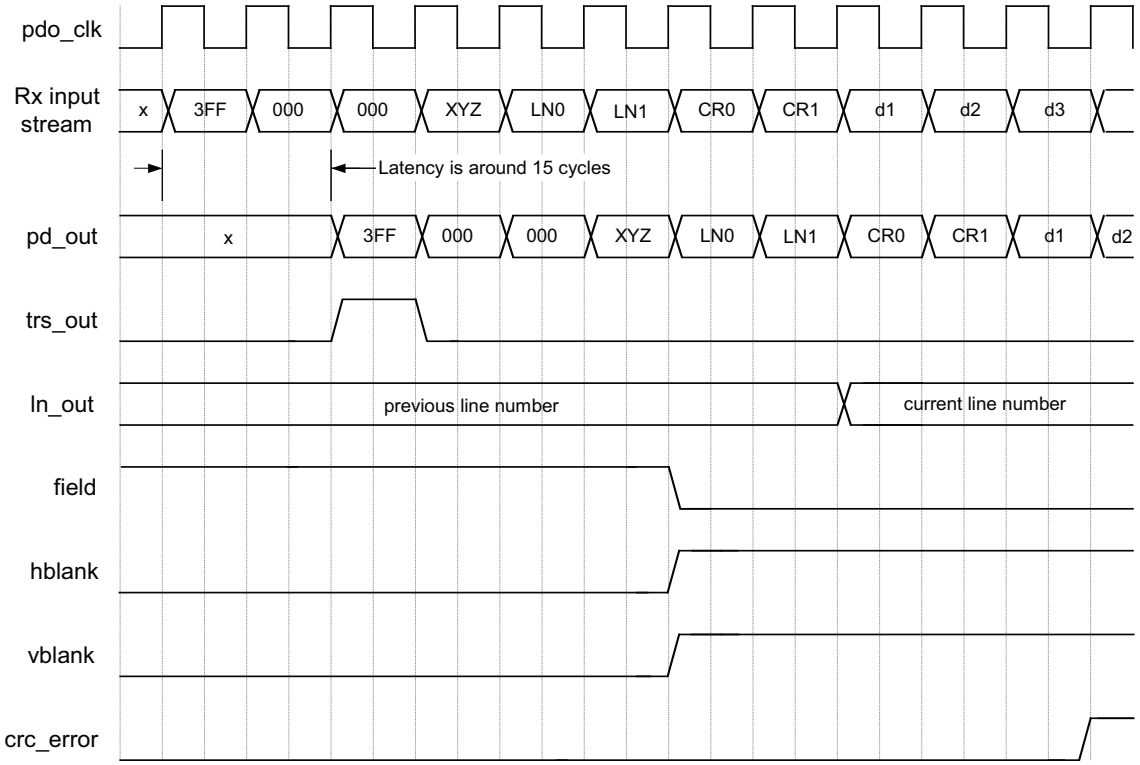


Figure 10. Transmit-Side Rate Changes

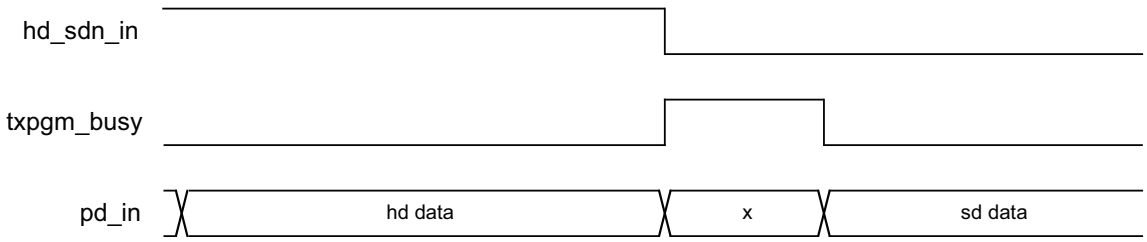
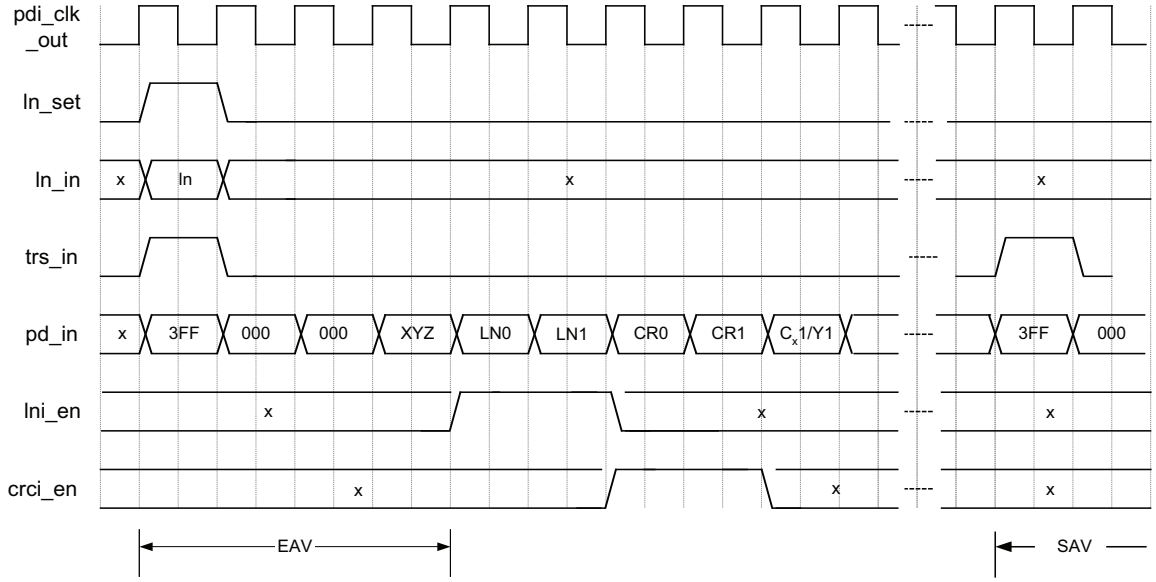


Figure 11. Transmit-Side Interface Signals



IPexpress User-Configurable IP Core

The Multi-Rate SDI PHY IP core is an IPexpress User Configurable IP core, which allows designers to configure the IP core and generate netlists and simulation files for use in designs. The IPexpress flow also supports a hardware evaluation capability, making it possible to create versions of the IP core that operate in hardware for a limited period of time without requiring the purchase on an IP core license.

To download a full evaluation version of the Multi-Rate SDI PHY IP Core, please go to the Lattice IP Server tab in the ispLEVER IPexpress GUI window. All ispLeverCORE™ IP cores available for download are visible on this tab. Also, refer to the Readme file to find out more about hardware evaluation.

To find out more about the IPexpress User Configurable IP cores, please see the Lattice IPexpress Quick Start Guide.

References

1. SMPTE 259M-2006- SDTV Digital Signal/Data- Serial Digital Interface.
2. SMPTE 292M-1998 Television- Bit-Serial Digital Interface for high-Definition Television Systems.
3. SMPTE 125M-1995 Television- Component Video Signal 4:2:2- Bit-Parallel Digital Interface.
4. ANSI/SMPTE 267M-1995 Television- Bit-Parallel Digital Interface- Component Video Signal 4:2:2 16x9 Aspect Ratio.
5. SMPTE 260M-1999 Television- 1125/60 High-Definition Production System- Digital Representation and Bit-Parallel Interface.
6. SMPTE 274M-2003 Television- 1920 x 1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple Picture Rates.
7. SMPTE 295M-1997 Television- 1920 x 1080 50 Hz- Scanning and Interface.
8. SMPTE 296M-2001 Television- 1280 x 720 Progressive Image Sample Structure- Analog and Digital Representation and Analog Interface.
9. LatticeECP2/M Family Data Sheet
10. Lattice technical note TN1124, LatticeECP2/M SERDES/PCS Usage Guide

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Revision History

Date	Version	Change Summary
October 2007	01.0	Initial release.
July 2008	01.1	Updated Appendix for LatticeECP2M Devices.
January 2012	01.2	Top-Level I/O Interface table – Fixed reference to Table 4 in the description for the vidstd port.

Appendix A. Source Format Parameters for SMPTE 292 Interface Standard

(extracted from SMPTE 292M [2])

Table 5. Source Format Parameters for SMPTE 292 Interface Standard

Reference SMPTE Standard	260M		295M	274M								296M	
Format	A	B	C	D	E	F	G	H	I	J	K	L	M
Lines per frame	1125	1125	1250	1125	1125	1125	1125	1125	1125	1125	1125	750	750
Words per active line[1]	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920	1920	1280	1280
Total active lines	1035	1035	1080	1080	1080	1080	1080	1080	1080	1080	1080	720	720
Words per total line[1]	2200	2200	2376	2200	2200	2640	2200	2200	2640	2750	2750	1650	1650
Frame rate (Hz)	30	30/M	25	30	30/M	25	30	30/M	25	24	24/M	60	60/M
Fields per frame	2	2	2	2	2	2	1	1	1	1	1	1	1
Data rate divisor	1	M	1	1	M	1	1	M	1	1	M	1	M

1. Each channel Y Cb/Cr.

Appendix for LatticeECP2M Devices

Table 6. Performance and Resource Utilization[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	Tx Clock f_{MAX} (MHz)	Rx Clock f_{MAX} (MHz)
1	497	987	646	202	152
2	122	224	229	227	N/A
3	439	867	506	N/A	148

1. Performance and utilization characteristics are generated using LFE2M-35E-5F672C, with Lattice's ispLEVER 7.1 software. When using this IP core in a different density, speed, or grade within the LatticeECP2M family, performance and utilization may vary.

Table 7. Parameter Settings for Standard Configurations[1, 2]

Parameter Name	Core Configuration		
	1	2	3
PHY Function	Both	Tx	Rx
Include SERDES Inside the IP	Yes	Yes	Yes
SERDES Channel	3	3	3
Tx Reference Clock	REFCLK	REFCLK	N/A
Rx Reference Clock	CORE_RXREFCLK	N/A	CORE_RXREFCLK
SD Data Width	10 bits	10 bits	N/A
LN Insert	Off	Off	N/A
CRC Insert	Off	Off	N/A
Clock Enable Port	No	No	No
Connect Reset Port to GSR	Yes	Yes	Yes

1. Example configurations shown above.
2. The Multi-Rate Serial Digital Interface (SDI) Physical Layer IP Core is an IPexpress user-configurable core and can be used to generate any allowable configuration.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Multi-Rate SDI PHY Layer targeting LatticeECP2M devices is MR-SDI-PHY-PM-U1.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

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