

# 74ALVC00

## Quad 2-input NAND gate

Rev. 3 — 16 May 2014

Product data sheet

### 1. General description

The 74ALVC00 is a quad 2-input NAND gate.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

### 2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC00D	−40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC00PW	−40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC00BQ	−40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1



## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state <sup>[1] [2]</sup>	-0.5	$V_{CC} + 0.5$	V
		output 3-state	-0.5	+4.6	V
		power-down mode, $V_{CC} = 0$ V <sup>[2]</sup>	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C <sup>[3]</sup>	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When  $V_{CC} = 0$  V (power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
 For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	output HIGH or LOW state	0	$V_{CC}$	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	1.51	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	2.10	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	2.01	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.53	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	2.76	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	0.11	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	0.17	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	0.25	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.16	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	0.23	0.4	V
$I_I$	input leakage current	$V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND	-	$\pm 0.1$	$\pm 5$	$\mu$ A
		$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 3.6 V	-	$\pm 0.1$	$\pm 10$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 3.6 V	-	$\pm 0.1$	$\pm 10$	$\mu$ A

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	20	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	750	μA
C <sub>I</sub>	input capacitance		-	3.5	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.8	4.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.1	2.8	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.6	3.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.1	3.0	ns
C <sub>PD</sub>	power dissipation capacitance	per gate; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <sup>[3]</sup>	-	28	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C[2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

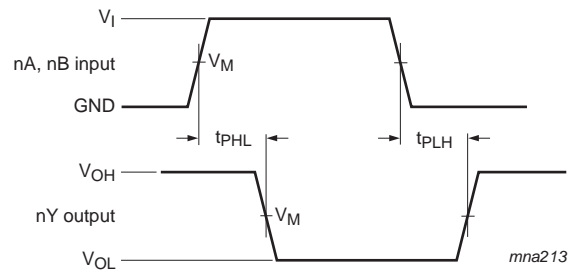
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHzC<sub>L</sub> = output load capacitance in pFV<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

## 11. Waveforms

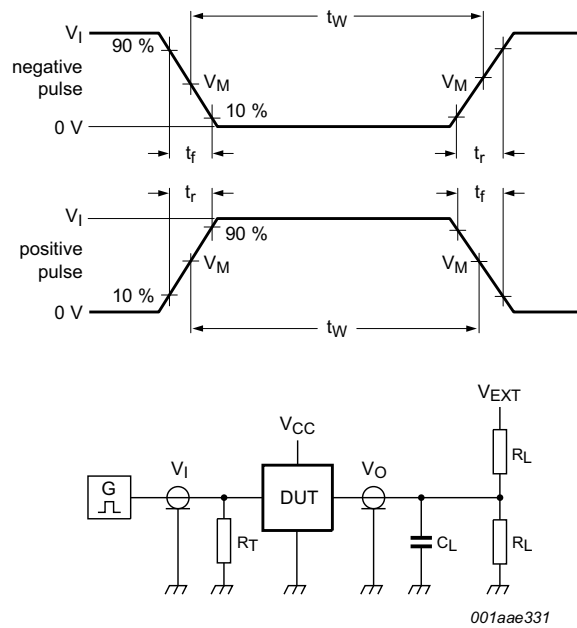


Measurement points are given in [Table 8](#).

**Fig 6. Inputs nA, nB to output nY propagation delay times**

**Table 8. Measurement points**

Supply voltage $V_{CC}$	Input $V_I$	$V_M$
1.65 V to 1.95 V	$V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$0.5V_{CC}$
2.7 V	2.7 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 7. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage $V_{CC}$	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

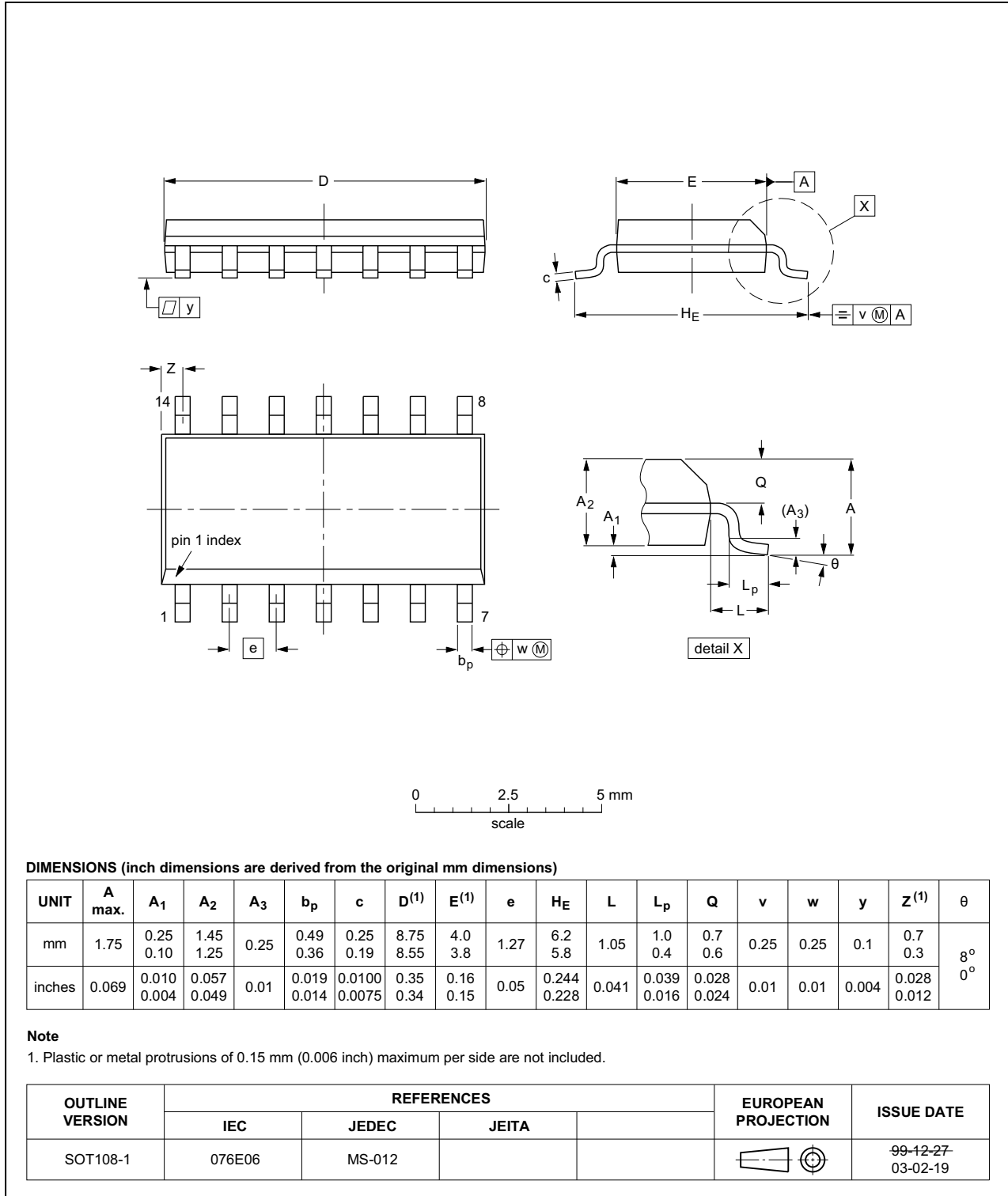


Fig 8. Package outline SOT108-1 (SO14)



TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

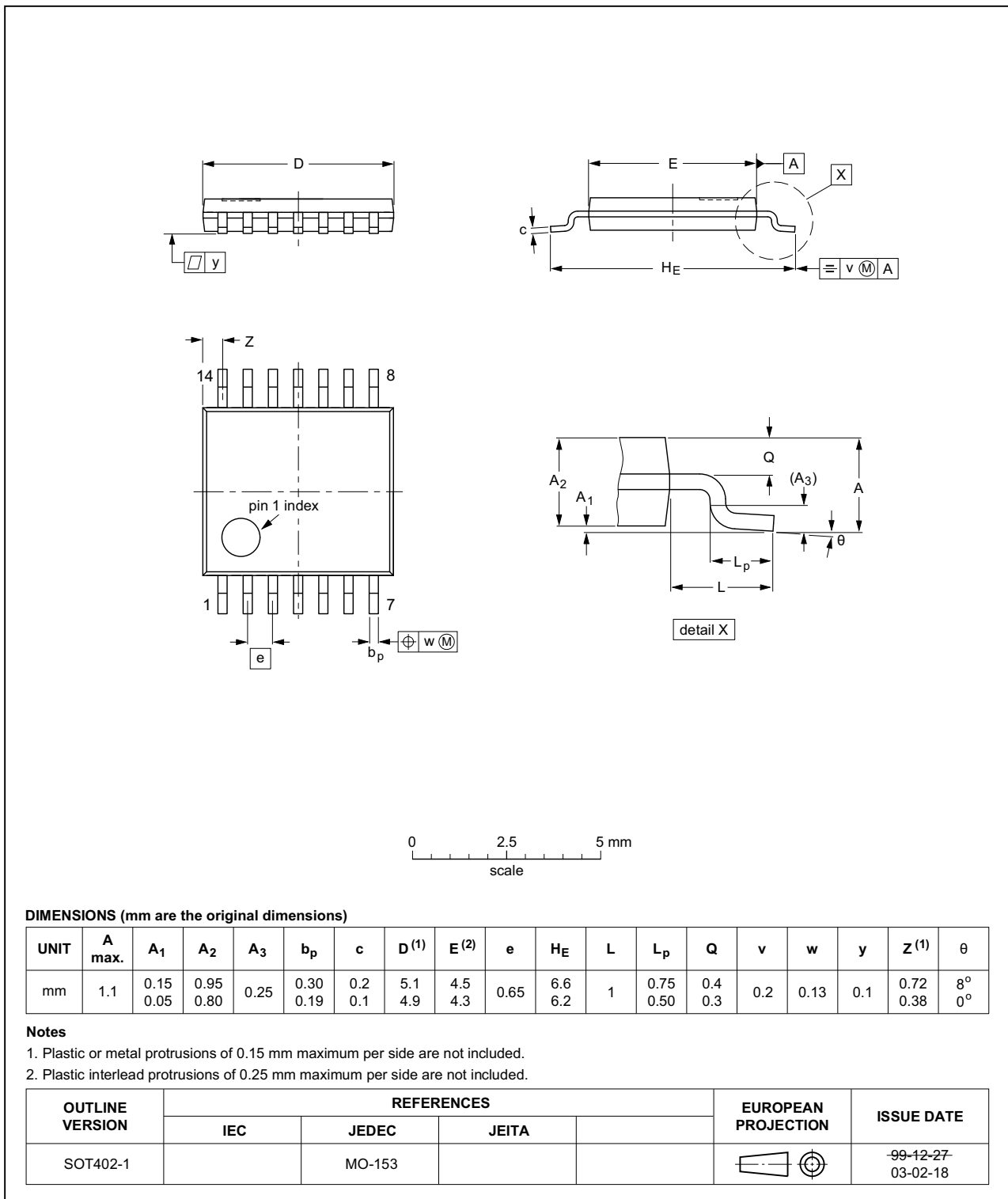


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

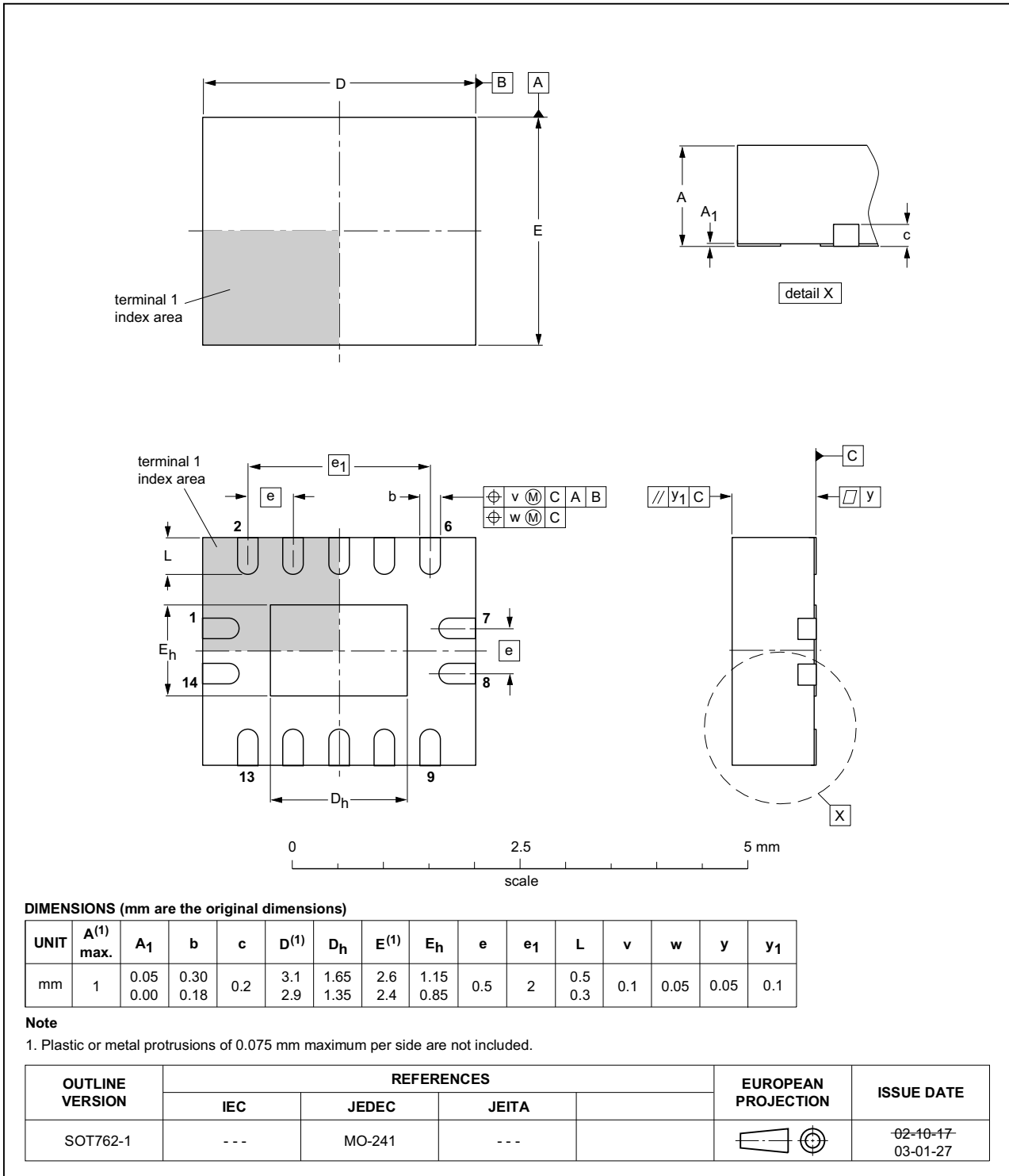


Fig 10. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC00 v.3	20140516	Product data sheet	-	74ALVC00 v.2
	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>			
74ALVC00 v.2	20030514	Product specification	-	74ALVC00 v.1
74ALVC00 v.1	20030206	Product specification	-	-

## 15. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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