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# RL78/G12

RENESAS MCU

True low-power platform (63 μA/MHz) for the general-purpose applications, with 1.8-V to 5.5-V operation, 2- to 16-Kbyte code flash memory, and 31 DMIPS at 24 MHz

## 1. OUTLINE

### 1.1 Features

**Ultra-low power consumption technology**
- $V_{DD}$ = single power supply voltage of 1.8 to 5.5 V which can operate at a low voltage
- HALT mode
- STOP mode
- SNOOZE mode

**RL78 CPU core**
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 μs: @ 24 MHz operation with high-speed on-chip oscillator) to ultra-low speed (1 μs: @ 1 MHz operation)
- Address space: 1 MB
- General-purpose registers: (8-bit register x 8) x 4 banks
- On-chip RAM: 256 B to 2 KB

**Code flash memory**
- Code flash memory: 2 to 16 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with flash shield window function)

**Data flash memory** Note
- Data flash memory: 2 KB
- Back ground operation (BGO): Instructions are executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD}$ = 1.8 to 5.5 V

**High-speed on-chip oscillator**
- Select from 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: +/- 1.0 % ($V_{DD}$ = 1.8 to 5.5 V, $T_A$ = -20 to +85 °C)

**Operating ambient temperature**
- $T_A$ = -40 to +85 °C (A: Consumer applications, D: Industrial applications)
- $T_A$ = -40 to +105 °C (G: Industrial applications) Note

**Power management and reset function**
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 12 levels)

**DMA (Direct Memory Access) controller** Note
- 2 channels
- Number of clocks during transfer between 8/16-bit SFR and internal RAM: 2 clocks

**Multiplier and divider/multiply-accumulator**
- 16 bits x 16 bits = 32 bits (Unsigned or signed)
- 32 bits x 32 bits = 32 bits (Unsigned)
- 16 bits x 16 bits + 32 bits = 32 bits (Unsigned or signed)

**Serial interface**
- CSI : 1 to 3 channels
- UART : 1 to 3 channels
- Simplified $I^2C$ communication : 0 to 3 channels
- $I^2C$ communication : 1 channel

**Timer**
- 16-bit timer : 4 to 8 channels
- 12-bit interval timer : 1 channel
- Watchdog timer : 1 channel (operable with the dedicated low-speed on-chip oscillator)

**A/D converter**
- 8/10-bit resolution A/D converter ($V_{DD}$ = 1.8 to 5.5 V)
- 8 to 11 channels, internal reference voltage (1.45 V), and temperature sensor Note

**I/O port**
- I/O port: 18 to 26
  (N-ch open drain I/O [withstand voltage of 6 V]: 2,
  N-ch open drain I/O [$V_{DD}$ withstand voltage]: 4 to 9)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

**Others**
- On-chip BCD (binary-coded decimal) correction circuit

**Note** Can be selected only in HS (high-speed main) mode.

**Remark** The functions mounted depend on the product. See **1.7 Outline of Functions.**

O ROM, RAM capacities

| Code flash | Data flash | RAM | 20 pins | 24 pins | 30 pins |
|---|---|---|---|---|---|
| 16 KB | 2 KB | 2 KB | – | – | R5F102AA |
| | – | | – | – | R5F103AA |
| | 2 KB | 1.5 KB | R5F1026A Note 1 | R5F1027A Note 1 | – |
| | – | | R5F1036A Note 1 | R5F1037A Note 1 | – |
| 12 KB | 2KB | 1 KB | R5F10269 Note 1 | R5F10279 Note 1 | R5F102A9 |
| | – | | R5F10369 Note 1 | R5F10379 Note 1 | R5F103A9 |
| 8 KB | 2 KB | 768 B | R5F10268 Note 1 | R5F10278 Note 1 | R5F102A8 |
| | – | | R5F10368 Note 1 | R5F10378 Note 1 | R5F103A8 |
| 4 KB | 2KB | 512 B | R5F10267 | R5F10277 | R5F102A7 |
| | – | | R5F10367 | R5F10377 | R5F103A7 |
| 2 KB | 2 KB | 256 B | R5F10266 Note 2 | – | – |
| | – | | R5F10366 Note 2 | – | – |

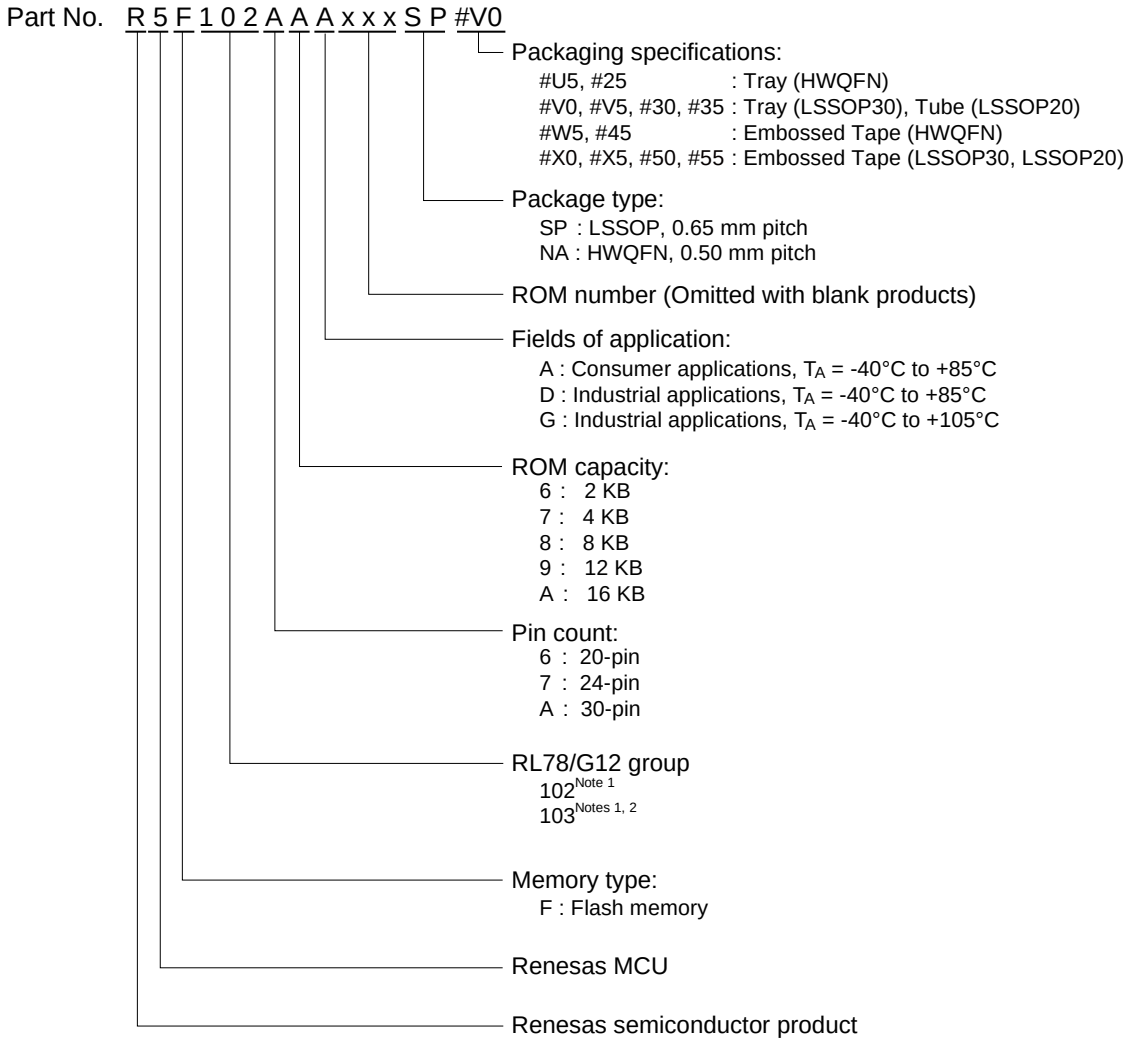
**Notes 1.** This is 640 bytes when the self-programming function or data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE** in the RL78/G12 User's Manual.)

**2.** The self-programming function cannot be used for R5F10266 and R5F10366.

**Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.**

## 1.2 List of Part Numbers

<R> **Figure 1-1. Part Number, Memory Size, and Package of RL78/G12**




**Notes 1.** For details about the differences between the R5F102 products and the R5F103 products of RL78/G12, see **1.3 Differences between the R5F102 Products and the R5F103 Products**.

**2.** Products only for “A: Consumer applications ($T_A$ = -40 to +85°C)” and “D: Industrial applications ($T_A$ = -40 to +85°C)”

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**Table 1-1. List of Ordering Part Numbers (1/2)**

| Pin count | Package | Data flash | Fields of Application Note | Part Number | RENESAS Code |
|---|---|---|---|---|---|
| 20 pins | 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch) | Mounted | A | R5F1026AASP#V5, R5F10269ASP#V5, R5F10268ASP#V5, R5F10267ASP#V5, R5F10266ASP#V5<br>R5F1026AASP#X5, R5F10269ASP#X5, R5F10268ASP#X5, R5F10267ASP#X5, R5F10266ASP#X5<br>R5F1026AASP#35, R5F10269ASP#35, R5F10268ASP#35, R5F10267ASP#35, R5F10266ASP#35<br>R5F1026AASP#55, R5F10269ASP#55, R5F10268ASP#55, R5F10267ASP#55, R5F10266ASP#55 | PLSP0020JB-A |
| | | | D | R5F1026ADSP#V5, R5F10269DSP#V5, R5F10268DSP#V5, R5F10267DSP#V5, R5F10266DSP#V5<br>R5F1026ADSP#X5, R5F10269DSP#X5, R5F10268DSP#X5, R5F10267DSP#X5, R5F10266DSP#X5<br>R5F1026ADSP#35, R5F10269DSP#35, R5F10268DSP#35, R5F10267DSP#35, R5F10266DSP#35<br>R5F1026ADSP#55, R5F10269DSP#55, R5F10268DSP#55, R5F10267DSP#55, R5F10266DSP#55 | |
| | | | G | R5F1026AGSP#V5, R5F10269GSP#V5, R5F10268GSP#V5, R5F10267GSP#V5, R5F10266GSP#V5<br>R5F1026AGSP#X5, R5F10269GSP#X5, R5F10268GSP#X5, R5F10267GSP#X5, R5F10266GSP#X5<br>R5F1026AGSP#35, R5F10269GSP#35, R5F10268GSP#35, R5F10267GSP#35, R5F10266GSP#35<br>R5F1026AGSP#55, R5F10269GSP#55, R5F10268GSP#55, R5F10267GSP#55, R5F10266GSP#55 | |
| | | Not mounted | A | R5F1036AASP#V5, R5F10369ASP#V5, R5F10368ASP#V5, R5F10367ASP#V5, R5F10366ASP#V5<br>R5F1036AASP#X5, R5F10369ASP#X5, R5F10368ASP#X5, R5F10367ASP#X5, R5F10366ASP#X5<br>R5F1036AASP#35, R5F10369ASP#35, R5F10368ASP#35, R5F10367ASP#35, R5F10366ASP#35<br>R5F1036AASP#55, R5F10369ASP#55, R5F10368ASP#55, R5F10367ASP#55, R5F10366ASP#55 | PLSP0020JB-A |
| | | | D | R5F1036ADSP#V5, R5F10369DSP#V5, R5F10368DSP#V5, R5F10367DSP#V5, R5F10366DSP#V5<br>R5F1036ADSP#X5, R5F10369DSP#X5, R5F10368DSP#X5, R5F10367DSP#X5, R5F10366DSP#X5<br>R5F1036ADSP#35, R5F10369DSP#35, R5F10368DSP#35, R5F10367DSP#35, R5F10366DSP#35<br>R5F1036ADSP#55, R5F10369DSP#55, R5F10368DSP#55, R5F10367DSP#55, R5F10366DSP#55 | |
| 24 pins | 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch) | Mounted | A | R5F1027AANA#U5, R5F10279ANA#U5, R5F10278ANA#U5, R5F10277ANA#U5<br>R5F1027AANA#W5, R5F10279ANA#W5, R5F10278ANA#W5, R5F10277ANA#W5 | PWQN0024KE-A |
| | | | | R5F1027AANA#25, R5F10279ANA#25, R5F10278ANA#25, R5F10277ANA#25<br>R5F1027AANA#45, R5F10279ANA#45, R5F10278ANA#45, R5F10277ANA#45 | PWQN0024KF-A |
| | | | D | R5F1027ADNA#U5, R5F10279DNA#U5, R5F10278DNA#U5, R5F10277DNA#U5<br>R5F1027ADNA#W5, R5F10279DNA#W5, R5F10278DNA#W5, R5F10277DNA#W5 | PWQN0024KE-A |
| | | | G | R5F1027AGNA#U5, R5F10279GNA#U5, R5F10278GNA#U5, R5F10277GNA#U5<br>R5F1027AGNA#W5, R5F10279GNA#W5, R5F10278GNA#W5, R5F10277GNA#W5 | |
| | | | | R5F1027AGNA#25, R5F10279GNA#25, R5F10278GNA#25, R5F10277GNA#25<br>R5F1027AGNA#45, R5F10279GNA#45, R5F10278GNA#45, R5F10277GNA#45 | PWQN0024KF-A |

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**Table 1-1. List of Ordering Part Numbers (2/2)**

| Pin count | Package | Data flash | Fields of Application Note | Part Number | RENESAS Code |
|---|---|---|---|---|---|
| 24 pins | 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch) | Not mounted | A | R5F1037AANA#U5, R5F10379ANA#U5, R5F10378ANA#U5, R5F10377ANA#U5,<br>R5F1037AANA#W5, R5F10379ANA#W5, R5F10378ANA#W5, R5F10377ANA#W5 | PWQN0024KE-A |
| | | | | R5F1037AANA#25, R5F10379ANA#25, R5F10378ANA#25, R5F10377ANA#25,<br>R5F1037AANA#45, R5F10379ANA#45, R5F10378ANA#45, R5F10377ANA#45 | PWQN0024KF-A |
| | | | D | R5F1037ADNA#U5, R5F10379DNA#U5, R5F10378DNA#U5, R5F10377DNA#U5,<br>R5F1037ADNA#W5, R5F10379DNA#W5, R5F10378DNA#W5, R5F10377DNA#W5 | PWQN0024KE-A |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch ) | Mounted | A | R5F102AAASP#V0, R5F102A9ASP#V0, R5F102A8ASP#V0, R5F102A7ASP#V0<br>R5F102AAASP#X0, R5F102A9ASP#X0, R5F102A8ASP#X0, R5F102A7ASP#X0<br>R5F102AAASP#30, R5F102A9ASP#30, R5F102A8ASP#30, R5F102A7ASP#30<br>R5F102AAASP#50, R5F102A9ASP#50, R5F102A8ASP#50, R5F102A7ASP#50 | PLSP0030JB-B |
| | | | D | R5F102AADSP#V0, R5F102A9DSP#V0, R5F102A8DSP#V0, R5F102A7DSP#V0<br>R5F102AADSP#X0, R5F102A9DSP#X0, R5F102A8DSP#X0, R5F102A7DSP#X0<br>R5F102AADSP#30, R5F102A9DSP#30, R5F102A8DSP#30, R5F102A7DSP#30<br>R5F102AADSP#50, R5F102A9DSP#50, R5F102A8DSP#50, R5F102A7DSP#50 | |
| | | | G | R5F102AAGSP#V0, R5F102A9GSP#V0, R5F102A8GSP#V0, R5F102A7GSP#V0<br>R5F102AAGSP#X0, R5F102A9GSP#X0, R5F102A8GSP#X0, R5F102A7GSP#X0<br>R5F102AAGSP#30, R5F102A9GSP#30, R5F102A8GSP#30, R5F102A7GSP#30<br>R5F102AAGSP#50, R5F102A9GSP#50, R5F102A8GSP#50, R5F102A7GSP#50 | |
| | | Not mounted | A | R5F103AAASP#V0, R5F103A9ASP#V0, R5F103A8ASP#V0, R5F103A7ASP#V0<br>R5F103AAASP#X0, R5F103A9ASP#X0, R5F103A8ASP#X0, R5F103A7ASP#X0<br>R5F103AAASP#30, R5F103A9ASP#30, R5F103A8ASP#30, R5F103A7ASP#30<br>R5F103AAASP#50, R5F103A9ASP#50, R5F103A8ASP#50, R5F103A7ASP#50 | PLSP0030JB-B |
| | | | D | R5F103AADSP#V0, R5F103A9DSP#V0, R5F103A8DSP#V0, R5F103A7DSP#V0<br>R5F103AADSP#X0, R5F103A9DSP#X0, R5F103A8DSP#X0, R5F103A7DSP#X0<br>R5F103AADSP#30, R5F103A9DSP#30, R5F103A8DSP#30, R5F103A7DSP#30<br>R5F103AADSP#50, R5F103A9DSP#50, R5F103A8DSP#50, R5F103A7DSP#50 | |

**Note** For fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G12**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

## 1.3 Differences between the R5F102 Products and the R5F103 Products

The following are differences between the R5F102 products and the R5F103 products.

O Whether the data flash memory is mounted or not

O High-speed on-chip oscillator oscillation frequency accuracy

O Number of channels in serial interface

O Whether the DMA function is mounted or not

O Whether a part of the safety functions are mounted or not

### 1.3.1 Data Flash

The data flash memory of 2 KB is mounted on the R5F102 products, but not on the R5F103 products.

| Product | Data Flash |
|---|---|
| **R5F102 products**<br>R5F1026A, R5F1027A, R5F102AA,<br>R5F10269, R5F10279, R5F102A9,<br>R5F10268, R5F10278, R5F102A8,<br>R5F10267, R5F10277, R5F102A7,<br>R5F10266 Note | 2 KB |
| **R5F103 products**<br>R5F1036A, R5F1037A, R5F103AA,<br>R5F10369, R5F10379, R5F103A9,<br>R5F10368, R5F10378 R5F103A8,<br>R5F10367, R5F10377, R5F103A7,<br>R5F10366 | Not mounted |

**Note** The RAM in the R5F10266 has capacity as small as 256 bytes. Depending on the customer's program specification, the stack area to execute the data flash library may not be kept and data may not be written to or erased from the data flash memory.

**Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.**

### 1.3.2 On-chip oscillator characteristics

(1) High-speed on-chip oscillator oscillation frequency of the R5F102 products

| Oscillator | Condition | MIN | MAX | Unit |
|---|---|---|---|---|
| High-speed on-chip oscillator oscillation frequency accuracy | $T_A$ = -20 to +85°C | -1.0 | +1.0 | % |
| | $T_A$ = -40 to -20°C | -1.5 | +1.5 | |
| | $T_A$ = +85 to +105°C | -2.0 | +2.0 | |

(2) High-speed on-chip oscillator oscillation frequency of the R5F103 products

| Oscillator | Condition | MIN | MAX | Unit |
|---|---|---|---|---|
| High-speed on-chip oscillator oscillation frequency accuracy | $T_A$ = -40 to + 85°C | -5.0 | +5.0 | % |

### 1.3.3 Peripheral Functions

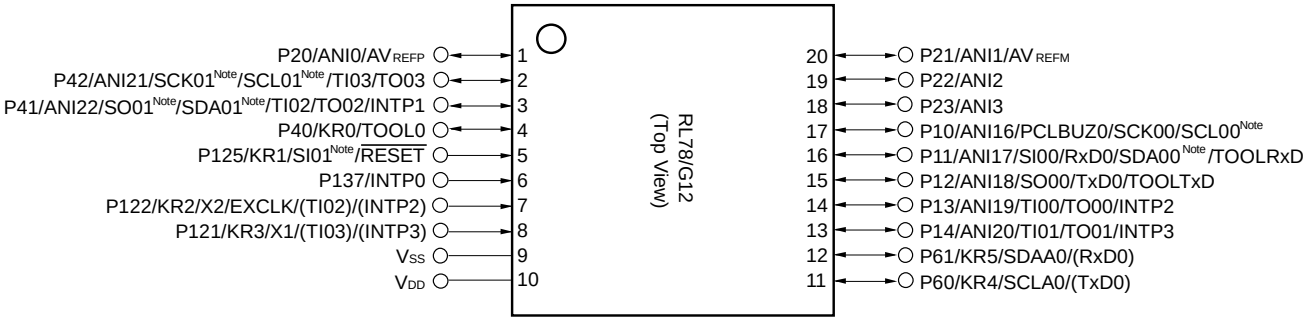
The following are differences in peripheral functions between the R5F102 products and the R5F103 products.

| RL78/G12 | | R5F102 product | | R5F103 product | |
|---|---|---|---|---|---|
| | | 20, 24 pin product | 30 pin product | 20, 24 pin product | 30 pin product |
| Serial interface | UART | 1 channel | 3 channels | 1 channel | |
| | CSI | 2 channels | 3 channels | 1 channel | |
| | Simplified $I^2C$ | 2 channels | 3 channels | None | |
| DMA function | | 2 channels | | None | |
| Safety function | CRC operation | Yes | | None | |
| | RAM guard | Yes | | None | |
| | SFR guard | Yes | | None | |

## 1.4 Pin Configuration (Top View)

### 1.4.1 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)



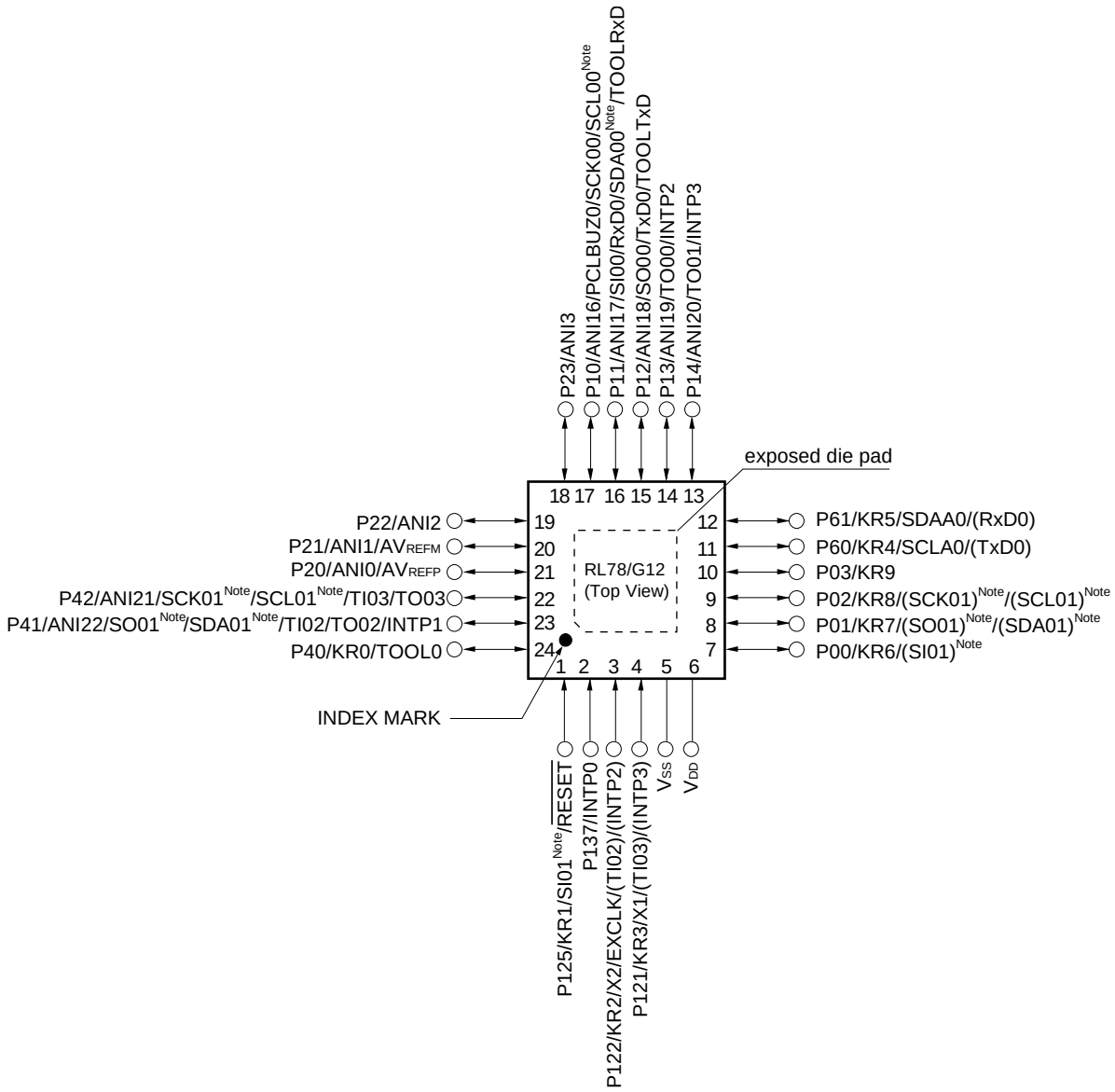

**Note** Provided only in the R5F102 products.

**Remarks 1.** For pin identification, see **1.5 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G12 User's Manual.

### 1.4.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)




**Note** Provided only in the R5F102 products.

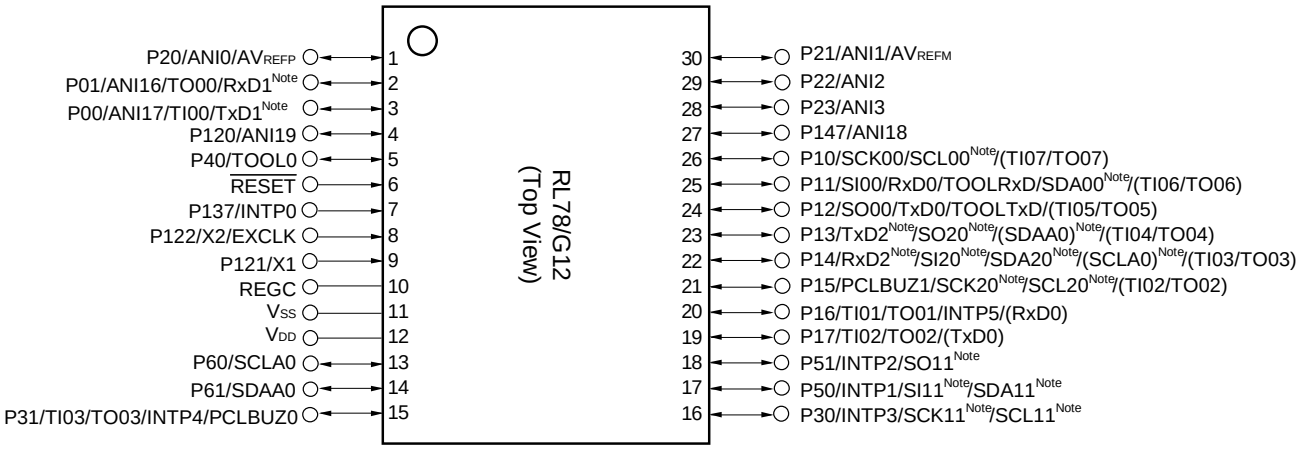
**Remarks 1.** For pin identification, see **1.5 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G12 User's Manual.

**3.** It is recommended to connect an exposed die pad to Vss.

### 1.4.3 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)




**Note** Provided only in the R5F102 products.

**Caution Connect the REGC pin to VSS via capacitor (0.47 to 1 µF).**

**Remarks 1.** For pin identification, see **1.5 Pin Identification**.

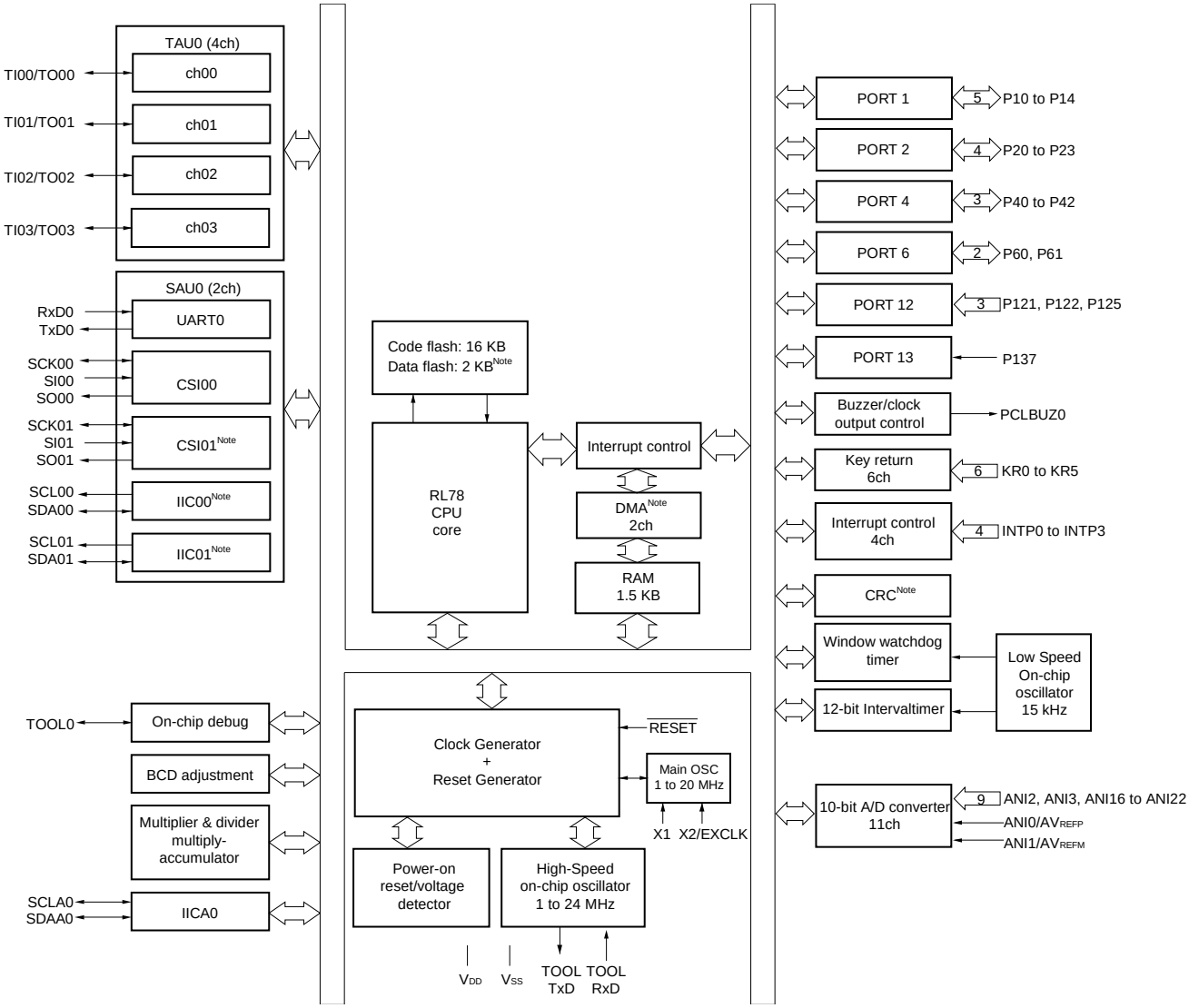
**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G12 User's Manual.

## 1.5 Pin Identification

| | |
|---|---|
| ANI0 to ANI3, ANI16 to ANI22: | Analog input |
| $AV_{REFM}$: | Analog Reference Voltage Minus |
| $AV_{REFP}$: | Analog reference voltage plus |
| EXCLK: | External Clock Input (Main System Clock) |
| INTP0 to INTP5 | Interrupt Request From Peripheral |
| KR0 to KR9: | Key Return |
| P00 to P03: | Port 0 |
| P10 to P17: | Port 1 |
| P20 to P23: | Port 2 |
| P30 to P31: | Port 3 |
| P40 to P42: | Port 4 |
| P50, P51: | Port 5 |
| P60, P61: | Port 6 |
| P120 to P122, P125: | Port 12 |
| P137: | Port 13 |
| P147: | Port 14 |
| PCLBUZ0, PCLBUZ1: | Programmable Clock Output/ Buzzer Output |
| REGC: | Regulator Capacitance |
| $\overline{\text{RESET}}$: | Reset |
| RxD0 to RxD2: | Receive Data |
| SCK00, SCK01, SCK11, SCK20: | Serial Clock Input/Output |
| SCL00, SCL01, SCL11, SCL20, SCLA0: | Serial Clock Input/Output |
| SDA00, SDA01, SDA11, SDA20, SDAA0: | Serial Data Input/Output |
| SI00, SI01, SI11, SI20: | Serial Data Input |
| SO00, SO01, SO11, SO20: | Serial Data Output |
| TI00 to TI07: | Timer Input |
| TO00 to TO07: | Timer Output |
| TOOL0: | Data Input/Output for Tool |
| TOOLRxD, TOOLTxD: | Data Input/Output for External Device |
| TxD0 to TxD2: | Transmit Data |
| $V_{DD}$: | Power supply |
| $V_{SS}$: | Ground |
| X1, X2: | Crystal Oscillator (Main System Clock) |

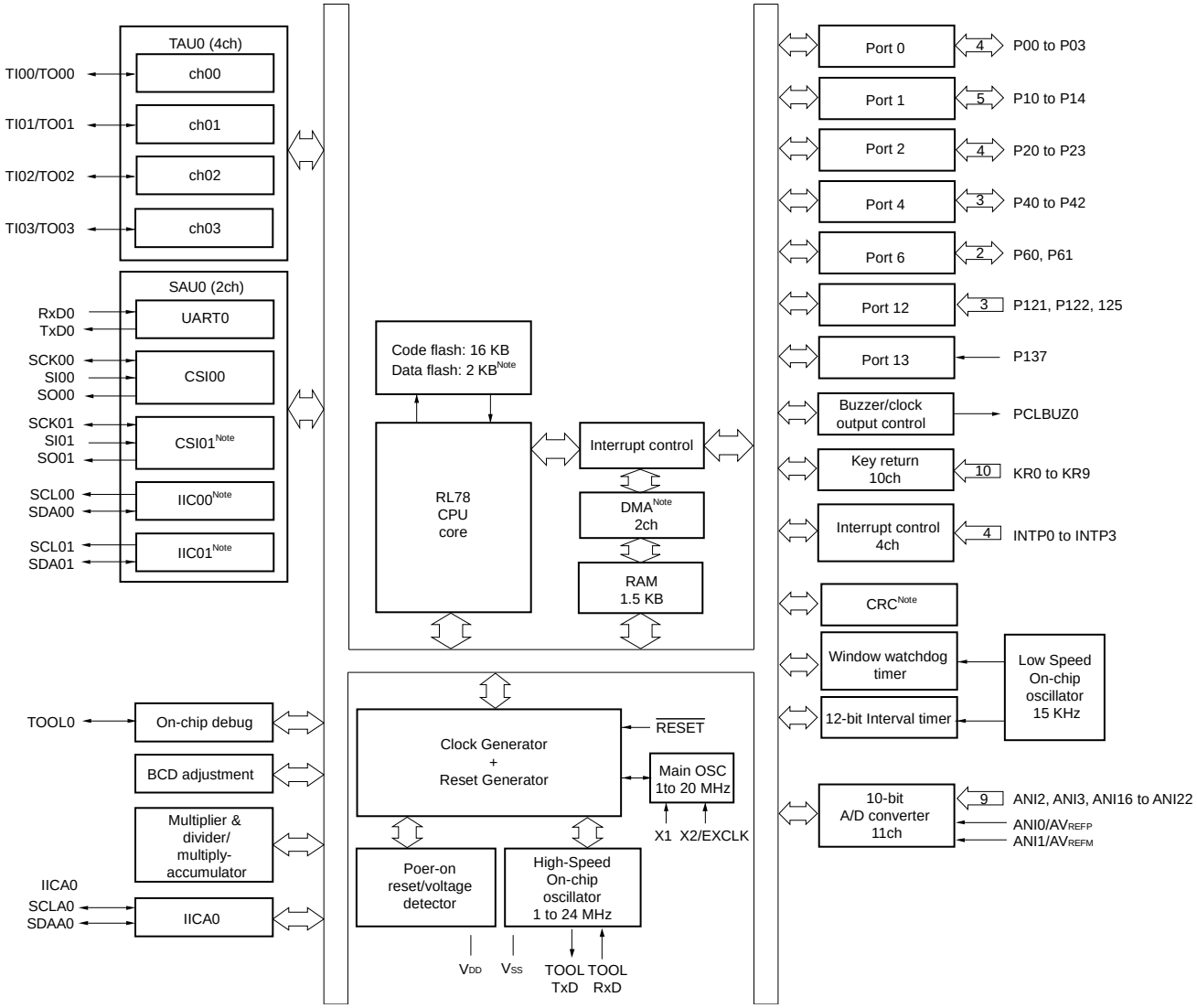
## 1.6 Block Diagram

### 1.6.1 20-pin products



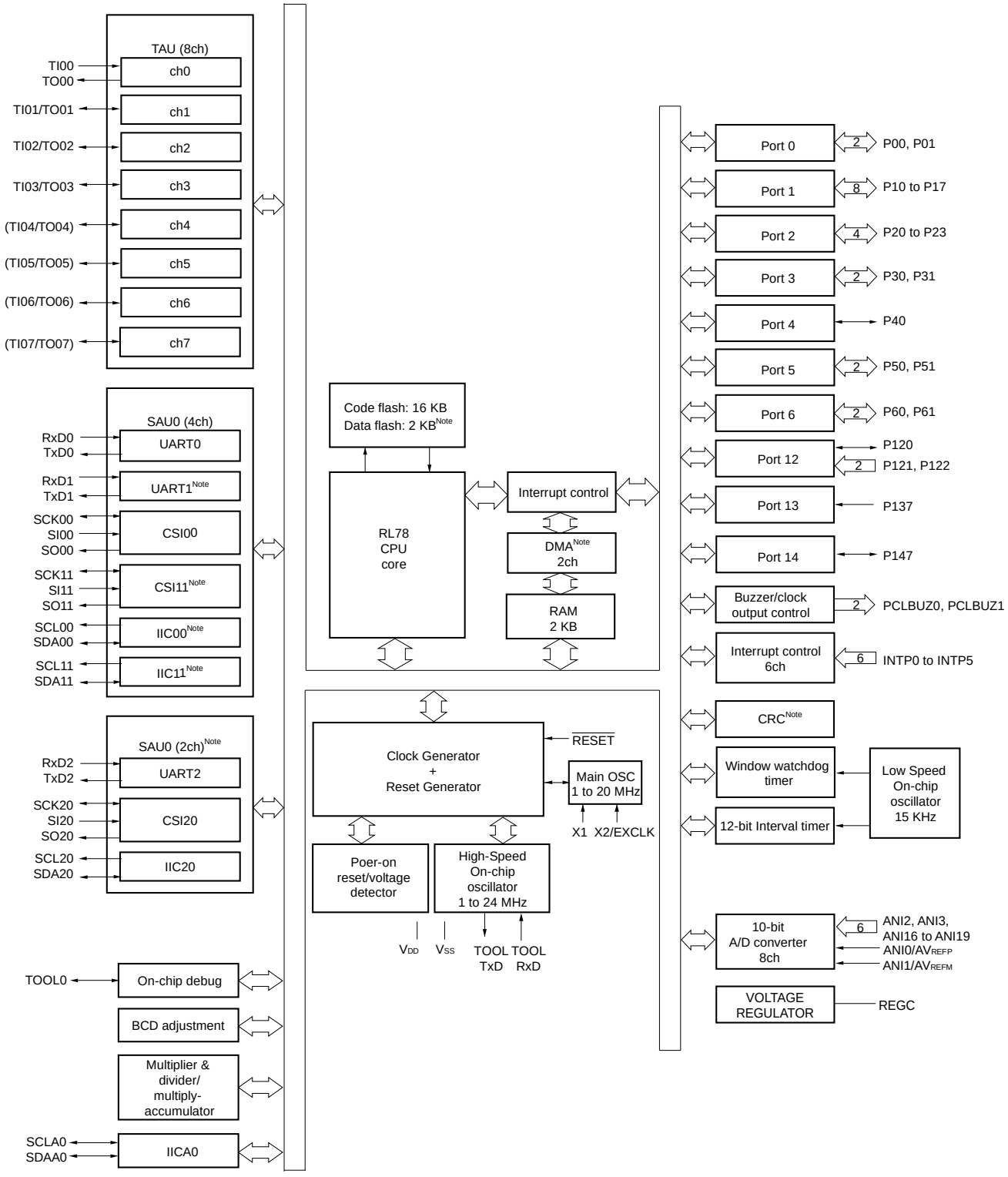

**Note** Provided only in the R5F102 products.

### 1.6.2 24-pin products




**Note** Provided only in the R5F102 products.

### 1.6.3 30-pin products




**Note** Provided only in the R5F102 products.

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G12 User's Manual.

## 1.7 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

| Item | | 20-pin | | 24-pin | | 30-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F1026x | R5F1036x | R5F1027x | R5F1037x | R5F102Ax | R5F103Ax |
| Code flash memory | | 2 to 16 KB Note 1 | | 4 to 16 KB | | | |
| Data flash memory | | 2 KB | – | 2 KB | – | 2 KB | – |
| RAM | | 256 B to 1.5 KB | | 512 B to 1.5 KB | | 512 B to 2KB | |
| Address space | | 1 MB | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode : 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode : 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode : 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V) | | | | | |
| | High-speed on-chip oscillator clock | HS (High-speed main) mode : 1 to 24 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode : 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode : 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V) | | | | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP) | | | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | | | |
| Minimum instruction execution time | | 0.04167 µs (High-speed on-chip oscillator clock: $f_{IH}$ = 24 MHz operation) | | | | | |
| | | 0.05 µs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | |
| Instruction set | | ● Data transfer (8/16 bits)<br>● Adder and subtractor/logical operation (8/16 bits)<br>● Multiplication (8 bits × 8 bits)<br>● Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc. | | | | | |
| I/O port | Total | 18 | | 22 | | 26 | |
| | CMOS I/O | 12<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand voltage]: 4) | | 16<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand voltage]: 5) | | 21<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand voltage]: 9) | |
| | CMOS input | 4 | | 4 | | 3 | |
| | N-ch open-drain I/O<br>(6 V tolerance) | 2 | | | | | |
| Timer | 16-bit timer | 4 channels | | | | 8 channels | |
| | Watchdog timer | 1 channel | | | | | |
| | 12-bit Interval timer | 1 channel | | | | | |
| | Timer output | 4 channels<br>(PWM outputs: 3 Note 3) | | | | 8 channels<br>(PWM outputs: 7 Notes 2, 3) | |

**Notes 1.** The self-programming function cannot be used in the R5F10266 and R5F10366.

**2.** The maximum number of channels when PIOR0 is set to 1.

**3.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (See **6.9.3 Operation as multiple PWM output function** in the RL78/G12 User's Manual.)

**Caution When the flash memory is rewritten via a user program, the code flash area and RAM area are used because each library is used. When using the library, refer to RL78 Family Flash Self Programming Library Type01 User's Manual and RL78 Family Data Flash Library Type04 User's Manual.**

(2/2)

| Item | | 20-pin | | 24-pin | | 30-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F1026x | R5F1036x | R5F1027x | R5F1037x | R5F102Ax | R5F103Ax |
| Clock output/buzzer output | | 1 | | | | 2 | |
| | | 2.44 kHz to 10 MHz: (Peripheral hardware clock: $f_{MAIN}$ = 20 MHz operation) | | | | | |
| 8/10-bit resolution A/D converter | | 11 channels | | | | 8 channels | |
| Serial interface | | [R5F1026x (20-pin), R5F1027x (24-pin)]<br>● CSI: 2 channels/Simplified $I^2C$: 2 channels/UART: 1 channel<br>[R5F102Ax (30-pin)]<br>● CSI: 1 channel/Simplified $I^2C$: 1 channel/UART: 1 channel<br>● CSI: 1 channel/Simplified $I^2C$: 1 channel/UART: 1 channel<br>● CSI: 1 channel/Simplified $I^2C$: 1 channel/UART: 1 channel<br>[R5F1036x (20-pin), R5F1037x (24-pin)]<br>● CSI: 1 channel/Simplified $I^2C$: 0 channel/UART: 1 channel<br>[R5F103Ax (30-pin)]<br>● CSI: 1 channel/Simplified $I^2C$: 0 channel/UART: 1 channel | | | | | |
| | $I^2C$ bus | 1 channel | | | | | |
| Multiplier and divider/multiply-accumulator | | ● 16 bits × 16 bits = 32 bits (unsigned or signed)<br>● 32 bits × 32 bits = 32 bits (unsigned)<br>● 16 bits × 16 bits + 32 bits = 32 bits (unsigned or signed) | | | | | |
| DMA controller | | 2 channels | – | 2 channels | – | 2 channels | – |
| Vectored interrupt sources | Internal | 18 | 16 | 18 | 16 | 26 | 19 |
| | External | 5 | | | | 6 | |
| Key interrupt | | 6 | | 10 | | – | |
| Reset | | ● Reset by $\overline{\text{RESET}}$ pin<br>● Internal reset by watchdog timer<br>● Internal reset by power-on-reset<br>● Internal reset by voltage detector<br>● Internal reset by illegal instruction execution Note<br>● Internal reset by RAM parity error<br>● Internal reset by illegal-memory access | | | | | |
| Power-on-reset circuit | | ● Power-on-reset: 1.51 V (TYP)<br>● Power-down-reset: 1.50 V (TYP) | | | | | |
| Voltage detector | | ● Rising edge : 1.88 to 4.06 V (12 stages)<br>● Falling edge : 1.84 to 3.98 V (12 stages) | | | | | |
| On-chip debug function | | Provided | | | | | |
| Power supply voltage | | $V_{DD}$ = 1.8 to 5.5 V | | | | | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C (A: Consumer applications, D: Industrial applications), $T_A$ = –40 to +105°C (G: Industrial applications) | | | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

# 2. ELECTRICAL SPECIFICATIONS ($T_A$ = –40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A$ = -40 to +85°C
R5F102xxAxx, R5F103xxAxx
D: Industrial applications $T_A$ = -40 to +85°C
R5F102xxDxx, R5F103xxDxx
G: Industrial applications when $T_A$ = -40 to +105°C products is used in the range of $T_A$ = -40 to +85°C
R5F102xxGxx

**Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G12 User's Manual.**

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | –0.5 to + 6.5 | V |
| REGC terminal input voltage[Note1] | $V_{IREGC}$ | REGC | | –0.3 to +2<br>and –0.3 to $V_{DD}$ + 0.3<br>Note 2 | V |
| Input Voltage | $V_{I1}$ | Other than P60, P61 | | –0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | –0.3 to 6.5 | V |
| Output Voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| Analog input voltage | $V_{AI}$ | 20-, 24-pin products: ANI0 to ANI3, ANI16 to ANI22<br>30-pin products: ANI0 to ANI3, ANI16 to ANI19 | | –0.3 to $V_{DD}$ + 0.3<br>and –0.3 to $AV_{REF}(+)$+0.3 [Notes 3, 4] | V |
| Output current, high | $I_{OH1}$ | Per pin | Other than P20 to P23 | –40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | –170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | –70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14<br>30-pin products: P10 to P17, P30, P31, P50, P51, P147 | –100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P23 | –0.5 | mA |
| | | Total of all pins | | –2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | Other than P20 to P23 | 40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | 170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | 70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14, P60, P61<br>30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Notes 1.** 30-pin product only.

**2.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 µF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

**3.** Must be 6.5 V or lower.

**4.** Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

**5.** 24-pin products only.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

## 2.2 Oscillator Characteristics

### 2.2.1 X1 oscillator characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator / crystal oscillator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 8.0 | |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G12 User's Manual.

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | R5F102 products | $T_A$ = –20 to +85°C | -1.0 | | +1.0 | % |
| | | | $T_A$ = –40 to –20°C | -1.5 | | +1.5 | % |
| | | R5F103 products | | -5.0 | | +5.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | –10.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –30.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –6.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | –4.5 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –80.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –18.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | –10.0 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | | | | –100 | mA |
| | $I_{OH2}$ | Per pin for P20 to P23 | | | | –0.1 | mA |
| | | Total of all pins | | | | –0.4 | mA |

**Notes 1.** value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Caution P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03 Note 4, P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | 20.0 Note 2 | mA |
| | | Per pin for P60, P61 | | | | 15.0 Note 2 | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% Note 3) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 60.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 9.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 1.8 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03 Note 4, P10 to P14, P60, P61<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147<br>(When duty ≤ 70% Note 3) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 27.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 5.4 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 140 | mA |
| | $I_{OL2}$ | Per pin for P20 to P23 | | | | 0.4 | mA |
| | | Total of all pins | | | | 1.6 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (3/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 2.2 | | $V_{DD}$ | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 2.0 | | $V_{DD}$ | V |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V | 1.5 | | $V_{DD}$ | V |
| | $V_{IH3}$ | P20 to P23 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P23 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –10.0 mA | $V_{DD}$–1.5 | | | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $V_{DD}$–0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $V_{DD}$–0.6 | | | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $V_{DD}$–0.5 | | | V |
| | $V_{OH2}$ | P20 to P23 | $I_{OH2}$ = –100 µA | $V_{DD}$–0.5 | | | V |

**Notes 1.** 20, 24-pin products only.

**2.** 24-pin products only.

**Caution The maximum value of $V_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is $V_{DD}$ even in N-ch open-drain mode.**
**High level is not output in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (4/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, low | $V_{OL1}$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 20.0 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P23 | $I_{OL2}$ = 400 µA | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 2.0 mA | | | 0.4 | V |
| Input leakage current, high | $I_{LIH1}$ | Other than P121, P122 | $V_I$ = $V_{DD}$ | | | 1 | µA |
| | $I_{LIH2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{DD}$ Input port or external clock input | | | 1 | µA |
| | | | $V_I$ = $V_{DD}$ When resonator connected | | | 10 | µA |
| Input leakage current, low | $I_{LIL1}$ | Other than P121, P122 | $V_I$ = $V_{SS}$ | | | –1 | µA |
| | $I_{LIL2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{SS}$ Input port or external clock input | | | –1 | µA |
| | | | $V_I$ = $V_{SS}$ When resonator connected | | | –10 | µA |
| On-chip pull-up resistance | $R_U$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | $V_I$ = $V_{SS}$, input port | 10 | 20 | 100 | kΩ |

**Note** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 2.3.2 Supply current characteristics

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS(High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.0 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.5 | 3.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | 3.7 | |
| | | | LS(Low-speed main) mode[Note 4] | $f_{IH}$ = 8 MHz[Note 3] | | $V_{DD}$ = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.8 | |
| | | | HS(High-speed main) mode[Note4] | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 2.8 | 4.4 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.6 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 2.8 | 4.4 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.6 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.8 | 2.6 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.6 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.8 | 2.6 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.6 | |
| | | | LS(Low-speed main) mode[Note 4] | $f_{MX}$ = 8 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |
| | | | | $f_{MX}$ = 8 MHz[Note 2], $V_{DD}$ = 2.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 1210 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 1210 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 950 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 950 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 542 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 542 | |
| | | | HS (High-speed main) mode Note 6 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 590 | μA |
| | | | | | Resonator connection | | 260 | 660 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 590 | μA |
| | | | | | Resonator connection | | 260 | 660 | |
| | | | LS (Low-speed main) mode Note 6 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 150 | 416 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 360 | μA |
| | | | | | Resonator connection | | 150 | 416 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.19 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.32 | 0.80 | |
| | | | $T_A$ = +70°C | | | | 0.48 | 1.20 | |
| | | | $T_A$ = +85°C | | | | 0.74 | 2.20 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except temperature condition of the TYP. value is $T_A$ = 25°C, other than STOP mode

**(2) 30-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS (High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.5 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.7 | 4.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.0 | |
| | | | LS (Low-speed main) mode[Note 4] | $f_{IH}$ = 8 MHz[Note 3] | | $V_{DD}$ = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.8 | |
| | | | HS (High-speed main) mode[Note 4] | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | |
| | | | LS (Low-speed main) mode[Note 4] | $f_{MX}$ = 8 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |
| | | | | $f_{MX}$ = 8 MHz[Note 2], $V_{DD}$ = 2.0 V | | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

**(2) 30-pin products**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD2}$[Note 2] | HALT mode | HS (High-speed main) mode[Note 6] | $f_{IH}$ = 24 MHz[Note 4] | $V_{DD}$ = 5.0 V | | 440 | 1280 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 1280 | |
| | | | | $f_{IH}$ = 16 MHz[Note 4] | $V_{DD}$ = 5.0 V | | 400 | 1000 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1000 | |
| | | | LS (Low-speed main) mode[Note 6] | $f_{IH}$ = 8 MHz[Note 4] | $V_{DD}$ = 3.0 V | | 260 | 530 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 530 | |
| | | | HS (High-speed main) mode[Note 6] | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1000 | μA |
| | | | | | Resonator connection | | 450 | 1170 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 190 | 600 | μA |
| | | | | | Resonator connection | | 260 | 670 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 190 | 600 | μA |
| | | | | | Resonator connection | | 260 | 670 | |
| | | | LS (Low-speed main) mode[Note 6] | $f_{MX}$ = 8 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | | | | $f_{MX}$ = 8 MHz[Note 3], $V_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | |
| | $I_{DD3}$[Note 5] | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

LS (Low speed main) mode: $V_{DD}$ = 1.8 V to 5.5 V @1 MHz to 8 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

### (3) Peripheral functions (Common to all products)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed onchip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 4 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 5 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.30 | 1.70 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.50 | 0.70 | mA |
| A/D converter reference voltage operating current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 6 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 8 | | | | 2.00 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 7 | | | | 2.00 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 9 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes 1.** Current flowing to the $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{FIL}$ and $I_{TMKA}$ when the 12-bit interval timer operates.

**4.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

**5.** Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**6.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit operates.

**7.** Current flowing only during data flash rewrite.

**8.** Current flowing only during self programming.

**9.** For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode** in the RL78/G12 User's Manual.

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.4 AC Characteristics

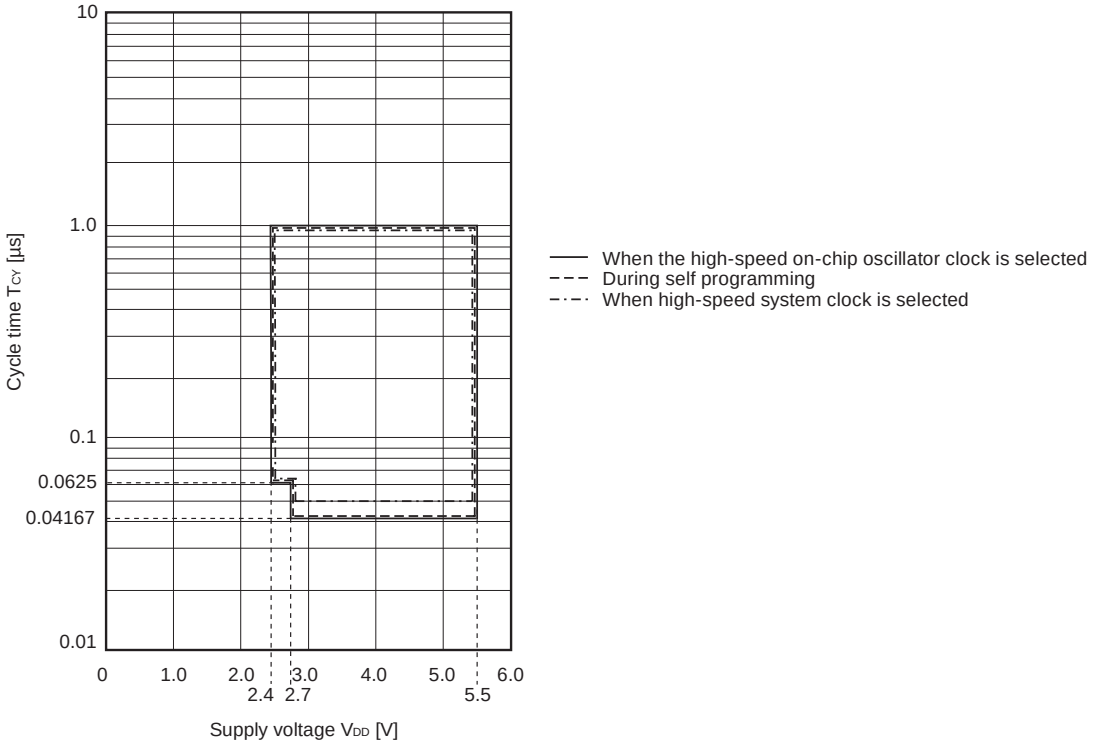
**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (Low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| | | During self programming | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | | LS (Low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | µs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 | | | ns |
| TO00 to TO07 output frequency | $f_{TO}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 12 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| PCLBUZ0, or PCLBUZ1 output frequency | $f_{PCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 16 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| INTP0 to INTP5 input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | | | | 1 | | | µs |
| KR0 to KR9 input available width | $t_{KR}$ | | | | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | µs |

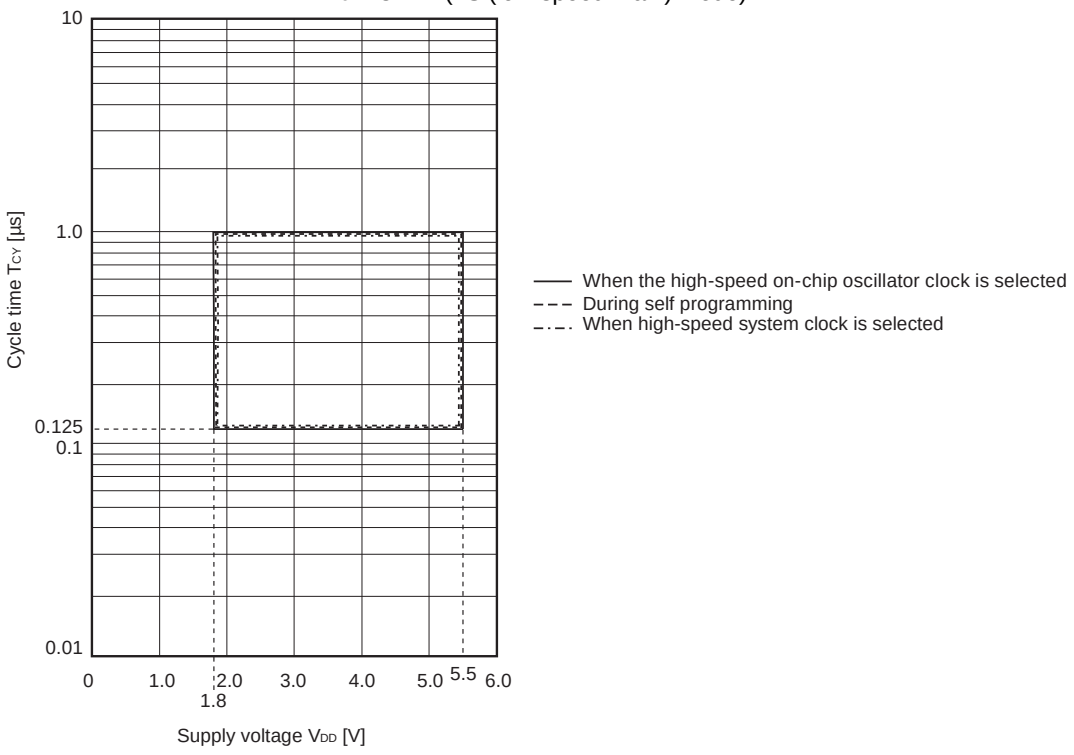
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

**Minimum Instruction Execution Time during Main System Clock Operation**

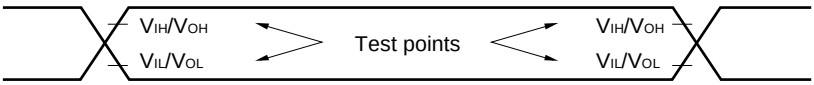
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



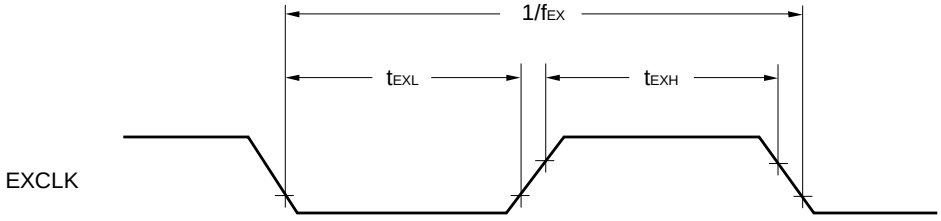

$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



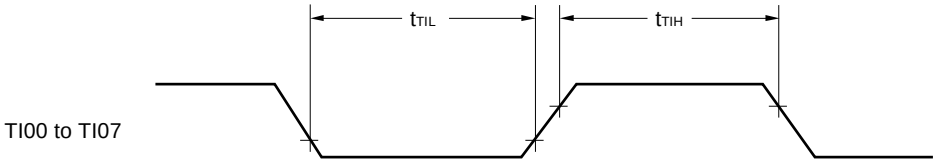
**AC Timing Test Point**

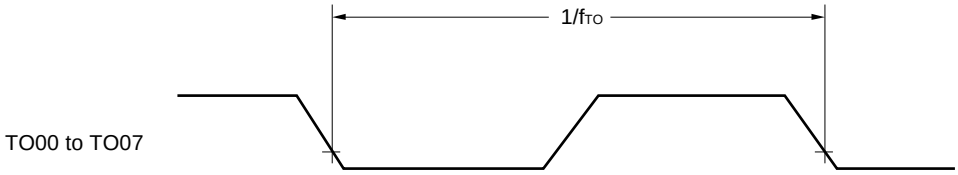



**External Main System Clock Timing**

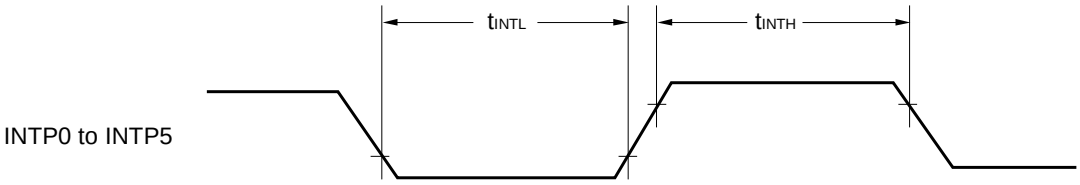



**TI/TO Timing**

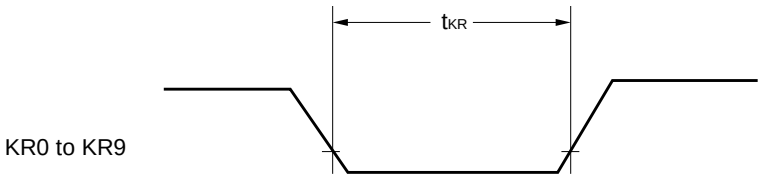


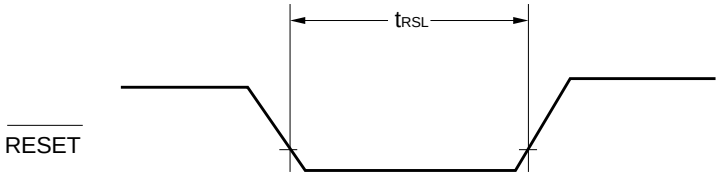

**Interrupt Request Input Timing**




**Key Interrupt Input Timing**

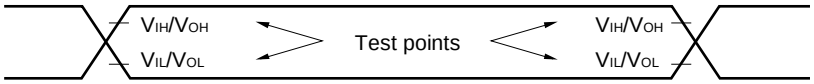



**$\overline{\text{RESET}}$ Input Timing**



## 2.5 Peripheral Functions Characteristics

### AC Timing Test Point




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}$ Note 2 | | 4.0 | | 1.3 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

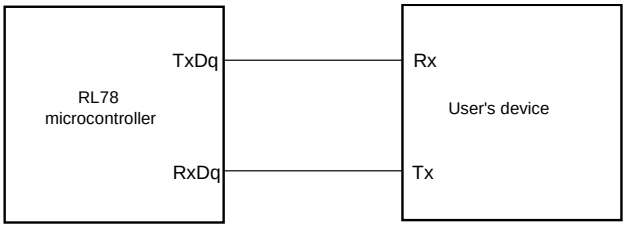
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)

16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

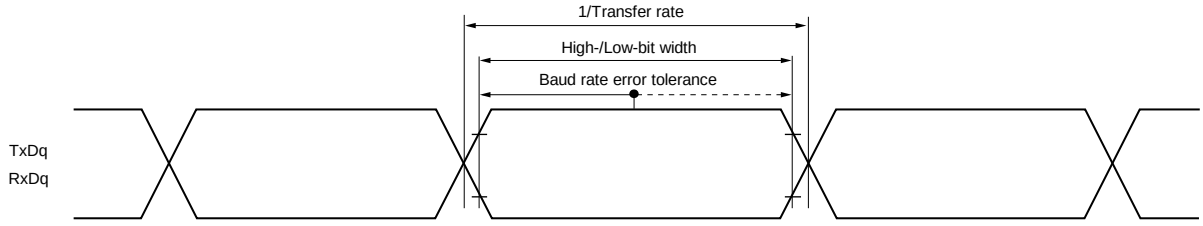
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(2) During communication at same potential (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 83.3 | | 250 | | ns |
| SCK00 high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | $t_{KCY1}/2–7$ | | $t_{KCY1}/2–50$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | $t_{KCY1}/2–10$ | | $t_{KCY1}/2–50$ | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↑) Note 2 | $t_{KSI1}$ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | 10 | | 10 | ns |

**Notes 1.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 setup time becomes “to SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

**2.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The SI00 hold time becomes “from SCK00↓” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

**3.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1. The delay time to SO00 output becomes “from SCK00↑” when DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

**4.** C is the load capacitance of the SCK00 and SO00 output lines.

**Caution Select the normal input buffer for the SI00 pin and the normal output mode for the SO00 and SCK00 pins by using port input mode register 1 (PIM1) and port output mode register 1 (POM1).**

**Remarks 1.** This specification is valid only when CSI00’s peripheral I/O redirect function is not used.

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 167 | | 500 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 250 | | 500 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | – | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2–12 | | $t_{KCY1}$/2–50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2–18 | | $t_{KCY1}$/2–50 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2–38 | | $t_{KCY1}$/2–50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | $t_{KCY1}$/2–50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | 44 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 44 | | 110 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 75 | | 110 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | | | 25 | | 25 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).**

**Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | – | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 6/$f_{MCK}$ and 750 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–7 | | $t_{KCY2}$/2–7 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–8 | | $t_{KCY2}$/2–8 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–18 | | $t_{KCY2}$/2–18 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | $t_{KCY2}$/2–18 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 75 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | – | | 2/$f_{MCK}$ + 110 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

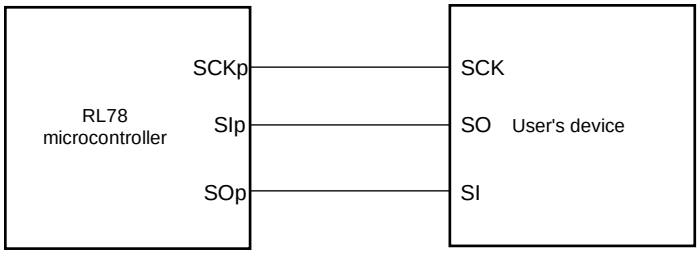
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

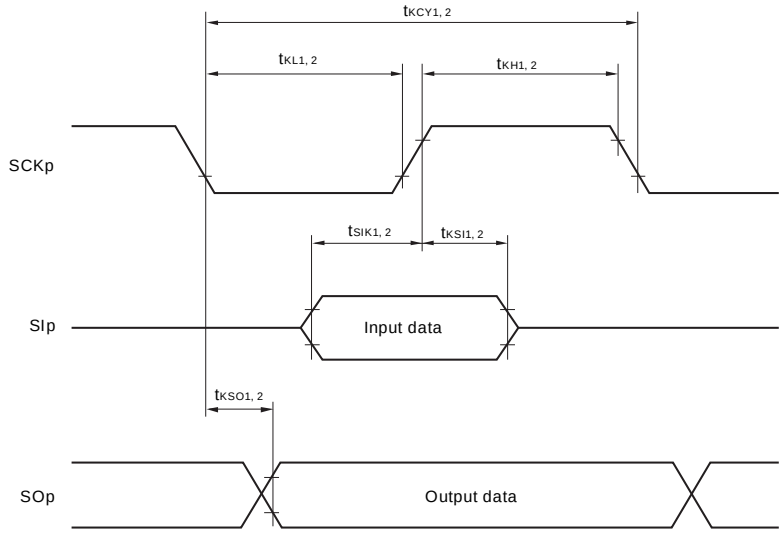
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps.

**Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).**

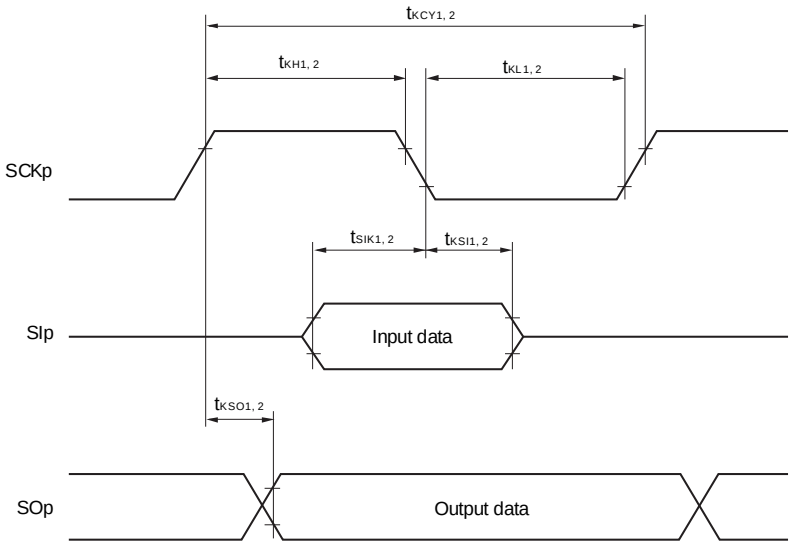
**CSI mode connection diagram (during communication at same potential)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




(**Remarks** are listed on the next page.)

**Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3: “1, 3” is only for the R5F102 products.))

**(5) During communication at same potential (simplified $I^2C$ mode)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode<br>LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | $1/f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | $1/f_{MCK}$ + 230 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | ns |

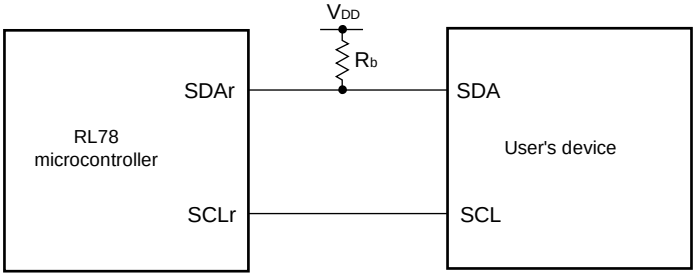
**Notes 1.** The value must be equal to or less than $f_{MCK}$/4.

**2.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = “L” or SCLr = “H”.

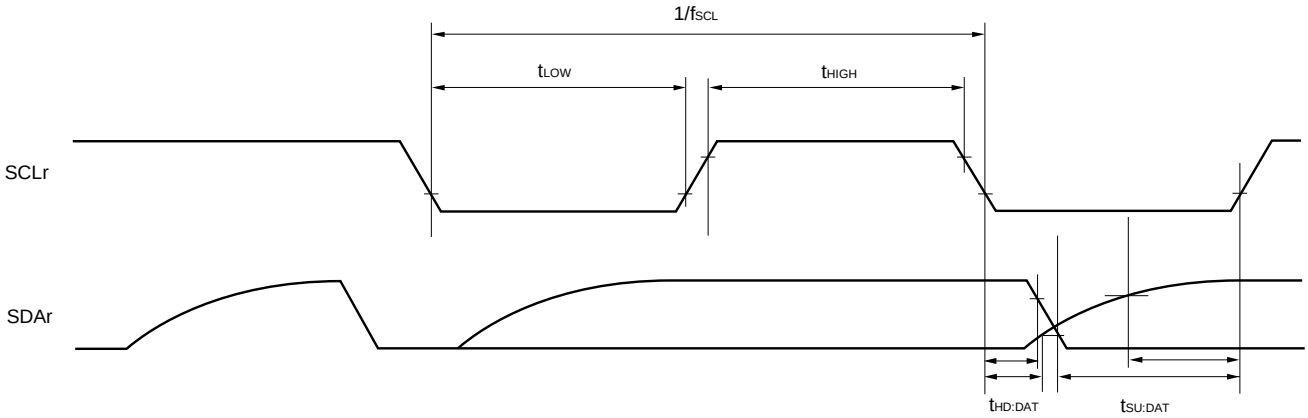
**Caution Select the N-ch open drain output ($V_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$ [Ω]:Communication line (SDAr) pull-up resistance
$C_b$ [F]: Communication line (SCLr, SDAr) load capacitance

**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

**4.** Simplified I²C mode is supported only by the R5F102 products.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate **Note4** | | Reception | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | $f_{MCK}$/6 **Note1** | | $f_{MCK}$/6 **Note1** | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note3** | | 4.0 | | 1.3 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/6 **Note1** | | $f_{MCK}$/6 **Note1** | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note3** | | 4.0 | | 1.3 | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | $f_{MCK}$/6 **Notes1, 2** | | $f_{MCK}$/6 **Notes1, 2** | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note3** | | 4.0 | | 1.3 | Mbps |
| | | Transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | **Note4** | | **Note4** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.8 **Note5** | | 2.8 **Note5** | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, | | | **Note6** | | **Note6** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 **Note7** | | 1.2 **Note7** | Mbps |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | **Notes 2, 8** | | **Notes 2, 8** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 **Note9** | | 0.43 **Note9** | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $V_{DD} \geq V_b$.

**3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

**4.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**5.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

**6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**7.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**8.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

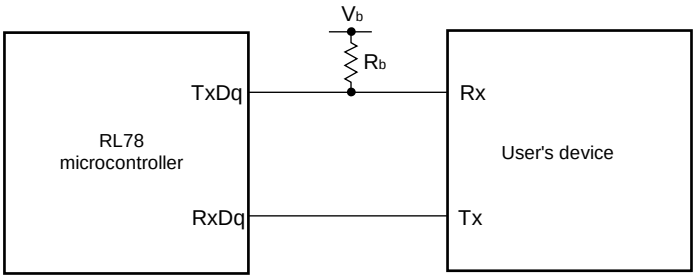
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

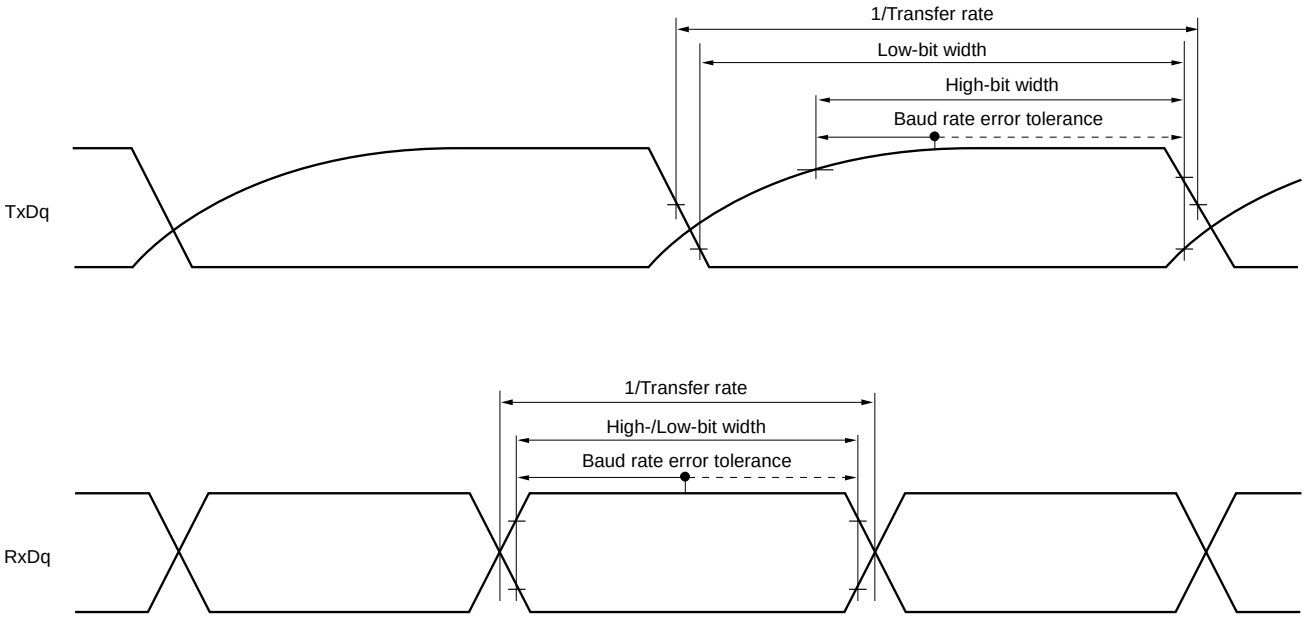
**9.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 8** above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

**(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCK00... internal clock output, corresponding CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCK00 cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | ns |
| SCK00 high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 120 | | $t_{KCY1}$/2 – 120 | | ns |
| SCK00 low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 – 7 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 – 10 | | $t_{KCY1}$/2 – 50 | | ns |
| SI00 setup time (to SCK00↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | ns |
| SI00 hold time (from SCK00↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↓ to SO00 output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | ns |
| SI00 setup time (to SCK00↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 23 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 33 | | 110 | | ns |
| SI00 hold time (from SCK00↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | ns |
| Delay time from SCK00↑ to SO00 output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 10 | | 10 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 10 | | 10 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**Notes 1.** When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1

**2.** When DAP00 = 0 and CKP00 = 1, or DAP00 = 1 and CKP00 = 0.

**Caution Select the TTL input buffer for the SI00 pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SO00 pin and SCK00 pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $R_b$ [Ω]:Communication line (SCK00, SO00) pull-up resistance, $C_b$ [F]: Communication line (SCK00, SO00) load capacitance, $V_b$ [V]: Communication line voltage

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS00 bit of serial mode register 00 (SMR00).)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –75 | | $t_{KCY1}$/2–75 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –170 | | $t_{KCY1}$/2–170 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –458 | | $t_{KCY1}$/2–458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –12 | | $t_{KCY1}$/2–50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –18 | | $t_{KCY1}$/2–50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –50 | | $t_{KCY1}$/2–50 | | ns |

**Note** Use it with $V_{DD}$ ≥ $V_b$.

**Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2. CSI01 and CSI11 cannot communicate at different potential.**

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**2.** Use it with $V_{DD} \geq V_b$.

(**Cautions** and **Remarks** are listed on the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** Use it with $V_{DD} \geq V_b$.

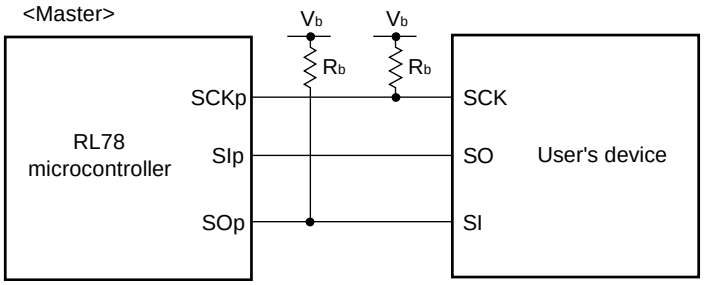
**Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2. CSI01 and CSI11 cannot communicate at different potential.**

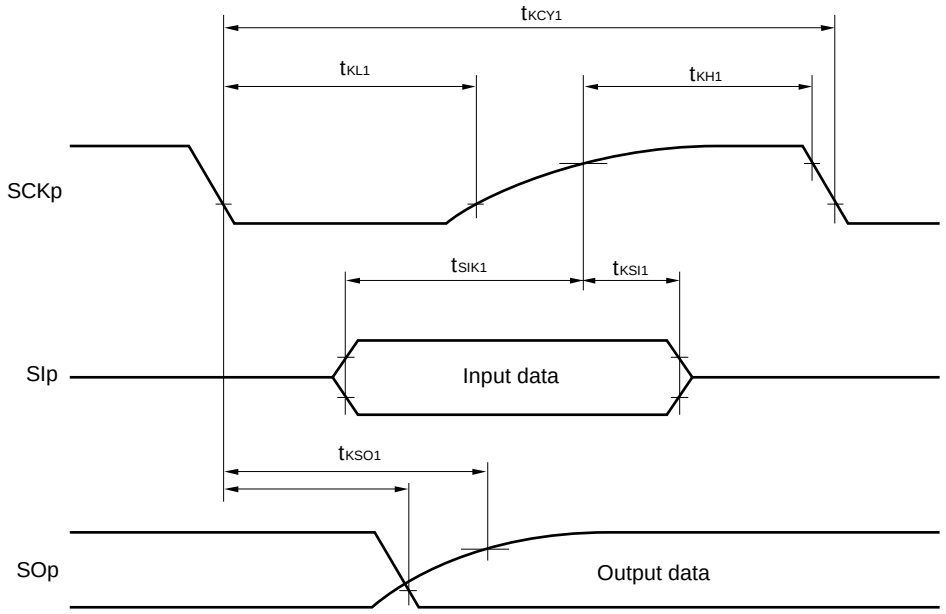
**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

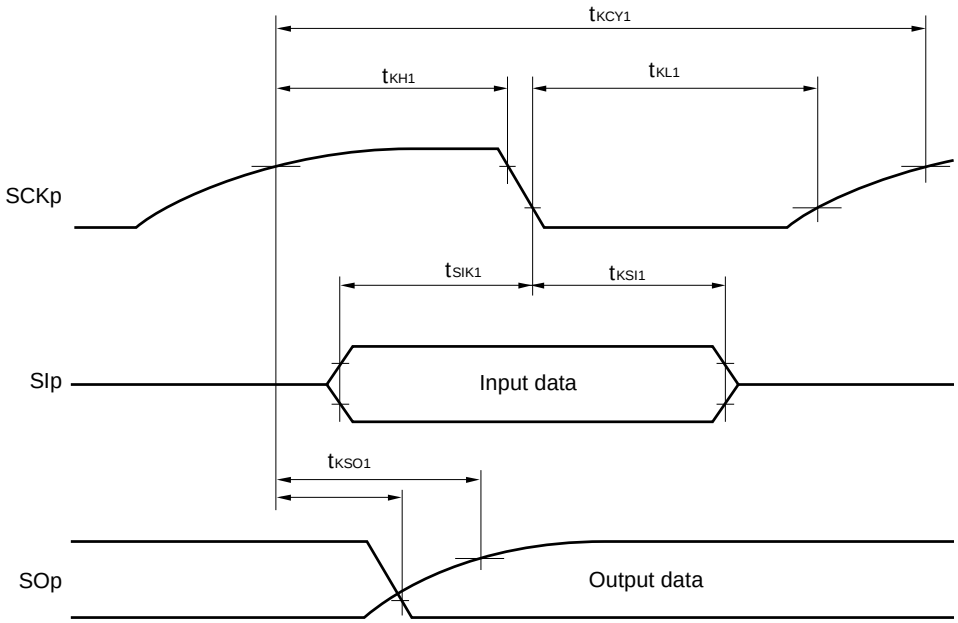
**CSI mode connection diagram (during communication at different potential)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | – | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | – | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | – | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 12 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** Use it with $V_{DD} \geq V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

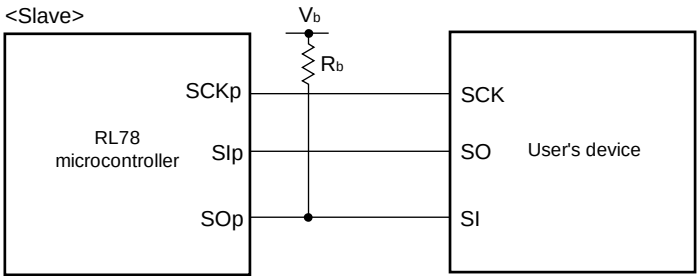
**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2. CSI01 and CSI11 cannot communicate at different potential.**

**CSI mode connection diagram (during communication at different potential)**

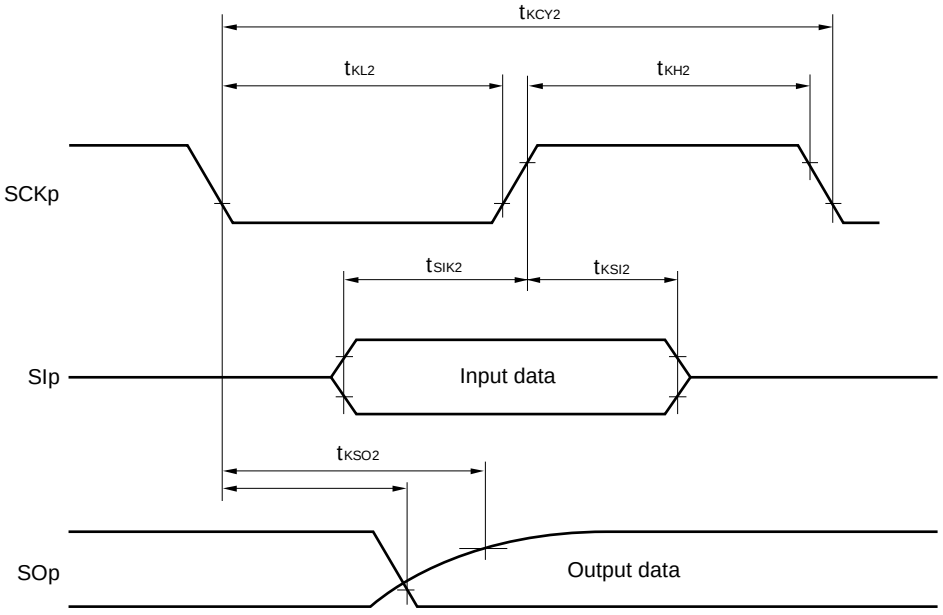



**Remarks 1.** $R_b$ [Ω]: Communication line (SOp) pull-up resistance, $C_b$ [F]: Communication line (SOp) load capacitance, $V_b$ [V]: Communication line voltage

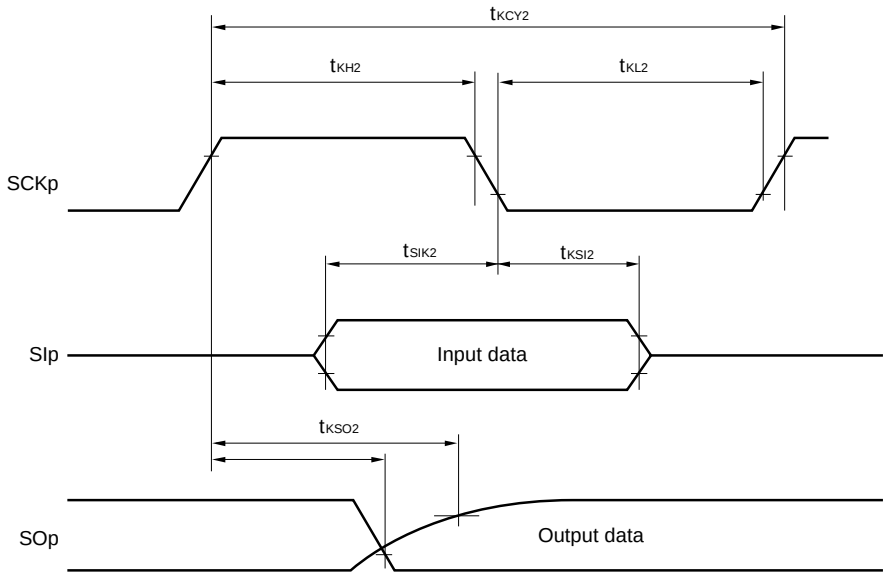
**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 10))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note1 | | 300 Note1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note1 | | 300 Note1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note1 | | 300 Note1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | $1/f_{MCK}$ + 190 Note3 | | $1/f_{MCK}$ + 190 Note3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 190 Note3 | | $1/f_{MCK}$ + 190 Note3 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | $1/f_{MCK}$ + 190 Note3 | | $1/f_{MCK}$ + 190 Note3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, Note2 $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | ns |

**Notes 1.** The value must be equal to or less than $f_{MCK}$/4.

**2.** Use it with $V_{DD} \geq V_b$.

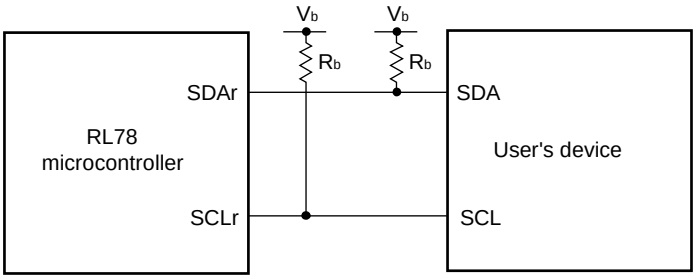
**3.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = “L” or SCLr = “H”.

**Cautions 1. Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

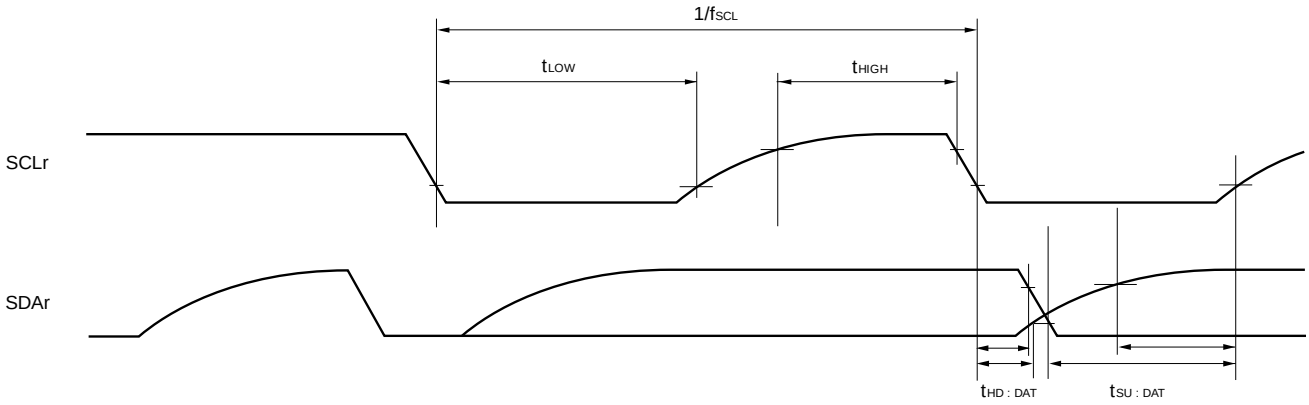
**2. IIC01 and IIC11 cannot communicate at different potential.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$ [F]: Communication line (SDAr, SCLr) load capacitance, $V_b$ [V]: Communication line voltage

**2.** r: IIC Number (r = 00, 20)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

**4.** Simplified I²C mode is supported only by the R5F102 products.

### 2.5.2 Serial interface IICA

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode / LS (low-speed main) mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | | | 0 | 400 | kHz |
| | | Normal mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | 0.6 | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | 0.6 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 4.7 | | 1.3 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 4.0 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

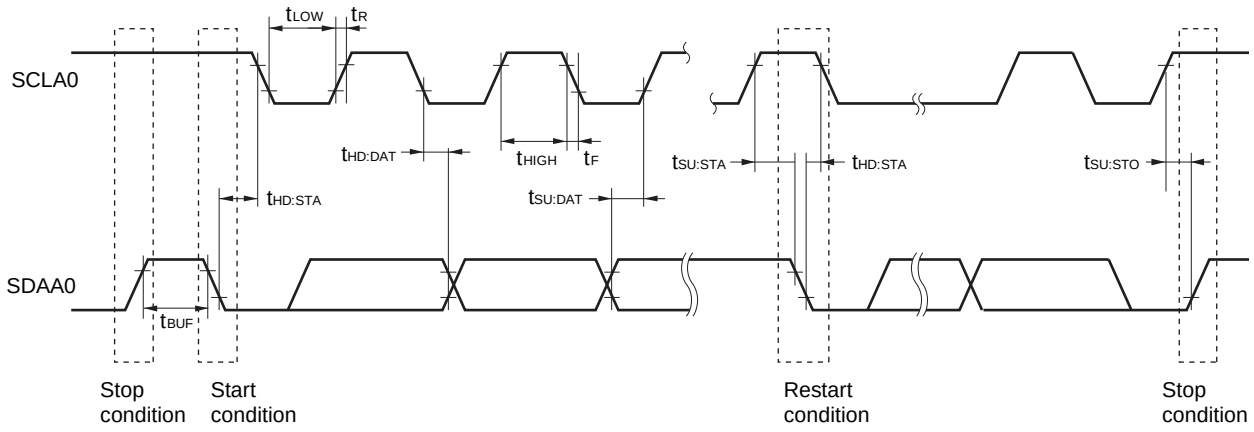
**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b$ = 400 pF, Rb = 2.7 kΩ
Fast mode: $C_b$ = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI3 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI22 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | – |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | | | 1.2 | ±3.5 | LSB |
| | | | | | 1.2 | ±7.0 Note 4 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2, ANI3 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | | 57 | | 95 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | | | | ±0.25 | %FSR |
| | | | | | | ±0.50 Note 4 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | | | | ±0.25 | %FSR |
| | | | | | | ±0.50 Note 4 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | | | | ±2.5 | LSB |
| | | | | | | ±5.0 Note 4 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | | | | ±1.5 | LSB |
| | | | | | | ±2.0 Note 4 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2, ANI3 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 5 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 5 | | | V |

(**Notes** are listed on the next page.)

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Values when the conversion time is set to 57 µs (min.) and 95 µs (max.).

**5.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | 1.2 | ±5.0 | LSB |
| | | | | | 1.2 | ±8.5 Note 4 | LSB |
| Conversion time | tCONV | 10-bit resolution<br>Target ANI pin: ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | | 57 | | 95 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| | | | | | | ±0.60 Note 4 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| | | | | | | ±0.60 Note 4 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±3.5 | LSB |
| | | | | | | ±6.0 Note 4 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±2.0 | LSB |
| | | | | | | ±2.5 Note 4 | LSB |
| Analog input voltage | VAIN | ANI16 to ANI22 | | 0 | | $AV_{REFP}$ and $V_{DD}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** When the conversion time is set to 57 µs (min.) and 95 µs (max.).

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | | | 1.2 | ±7.0 | LSB |
| | | | | | 1.2 | ±10.5 Note 3 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | | | 57 | | 95 | µs |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution | | | | ±0.60 | %FSR |
| | | | | | | ±0.85 Note 3 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution | | | | ±0.60 | %FSR |
| | | | | | | ±0.85 Note 3 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | | | | ±4.0 | LSB |
| | | | | | | ±6.5 Note 3 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | | | | ±2.0 | LSB |
| | | | | | | ±2.5 Note 3 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI3, ANI16 to ANI22 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When the conversion time is set to 57 µs (min.) and 95 µs (max.).

**4.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22**

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 8-bit resolution | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

### 2.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode**

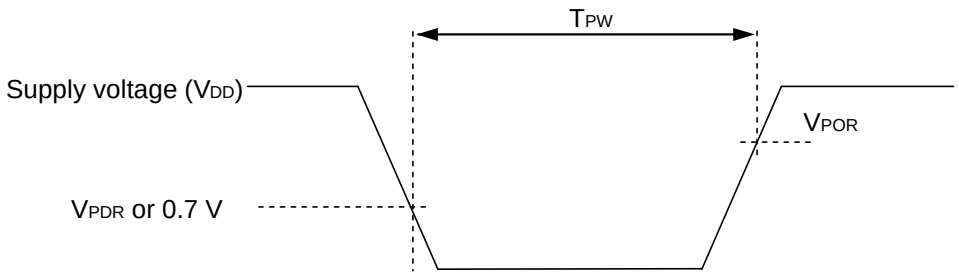
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.50 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Power supply fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 2.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**

**($T_A$ = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection supply voltage | $V_{LVD0}$ | Power supply rise time | 3.98 | 4.06 | 4.14 | V |
| | | Power supply fall time | 3.90 | 3.98 | 4.06 | V |
| | $V_{LVD1}$ | Power supply rise time | 3.68 | 3.75 | 3.82 | V |
| | | Power supply fall time | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVD2}$ | Power supply rise time | 3.07 | 3.13 | 3.19 | V |
| | | Power supply fall time | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVD3}$ | Power supply rise time | 2.96 | 3.02 | 3.08 | V |
| | | Power supply fall time | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVD4}$ | Power supply rise time | 2.86 | 2.92 | 2.97 | V |
| | | Power supply fall time | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVD5}$ | Power supply rise time | 2.76 | 2.81 | 2.87 | V |
| | | Power supply fall time | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVD6}$ | Power supply rise time | 2.66 | 2.71 | 2.76 | V |
| | | Power supply fall time | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVD7}$ | Power supply rise time | 2.56 | 2.61 | 2.66 | V |
| | | Power supply fall time | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVD8}$ | Power supply rise time | 2.45 | 2.50 | 2.55 | V |
| | | Power supply fall time | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVD9}$ | Power supply rise time | 2.05 | 2.09 | 2.13 | V |
| | | Power supply fall time | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVD10}$ | Power supply rise time | 1.94 | 1.98 | 2.02 | V |
| | | Power supply fall time | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVD11}$ | Power supply rise time | 1.84 | 1.88 | 1.91 | V |
| | | Power supply fall time | 1.80 | 1.84 | 1.87 | V |
| Minimum pulse width | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | 300 | µs |

**LVD detection voltage of interrupt & reset mode**

**($T_A$ = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 1.94 | 1.98 | 2.02 | V |
| | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.05 | 2.09 | 2.13 | V |
| | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.07 | 3.13 | 3.19 | V |
| | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 2.56 | 2.61 | 2.66 | V |
| | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.66 | 2.71 | 2.76 | V |
| | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.68 | 3.75 | 3.82 | V |
| | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC1}$ = 0, 1, 1, falling reset voltage | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.96 | 3.02 | 3.08 | V |
| | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.98 | 4.06 | 4.14 | V |
| | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

### 2.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

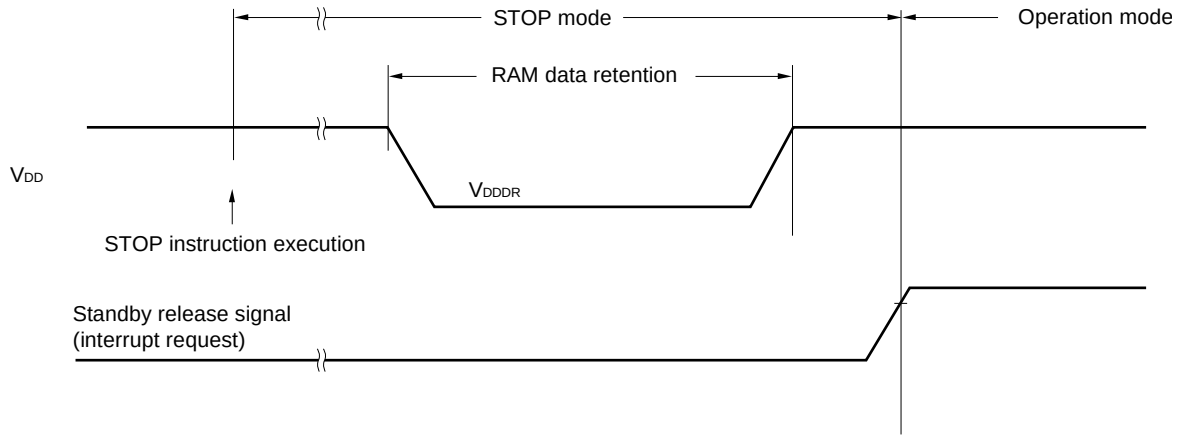
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

## 2.7 RAM Data Retention Characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | | 1 | | 24 | MHz |
| Code flash memory rewritable times Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C | 1,000 | | | Times |
| Data flash memory rewritable times Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

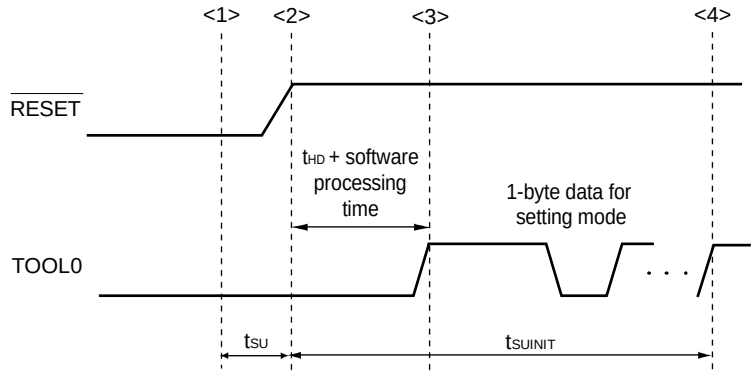
**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset are released before external reset release | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset are released before external reset release | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released<br>(excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset are released before external reset release | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = –40 to +105°C)

This chapter describes the following electrical specifications.
Target products G: Industrial applications $T_A$ = -40 to +105°C
R5F102xxGxx

**Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G12 User's Manual.**

**3. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When the RL78 microcontroller is used in the range of $T_A$ = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)**.

There are following differences between the products "G: Industrial applications ($T_A$ = -40 to +105°C)" and the products "A: Consumer applications, and D: Industrial applications".

| Parameter | Application | |
|---|---|---|
| | A: Consumer applications, D: Industrial applications | G: Industrial applications |
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode<br>Operating voltage range | HS (high-speed main) mode:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz<br>LS (low-speed main) mode:<br>1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz | HS (high-speed main) mode only:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | R5F102 products, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±1.0%@ $T_A$ = -20 to +85°C<br>±1.5%@ $T_A$ = -40 to -20°C<br>R5F103 products, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±5.0%@ $T_A$ = -40 to +85°C | R5F102 products, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±2.0%@ $T_A$ = +85 to +105°C<br>±1.0%@ $T_A$ = -20 to +85°C<br>±1.5%@ $T_A$ = -40 to -20°C |
| Serial array unit | UART<br>CSI: $f_{CLK}$/2 (supporting 12 Mbps), $f_{CLK}$/4<br>Simplified $I^2C$ communication | UART<br>CSI: $f_{CLK}$/4<br>Simplified $I^2C$ communication |
| Voltage detector | Rise detection voltage: 1.88 V to 4.06 V (12 levels)<br>Fall detection voltage: 1.84 V to 3.98 V (12 levels) | Rise detection voltage: 2.61 V to 4.06 V (8 levels)<br>Fall detection voltage: 2.55 V to 3.98 V (8 levels) |

**Remark** The electrical characteristics of the products G: Industrial applications ($T_A$ = -40 to +105°C) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **3.1** to **3.10**.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | –0.5 to + 6.5 | V |
| REGC terminal input voltage[Note1] | $V_{IREGC}$ | REGC | | –0.3 to +2.8 and –0.3 to $V_{DD}$ + 0.3 [Note 2] | V |
| Input Voltage | $V_{I1}$ | Other than P60, P61 | | –0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | –0.3 to 6.5 | V |
| Output Voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3[Note 3] | V |
| Analog input voltage | $V_{AI}$ | 20, 24-pin products: ANI0 to ANI3, ANI16 to ANI22<br>30-pin products: ANI0 to ANI3, ANI16 to ANI19 | | –0.3 to $V_{DD}$ + 0.3 and –0.3 to $AV_{REF}(+)$+0.3 [Notes 3, 4] | V |
| Output current, high | $I_{OH1}$ | Per pin | Other than P20 to P23 | –40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | –170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | –70 | mA |
| | | | 20-, 24-pin products: P00 to P03[Note 5], P10 to P14<br>30-pin products: P10 to P17, P30, P31, P50, P51, P147 | –100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P23 | –0.5 | mA |
| | | Total of all pins | | –2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | Other than P20 to P23 | 40 | mA |
| | | Total of all pins | All the terminals other than P20 to P23 | 170 | mA |
| | | | 20-, 24-pin products: P40 to P42<br>30-pin products: P00, P01, P40, P120 | 70 | mA |
| | | | 20-, 24-pin products: P00 to P03 [Note 5], P10 to P14, P60, P61<br>30-pin products: P10 to P17, P30, P31, P50, P51, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +105 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Notes 1.** 30-pin product only.

**2.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 µF). This value determines the absolute maximum rating of the REGC pin. Do not use it with voltage applied.

**3.** Must be 6.5 V or lower.

**4.** Do not exceed $AV_{REF}(+)$ + 0.3 V in case of A/D conversion target pin.

**5.** 24-pin products only.

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**3.** $V_{SS}$ : Reference voltage

## 3.2 Oscillator Characteristics

### 3.2.1 X1 oscillator characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)Note | Ceramic resonator / crystal oscillator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 8.0 | |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G12 User's Manual.

### 3.2.2 On-chip oscillator characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 24 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | R5F102 products | $T_A$ = –20 to +85°C | -1.0 | | +1.0 | % |
| | | | $T_A$ = –40 to –20°C | -1.5 | | +1.5 | % |
| | | | $T_A$ = +85 to +105°C | -2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | –3.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –9.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –6.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | –4.5 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | –27.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | –18.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | –10.0 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | | | | –36.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P23 | | | | –0.1 | mA |
| | | Total of all pins | | | | –0.4 | mA |

**Notes 1.** value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Caution P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | 20-, 24-pin products:<br>Per pin for P00 to P03[Note 4], P10 to P14, P40 to P42<br>30-pin products:<br>Per pin for P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | | | 8.5 [Note 2] | mA |
| | | Per pin for P60, P61 | | | | 15.0 [Note 2] | mA |
| | | 20-, 24-pin products:<br>Total of P40 to P42<br>30-pin products:<br>Total of P00, P01, P40, P120<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 25.5 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 9.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.8 | mA |
| | | 20-, 24-pin products:<br>Total of P00 to P03[Note 4], P10 to P14, P60, P61<br>30-pin products:<br>Total of P10 to P17, P30, P31, P50, P51, P60, P61, P147<br>(When duty ≤ 70% [Note 3]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 27.0 | mA |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 5.4 | mA |
| | | Total of all pins (When duty ≤ 70%[Note 3]) | | | | 65.5 | mA |
| | $I_{OL2}$ | Per pin for P20 to P23 | | | | 0.4 | mA |
| | | Total of all pins | | | | 1.6 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $V_{SS}$ pin.

**2.** However, do not exceed the total current value.

**3.** The output current value under conditions where the duty factor ≤ 70%.
If duty factor > 70%: The output current value can be calculated with the following expression (where n represents the duty factor as a percentage).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (3/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 2.2 | | $V_{DD}$ | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 2.0 | | $V_{DD}$ | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 1.5 | | $V_{DD}$ | V |
| | $V_{IH3}$ | Normal input buffer<br>P20 to P23 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| | $V_{IH5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Normal input buffer<br>20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | TTL input buffer<br>20-, 24-pin products: P10, P11<br>30-pin products: P01, P10, P11, P13 to P17 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | 3.3 V ≤ $V_{DD}$ < 4.0 V | 0 | | 0.5 | V |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P23 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60, P61 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL5}$ | P121, P122, P125[Note 1], P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | 20-, 24-pin products: P00 to P03[Note 2], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $V_{DD}$–0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $V_{DD}$–0.6 | | | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $V_{DD}$–0.5 | | | V |
| | $V_{OH2}$ | P20 to P23 | $I_{OH2}$ = –100 µA | $V_{DD}$–0.5 | | | V |

**Notes 1.** 20, 24-pin products only.

**2.** 24-pin products only.

**Caution The maximum value of $V_{IH}$ of pins P10 to P12 and P41 for 20-pin products, P01, P10 to P12, and P41 for 24-pin products, and P00, P10 to P15, P17, and P50 for 30-pin products is $V_{DD}$ even in N-ch open-drain mode.**
**High level is not output in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (4/4)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, low | $V_{OL1}$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P23 | $I_{OL2}$ = 400 µA | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 2.0 mA | | | 0.4 | V |
| Input leakage current, high | $I_{LIH1}$ | Other than P121, P122 | $V_I$ = $V_{DD}$ | | | 1 | µA |
| | $I_{LIH2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{DD}$ Input port or external clock input | | | 1 | µA |
| | | | $V_I$ = $V_{DD}$ When resonator connected | | | 10 | µA |
| Input leakage current, low | $I_{LIL1}$ | Other than P121, P122 | $V_I$ = $V_{SS}$ | | | –1 | µA |
| | $I_{LIL2}$ | P121, P122 (X1, X2/EXCLK) | $V_I$ = $V_{SS}$ Input port or external clock input | | | –1 | µA |
| | | | $V_I$ = $V_{SS}$ When resonator connected | | | –10 | µA |
| On-chip pull-up resistance | $R_U$ | 20-, 24-pin products: P00 to P03[Note], P10 to P14, P40 to P42, P125, $\overline{\text{RESET}}$<br>30-pin products: P00, P01, P10 to P17, P30, P31, P40, P50, P51, P120, P147 | $V_I$ = $V_{SS}$, input port | 10 | 20 | 100 | kΩ |

**Note** 24-pin products only.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 3.3.2 Supply current characteristics

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS (High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.3 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.5 | 3.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | 3.9 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 2.8 | 4.7 | mA |
| | | | | | | Resonator connection | | 3.0 | 4.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.8 | 2.8 | mA |
| | | | | | | Resonator connection | | 1.8 | 2.8 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

**(1) 20-, 24-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD2}$ [Note 2] | HALT mode | HS (High-speed main) mode[Note 6] | $f_{IH}$ = 24 MHz[Note 4] | $V_{DD}$ = 5.0 V | | 440 | 2230 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2230 | |
| | | | | $f_{IH}$ = 16 MHz[Note 4] | $V_{DD}$ = 5.0 V | | 400 | 1650 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1650 | |
| | | | | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1010 | μA |
| | | | | | Resonator connection | | 260 | 1090 | |
| | | | | $f_{MX}$ = 10 MHz[Note 3], $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1010 | μA |
| | | | | | Resonator connection | | 260 | 1090 | |
| | $I_{DD3}$ [Note 5] | STOP mode | $T_A$ = –40°C | | | | 0.19 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.32 | 0.80 | |
| | | | $T_A$ = +70°C | | | | 0.48 | 1.20 | |
| | | | $T_A$ = +85°C | | | | 0.74 | 2.20 | |
| | | | $T_A$ = +105°C | | | | 1.50 | 10.20 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except temperature condition of the TYP. value is $T_A$ = 25°C, other than STOP mode

**(2) 30-pin products**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current[Note 1] | $I_{DD1}$ | Operating mode | HS (High-speed main) mode[Note 4] | $f_{IH}$ = 24 MHz[Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 1.5 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.5 | | |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.8 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.8 | |
| | | | | $f_{IH}$ = 16 MHz[Note 3] | | $V_{DD}$ = 5.0 V | | 2.7 | 4.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.2 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | |
| | | | | $f_{MX}$ = 20 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 5.0 V | | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | |
| | | | | $f_{MX}$ = 10 MHz[Note 2], $V_{DD}$ = 3.0 V | | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator clock is stopped.

**3.** When high-speed system clock is stopped

**4.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz

$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Temperature condition of the TYP. value is $T_A$ = 25°C.

### (2) 30-pin products

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 6 | $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 440 | 2300 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 440 | 2300 | |
| | | | | $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 400 | 1700 | μA |
| | | | | | $V_{DD}$ = 3.0 V | | 400 | 1700 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 280 | 1900 | μA |
| | | | | | Resonator connection | | 450 | 2000 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 190 | 1020 | μA |
| | | | | | Resonator connection | | 260 | 1100 | |
| | $I_{DD3}$ Note 5 | STOP mode | $T_A$ = –40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | |
| | | | $T_A$ = +50°C | | | | 0.30 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.46 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.75 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator clock is stopped.

**4.** When high-speed system clock is stopped.

**5.** Not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as follows.

HS (High speed main) mode: $V_{DD}$ = 2.7 V to 5.5 V @1 MHz to 24 MHz
$V_{DD}$ = 2.4 V to 5.5 V @1 MHz to 16 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: high-speed on-chip oscillator clock frequency

**3.** Except STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C.

### (3) Peripheral functions (Common to all products)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed onchip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | µA |
| 12-bit interval timer operating current | $I_{TMKA}$ Notes 1, 2, 3 | | | | 0.02 | | µA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 4 | $f_{IL}$ = 15 kHz | | | 0.22 | | µA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 5 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.30 | 1.70 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.50 | 0.70 | mA |
| A/D converter reference voltage operating current | $I_{ADREF}$ Note 1 | | | | 75.0 | | µA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | µA |
| LVD operating current | $I_{LVD}$ Notes 1, 6 | | | | 0.08 | | µA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 8 | | | | 2.00 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 7 | | | | 2.00 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 9 | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 2.04 | mA |
| | | CSI/UART operation | | | 0.70 | 1.54 | mA |

**Notes 1.** Current flowing to the $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$, and $I_{FIL}$ and $I_{TMKA}$ when the 12-bit interval timer operates.

**4.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

**5.** Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**6.** Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit operates.

**7.** Current flowing only during data flash rewrite.

**8.** Current flowing only during self programming.

**9.** For shift time to the SNOOZE mode, see **17.3.3 SNOOZE mode** in the RL78/G12 User's Manual.

**Remarks 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**2.** Temperature condition of the TYP. value is $T_A$ = 25°C

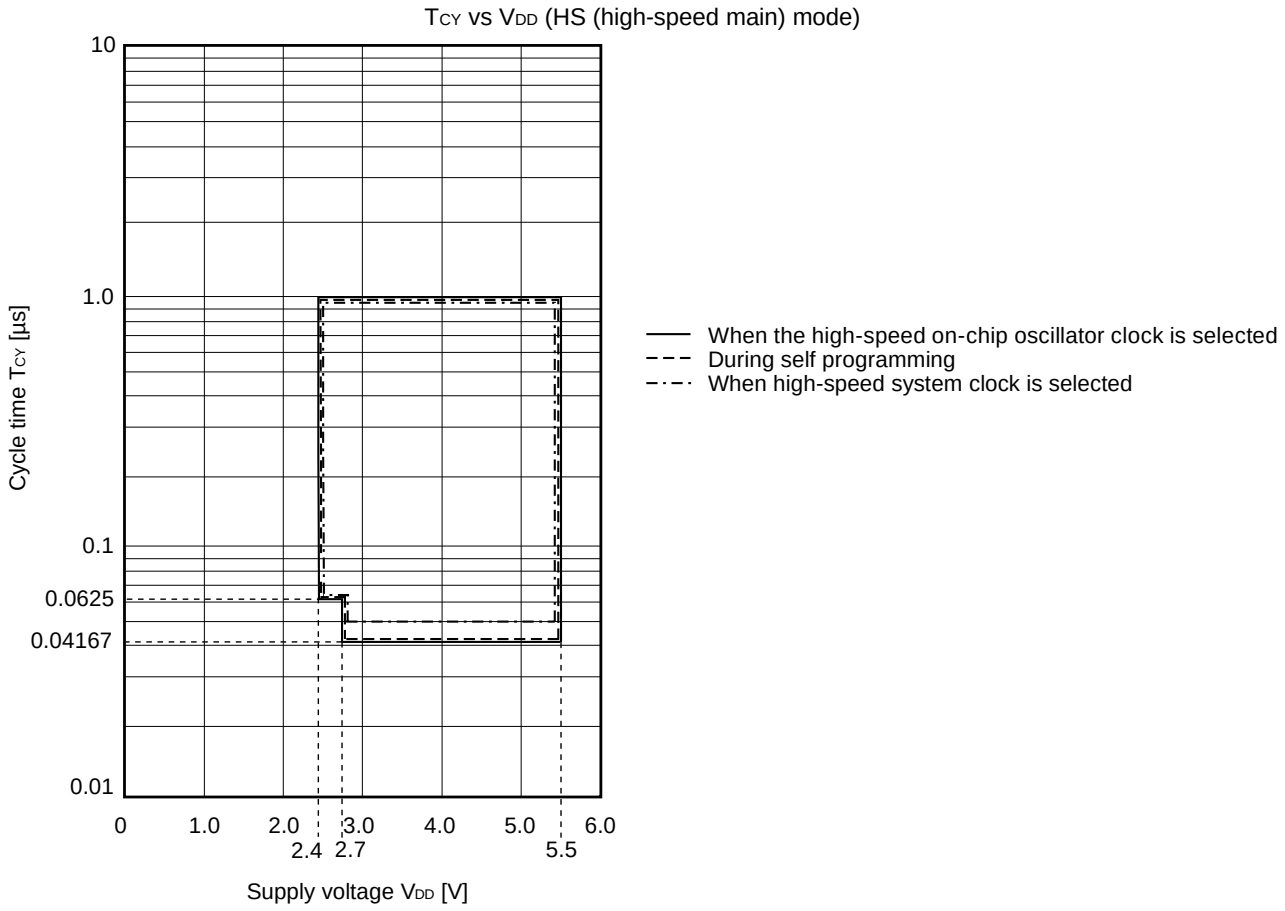
## 3.4 AC Characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

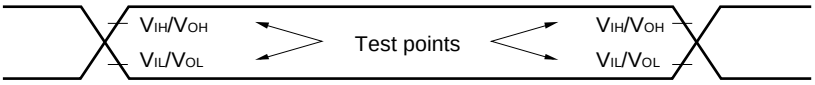
| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | During self programming | HS (High-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.04167 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| External main system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 1.0 | | 16.0 | MHz |
| External main system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 30 | | | ns |
| TI00 to TI07 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 | | | ns |
| TO00 to TO07 output frequency | $f_{TO}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 12 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| PCLBUZ0, or PCLBUZ1 output frequency | $f_{PCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | | 16 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | | 8 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | | | 4 | MHz |
| INTP0 to INTP5 input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | | | | 1 | | | µs |
| KR0 to KR9 input available width | $t_{KR}$ | | | | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | | 10 | | | µs |

**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

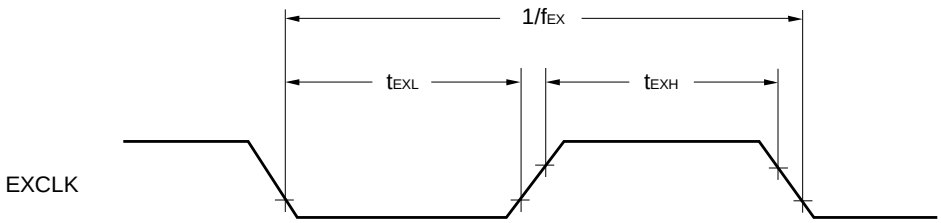
**Minimum Instruction Execution Time during Main System Clock Operation**



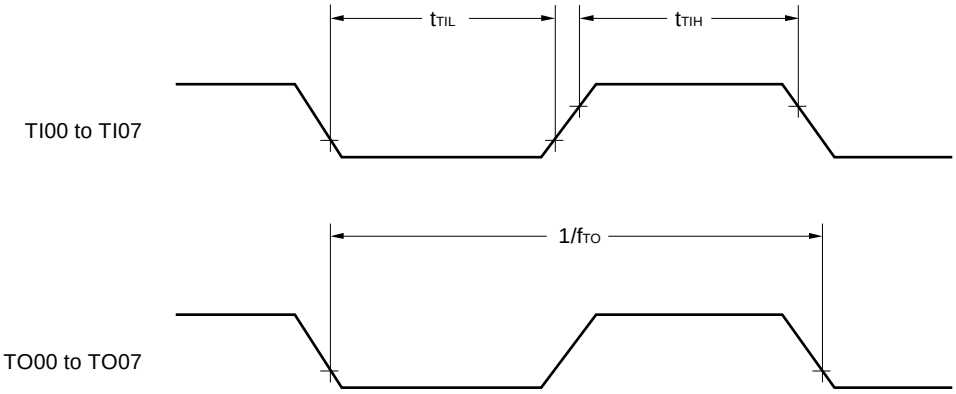

**AC Timing Test Point**



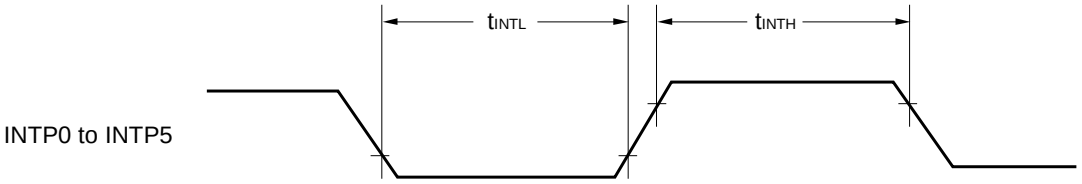

**External Main System Clock Timing**



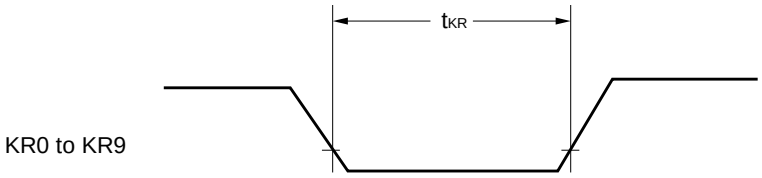
**TI/TO Timing**



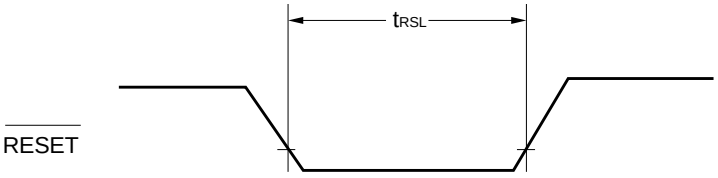

**Interrupt Request Input Timing**




**Key Interrupt Input Timing**

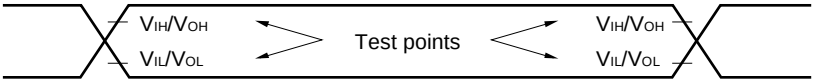



**$\overline{\text{RESET}}$ Input Timing**



## 3.5 Peripheral Functions Characteristics

### AC Timing Test Point




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

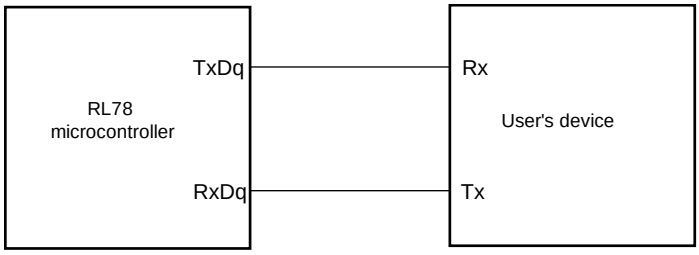
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/12 | bps |
| | | Theoretical value of the maximum transfer rate $f_{CLK} = f_{MCK}$ Note 2 | | 2.0 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

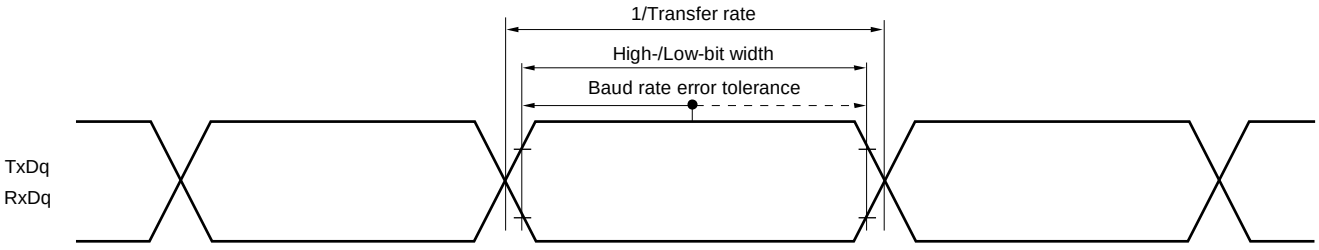
**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remarks 1.** q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 334 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2–24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2–36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY1}$/2–76 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 113 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | | | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | | | 50 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp and SCKp pins by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).**

**Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3))

**(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–14 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–16 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | $t_{KCY2}$/2–36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 113 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

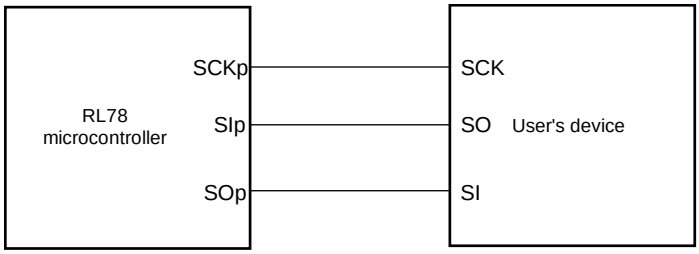
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

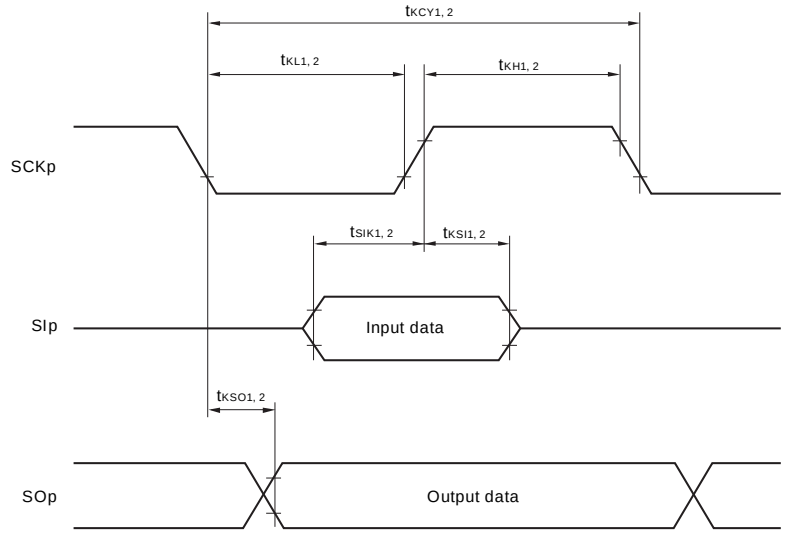
**5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps.

**Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode registers 0, 1, 4 (POM0, POM1, POM4).**

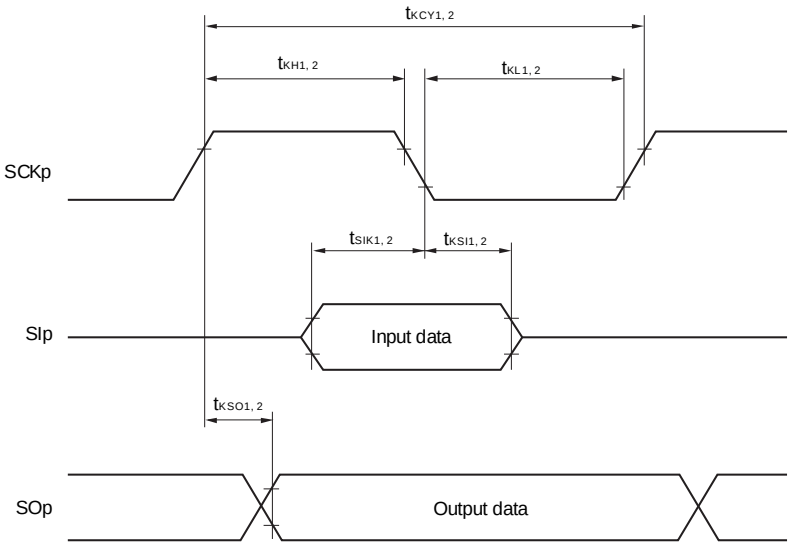
**CSI mode connection diagram (during communication at same potential)**



**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 11, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0,1), n: Channel number (n = 0, 1, 3))

### (4) During communication at same potential (simplified I²C mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

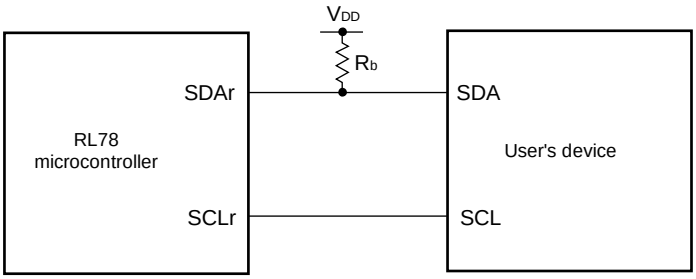
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | $1/f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Notes 1.** The value must be equal to or less than $f_{MCK}$/4.

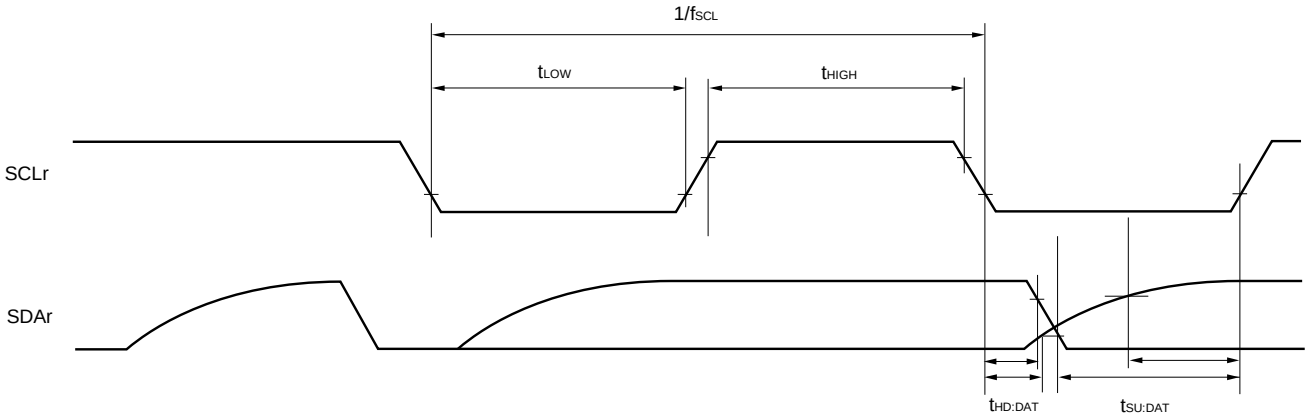
**2.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = “L” or SCLr = “H”.

**Caution Select the N-ch open drain output ($V_{DD}$ tolerance) mode for SDAr by using port output mode register h (POMh).**

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remarks 1.** $R_b$ [Ω]:Communication line (SDAr) pull-up resistance

$C_b$ [F]: Communication line (SCLr, SDAr) load capacitance

**2.** r: IIC number (r = 00, 01, 11, 20), h: = POM number (h = 0, 1, 4, 5)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (0, 1, 3))

**(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate Note4 | | Reception | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 2 | | 2.0 | Mbps |
| | | Transmission | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | **Note 3** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.0 Note 4 | Mbps |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, | | **Note 5** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 6 | Mbps |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | **Notes 2, 7** | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 8 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $V_{DD}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**5.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $V_{DD}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3}\ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**6.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

**7.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3}\ [\text{bps}]$$

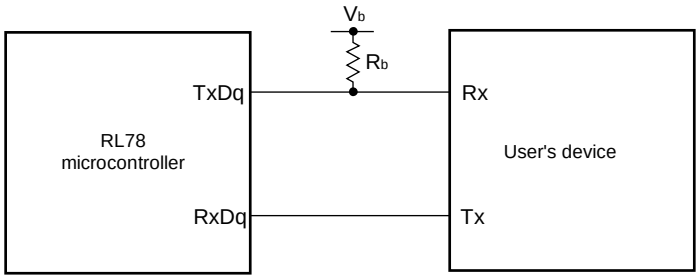
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

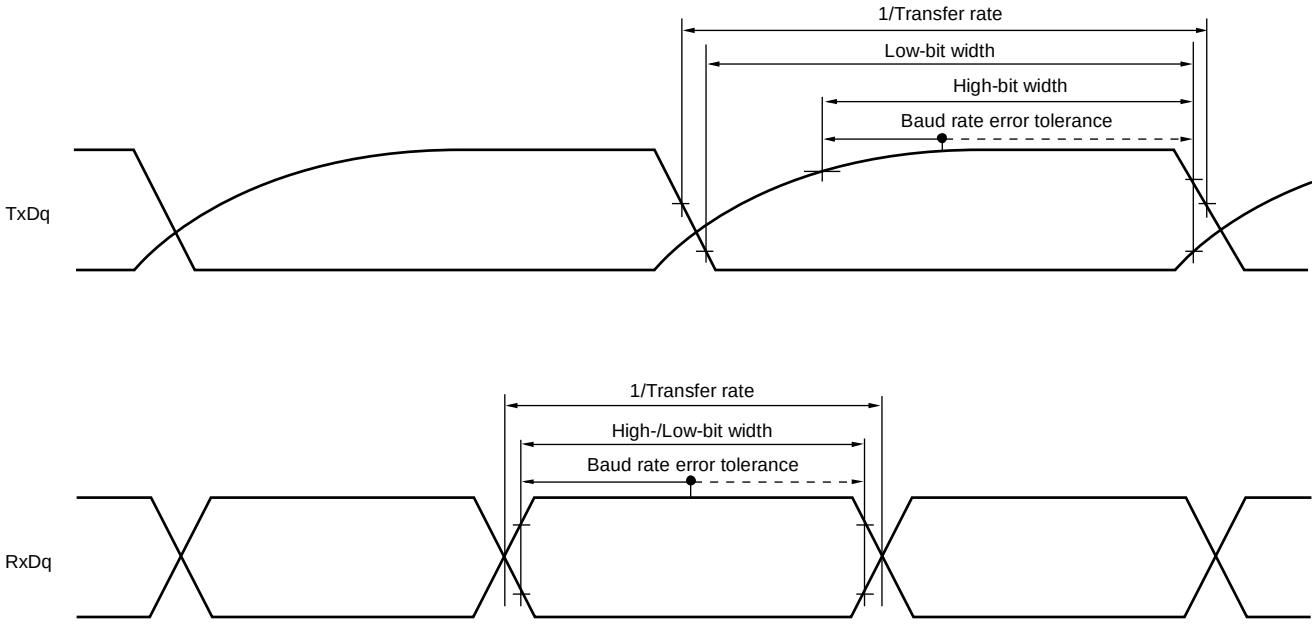
**8.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remarks 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance, $C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

**4.** UART0 of the 20- and 24-pin products supports communication at different potential only when the peripheral I/O redirection function is not used.

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –150 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –340 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 –24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 –36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 –100 | | ns |

**Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2. CSI01 and CSI11 cannot communicate at different potential.**

**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

(**Cautions** and **Remarks** are listed on the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note | $t_{KSI1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

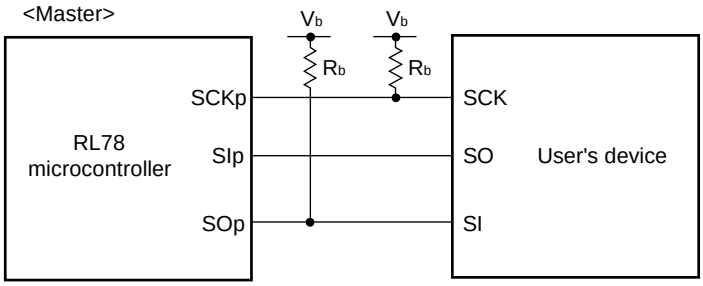
**Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2. CSI01 and CSI11 cannot communicate at different potential.**

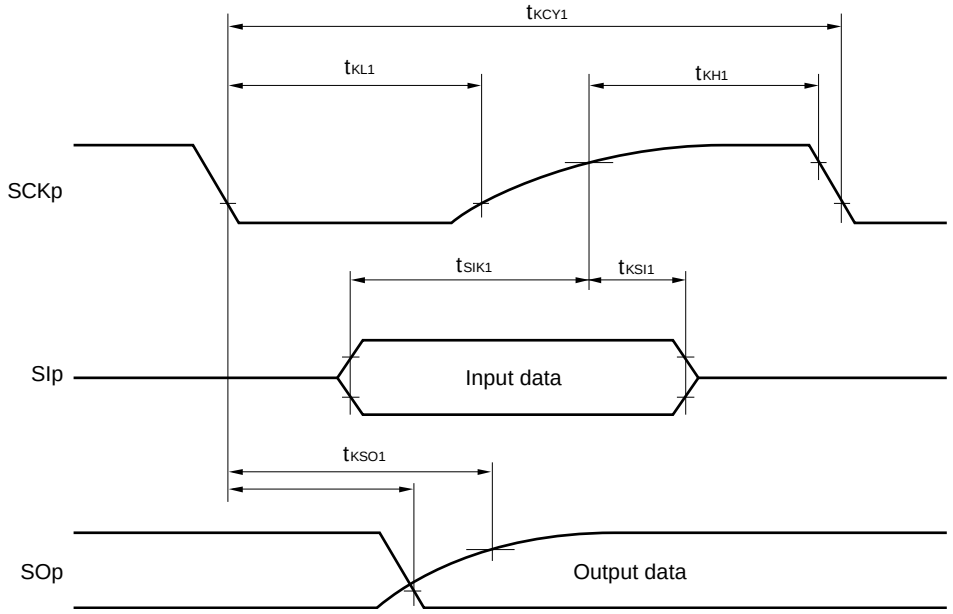
**Remarks 1.** $R_b$ [Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$ [F]: Communication line (SCKp, SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

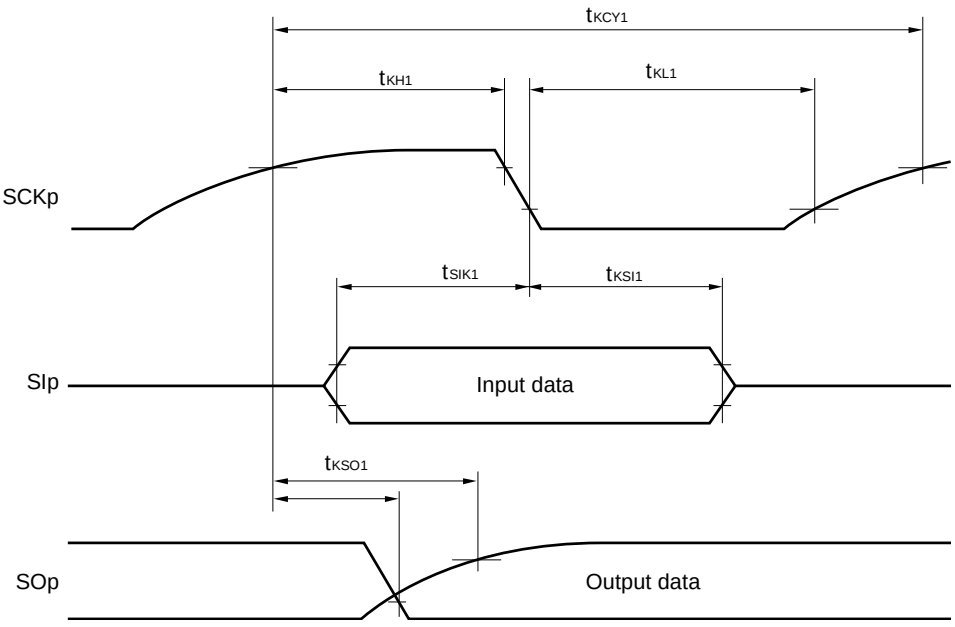
**CSI mode connection diagram (during communication at different potential)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD}$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_{DD}$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

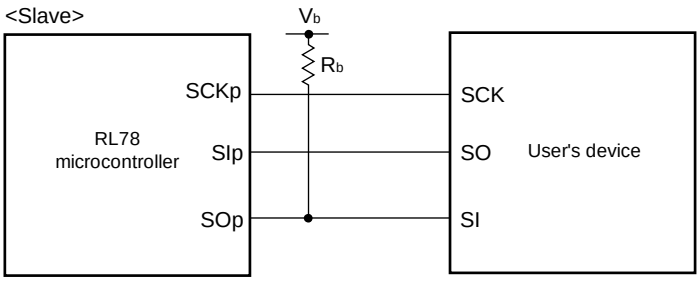
**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

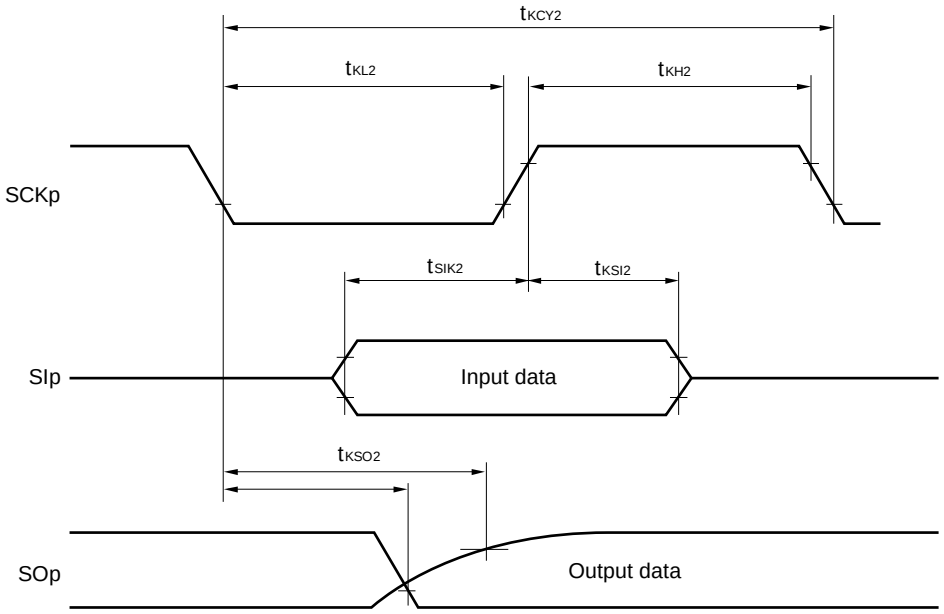
**Cautions 1. Select the TTL input buffer for the SIp and SCKp pins and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**2. CSI01 and CSI11 cannot communicate at different potential.**

**CSI mode connection diagram (during communication at different potential)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**

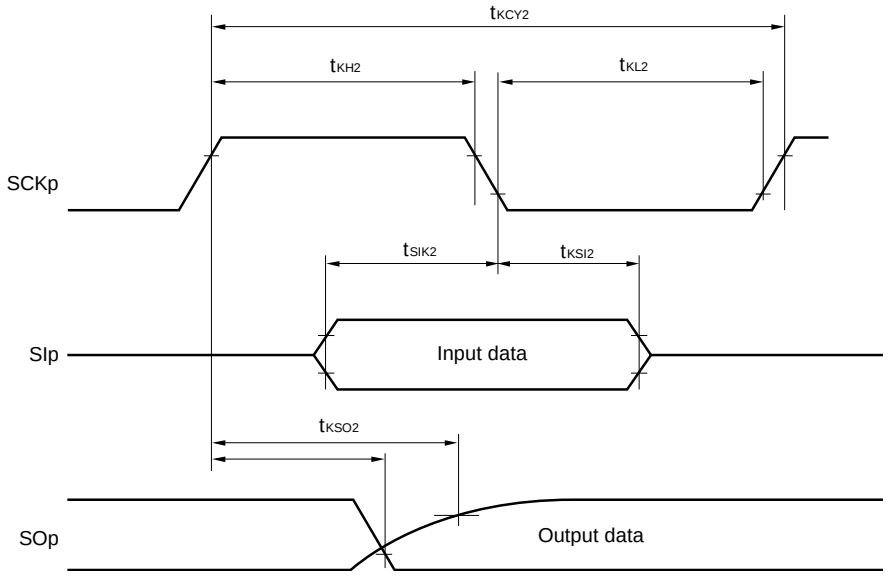



**Remarks 1.** $R_b$ [Ω]: Communication line (SOp) pull-up resistance, $C_b$ [F]: Communication line (SOp) load capacitance, $V_b$ [V]: Communication line voltage

**2.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 100 Note1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note1 | kHz |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 4600 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 2700 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 760 Note2 | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 760 Note2 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 570 Note2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

**Notes 1.** The value must be equal to or less than $f_{MCK}$/4.

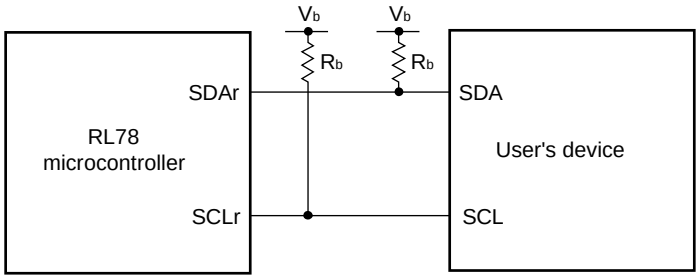
**2.** Set $t_{SU:DAT}$ so that it will not exceed the hold time when SCLr = “L” or SCLr = “H”.

**Cautions 1. Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register 1 (PIM1) and port output mode register 1 (POM1). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

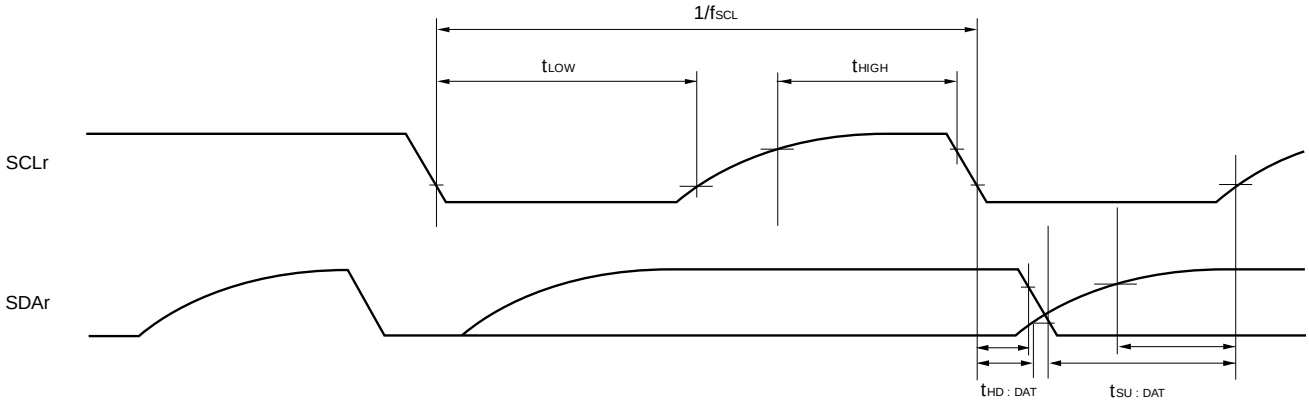
**2. IIC01 and IIC11 cannot communicate at different potential.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$ [Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$ [F]: Communication line (SDAr, SCLr) load capacitance, $V_b$ [V]: Communication line voltage

**2.** r: IIC Number (r = 00, 20)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0,1), n: Channel number (n = 0))

### 3.5.2 Serial interface IICA

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | | | 0 | 400 | kHz |
| | | Normal mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | 0.6 | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | 0.6 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 4.7 | | 1.3 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 4.0 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

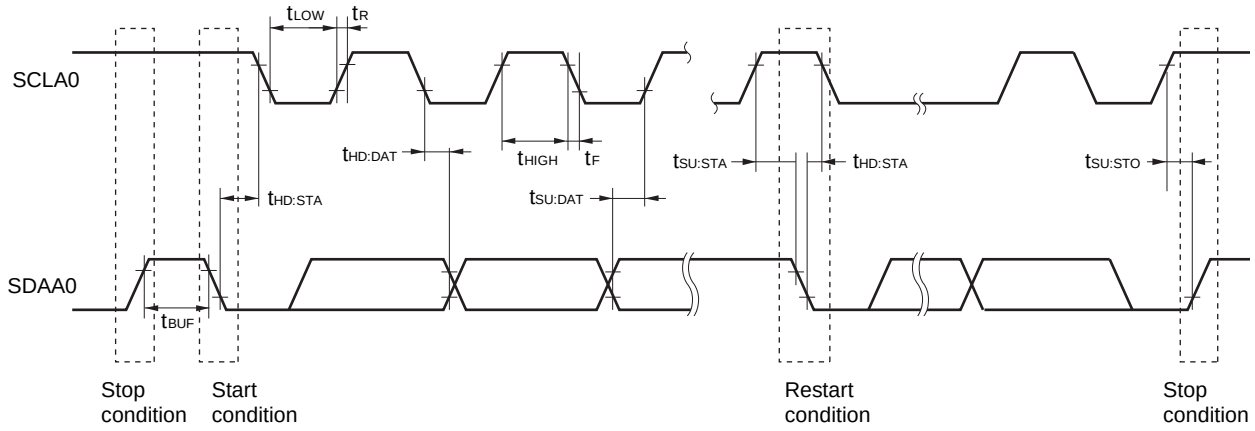
**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution Only in the 30-pin products, the values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Normal mode: $C_b$ = 400 pF, Rb = 2.7 kΩ
Fast mode: $C_b$ = 320 pF, Rb = 1.1 kΩ

**IICA serial transfer timing**



## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Input channel | Reference Voltage | | |
|---|---|---|---|
| | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (–) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (–) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (–) = $AV_{REFM}$ |
| ANI0 to ANI3 | Refer to **3.6.1 (1)**. | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. |
| ANI16 to ANI22 | Refer to **3.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **3.6.1 (1)**. | | – |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2, ANI3, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | 1.2 | ±3.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2, ANI3 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error[Notes 1, 2] | EZS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±0.25 | %FSR |
| Full-scale error[Notes 1, 2] | EFS | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±0.25 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±2.5 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ [Note 3] | | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2, ANI3 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(HS (high-speed main) mode) | | $V_{BGR}$ [Note 4] | | | V |
| | | Temperature sensor output voltage<br>(HS (high-speed main) mode) | | $V_{TMPS25}$ [Note 4] | | | V |

(**Notes** are listed on the next page.)

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target ANI pin: ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±0.35 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ Note 3 | | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI22 | | 0 | | $AV_{REFP}$ and $V_{DD}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 10-bit resolution | | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution | | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI3, ANI16 to ANI22 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage (HS (high-speed main) mode) | | $V_{BGR}$ Note 3 | | | V |
| | | Temperature sensor output voltage (HS (high-speed main) mode) | | $V_{TMPS25}$ Note 3 | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$ (ADREFM = 1), target pin: ANI0, ANI2, ANI3, and ANI16 to ANI22**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | 8 | | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | EZS | 8-bit resolution | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

### 3.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode**

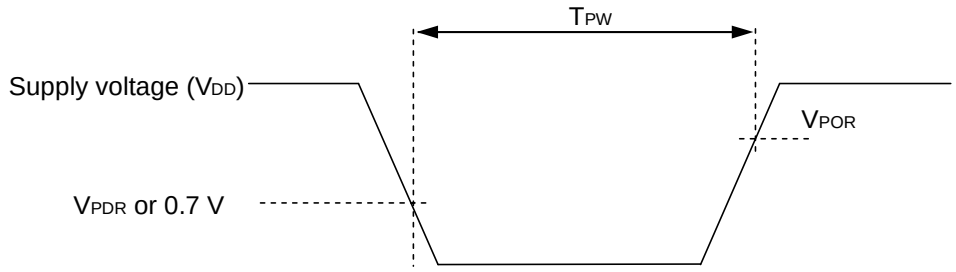
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.50 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 3.6.3 POR circuit characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width Note | $T_{PW}$ | | 300 | | | μs |

**Note** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 3.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection supply voltage | $V_{LVD0}$ | Power supply rise time | 3.90 | 4.06 | 4.22 | V |
| | | Power supply fall time | 3.83 | 3.98 | 4.13 | V |
| | $V_{LVD1}$ | Power supply rise time | 3.60 | 3.75 | 3.90 | V |
| | | Power supply fall time | 3.53 | 3.67 | 3.81 | V |
| | $V_{LVD2}$ | Power supply rise time | 3.01 | 3.13 | 3.25 | V |
| | | Power supply fall time | 2.94 | 3.06 | 3.18 | V |
| | $V_{LVD3}$ | Power supply rise time | 2.90 | 3.02 | 3.14 | V |
| | | Power supply fall time | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVD4}$ | Power supply rise time | 2.81 | 2.92 | 3.03 | V |
| | | Power supply fall time | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVD5}$ | Power supply rise time | 2.70 | 2.81 | 2.92 | V |
| | | Power supply fall time | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVD6}$ | Power supply rise time | 2.61 | 2.71 | 2.81 | V |
| | | Power supply fall time | 2.55 | 2.65 | 2.75 | V |
| | $V_{LVD7}$ | Power supply rise time | 2.51 | 2.61 | 2.71 | V |
| | | Power supply fall time | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | 300 | µs |

**LVD detection voltage of interrupt & reset mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC1}$ = 0, 1, 1, falling reset voltage | | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising reset release voltage | 2.81 | 2.92 | 3.03 | V |
| | | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising reset release voltage | 2.90 | 3.02 | 3.14 | V |
| | | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising reset release voltage | 3.90 | 4.06 | 4.22 | V |
| | | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

### 3.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

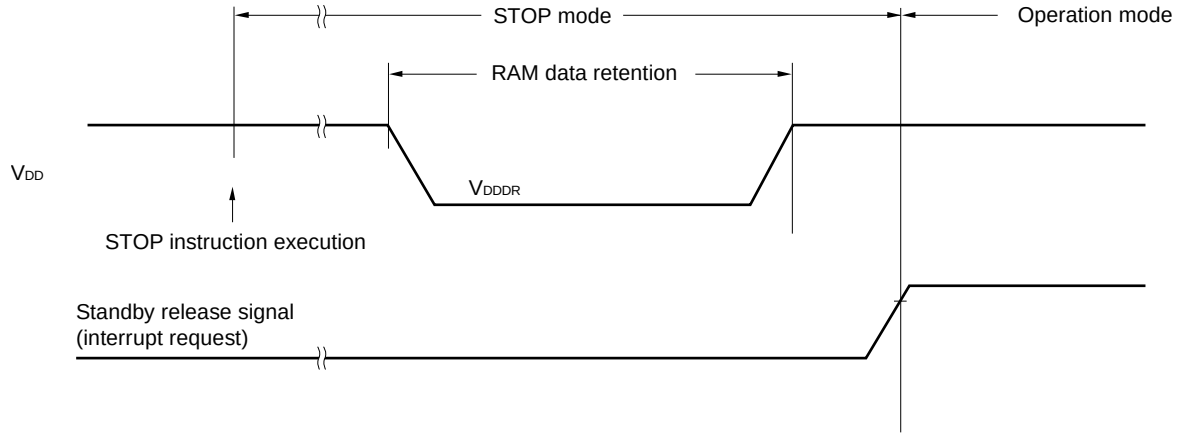
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

## 3.7 RAM Data Retention Characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44 Note | | 5.5 | V |

**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.




## 3.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | | 1 | | 24 | MHz |
| Code flash memory rewritable times Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years $T_A$ = 85°C Note 4 | 1,000 | | | Times |
| Data flash memory rewritable times Notes 1, 2, 3 | | Retained for 1 year $T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years $T_A$ = 85°C Note 4 | 100,000 | | | |
| | | Retained for 20 years $T_A$ = 85°C Note 4 | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

**4.** This temperature is the average value at which data are retained.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

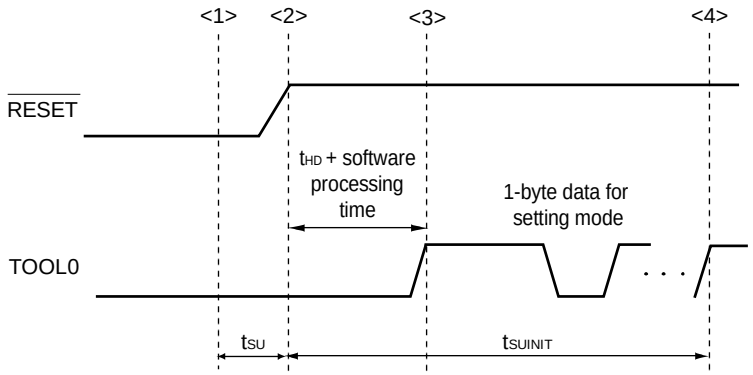
**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 3.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset are released before external release | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset are released before external release | 10 | | | µs |
| Time to hold the TOOL0 pin at the low level after the external reset is released<br>(excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset are released before external release | 1 | | | ms |



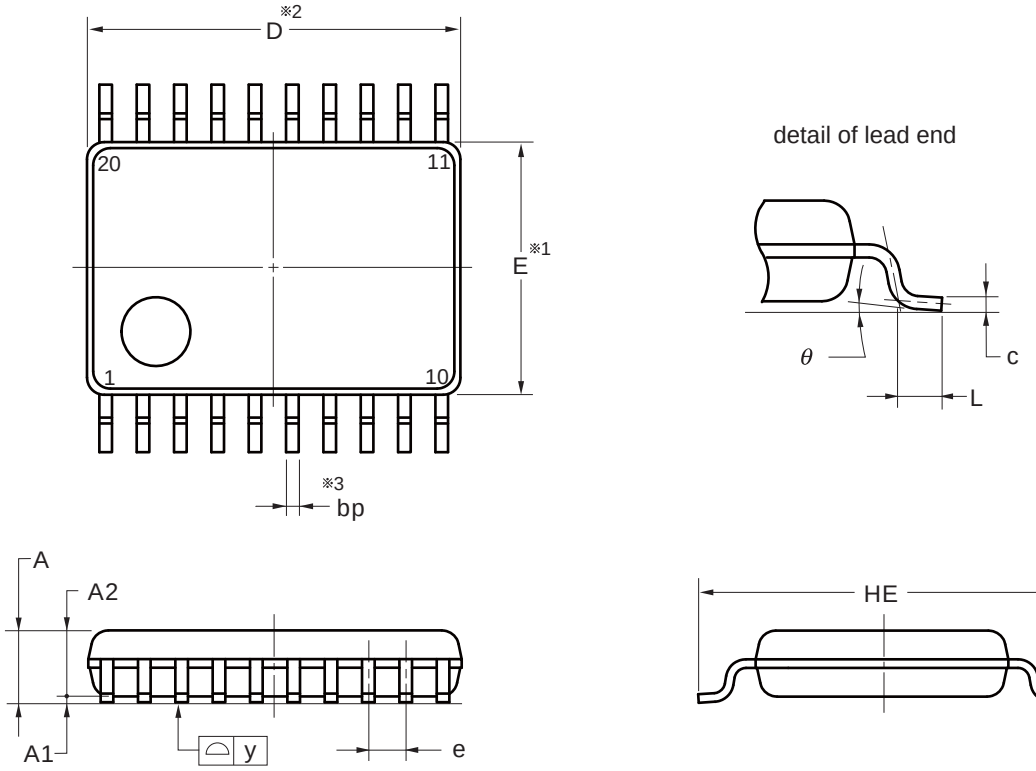

<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level
$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

# 4. PACKAGE DRAWINGS

## <R> 4.1 20-pin package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 6.50±0.10 |
| E | 4.40±0.10 |
| HE | 6.40±0.20 |
| A | 1.45 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.15 |
| e | 0.65±0.12 |
| bp | $0.22^{+0.10}_{-0.05}$ |
| c | $0.15^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| y | 0.10 |
| θ | 0° to 10° |

**NOTE**

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

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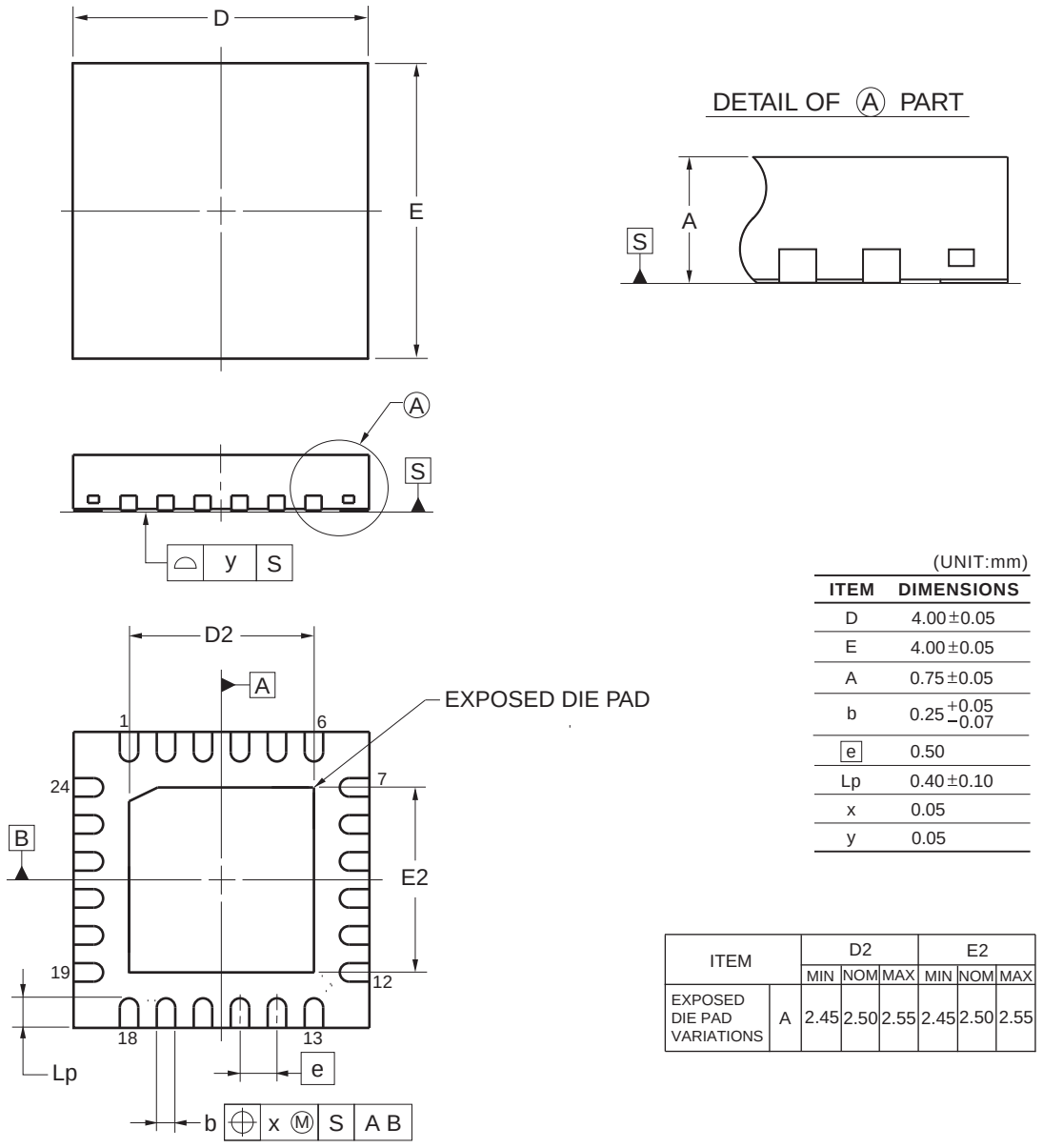
<R> **4.2 24-pin package**

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-1 | 0.04 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.05 |
| E | 4.00±0.05 |
| A | 0.75±0.05 |
| b | $0.25^{+0.05}_{-0.07}$ |
| e | 0.50 |
| Lp | 0.40±0.10 |
| x | 0.05 |
| y | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 2.45 | 2.50 | 2.55 | 2.45 | 2.50 | 2.55 |

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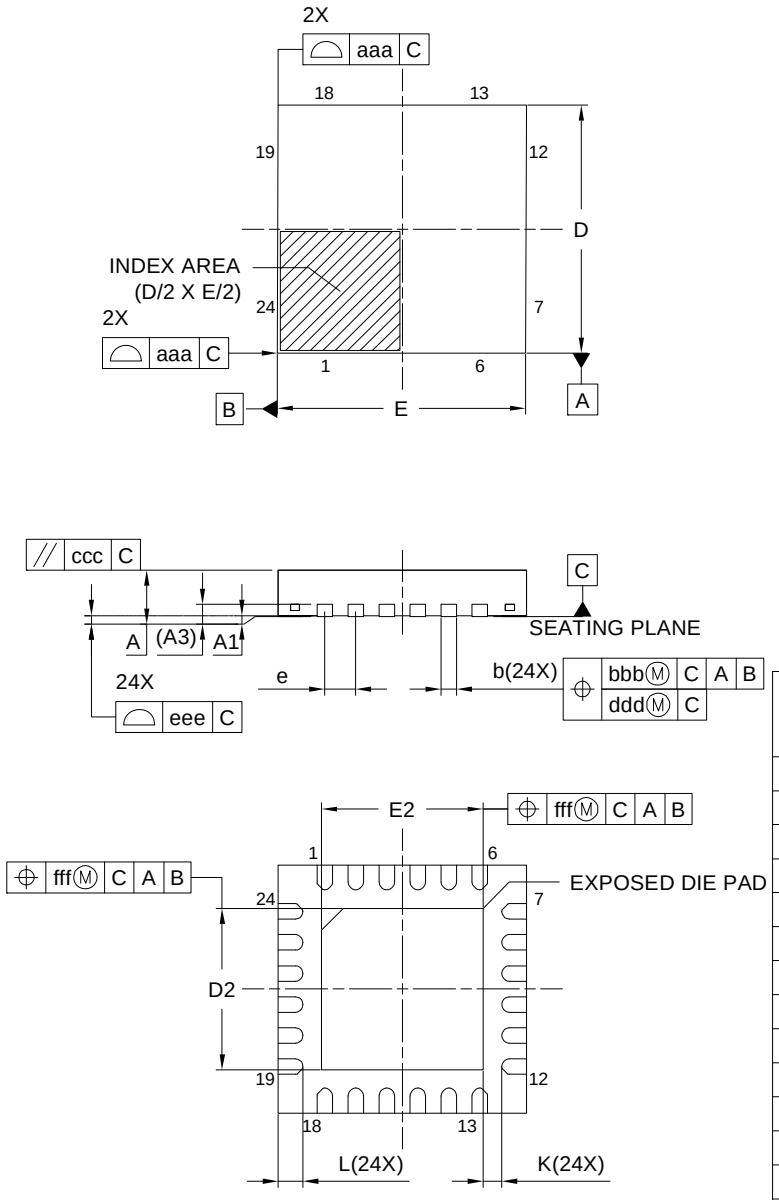
<R>

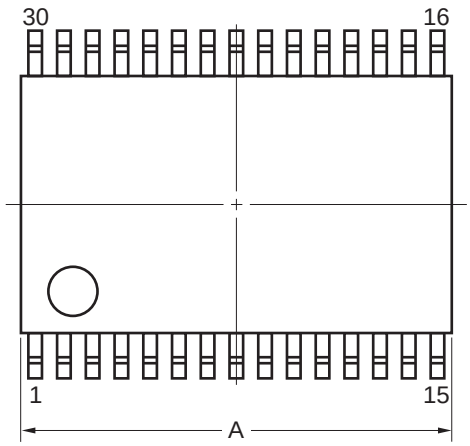
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN024-4x4-0.50 | PWQN0024KF-A | 0.04 |



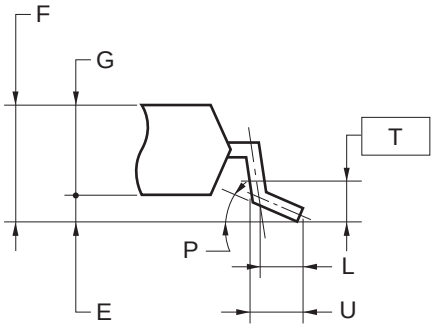

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | – | – | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 4.00 BSC | |
| E | | 4.00 BSC | |
| e | | 0.50 BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | – | – |
| D2 | 2.55 | 2.60 | 2.65 |
| E2 | 2.55 | 2.60 | 2.65 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

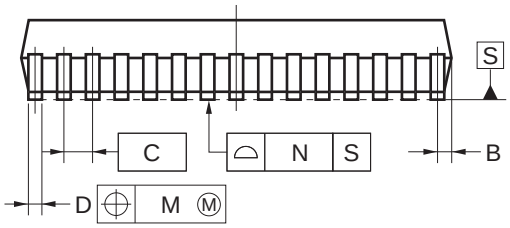
## <R> 4.3 30-pin package

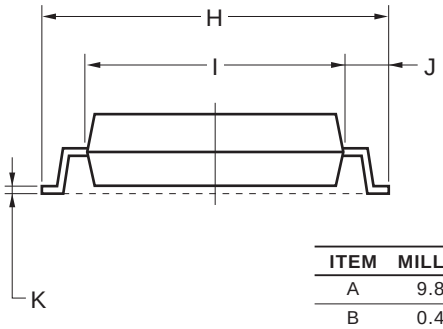
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |




detail of lead end




**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

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| Revision History | RL78/G12 Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Dec 10, 2012 | - | First Edition issued |
| 2.00 | Sep 06, 2013 | 1 | Modification of 1.1 Features |
| | | 3 | Modification of 1.2 List of Part Numbers |
| | | 4 | Modification of Table 1-1. List of Ordering Part Numbers, Note, and Caution |
| | | 7 to 9 | Modification of package name in 1.4.1 to 1.4.3 |
| | | 14 | Modification of tables in 1.7 Outline of Functions |
| | | 17 | Modification of description of table in 2.1 Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 18 | Modification of table, Note, and Caution in 2.2.1 X1 oscillator characteristics |
| | | 18 | Modification of table in 2.2.2 On-chip oscillator characteristics |
| | | 19 | Modification of Note 3 in 2.3.1 Pin characteristics (1/4) |
| | | 20 | Modification of Note 3 in 2.3.1 Pin characteristics (2/4) |
| | | 23 | Modification of Notes 1 and 2 in (1) 20-, 24-pin products (1/2) |
| | | 24 | Modification of Notes 1 and 3 in (1) 20-, 24-pin products (2/2) |
| | | 25 | Modification of Notes 1 and 2 in (2) 30-pin products (1/2) |
| | | 26 | Modification of Notes 1 and 3 in (2) 30-pin products (2/2) |
| | | 27 | Modification of (3) Peripheral functions (Common to all products) |
| | | 28 | Modification of table in 2.4 AC Characteristics |
| | | 29 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 30 | Modification of figures of AC Timing Test Point and External Main System Clock Timing |
| | | 31 | Modification of figure of AC Timing Test Point |
| | | 31 | Modification of description and Note 2 in (1) During communication at same potential (UART mode) |
| | | 32 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 33 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 34 | Modification of description in (4) During communication at same potential (CSI mode) |
| | | 36 | Modification of table and Note 2 in (5) During communication at same potential (simplified $I^2C$ mode) |
| | | 38, 39 | Modification of table and Notes 1 to 9 in (6) Communication at different potential<br>(1.8 V, 2.5 V, 3 V) (UART mode) |
| | | 40 | Modification of Remarks 1 to 3 in (6) Communication at different potential (1.8 V,<br>2.5 V, 3 V) (UART mode) |
| | | 41 | Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) |
| | | 42 | Modification of Caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) |
| | | 43 | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 44 | Modification of table and Notes 1 and 2 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| | | 45 | Modification of table, Note 1, and Caution 1 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 47 | Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) |
| | | 50 | Modification of table, Note 1, and Caution 1 in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode) |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Sep 06, 2013 | 52 | Modification of Remark in 2.5.2 Serial interface IICA |
| | | 53 | Addition of table to 2.6.1 A/D converter characteristics |
| | | 53 | Modification of description in 2.6.1 (1) |
| | | 54 | Modification of Notes 3 to 5 in 2.6.1 (1) |
| | | 54 | Modification of description and Notes 2 to 4 in 2.6.1 (2) |
| | | 55 | Modification of description and Notes 3 and 4 in 2.6.1 (3) |
| | | 56 | Modification of description and Notes 3 and 4 in 2.6.1 (4) |
| | | 57 | Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics |
| | | 57 | Modification of table and Note in 2.6.3 POR circuit characteristics |
| | | 58 | Modification of table in 2.6.4 LVD circuit characteristics |
| | | 59 | Modification of table of LVD detection voltage of interrupt & reset mode |
| | | 59 | Modification of number and title to 2.6.5 Power supply voltage rising slope characteristics |
| | | 61 | Modification of table, figure, and Remark in 2.10 Timing of Entry to Flash Memory Programming Modes |
| | | 62 to 103 | Addition of products of industrial applications (G: $T_A$ = -40 to +105°C) |
| | | 104 to 106 | Addition of products of industrial applications (G: $T_A$ = -40 to +105°C) |
| 2.10 | Mar 25, 2016 | 6 | Modification of Figure 1-1 Part Number, Memory Size, and Package of RL78/G12 |
| | | 7 | Modification of Table 1-1 List of Ordering Part Numbers |
| | | 8 | Addition of product name (RL78/G12) and description (Top View) in 1.4.1 20-pin products |
| | | 9 | Addition of product name (RL78/G12) and description (Top View) in 1.4.2 24-pin products |
| | | 10 | Addition of product name (RL78/G12) and description (Top View) in 1.4.3 30-pin products |
| | | 15 | Modification of description in 1.7 Outline of Functions |
| | | 16 | Modification of description, and addition of target products |
| | | 52 | Modification of note 2 in 2.5.2 Serial interface IICA |
| | | 60 | Modification of title and note, and addition of caution in 2.7 RAM Data Retention Characteristics |
| | | 60 | Modification of conditions in 2.8 Flash Memory Programming Characteristics |
| | | 62 | Modification of description, and addition of target products and remark |
| | | 94 | Modification of note 2 in 3.5.2 Serial interface IICA |
| | | 102 | Modification of title and note in 3.7 RAM Data Retention Characteristics |
| | | 102 | Modification of conditions in 3.8 Flash Memory Programming Characteristics |
| | | 104 to 106 | Addition of package name |
| 2.20 | Oct 31, 2018 | 4 | Modification of Table 1-1 List of Ordering Part Numbers |
| | | 7 | Modification of pin configuration diagram in 1.4.1 20-pin products |
| 2.21 | Jan 31, 2020 | 3 | Addition of packaging specifications in Figure 1-1 Part Number, Memory Size, and Package of RL78/G12 |
| | | 4, 5 | Addition of part numbers and RENESAS codes in Table 1-1 List of Ordering Part Numbers |
| | | 105, 106, 108 | Modification of the titles of the subchapters and deletion of product names in Chapter 4 |
| | | 107 | Addition of figure in 4.2 24-pin package |

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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