

1. General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

2. Features and benefits

- · 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- · High commutation capability with very sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

3. Applications

- Low power motor controls
- Small inductive loads e.g. solenoids, door locks, water valves
- Small loads in large white goods

4. Quick reference data

Table 1. Quick reference data

		12	 			
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DRM}	repetitive peak off- state voltage		-	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{lead} \le 70 \text{ °C}$; <u>Fig. 1</u> ; Fig. 2; Fig. 3	-	-	0.8	A
	non-repetitive peak on- state current	full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; <u>Fig. 4</u> ; <u>Fig. 5</u>	-	-	9	A
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	-	9.9	A
Tj	junction temperature		-	-	125	°C
Static charact	eristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 7</u>	0.25	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 7</u>	0.25	-	5	mA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	0.25	-	5	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	10	mA
V _T	on-state voltage	I _T = 0.85 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.35	1.6	V
Dynamic chai	acteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	200	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	$\label{eq:VD} \begin{array}{l} V_D = 400 \text{ V}; T_j = 125 \ ^\circ\text{C}; \\ I_{T(\text{RMS})} = 0.8 \text{A}; \text{dV}_{\text{com}}/\text{dt} = 10 \text{V}/\mu\text{s}; \\ \text{gate open circuit} \end{array}$	0.5	-	-	A/ms

5. Pinning information

Table 2. F	Pinning inf	ormation		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2		T2-71
2	G	gate		sym051
3	Τ1	main terminal 1	TO-92 (SOT54)	Symoor

6. Ordering information

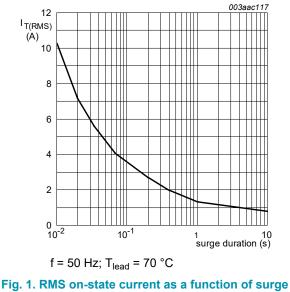
Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
BTA2008-800D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54			

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{lead} \le 70 \text{ °C}$; <u>Fig. 1</u> ; <u>Fig. 2</u> ; Fig. 3	-	0.8	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	9	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms	-	9.9	А
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.41	A²s
dl _T /dt	rate of rise of on-state current	I _G = 20 mA	-	100	A/µs
I _{GM}	peak gate current		-	1	А
P _{GM}	peak gate power		-	2	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
T _i	junction temperature		-	125	°C



duration; maximum values

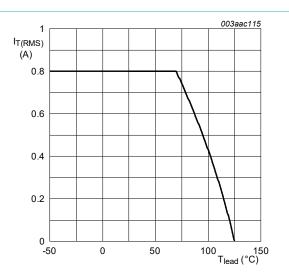
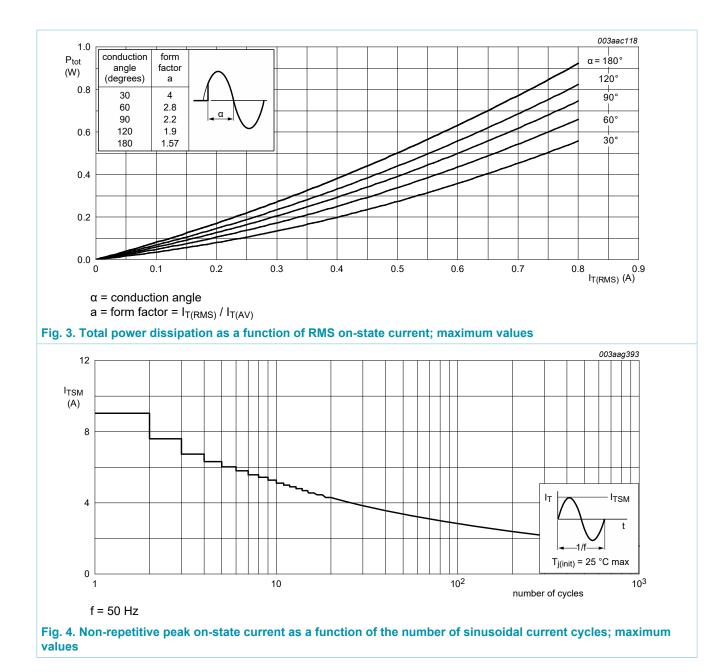


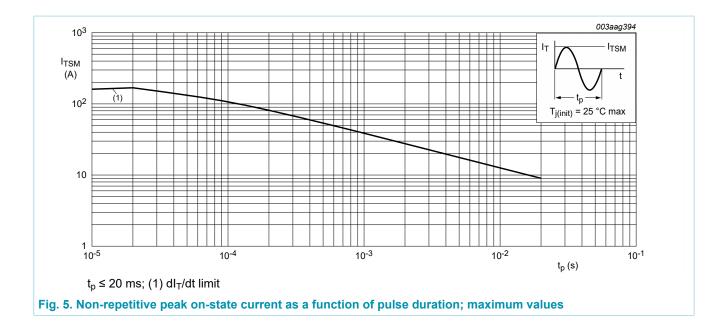
Fig. 2. RMS on-state current as a function of lead temperature; maximum values

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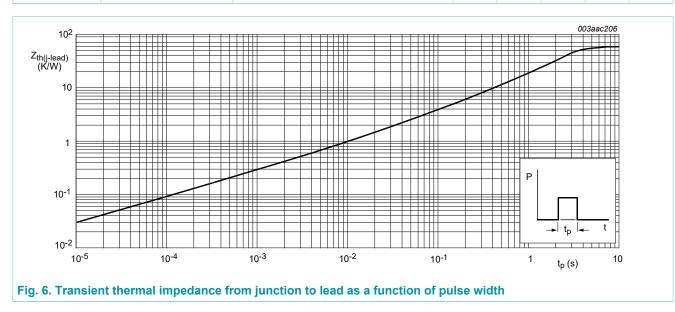
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8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; <u>Fig. 6</u>	-	-	60	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



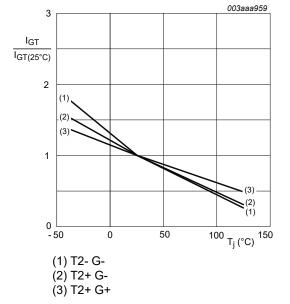
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9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 7</u>	0.25	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2+ G-};$ T _j = 25 °C; <u>Fig. 7</u>	0.25	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	0.25	-	5	mA
ΙL	latching current	V_D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 8</u>	-	-	10	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	20	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	10	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	10	mA
V _T	on-state voltage	I _T = 0.85 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.35	1.6	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 11</u>	-	0.9	1.5	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; <u>Fig. 11</u>	0.2	0.3	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic ch	naracteristics		·			
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	200	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T _j = 125 °C; I _{T(RMS)} = 0.8 A; dV _{com} /dt = 10 V/µs; gate open circuit	0.5	-	-	A/ms

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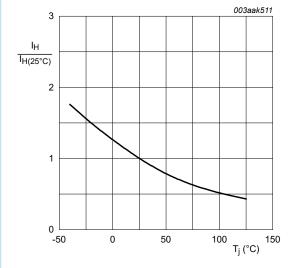
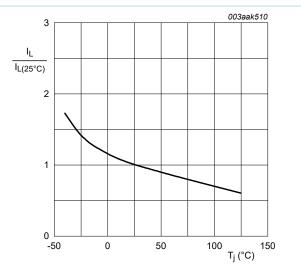
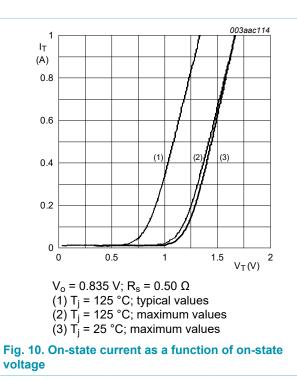


Fig. 9. Normalized holding current as a function of junction temperature

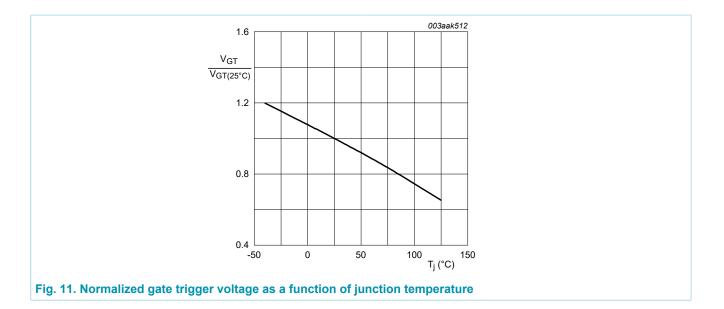






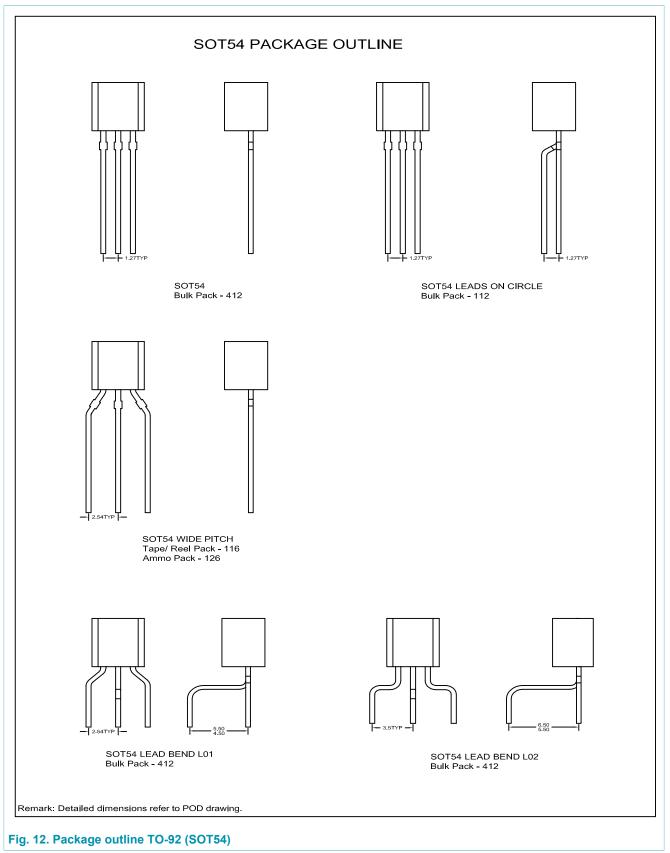
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10. Package outline



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Document status [1][2]	Product status [<u>3]</u>	Definition
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