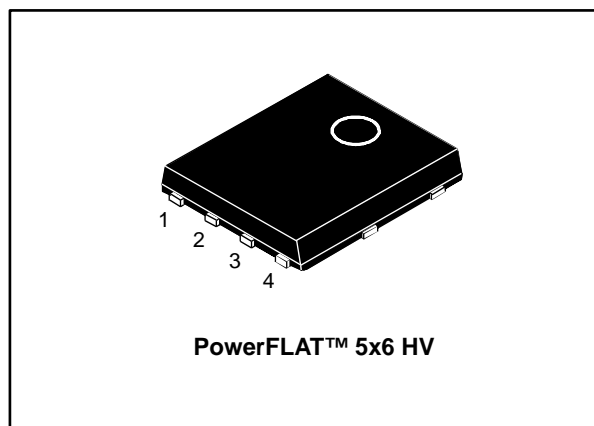
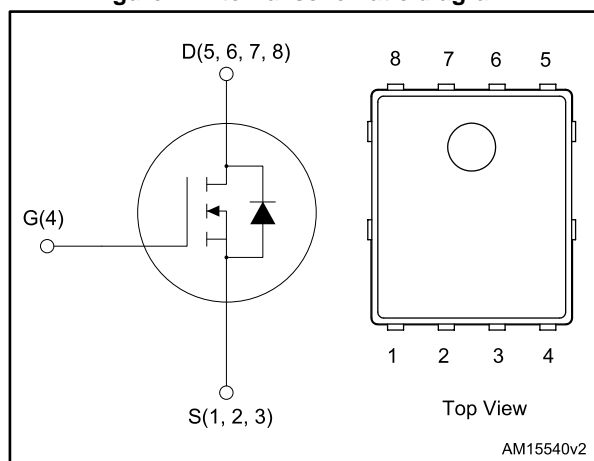


## N-channel 600 V, 0.400 $\Omega$ typ., 6.5 A MDmesh™ M2 Power MOSFET in a PowerFLAT 5x6 HV package

Datasheet - production data



**Figure 1: Internal schematic diagram**



**Table 1: Device summary**

Order code	Marking	Package	Packing
STL12N60M2	12N60M2	PowerFLAT 5x6 HV	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL12N60M2	600 V	0.495 $\Omega$	6.5 A	52 W

- Extremely low gate charge
- Excellent output capacitance (C<sub>OSS</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	6.5	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	4.1	
$I_{DM}^{(2)}$	Drain current (pulsed)	26	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	52	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature		

**Notes:**

- (1) Limited by maximum junction temperature.  
 (2) Pulse width is limited by safe operating area.  
 (3)  $I_{SD} \leq 6.5\text{ A}$ ,  $di/dt=400\text{ A}/\mu\text{s}$ ;  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .  
 (4)  $V_{DS} \leq 480\text{ V}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.4	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

**Notes:**

- (1) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.6	A
$E_{AR}^{(2)}$	Single pulse avalanche energy	120	mJ

**Notes:**

- (1) Pulse width limited by  $T_{jmax}$ .  
 (2) starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 4.5\text{ A}$		0.400	0.495	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	538	-	pF
$C_{\text{oss}}$	Output capacitance		-	29	-	
$C_{\text{rss}}$	Reverse transfer capacitance		-	1.1	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	106	-	pF
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	7	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 400\text{ V}$ , $I_{\text{D}} = 9\text{ A}$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 15: "Gate charge test circuit"</a> )	-	16	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	2.3	-	
$Q_{\text{gd}}$	Gate-drain charge		-	8.5	-	

**Notes:**

<sup>(1)</sup>  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 4.5\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	9.2	-	ns
$t_{\text{r}}$	Rise time		-	9.2	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	56	-	
$t_{\text{f}}$	Fall time		-	18	-	

Table 8: Source-drain diode

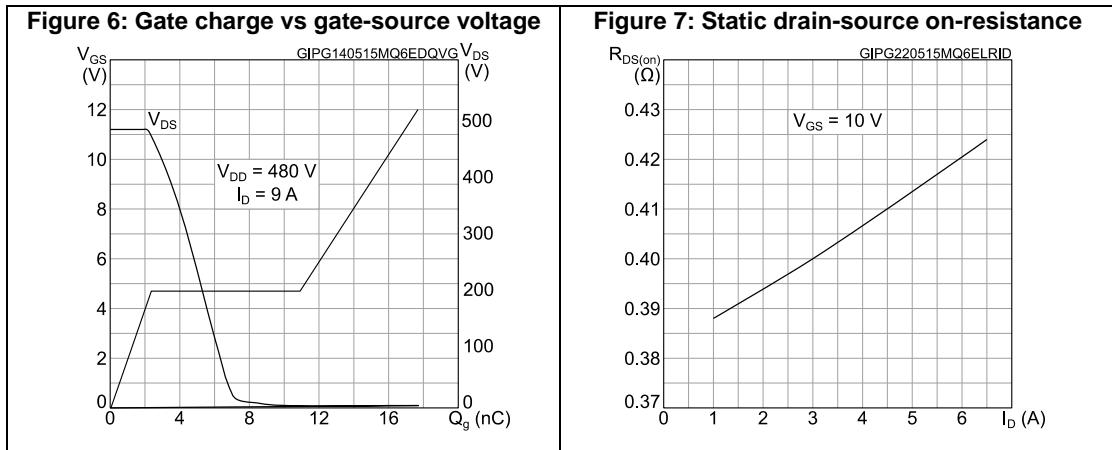
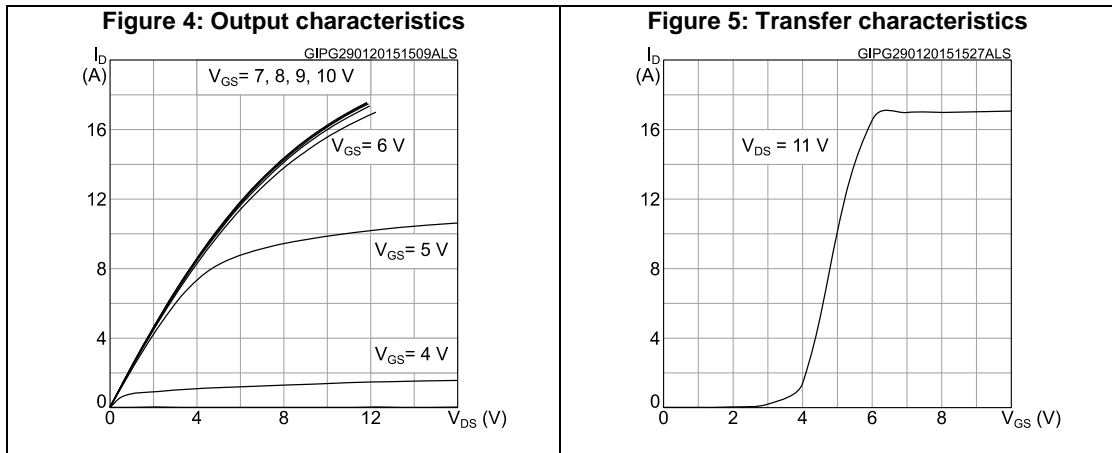
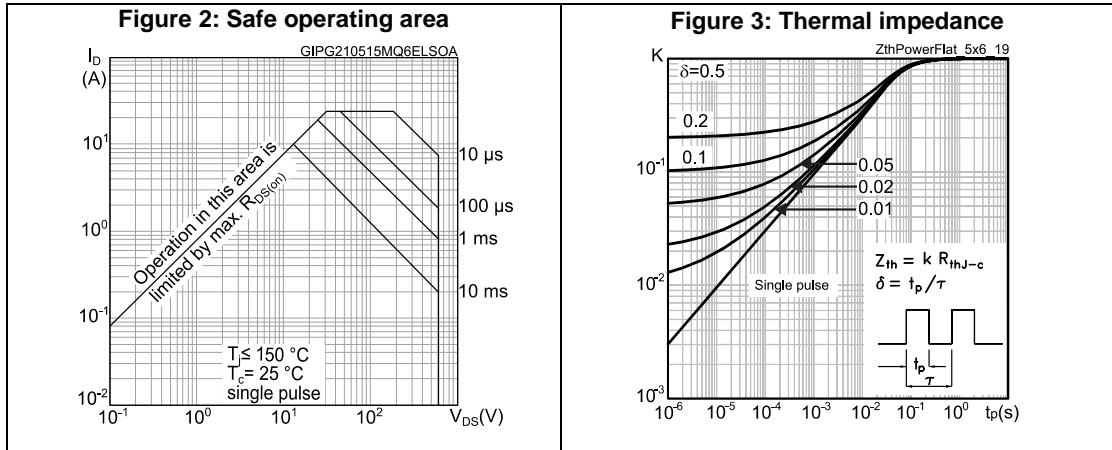
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 9\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	284		ns
$Q_{rr}$	Reverse recovery charge		-	2.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	404		ns
$Q_{rr}$	Reverse recovery charge		-	3.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17.5		A

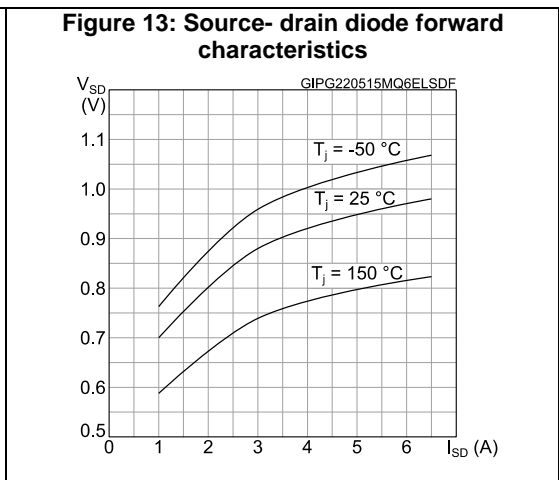
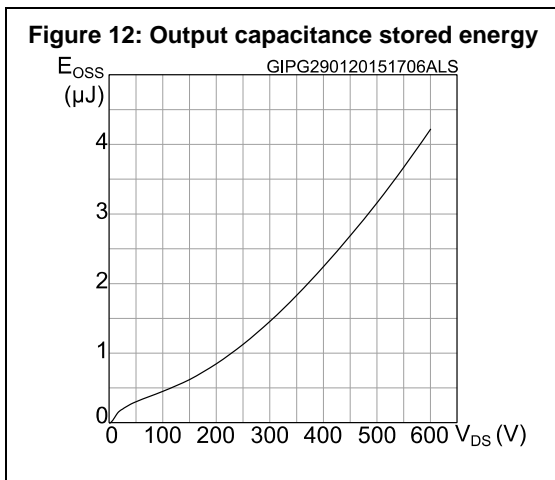
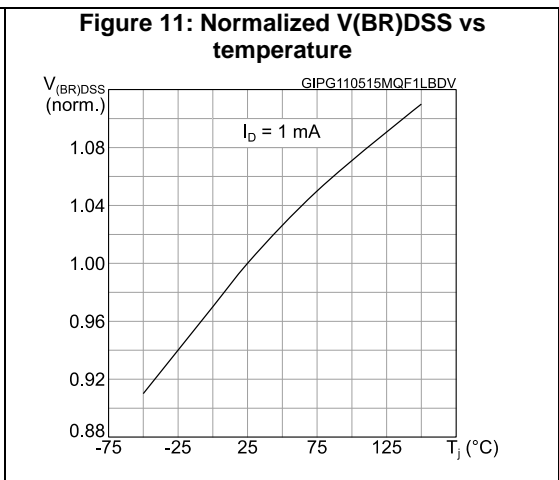
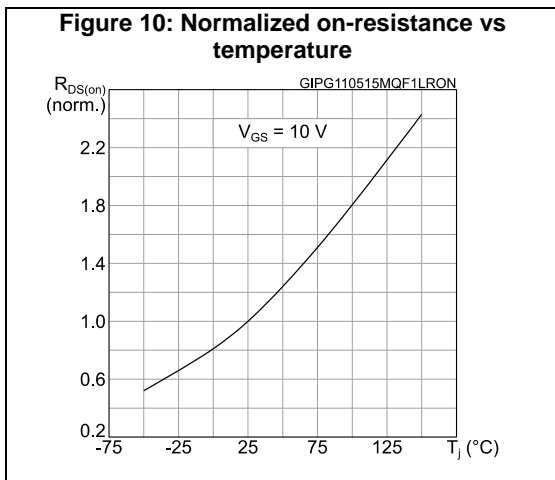
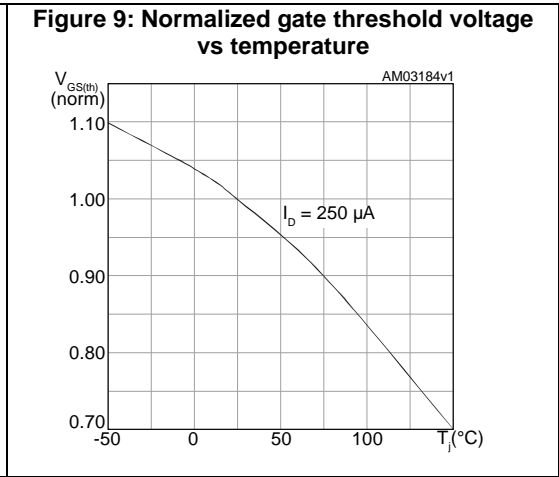
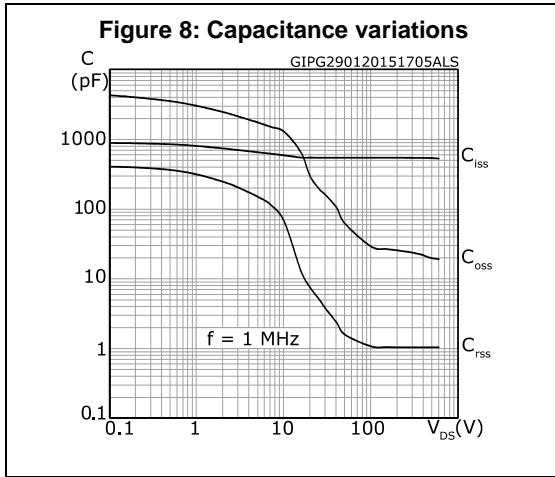
**Notes:**

(1) Pulse width is limited by safe operating area.

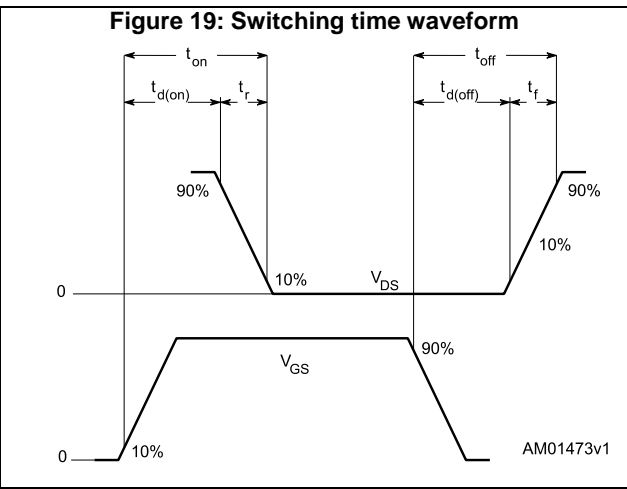
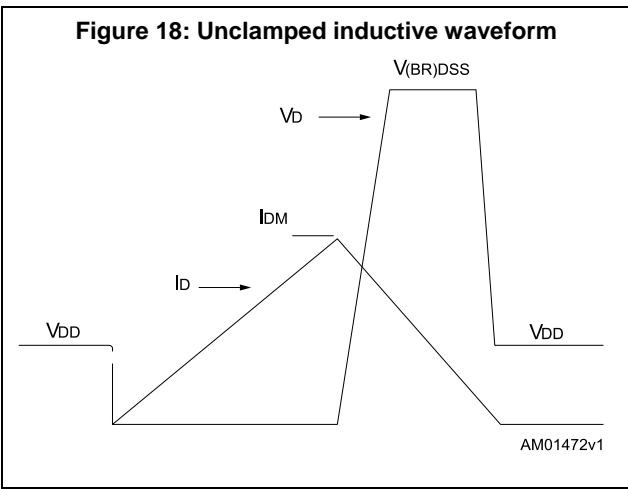
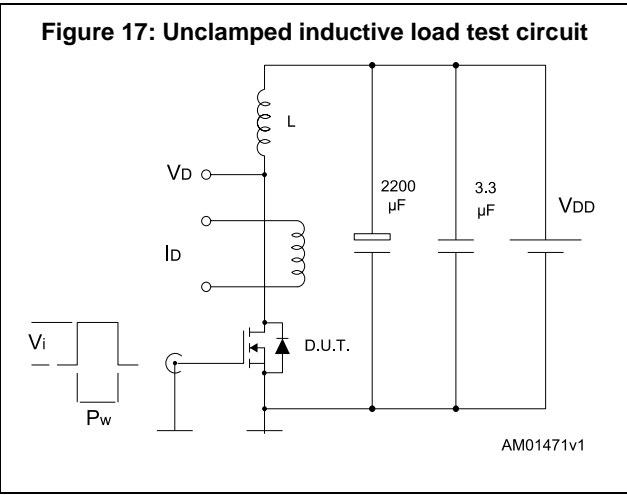
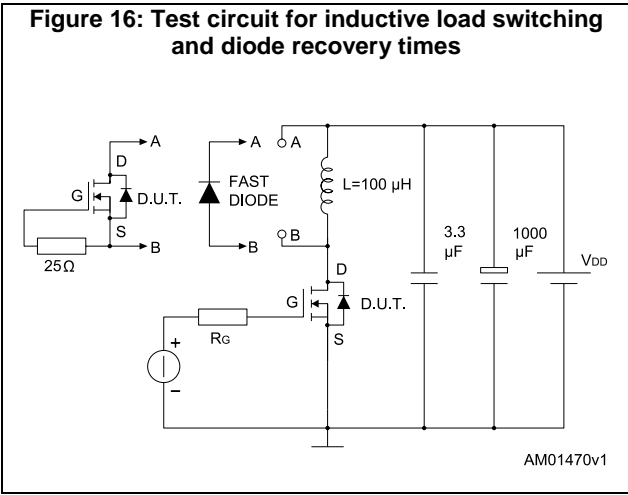
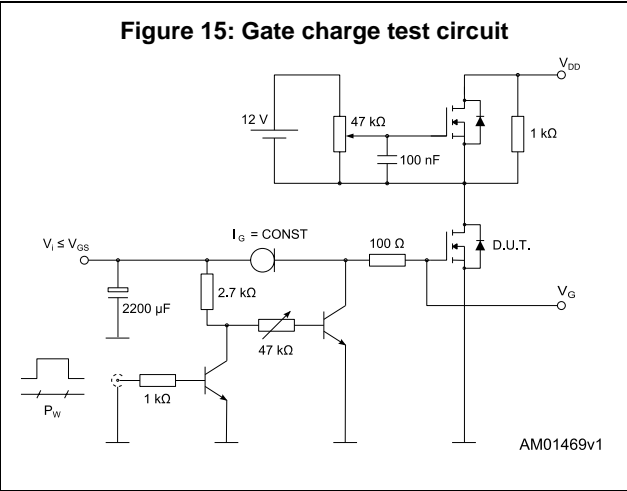
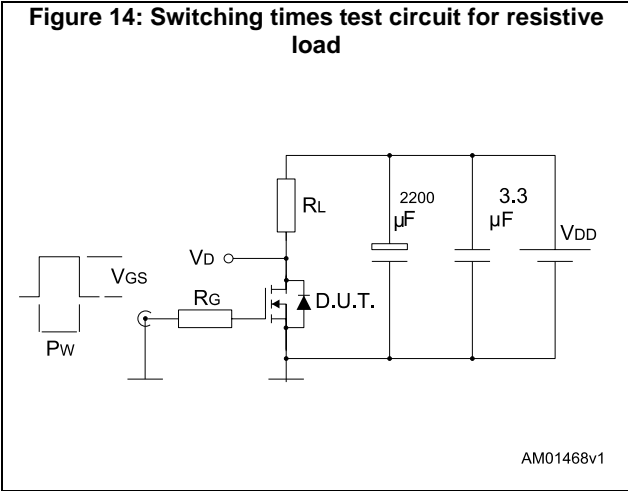
(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)





### 3 Test circuits



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

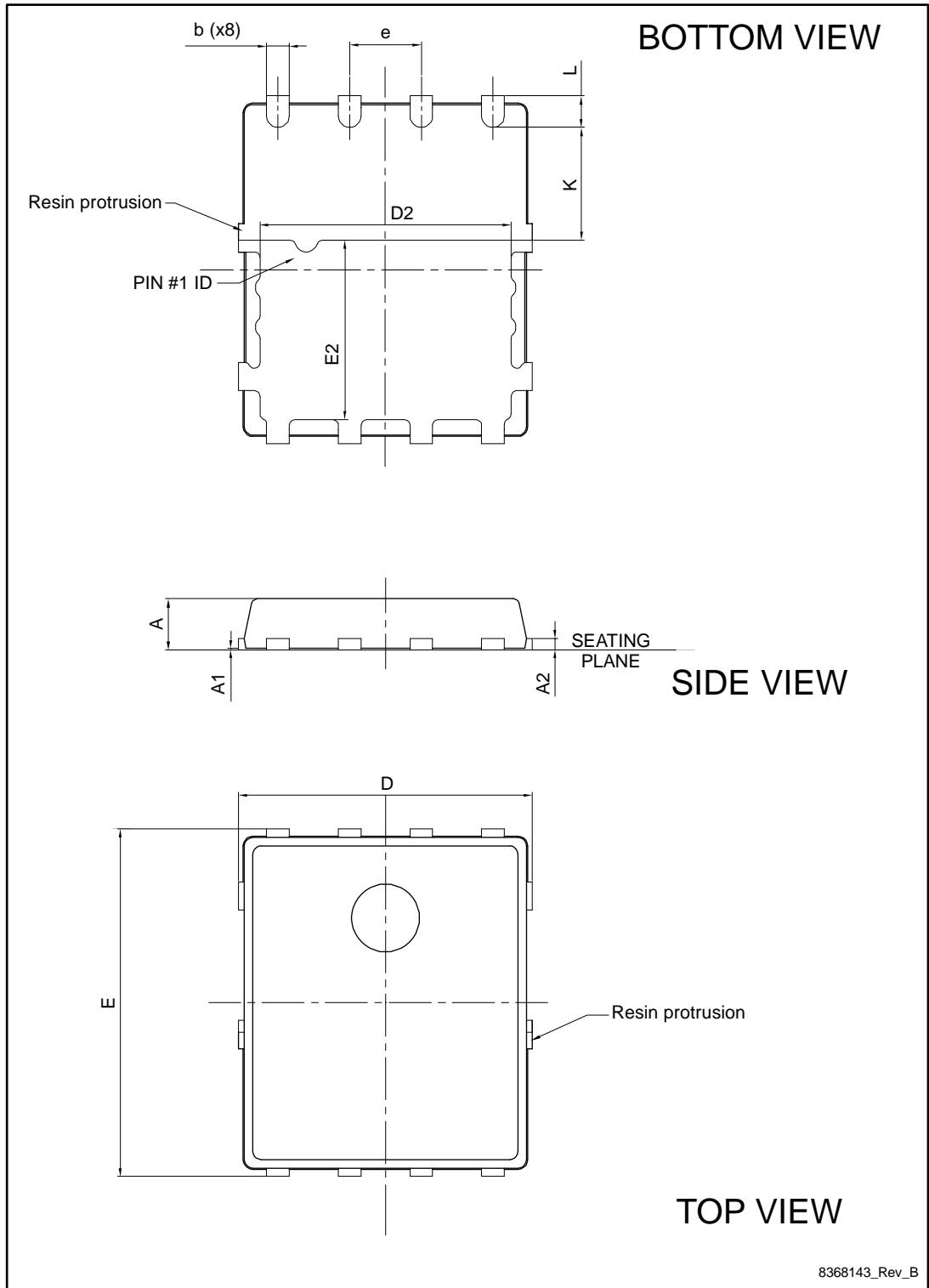
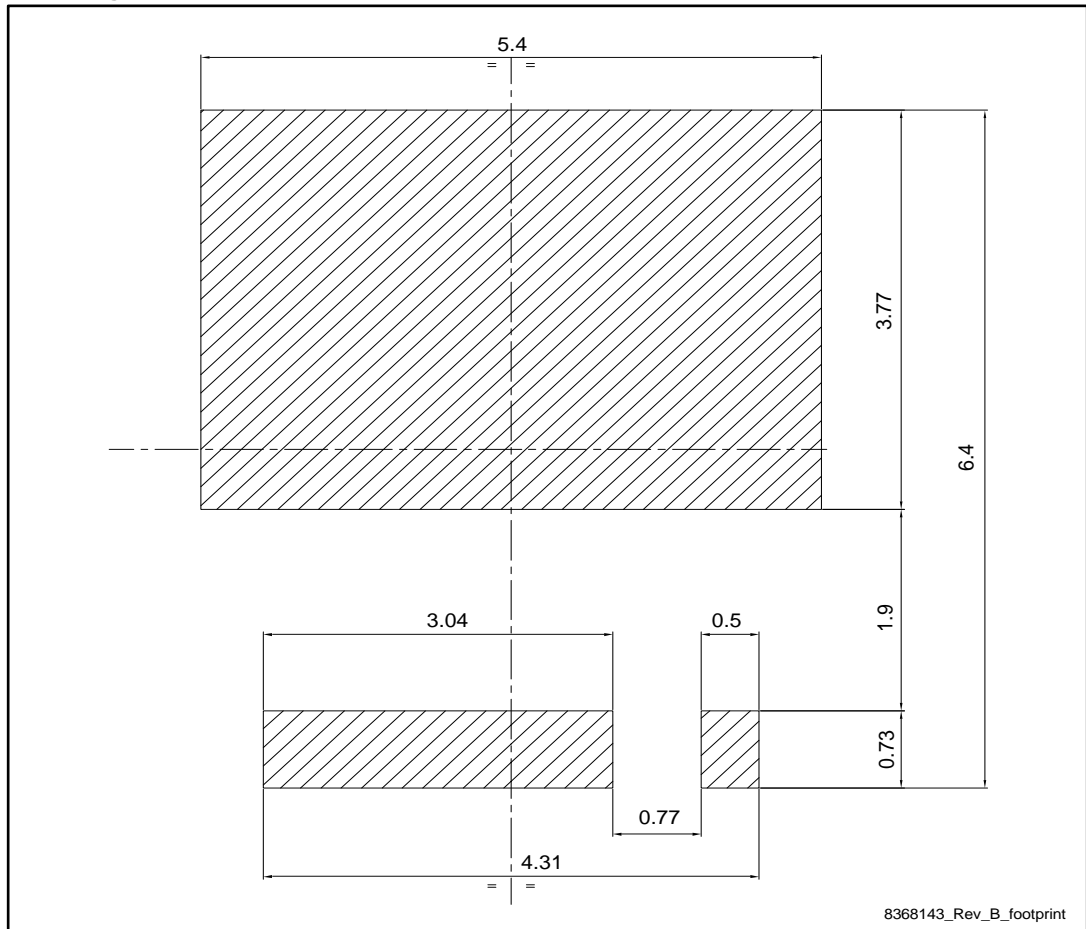


Table 9: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

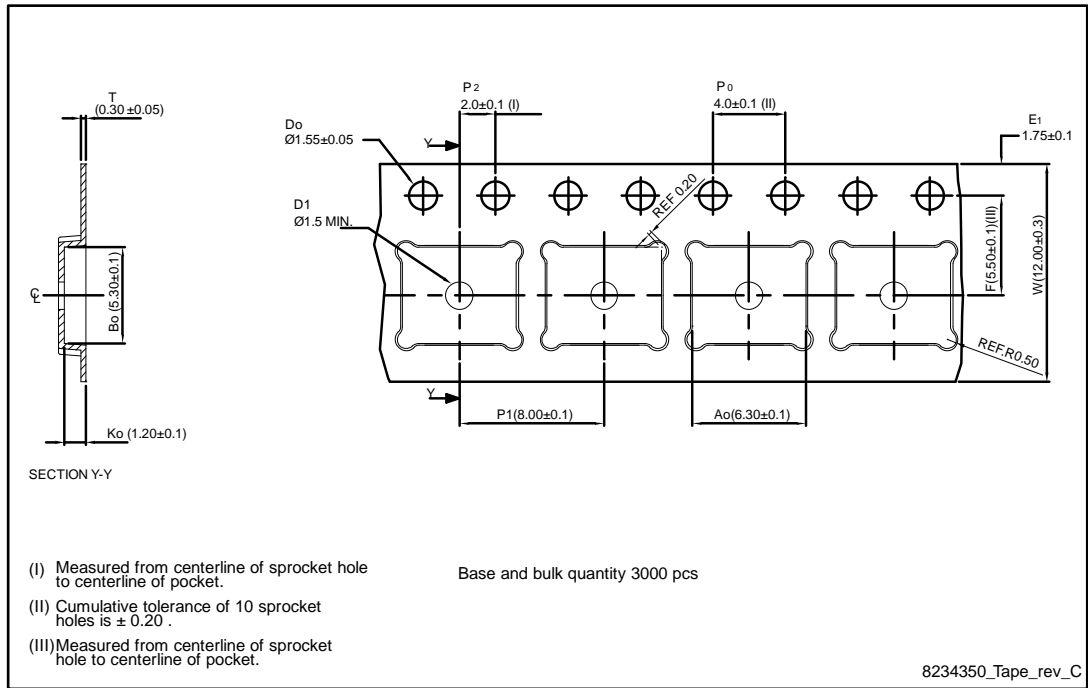


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

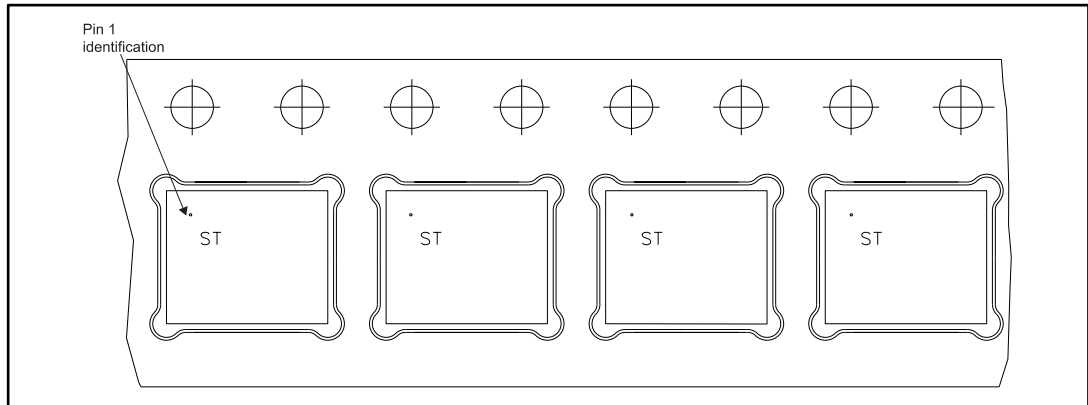
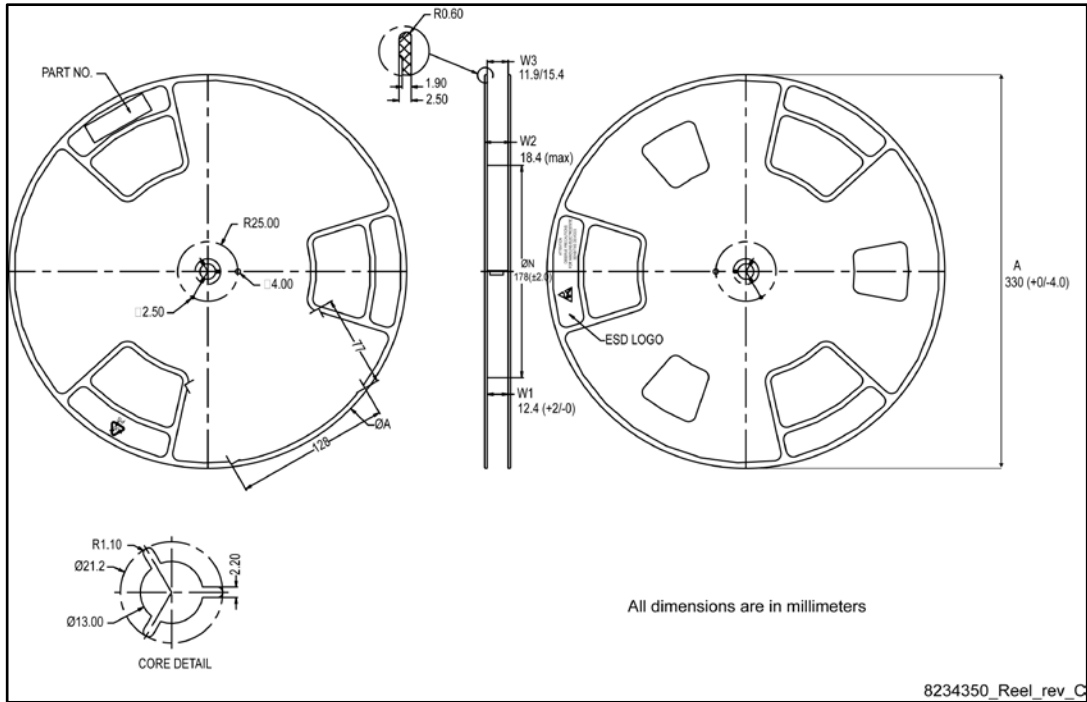


Figure 24: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
22-May-2015	1	First release.

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Тел: +7 (812) 336 43 04 (многоканальный)  
Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)