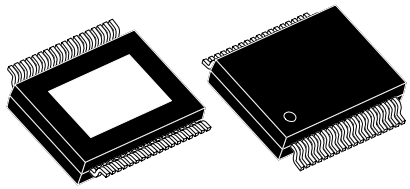
# STA333BW

## 2.1-channel 40-watt high-efficiency digital audio system Sound Terminal®

## Features

- Wide-range supply voltage, 4.5 V to 21.5 V
- Three power output configurations:
  - 2 channels of ternary PWM (2 x 20 W into 8 Ω at 18 V) + PWM output
  - 2 channels of ternary PWM (2 x 20 W into 8 Ω at 18 V) + ternary stereo line-out
  - 2.1 channels of binary PWM (left, right, LFE) (2 x 9 W into 4 Ω +1 x 20 W into 8 Ω at 18 V)
- FFX with 100-dB SNR and dynamic range
- Scalable FFX modulation index
- Selectable 32- to 192-kHz input sample rates
- $I^2C$ control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB with 0.5-dB/step resolution
- Soft volume update with programmable ratio
- Individual channel and master gain/attenuation
- Dynamic range compression (DRC) or anticlipping mode
- Audio presets:
  - 15 preset crossover filters
  - 5 preset anticlipping modes
  - Preset night-time listening mode
- Individual channel soft/hard mute
- Independent channel volume and DSP bypass
- $I^2S$ input data interface



**PowerSSO-36 with exposed pad down (EPD)**

- Input and output channel mapping
- Automatic invalid input-detect mute
- Up to 5 user-programmable biquads/channel
- Three coefficients banks for EQ presets storing with fast recall via $I^2C$ interface
- Bass/treble tones and de-emphasis control
- Selectable high-pass filter for DC blocking
- Advanced AM interference frequency switching and noise suppression modes
- Sub channel mix into left and right channels
- Selectable high- or low-bandwidth noise-shaping topologies
- Selectable clock input ratio
- 96-kHz internal processing sample rate
- Thermal overload and short-circuit protection technology
- Video apps: 576 x $f_S$ input mode supported
- Pin and SW compatible with STA335BW, STA339BW, STA339BWS, STA559BW and STA559BWS

**Table 1. Device summary**

| Order code | Package | Packaging |
|---|---|---|
| STA333BW | PowerSSO-36 EPD | Tube |
| STA333BW13TR | PowerSSO-36 EPD | Tape and reel |

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# 1 Description

The STA333BW is an integrated solution of digital audio processing, digital amplifier controls and power output stages to create a high-power single-chip FFX digital amplifier with high-quality and high-efficiency. Three channels of FFX processing are provided. The FFX processor implements the ternary, binary and binary differential processing capabilities of the full FFX processor.

The STA333BW is part of the Sound Terminal® family that provides full digital audio streaming to the speakers and offers cost effectiveness, low power dissipation and sound enrichment.

The power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes.

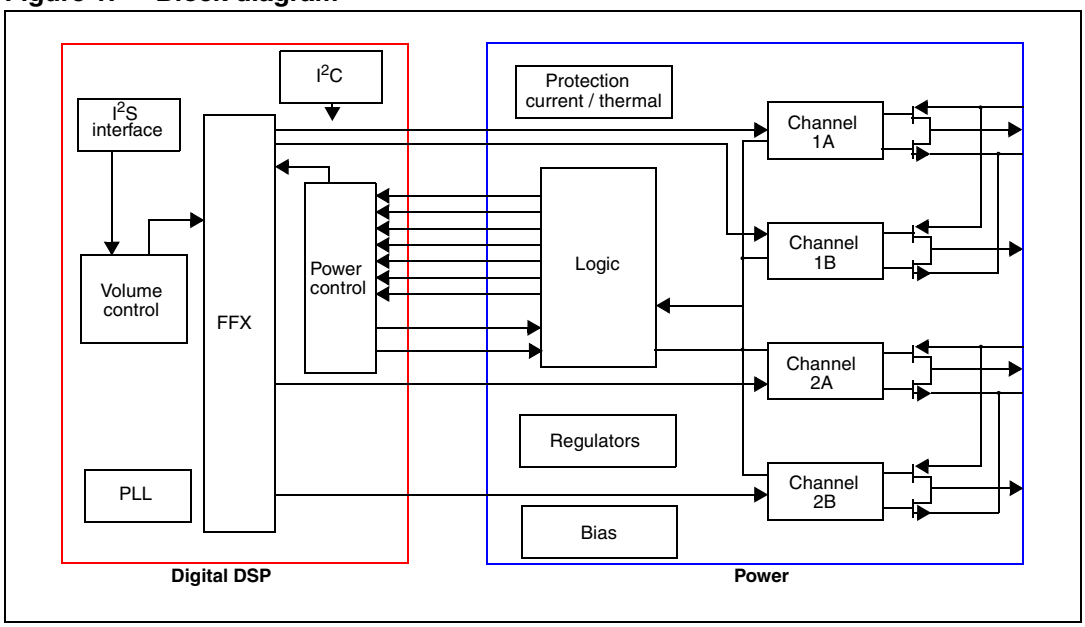
For example, 2.1 channels can be provided by two half-bridges and a single full-bridge, supplying up to 2 x 9 W + 1 x 20 W of output power or two channels can be provided by two full-bridges, supplying up to 2 x 20 W of output power.

The IC can also be configured as 2.1 channels with 2 x 20 W supplied by the device plus a drive for an external FFX power amplifier, such as STA533WF or STA515W.

The serial audio data input interface accepts all possible formats, including the popular $I^2S$ format. The high-quality conversion from PCM audio to FFX PWM switching provides over 100 dB of SNR and of dynamic range.

Also provided in the STA333BW are a full assortment of digital processing features. This includes up to 5 programmable biquads (EQ) per channel. Available presets enable a time-to-market advantage by substantially reducing the amount of software development needed for functions such as audio preset volume loudness, preset volume curves and preset EQ settings. There are also new advanced AM radio interference reduction modes. The DRC dynamically equalizes the system to provide a linear frequency speaker response regardless of output power level.

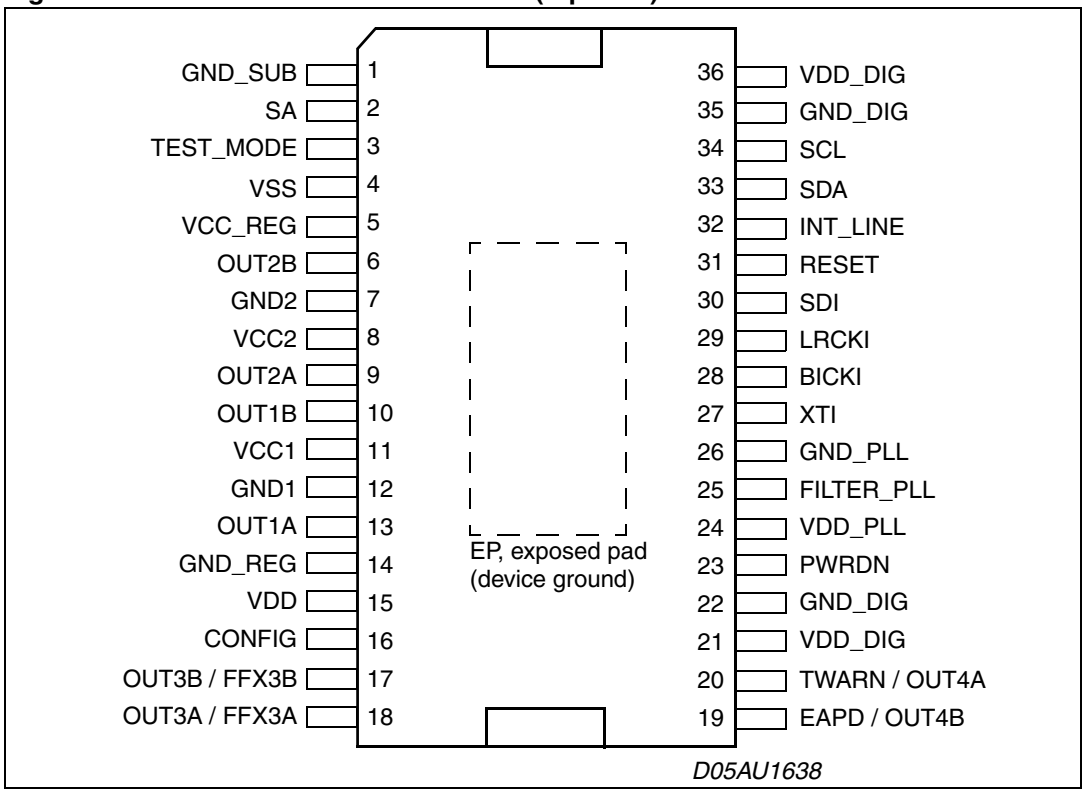
**Figure 1. Block diagram**



# 2 Pin connections

## 2.1 Connection diagram

**Figure 2. Pin connection PowerSSO-36 (top view)**




## 2.2 Pin description

**Table 2. Pin description**

| Pin | Type | Name | Description |
|---|---|---|---|
| 1 | GND | GND_SUB | Substrate ground |
| 2 | I | SA | $I^2C$ select address (pull-down) |
| 3 | I | TEST_MODE | This pin must be connected to ground (pull-down) |
| 4 | I/O | VSS | Internal reference at $V_{CC}$ - 3.3 V |
| 5 | I/O | VCC_REG | Internal $V_{CC}$ reference |
| 6 | O | OUT2B | Output half-bridge channel 2B |
| 7 | GND | GND2 | Power negative supply |
| 8 | Power | VCC2 | Power positive supply |
| 9 | O | OUT2A | Output half-bridge channel 2A |
| 10 | O | OUT1B | Output half-bridge channel 1B |

Table 2. Pin description (continued)

| Pin | Type | Name | Description |
|---|---|---|---|
| 11 | Power | VCC1 | Power positive supply |
| 12 | GND | GND1 | Power negative supply |
| 13 | O | OUT1A | Output half-bridge channel 1A |
| 14 | GND | GND_REG | Internal ground reference |
| 15 | Power | VDD | Internal 3.3 V reference voltage |
| 16 | I | CONFIG | Parallel mode command |
| 17 | O | OUT3B / FFX3B | PWM out channel 3B / external bridge driver |
| 18 | O | OUT3A / FFX3A | PWM out channel 3A / external bridge driver |
| 19 | O | EAPD / OUT4B | Power down for external bridge / PWM out channel 4B |
| 20 | I/O | TWARN / OUT4A | Thermal warning from external bridge (pull-up when input) / PWM out channel 4A |
| 21 | Power | VDD_DIG | Digital supply voltage |
| 22 | GND | GND_DIG | Digital ground |
| 23 | I | PWRDN | Power down (pull-up) |
| 24 | Power | VDD_PLL | Positive supply for PLL |
| 25 | I | FILTER_PLL | Connection to PLL filter |
| 26 | GND | GND_PLL | Negative supply for PLL |
| 27 | I | XTI | PLL input clock |
| 28 | I | BICKI | $I^2S$ serial clock |
| 29 | I | LRCKI | $I^2S$ left / right clock |
| 30 | I | SDI | $I^2S$ serial data channels 1 and 2 |
| 31 | I | RESET | Reset (pull-up) |
| 32 | O | INT_LINE | Fault interrupt |
| 33 | I/O | SDA | $I^2C$ serial data |
| 34 | I | SCL | $I^2C$ serial clock |
| 35 | GND | GND_DIG | Digital ground |
| 36 | Power | VDD_DIG | Digital supply voltage |
| - | - | EP | Exposed pad for PCB heatsink, to be connected to GND |

# 3 Electrical specifications

## 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage (pins VCCx) | -0.3 | - | 24 | V |
| $V_{DD}$ | Digital supply voltage (pins VDD_DIG) | -0.3 | - | 4.0 | V |
| $V_{DD}$ | PLL supply voltage (pin VDD_PLL) | -0.3 | - | 4.0 | V |
| $T_{op}$ | Operating junction temperature | -20 | - | 150 | °C |
| $T_{stg}$ | Storage temperature | -40 | - | 150 | °C |

**Warning: Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions, may experience some rising beyond the maximum operating conditions for a short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.**

## 3.2 Thermal data

**Table 4. Thermal data**

| | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case (thermal pad) | - | - | 1.5 | °C/W |
| $T_{th\text{-}sdj}$ | Thermal shut-down junction temperature | - | 150 | - | °C |
| $T_{th\text{-}w}$ | Thermal warning temperature | - | 130 | - | °C |
| $T_{th\text{-}sdh}$ | Thermal shut-down hysteresis | - | 20 | - | °C |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient (1) | - | 24 | - | °C/W |

1. See *Chapter 8: Package thermal characteristics on page 63* for details.

## 3.3 Recommended operating conditions

**Table 5. Recommended operating condition**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage (VCCxA, VCCxB) | 4.5 | - | 21.5 | V |
| $V_{DD_DIG}$ | Digital supply voltage | 2.7 | 3.3 | 3.6 | V |
| $V_{DD_PLL}$ | PLL supply voltage | 2.7 | 3.3 | 3.6 | V |
| $T_{amb}$ | Ambient temperature | -20 | - | 70 | °C |

## 3.4 Electrical specifications for the digital section

The specifications given in this section are valid for $T_{amb}$ = 25 °C unless otherwise specified.

**Table 6. Electrical specifications - digital section**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{il}$ | Low level input current without pull-up/down device | Vi = 0 V | - | - | 1 | µA |
| $I_{ih}$ | High level input current without pull-up/down device | Vi = VDD_DIG = 3.6 V | - | - | 1 | µA |
| $V_{il}$ | Low level input voltage | - | - | - | 0.2 * VDD_DIG | V |
| $V_{ih}$ | High level input voltage | - | 0.8 * VDD_DIG | - | - | V |
| $V_{ol}$ | Low level output voltage | Iol = 2 mA | | - | 0.4 * VDD_DIG | V |
| $V_{oh}$ | High level output voltage | Ioh = 2 mA | 0.8 * VDD_DIG | - | - | V |
| $R_{pu}$ | Equivalent pull-up/down resistance | - | - | 50 | - | kΩ |

## 3.5 Electrical specifications for the power section

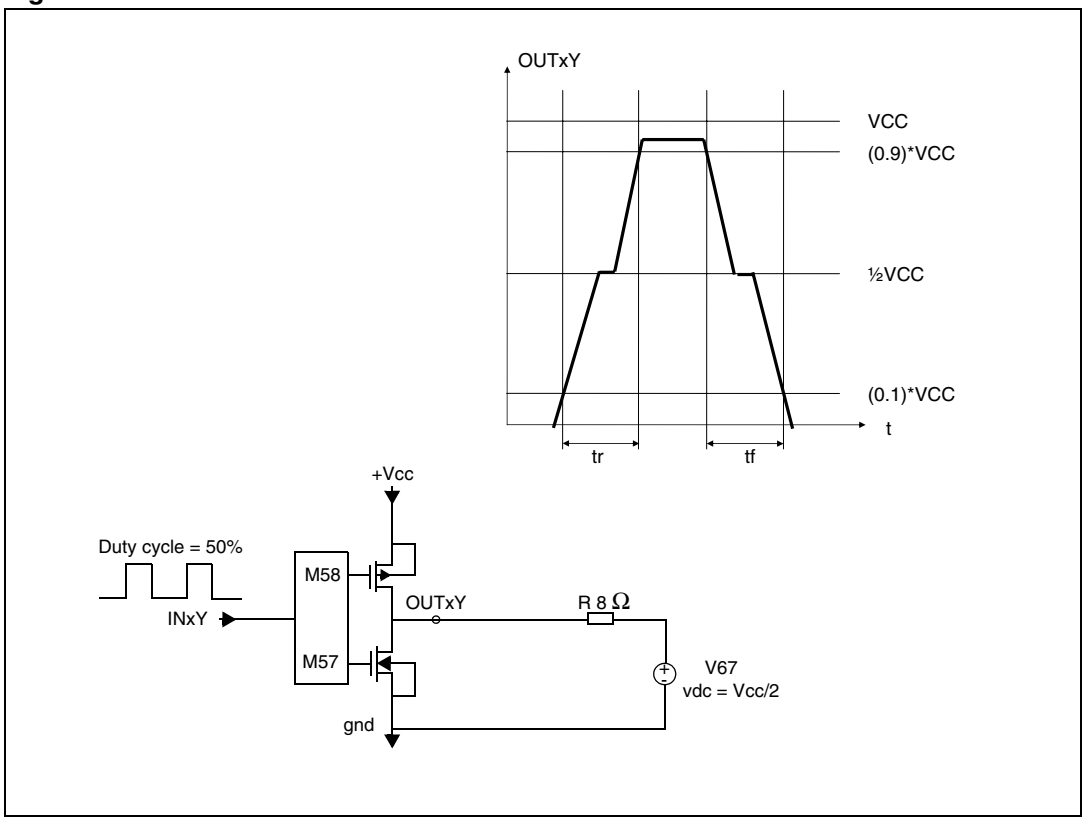
The specifications given in this section are valid for the operating conditions: $V_{CC}$ = 18 V, f = 1 kHz, $f_{sw}$ = 384 kHz, $T_{amb}$ = 25 °C and $R_L$ = 8 Ω, unless otherwise specified.

**Table 7. Electrical specifications - power section**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Po | Output power BTL | THD = 1% | - | 16 | - | W |
| | | THD = 10% | - | 20 | - | |
| | Output power SE | THD = 1%, $R_L$= 4 Ω | - | 7 | - | W |
| | | THD = 10%, $R_L$= 4 Ω | - | 9 | - | |
| $R_{dsON}$ | Power P-channel or N-channel MOSFET | $I_d$ = 0.75 A | - | - | 250 | mΩ |
| gP | Power P-channel $R_{dsON}$ matching | $I_d$ = 0.75 A | - | 100 | - | % |
| gN | Power N-channel $R_{dsON}$ matching | $I_d$ = 0.75 A | - | 100 | - | % |
| Idss | Power P-channel / N-channel leakage | $V_{CC}$ = 20 V | - | - | 1 | µA |
| $t_r$ | Rise time | Resistive load, see *Figure 3* below | - | - | 10 | ns |
| $t_f$ | Fall time | | - | - | 10 | ns |
| $I_{VCC}$ | Supply current from $V_{CC}$ in power down | PWRDN = 0 | - | 0.3 | - | µA |
| | Supply current from $V_{CC}$ in operation | PWRDN = 1 | - | 15 | - | mA |
| $I_{VDD}$ | Supply current FFX processing | Internal clock = 49.152 MHz | - | 55 | - | mA |
| $I_{LIM}$ | Overcurrent limit | (1) | 2.2 | 3.0 | - | A |
| $I_{SCP}$ | Short -circuit protection | $R_L$ = 0 Ω | 2.7 | 3.6 | - | A |
| $V_{UVP}$ | Undervoltage protection | - | - | - | 4.3 | V |
| $t_{min}$ | Output minimum pulse width | No load | 20 | 40 | 60 | ns |
| DR | Dynamic range | - | - | 100 | - | dB |
| SNR | Signal to noise ratio, ternary mode | A-Weighted | - | 100 | - | dB |
| | Signal to noise ratio binary mode | - | - | 90 | - | dB |
| THD+N | Total harmonic distortion + noise | FFX stereo mode, Po = 1 W f = 1 kHz | - | 0.2 | - | % |
| $X_{TALK}$ | Crosstalk | FFX stereo mode, <5 kHz One channel driven at 1 W, other channel measured | - | 80 | - | dB |
| η | Peak efficiency, FFX mode | Po = 2 x 20 W into 8 Ω | - | 90 | - | % |
| | Peak efficiency, binary modes | Po = 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω | - | 87 | - | |

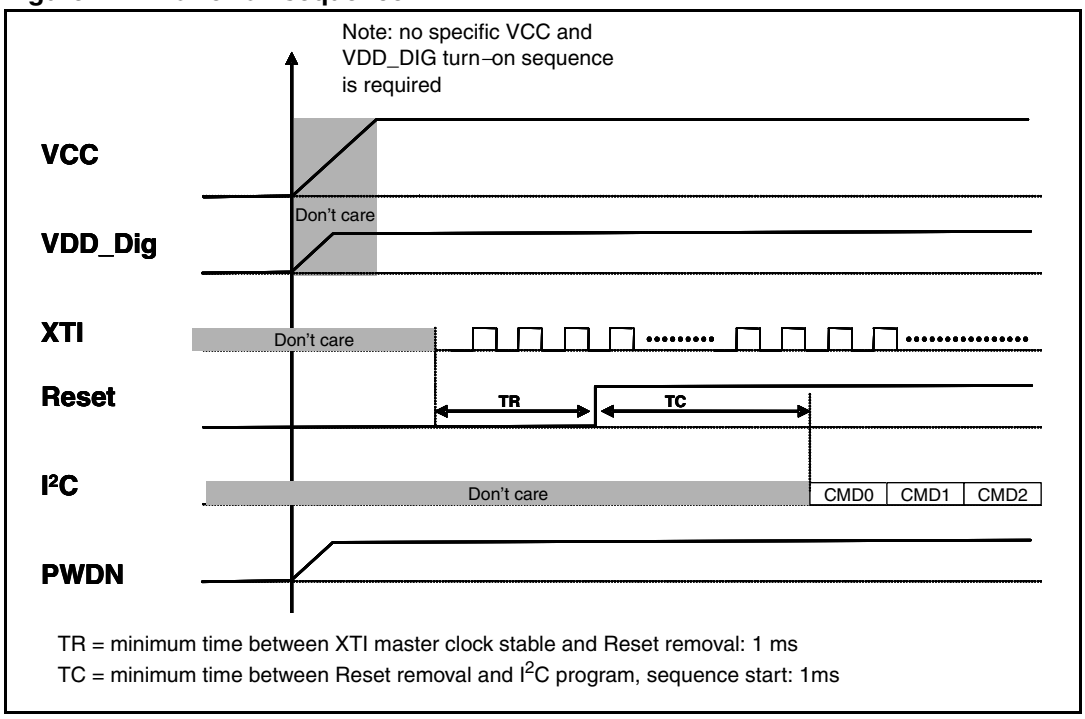
1. Limit the current if overcurrent warning detect adjustment bypass is enabled (register bit CONFC.OCRB *on page 28*). When disabled refer to the $I_{SCP}$.

**Figure 3. Test circuit**



## 3.6 Power-on/off sequence

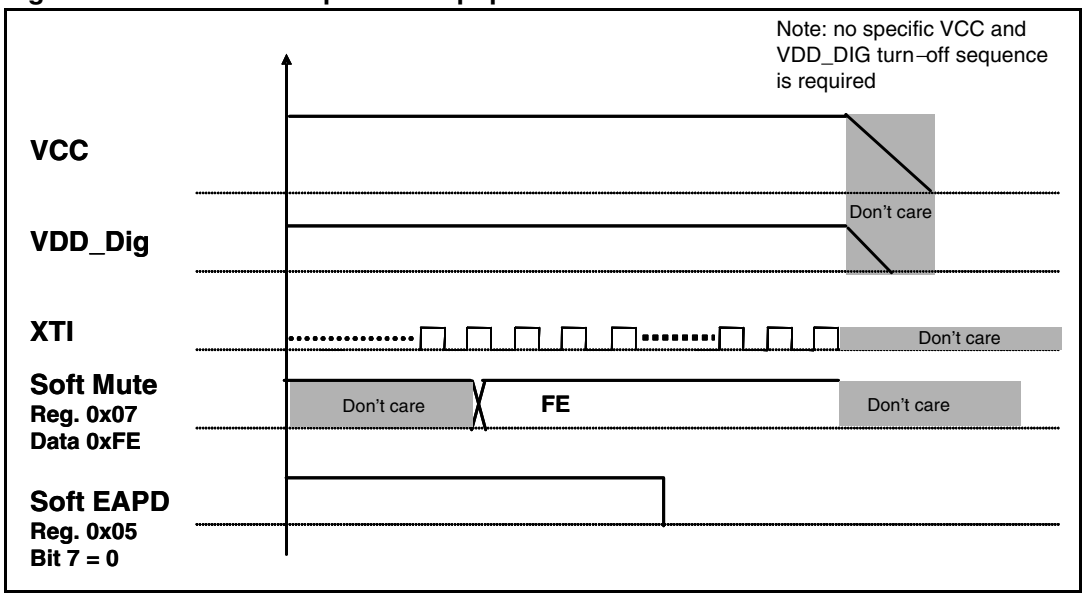
**Figure 4. Power-on sequence**




*Note: The definition of a stable clock is when $f_{max}$ - $f_{min}$ < 1 MHz.*

Section *Serial audio input interface format on page 25* gives information on setting up the $I^2S$ interface.

**Figure 5. Power-off sequence for pop-free turn-off**



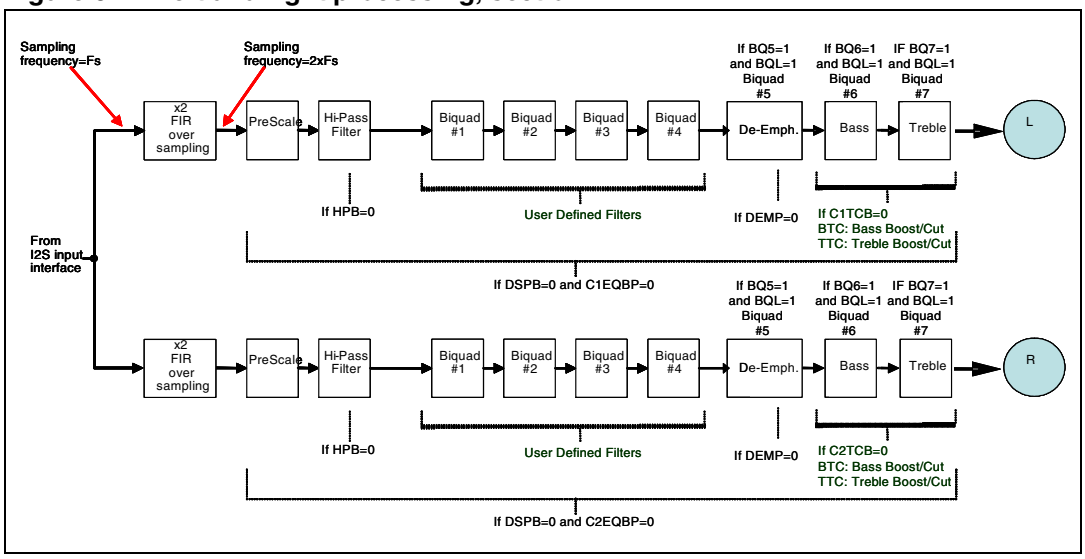
# 4 Processing data paths

*Figure 6* and *Figure 7* below show the data processing paths inside STA333BW. The whole processing chain is composed of two consecutive sections. In the first one, dual-channel processing is implemented and in the second section each channel is fed into the post mixing block either to generate a third channel (typically used in 2.1 output configuration and with crossover filters enabled) or to have the channels processed by the DRC block (2.0 output configuration with crossover filters used to define the cut-off frequency of the two bands).

The first section, *Figure 6*, begins with a 2x oversampling FIR filter providing 2 * $f_S$ audio processing. Then a selectable high-pass filter removes the DC level (enabled if HPB = 0). The left and right channel processing paths can include up to 8 filters, depending on the selected configuration (bits BQL, BQ5, BQ6, BQ7 and XO[3:0]). By default, four user programmable, independent filters per channel are enabled, plus the preconfigured de-emphasis, bass and treble controls (BQL = 0, BQ5 = 0, BQ6 = 0, BQ7 = 0).

If the coefficient sets for the two channels are linked (BQL = 1) it is possible to use the de-emphasis, bass and treble filters in a user defined configuration (provided the relevant BQx bits are set). In this case both channels use the same processing coefficients and can have up to seven filters each. If BQL = 0 the BQx bits are ignored and the fifth, sixth and seventh filters are configured as de-emphasis, bass and treble controls, respectively.

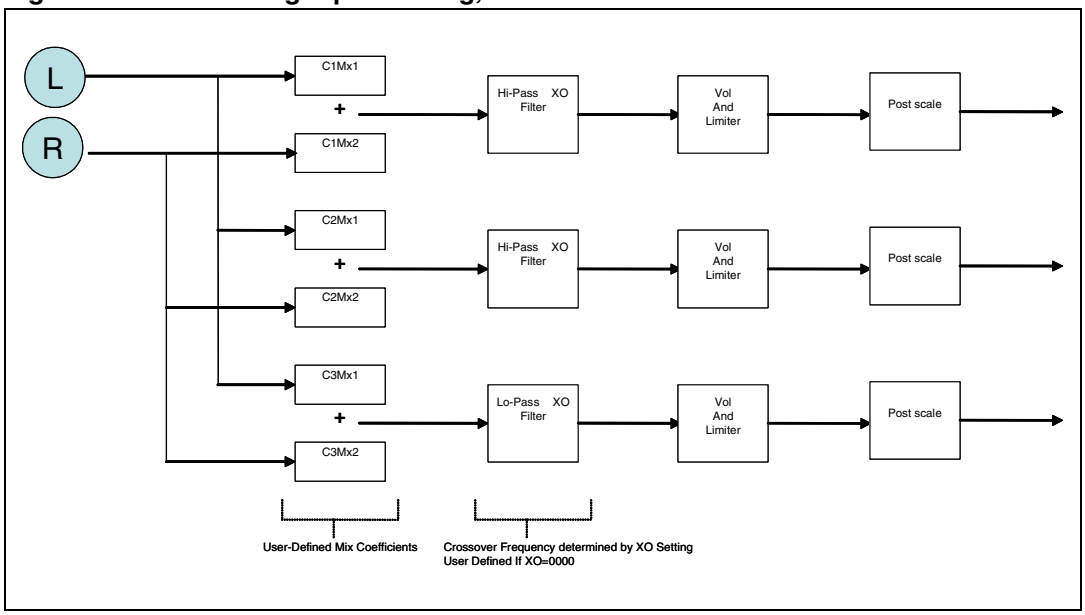
**Figure 6. Left and right processing, section 1**




Moreover, the common 8th filter can be available on both channels provided the predefined crossover frequencies are not used, XO[3:0] = 0, and the DRC is not used.

In the second section, *Figure 7*, mixing and crossover filters are available. If DRC is not enabled they are fully user-programmable and allow the generation of a third channel (2.1 outputs). Alternatively, in mode DRC, these blocks are used to split the sub-band and define the cut-off frequencies of the two bands. A prescaler and a final postscaler allow full control over the signal dynamics before and after the filtering stages. A mixer function is also available.

**Figure 7. Left and right processing, section 2**



# 5 I²C bus specification

The STA333BW supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA333BW is always a slave device in all of its communications. It supports up to 400 kb/s (fast-mode bit rate).

For correct operation of the I²C interface ensure that the master clock generated by the PLL has a frequency at least 10 times higher than the frequency of the applied SCL clock.

## 5.1 Communication protocol

### 5.1.1 Data transition or change

Data changes on the SDA line must only occur when the clock SCL is low. A SDA transition while the clock is high is used to identify a START or STOP condition.

### 5.1.2 Start condition

START is identified by a high to low transition of the data bus, SDA, while the clock, SCL, is stable in the high state. A START condition must precede any command for data transfer.

### 5.1.3 Stop condition

STOP is identified by low to high transition of SDA while SCL is stable in the high state. A STOP condition terminates communication between STA333BW and the bus master.

### 5.1.4 Data input

During the data input the STA333BW samples the SDA signal on the rising edge of SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

## 5.2 Device addressing

To start communication between the master and the STA333BW, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode bit.

The seven most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA333BW the I²C interface has two device addresses depending on the SA pin configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The eighth bit (LSB) identifies a read or write operation (R/W); this is set to 1 for read and to 0 for write. After a START condition the STA333BW identifies the device address on the SDA bus and if a match is found, acknowledges the identification during the 9th bit time frame. The byte following the device identification is the address of a device register.

## 5.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333BW acknowledges this and then waits for the byte of internal address. After receiving the internal byte address the STA333BW again responds with an acknowledgement.

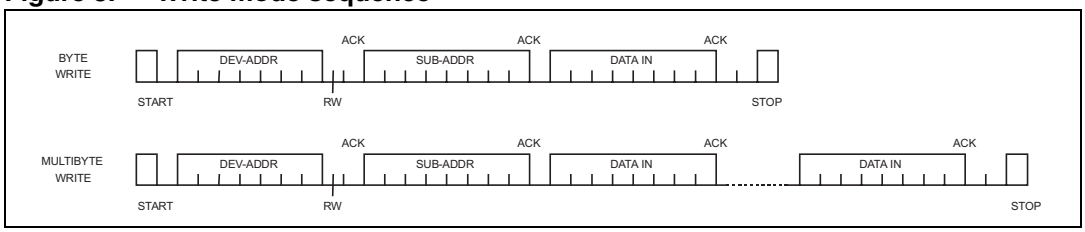
### 5.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA333BW. The master then terminates the transfer by generating a STOP condition.

### 5.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

**Figure 8. Write mode sequence**




## 5.4 Read operation

### 5.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA333BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

### 5.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA333BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

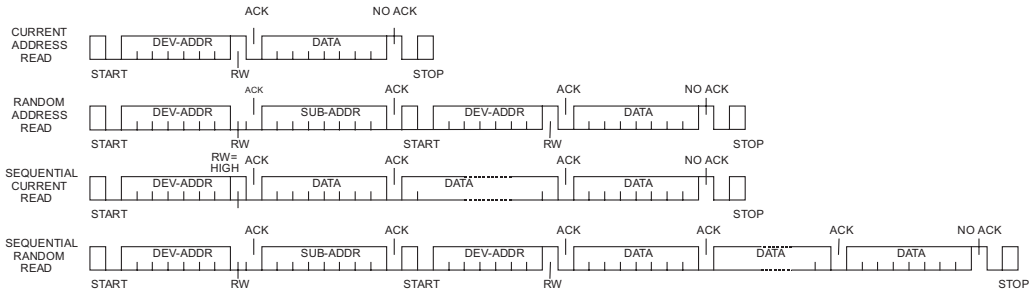
### 5.4.3 Random address byte read

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333BW acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA333BW again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA333BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

### 5.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA333BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

**Figure 9. Read mode sequence**



# 6 Register description

*Note: Addresses exceeding the maximum address number must not be written.*

**Table 8. Register summary**

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CONFA | FDRB | TWAB | TWRB | IR1 | IR0 | MCS2 | MCS1 | MCS0 |
| 0x01 | CONFB | C2IM | C1IM | DSCKE | SAIFB | SAI3 | SAI2 | SAI1 | SAI0 |
| 0x02 | CONFC | OCRB | Reserved | CSZ3 | CSZ2 | CSZ1 | CSZ0 | OM1 | OM0 |
| 0x03 | CONFD | SME | ZDE | DRC | BQL | PSL | DSPB | DEMP | HPB |
| 0x04 | CONFE | SVE | ZCE | DCCV | PWMS | AME | NSBW | MPC | MPCV |
| 0x05 | CONFF | EAPD | PWDN | ECLE | LDTE | BCLE | IDE | OCFG1 | OCFG0 |
| 0x06 | MUTELOC | LOC1 | LOC0 | Reserved | Reserved | C3M | C2M | C1M | Reserved |
| 0x07 | MVOL | MVOL[7:0] | | | | | | | |
| 0x08 | C1VOL | C1VOL[7:0] | | | | | | | |
| 0x09 | C2VOL | C2VOL[7:0] | | | | | | | |
| 0x0A | C3VOL | C3VOL[7:0] | | | | | | | |
| 0x0B | AUTO1 | Reserved | Reserved | AMGC[1:0] | | Reserved | Reserved | Reserved | Reserved |
| 0x0C | AUTO2 | XO3 | XO2 | XO1 | XO0 | AMAM2 | AMAM1 | AMAM0 | AMAME |
| 0x0D | AUTO3 | Reserved | | | | | | | |
| 0x0E | C1CFG | C1OM1 | C1OM0 | C1LS1 | C1LS0 | C1BO | C1VBP | C1EQBP | C1TCB |
| 0x0F | C2CFG | C2OM1 | C2OM0 | C2LS1 | C2LS0 | C2BO | C2VBP | C2EQBP | C2TCB |
| 0x10 | C3CFG | C3OM1 | C3OM0 | C3LS1 | C3LS0 | C3BO | C3VBP | Reserved | Reserved |
| 0x11 | TONE | TTC3 | TTC2 | TTC1 | TTC0 | BTC3 | BTC2 | BTC1 | BTC0 |
| 0x12 | L1AR | L1A3 | L1A2 | L1A1 | L1A0 | L1R3 | L1R2 | L1R1 | L1R0 |
| 0x13 | L1ATRT | L1AT3 | L1AT2 | L1AT1 | L1AT0 | L1RT3 | L1RT2 | L1RT1 | L1RT0 |
| 0x14 | L2AR | L2A3 | L2A2 | L2A1 | L2A0 | L2R3 | L2R2 | L2R1 | L2R0 |
| 0x15 | L2ATRT | L2AT3 | L2AT2 | L2AT1 | L2AT0 | L2RT3 | L2RT2 | L2RT1 | L2RT0 |
| 0x16 | CFADDR | Reserved | Reserved | CFA[5:0] | | | | | |
| 0x17 | B1CF1 | C1B[23:16] | | | | | | | |
| 0x18 | B1CF2 | C1B[15:8] | | | | | | | |
| 0x19 | B1CF3 | C1B[7:0] | | | | | | | |
| 0x1A | B2CF1 | C2B[23:16] | | | | | | | |
| 0x1B | B2CF2 | C2B[15:8] | | | | | | | |
| 0x1C | B2CF3 | C2B[7:0] | | | | | | | |
| 0x1D | A1CF1 | C3B[23:16] | | | | | | | |
| 0x1E | A1CF2 | C3B[15:8] | | | | | | | |

Table 8. Register summary (continued)

| Addr | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x1F | A1CF3 | C3B[7:0] | | | | | | | |
| 0x20 | A2CF1 | C4B[23:16] | | | | | | | |
| 0x21 | A2CF2 | C4B[15:8] | | | | | | | |
| 0x22 | A2CF3 | C4B[7:0] | | | | | | | |
| 0x23 | B0CF1 | C5B[23:16] | | | | | | | |
| 0x24 | B0CF2 | C5B[15:8] | | | | | | | |
| 0x25 | B0CF3 | C5B[7:0] | | | | | | | |
| 0x26 | CFUD | Reserved | | | | RA | R1 | WA | W1 |
| 0x27 | MPCC1 | MPCC[15:8] | | | | | | | |
| 0x28 | MPCC2 | MPCC[7:0] | | | | | | | |
| 0x29 | DCC1 | DCC[15:8] | | | | | | | |
| 0x2A | DCC2 | DCC[7:0] | | | | | | | |
| 0x2B | FDRC1 | FDRC[15:8] | | | | | | | |
| 0x2C | FDRC2 | FDRC[7:0] | | | | | | | |
| 0x2D | STATUS | PLLUL | FAULT | UVFAULT | Reserved | OCFAULT | OCWARN | TFAULT | TWARN |

# 6.1 Configuration registers (addr 0x00 to 0x05)

## 6.1.1 Configuration register A (addr 0x00)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FDRB | TWAB | TWRB | IR1 | IR0 | MCS2 | MCS1 | MCS0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

### Master clock select

Table 9. Master clock select

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 1 | MCS0 | Selects the ratio between the input $I^2S$ sample frequency and the input clock. |
| 1 | R/W | 1 | MCS1 | |
| 2 | R/W | 0 | MCS2 | |

The STA333BW supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency ($f_s$).

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

**Table 10. Input sampling rates**

| Input sample rate *fs* (kHz) | IR | MCS[2:0] | | | | | |
|---|---|---|---|---|---|---|---|
| | | 101 | 100 | 011 | 010 | 001 | 000 |
| 32, 44.1, 48 | 00 | 576 * fs | 128 * fs | 256 * fs | 384 * fs | 512 * fs | 768 * fs |
| 88.2, 96 | 01 | NA | 64 * fs | 128 * fs | 192 * fs | 256 * fs | 384 * fs |
| 176.4, 192 | 1X | NA | 32 * fs | 64 * fs | 96 * fs | 128 * fs | 192 * fs |

## Interpolation ratio select

**Table 11. Internal interpolation ratio**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 4:3 | R/W | 00 | IR [1:0] | Selects internal interpolation ratio based on input $I^2S$ sample frequency |

The STA333BW has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 2-times or 1-time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

**Table 12. IR bit settings as a function of input sample rate**

| Input sample rate fs (kHz) | IR | 1st stage interpolation ratio |
|---|---|---|
| 32 | 00 | 2-times oversampling |
| 44.1 | 00 | 2-times oversampling |
| 48 | 00 | 2-times oversampling |
| 88.2 | 01 | Pass-through |
| 96 | 01 | Pass-through |
| 176.4 | 10 | 2-times downsampling |
| 192 | 10 | 2-times downsampling |

### Thermal warning recovery bypass

**Table 13. Thermal warning recovery bypass**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 5 | R/W | 1 | TWRB | 0: thermal warning recovery enabled<br>1: thermal warning recovery disabled |

This bit sets the behavior of the IC after a thermal warning disappears. If TWRB is enabled the device automatically restores the normal gain and output limiting is no longer active. If it is disabled the device keeps the output limit active until a reset is asserted or until TWRB set to 0. This bit works in conjunction with TWAB

### Thermal warning adjustment bypass

**Table 14. Thermal warning adjustment bypass**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 6 | R/W | 1 | TWAB | 0: thermal warning adjustment enabled<br>1: thermal warning adjustment disabled |

Bit TWAB enables automatic output limiting when a power stage thermal warning condition persists for longer than 400ms. When the feature is active (TWAB = 0) the desired output limiting, set through bit TWOCL (-3 dB by default) at address 0x37 in the RAM coefficients bank, is applied. The way the limiting acts after the warning condition disappears is controlled by bit TWRB.

### Fault detect recovery bypass

**Table 15. Fault detect recovery bypass**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 7 | R/W | 0 | FDRB | 0: fault detect recovery enabled<br>1: fault detect recovery disabled |

The on-chip power block provides feedback to the digital controller which is used to indicate a fault condition (either overcurrent or thermal). When fault is asserted, the power control block attempts a recovery from the fault by asserting the 3-state output, holding it for period of time in the range of 0.1 ms to 1 second, as defined by the fault-detect recovery constant register (FDRC registers 0x2B-0x2C), then toggling it back to normal condition. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1. The fault condition is also asserted by a low-state pulse of the normally high INT_LINE output pin.

## 6.1.2 Configuration register B (addr 0x01)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C2IM | C1IM | DSCKE | SAIFB | SAI3 | SAI2 | SAI1 | SAI0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Serial audio input interface format

**Table 16. Serial audio input interface**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 0 | SAI0 | Determines the interface format of the input serial digital audio interface. |
| 1 | R/W | 0 | SAI1 | |
| 2 | R/W | 0 | SAI2 | |
| 3 | R/W | 0 | SAI3 | |

### Serial data interface

The STA333BW audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. STA333BW always acts as slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI.

Bits SAI and bit SAIFB are used to specify the serial data format. The default serial data format is $I^2S$, MSB first. Available formats are shown in the tables and figure that follow.

### Serial data first bit

**Table 17. Serial data first bit**

| SAIFB | Format |
|---|---|
| 0 | MSB-first |
| 1 | LSB-first |

**Table 18. Support serial audio input formats for MSB-first (SAIFB = 0)**

| BICKI | SAI [3:0] | SAIFB | Interface format |
|---|---|---|---|
| 32 * fs | 0000 | 0 | $I^2S$ 15-bit data |
| | 0001 | 0 | Left / right-justified 16-bit data |
| 48 * fs | 0000 | 0 | $I^2S$ 16 to 23-bit data |
| | 0001 | 0 | Left-justified 16 to 24-bit data |
| | 0010 | 0 | Right-justified 24-bit data |
| | 0110 | 0 | Right-justified 20-bit data |
| | 1010 | 0 | Right-justified 18-bit data |
| | 1110 | 0 | Right-justified 16-bit data |

Table 18. Support serial audio input formats for MSB-first (SAIFB = 0) (continued)

| BICKI | SAI [3:0] | SAIFB | Interface format |
|---|---|---|---|
| 64 * fs | 0000 | 0 | $I^2S$ 16 to 24-bit data |
| | 0001 | 0 | Left-justified 16 to 24-bit data |
| | 0010 | 0 | Right-justified 24-bit data |
| | 0110 | 0 | Right-justified 20-bit data |
| | 1010 | 0 | Right-justified 18-bit data |
| | 1110 | 0 | Right-justified 16-bit data |

Table 19. Supported serial audio input formats for LSB-first (SAIFB = 1)

| BICKI | SAI [3:0] | SAIFB | Interface Format |
|---|---|---|---|
| 32 * fs | 1100 | 1 | $I^2S$ 15-bit data |
| | 1110 | 1 | Left/right-justified 16-bit data |
| 48 * fs | 0100 | 1 | $I^2S$ 23-bit data |
| | 0100 | 1 | $I^2S$ 20-bit data |
| | 1000 | 1 | $I^2S$ 18-bit data |
| | 1100 | 1 | LSB first $I^2S$ 16-bit data |
| | 0001 | 1 | Left-justified 24-bit data |
| | 0101 | 1 | Left-justified 20-bit data |
| | 1001 | 1 | Left-justified 18-bit data |
| | 1101 | 1 | Left-justified 16-bit data |
| | 0010 | 1 | Right-justified 24-bit data |
| | 0110 | 1 | Right-justified 20-bit data |
| | 1010 | 1 | Right-justified 18-bit data |
| | 1110 | 1 | Right-justified 16-bit data |
| 64 * fs | 0000 | 1 | $I^2S$ 24-bit data |
| | 0100 | 1 | $I^2S$ 20-bit data |
| | 1000 | 1 | $I^2S$ 18-bit data |
| | 1100 | 1 | LSB first $I^2S$ 16-bit data |
| | 0001 | 1 | Left-justified 24-bit data |
| | 0101 | 1 | Left-justified 20-bit data |
| | 1001 | 1 | Left-justified 18-bit data |
| | 1101 | 1 | Left-justified 16-bit data |
| | 0010 | 1 | Right-justified 24-bit data |
| | 0110 | 1 | Right-justified 20-bit data |
| | 1010 | 1 | Right-justified 18-bit data |
| | 1110 | 1 | Right-justified 16-bit data |

To make the STA333BW work properly, the serial audio interface LRCKI clock must be synchronous to the PLL output clock. It means that:

- N-4< = (frequency of PLL clock) / (frequency of LRCKI) = < N+4 cycles, where N depends on the settings in *Table 12 on page 23*
- the PLL must be locked.

If these two conditions are not met, and IDE bit (register 0x05, bit 2) is set to 1, the STA333BW immediately mutes the $I^2S$ PCM data out (provided to the processing block) and it freezes any active processing task.

Clock desynchronization can happen during STA333BW operation because of source switching or TV channel change. To avoid audio side effects, like click or pop noise, it is strongly recommended to complete the following actions:

1. soft volume change
2. $I^2C$ read / write instructions

while the serial audio interface and the internal PLL are still synchronous.

### Delay serial clock enable

**Table 20. Delay serial clock enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 5 | R/W | 0 | DSCKE | 0: no serial clock delay<br>1: serial clock delay by 1 core clock cycle to tolerate anomalies in some $I^2S$ master devices |

### Channel input mapping

**Table 21. Channel input mapping**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 6 | R/W | 0 | C1IM | 0: processing channel 1 receives left $I^2S$ Input<br>1: processing channel 1 receives right $I^2S$ Input |
| 7 | R/W | 1 | C2IM | 0: processing channel 2 receives left $I^2S$ Input<br>1: processing channel 2 receives right $I^2S$ Input |

Each channel received via $I^2S$ can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing. The default settings of these registers maps each $I^2S$ input channel to its corresponding processing channel.

## 6.1.3 Configuration register C (addr 0x02)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| OCRB | Reserved | CSZ3 | CSZ2 | CSZ1 | CSZ0 | OM1 | OM0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

### FFX power output mode

The FFX power output mode selects how the FFX output timing is configured.

Different power devices use different output modes.

**Table 22. FFX power output mode**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 1 | OM0 | Selects configuration of FFX output:<br>00: drop compensation<br>01: discrete output stage: tapered compensation<br>10: full-power mode<br>11: variable drop compensation (CSZx bits) |
| 1 | R/W | 1 | OM1 | |

### FFX compensating pulse size register

**Table 23. FFX compensating pulse size bits**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 2 | R/W | 1 | CSZ0 | When OM[1,0] = 11, this register determines the size of the FFX compensating pulse from 0 clock ticks to 15 clock periods. |
| 3 | R/W | 1 | CSZ1 | |
| 4 | R/W | 1 | CSZ2 | |
| 5 | R/W | 0 | CSZ3 | |

**Table 24. Compensating pulse size**

| CSZ[3:0] | Compensating pulse size |
|---|---|
| 0000 | 0 ns (0 tick) compensating pulse size |
| 0001 | 20 ns (1 tick) clock period compensating pulse size |
| … | … |
| 1111 | 300 ns (15 tick) clock period compensating pulse size |

### Overcurrent warning adjustment bypass

**Table 25. Overcurrent warning bypass**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 7 | R/W | 1 | OCRB | 0: overcurrent warning adjustment enabled<br>1: overcurrent warning adjustment disabled |

The OCRB is used to indicate how STA333BW behaves when an overcurrent warning condition occurs. If OCRB = 0 and the overcurrent condition happens, the power control block forces an adjustment to the modulation limit (default is -3 dB) in an attempt to eliminate the overcurrent warning condition. Once the overcurrent warning clipping adjustment is applied, it remains in this state until reset is applied or OCRB is set to 1. The level of adjustment can be changed via the TWOCL (thermal warning / overcurrent limit) setting at address 0x37 of the user defined coefficient RAM (*Section 6.7.7 on page 54*). The OCRB can be enabled when the output bridge is already on.

### 6.1.4 Configuration register D (addr 0x03)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SME | ZDE | DRC | BQL | PSL | DSPB | DEMP | HPB |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

#### High-pass filter bypass

**Table 26. High-pass filter bypass**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 0 | HPB | 1: bypass internal AC coupling digital high-pass filter |

The STA333BW features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a FFX amplifier. DC signals can cause speaker damage. When HPB = 0, this filter is enabled.

#### De-emphasis

**Table 27. De-emphasis**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 1 | R/W | 0 | DEMP | 0: no de-emphasis<br>1: enable de-emphasis on all channels |

#### DSP bypass

**Table 28. DSP bypass**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 2 | R/W | 0 | DSPB | 0: normal operation<br>1: bypass of biquad and bass / treble functions |

Setting the DSPB bit bypasses the EQ function of the STA333BW.

#### Postscale link

**Table 29. Postscale link**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 3 | R/W | 0 | PSL | 0: each channel uses individual postscale value<br>1: each channel uses channel 1 postscale value |

Postscale function can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the postscale values can be linked to the value of channel 1 for ease of use and update the values faster.

### Biquad coefficient link

**Table 30. Biquad coefficient link**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 4 | R/W | 0 | BQL | 0: each channel uses coefficient values<br>1: each channel uses channel 1 coefficient values |

For ease of use, all channels can use the biquad coefficients loaded into the Channel-1 coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

### Dynamic range compression / anticlipping bit

**Table 31. Dynamic range compression / anticlipping bit**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 5 | R/W | 0 | DRC | 0: limiters act in anticlipping mode<br>1: limiters act in dynamic range compression mode |

Both limiters can be used in one of two ways, anticlipping or dynamic range compression. When used in anticlipping mode the limiter threshold values are constant and dependent on the limiter settings. In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

### Zero-detect mute enable

**Table 32. Zero-detect mute enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 6 | R/W | 1 | ZDE | 0: automatic zero-detect mute disabled<br>1: automatic zero-detect mute enabled |

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the data for each processing channel at the output of the crossover (bass management) filter. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

### Submix mode enable

**Table 33. Submix mode enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 7 | R/W | 0 | SME | 0: submix into left / right disabled<br>1: submix into left / right enabled |

### 6.1.5 Configuration register E (addr 0x04)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SVE | ZCE | DCCV | PWMS | AME | NSBW | MPC | MPCV |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

#### Max power correction variable

**Table 34. Max power correction variable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 0 | MPCV | 0: use standard MPC coefficient<br>1: use MPCC bits for MPC coefficient |

#### Max power correction

**Table 35. Max power correction**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 1 | R/W | 1 | MPC | 0: function disabled<br>1: enables power bridge correction for THD reduction near maximum power output. |

Setting the MPC bit turns on special processing that corrects the STA333BW power device at high power. This mode should lower the THD+N of a full FFX system at maximum power output and slightly below. If enabled, MPC is operational in all output modes except tapered (OM[1,0] = 01) and binary. When OCFG = 00, MPC has no effect on channels 3 and 4, the line-out channels.

#### Noise-shaper bandwidth selection

**Table 36. Noise-shaper bandwidth selection**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 2 | R/W | 0 | NSBW | 1: third-order NS<br>0: fourth-order NS |

#### AM mode enable

**Table 37. AM mode enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 3 | R/W | 0 | AME | 0: normal FFX operation.<br>1: AM reduction mode FFX operation |

STA333BW features a FFX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an AM tuner active. The SNR of the FFX processing is reduced to approximately 83 dB in this mode, which is still greater than the SNR of AM radio.

### PWM speed mode

**Table 38. PWM speed mode**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 4 | R/W | 0 | PWMS | 0: normal speed (384 kHz) all channels<br>1: odd speed (341.3 kHz) all channels |

### Distortion compensation variable enable

**Table 39. Distortion compensation variable enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 5 | R/W | 0 | DCCV | 0: use preset DC coefficient<br>1: use DCC coefficient |

### Zero-crossing volume enable

**Table 40. Zero-crossing volume enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 6 | R/W | 1 | ZCE | 1: volume adjustments only occur at digital zero-crossings<br>0: volume adjustments occur immediately |

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks are audible.

### Soft volume update enable

**Table 41. Soft volume update enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 7 | R/W | 1 | SVE | 1: volume adjustments ramp according to SVUP / SVDW settings<br>0: volume adjustments occur immediately |

## 6.1.6 Configuration register F (addr 0x05)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| EAPD | PWDN | ECLE | LDTE | BCLE | IDE | OCFG1 | OCFG0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |

## Output configuration

**Table 42. Output configuration**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 0 | OCFG0 | Selects the output configuration |
| 1 | R/W | 0 | OCFG1 | |

**Table 43. Output configuration engine selection**

| OCFG[1:0] | Output configuration | Config pin |
|---|---|---|
| 00 | 2 channel (full-bridge) power, 2 channel data-out:<br>1A/1B → 1A/1B<br>2A/2B → 2A/2B<br>LineOut1 → 3A/3B<br>LineOut2 → 4A/4B<br>Line Out Configuration determined by LOC register | 0 |
| 01 | 2 (half-bridge), 1(full-bridge) on-board power:<br>1A → 1A Binary 0 °<br>2A → 1B Binary 90°<br>3A/3B → 2A/2B Binary 45°<br>1A/B → 3A/B Binary 0°<br>2A/B → 4A/B Binary 90° | 0 |
| 10 | 2 channel (full-bridge) power, 1 channel FFX:<br>1A/1B → 1A/1B<br>2A/2B → 2A/2B<br>3A/3B → 3A/3B<br>EAPDEXT and TWARNEXT Active | 0 |
| 11 | 1 channel mono-parallel:<br>3A → 1A/1B w/ C3BO 45°<br>3B → 2A/2B w/ C3BO 45°<br>1A/1B → 3A/3B<br>2A/2B → 4A/4B | 1 |

*Note: To the left of the arrow is the processing channel. When using channel output mapping, any of the three processing channel outputs can be used for any of the three inputs.*

**Figure 10. OCFG = 00 (default value)**

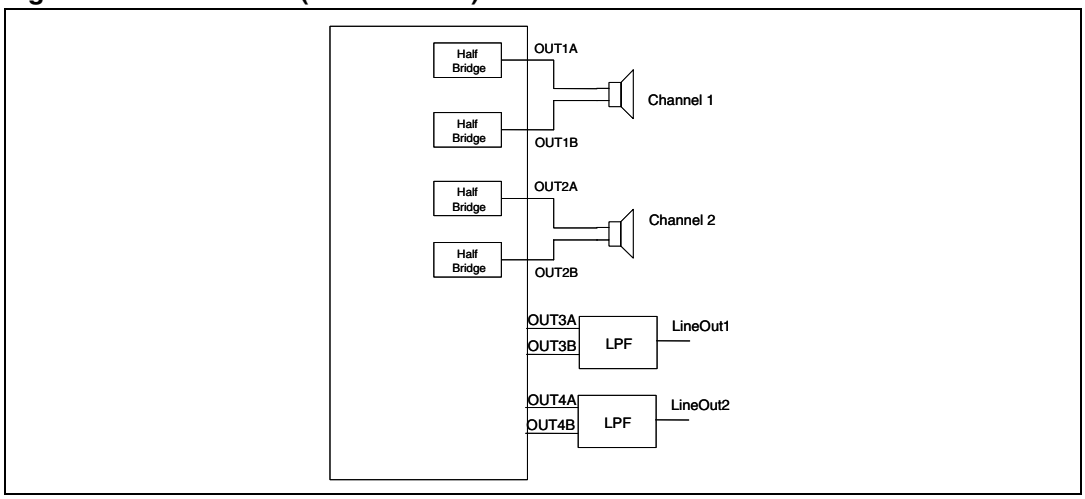



**Figure 11. OCFG = 01**

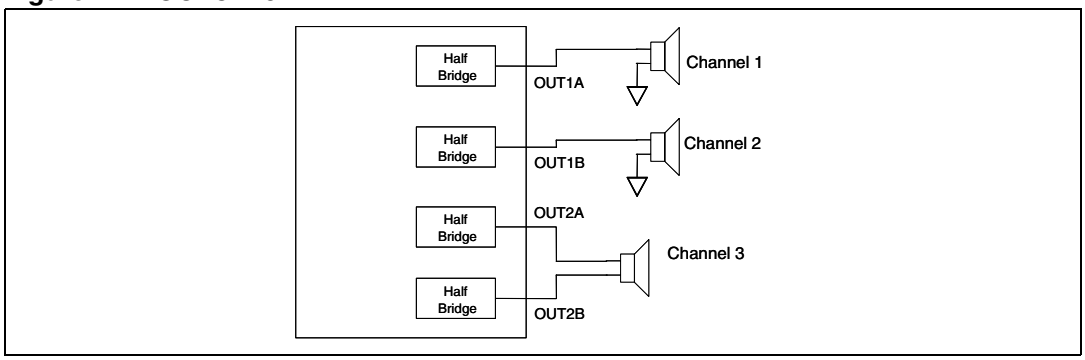



**Figure 12. OCFG = 10**

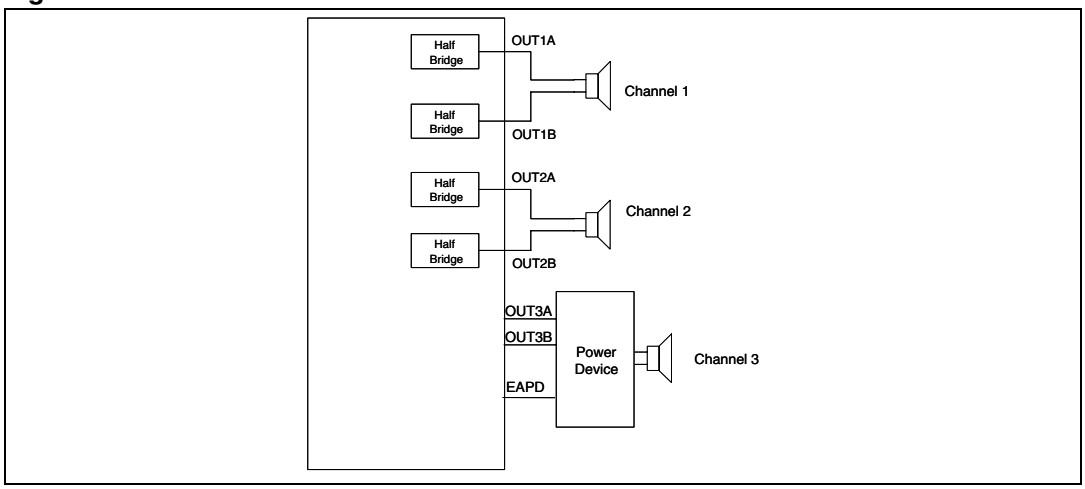
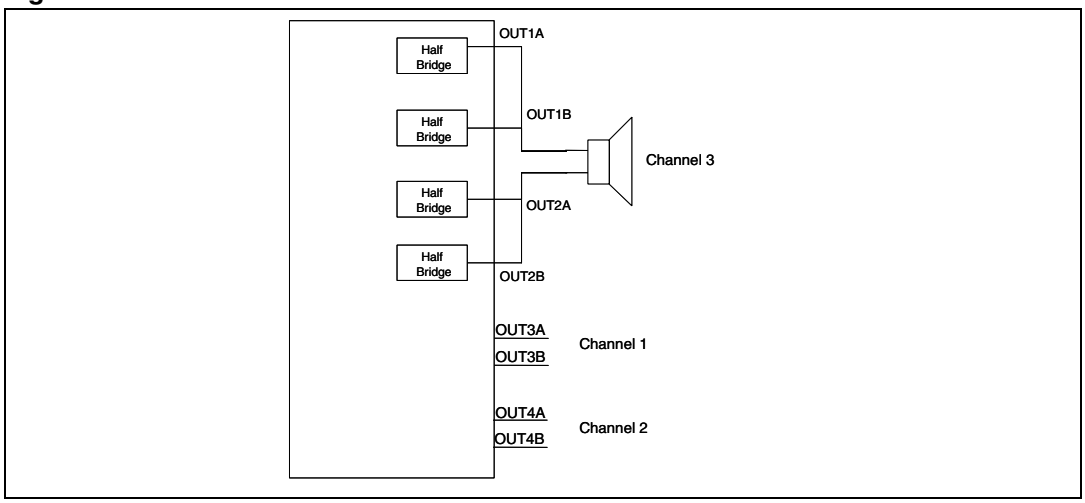
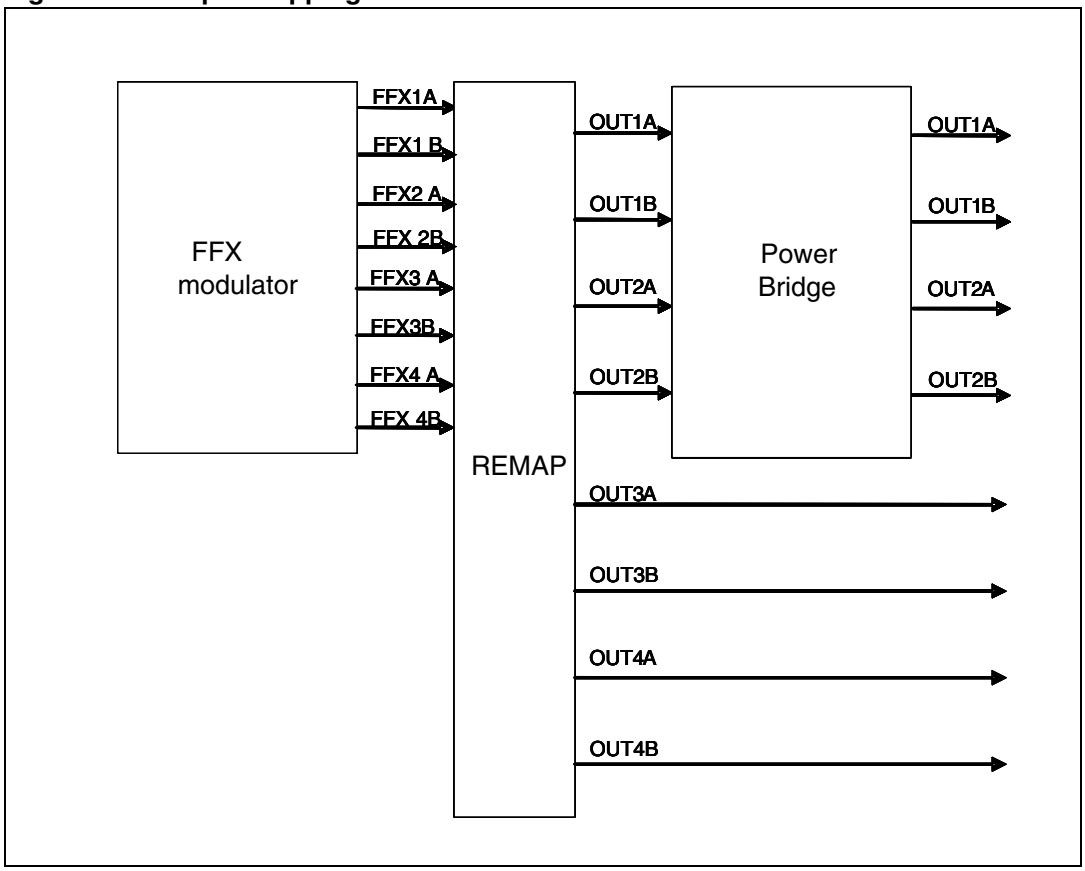


**Figure 13. OCFG = 11**




The STA333BW can be configured to support different output configurations. For each PWM output channel a PWM slot is defined. A PWM slot is always 1 / (8 * fs) seconds length. The PWM slot define the maximum extension for PWM rise and fall edge, that is, rising edge as far as the falling edge cannot range outside PWM slot boundaries.

**Figure 14. Output mapping scheme**




For each configuration the PWM signals from the digital driver are mapped in different ways to the power stage:

### 2.0 channels, two full-bridges (OCFG = 00)

Mapping:

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- FFX4A -> OUT4A
- FFX4B -> OUT4B

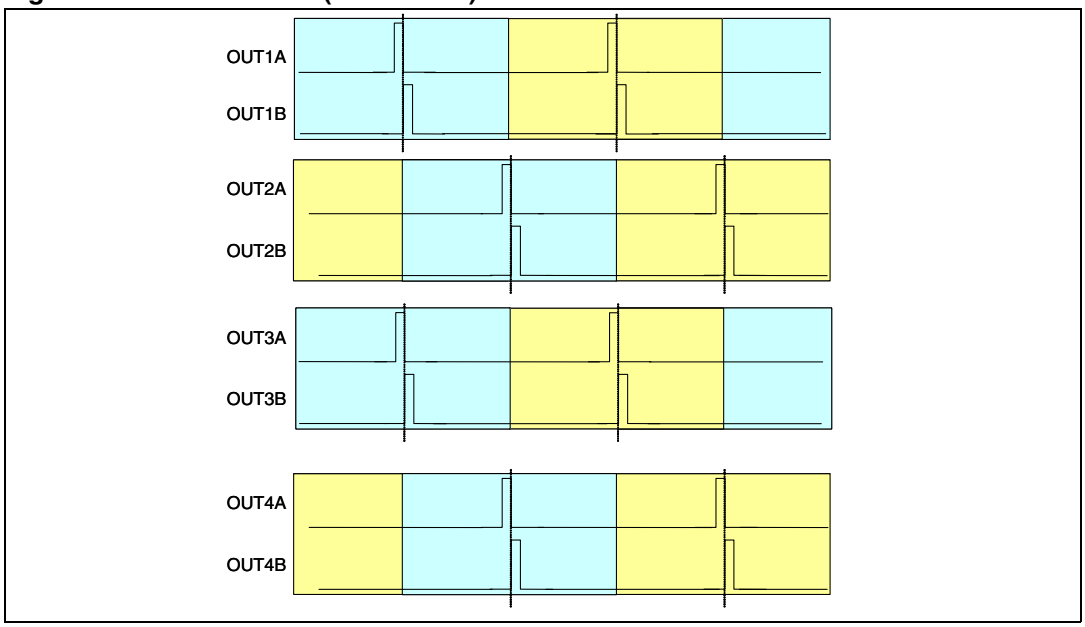
Default modulation:

- FFX1A / 1B configured as ternary
- FFX2A / 2B configured as ternary
- FFX3A / 3B configured as lineout ternary
- FFX4A / 4B configured as lineout ternary

On channel 3 line out (LOC bits = 00) the same data as channel 1 processing is sent. On channel 4 line out (LOC bits = 00) the same data as channel 2 processing is sent. In this configuration, volume control or EQ have no effect on channels 3 and 4.

In this configuration the PWM slot phase is the following as shown in *Figure 15*.

**Figure 15. 2.0 channels (OCFG = 00) PWM slots**



### 2.1 channels, two half-bridges + one full-bridge (OCFG = 01)

Mapping:

- FFX1A -> OUT1A
- FFX2A -> OUT1B
- FFX3A -> OUT2A
- FFX3B -> OUT2B
- FFX1A -> OUT3A
- FFX1B -> OUT3B
- FFX2A -> OUT4A
- FFX2B -> OUT4B

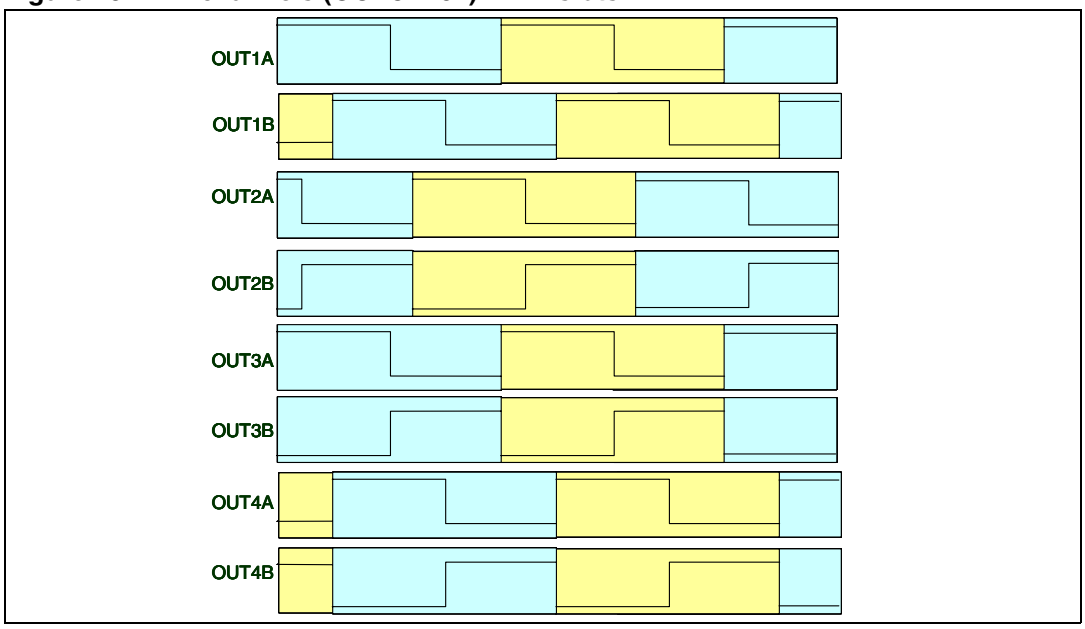
Modulation:

- FFX1A / 1B configured as binary
- FFX2A / 2B configured as binary
- FFX3A / 3B configured as binary
- FFX4A / 4B configured as binary

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT3 / OUT4 channels the channel 1 and channel 2 PWM are replicated.

In this configuration the PWM slot phase is the following as shown in *Figure 16*.

**Figure 16. 2.1 channels (OCFG = 01) PWM slots**



### 2.1 channels, two full-bridges + one external full-bridge (OCFG = 10)

Mapping:

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- EAPD -> OUT4A
- TWARN -> OUT4B

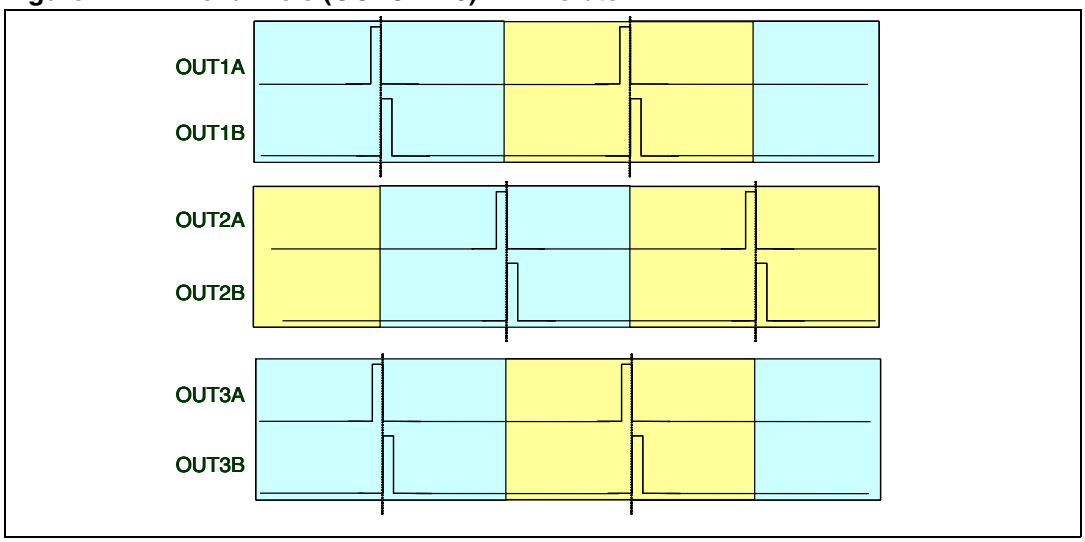
Default modulation:

- FFX1A / 1B configured as ternary
- FFX2A / 2B configured as ternary
- FFX3A / 3B configured as ternary
- FFX4A / 4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT4 channel the external bridge control signals are muxed.

In this configuration the PWM slot phase is the following as shown in *Figure 17*.

**Figure 17. 2.1 channels (OCFG = 10) PWM slots**



### Invalid input detect mute enable

**Table 44. Invalid input detect mute enable**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 2 | R/W | 1 | IDE | 0: disables the automatic invalid input detect mute<br>1: enables the automatic invalid input detect mute |

Setting the IDE bit enables this function, which looks at the input $I^2S$ data and automatically mutes if the signals are perceived as invalid.

### Binary output mode clock loss detection

**Table 45. Binary output mode clock loss detection**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 3 | R/W | 1 | BCLE | 0: binary output mode clock loss detection disabled<br>1: binary output mode clock loss detection enable |

Detects loss of input MCLK in binary mode and will output 50% duty cycle.

### LRCK double trigger protection

**Table 46. LRCK double trigger protection**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 4 | R/W | 1 | LDTE | 0: LRCLK double trigger protection disabled<br>1: LRCLK double trigger protection enabled |

LDTE, when enabled, prevents double trigger of LRCLK on instable I2S input.

### Auto EAPD on clock loss

**Table 47. Auto EAPD on clock loss**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 5 | R/W | 0 | ECLE | 0: auto EAPD on clock loss not enabled<br>1: auto EAPD on clock loss |

When active, issues a power device power down signal (EAPD) on clock loss detection.

### IC power down

**Table 48. IC power down**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 6 | R/W | 1 | PWDN | 0: IC power down low-power condition<br>1: IC normal operation |

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output begins a soft-mute. After the mute condition is reached, EAPD is asserted to power down the power-stage, then the master clock to all internal hardware expect the $I^2C$ block is gated. This places the IC in a very low power consumption state.

### External amplifier power down

**Table 49. External amplifier power down**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 7 | R/W | 0 | EAPD | 0: external power stage power down active<br>1: normal operation |

The EAPD register directly disables / enables the internal power circuitry.

When EAPD = 0, the internal power section is placed in a low-power state (disabled). This register also controls the FFX4B / EAPD output pin when OCFG = 10.

## 6.2 Volume control registers (addr 0x06 - 0x0A)

The volume structure of the STA333BW consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to -80 dB.

As an example if C3VOL = 0x00 or +48 dB and MVOL = 0x18 or -12 dB, then the total gain for channel 3 = +36 dB.

The channel mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (approximately 96 kHz).

A “hard (instantaneous) mute” can be obtained by programming a value of 0xFF (255) in any channel volume register. When volume offsets are provided via the master volume register any channel whose total volume is less than -80 dB is muted.

All changes in volume take place at zero-crossings when ZCE = 1 (*Configuration register E (addr 0x04)*) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates occur immediately.

### 6.2.1 Mute / line output configuration register (addr 0x06)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| LOC1 | LOC0 | Reserved | Reserved | C3M | C2M | C1M | Reserved |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 50. Line output configuration**

| LOC[1:0] | Line output configuration |
|---|---|
| 00 | Line output fixed - no volume, no EQ |
| 01 | Line output variable - channel 3 volume effects line output, no EQ |
| 10 | Line output variable with EQ - channel 3 volume effects line output |

Line output is only active when OCFG = 00. In this case LOC determines the line output configuration. The source of the line output is always the channel 1 and 2 inputs.

### 6.2.2 Master volume register (addr 0x07)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MVOL7 | MVOL6 | MVOL5 | MVOL4 | MVOL3 | MVOL2 | MVOL1 | MVOL0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 51. Master volume offset as a function of MVOL**

| MVOL[7:0] | Volume offset from channel value |
|---|---|
| 00000000 (0x00) | 0 dB |
| 00000001 (0x01) | -0.5 dB |
| 00000010 (0x02) | -1 dB |
| … | … |
| 01001100 (0x4C) | -38 dB |
| … | … |
| 11111110 (0xFE) | -127.5 dB |
| 11111111 (0xFF) | Default mute, not to be used during operation |

### 6.2.3 Channel 1 volume (addr 0x08)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1VOL7 | C1VOL6 | C1VOL5 | C1VOL4 | C1VOL3 | C1VOL2 | C1VOL1 | C1VOL0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

### 6.2.4 Channel 2 volume (addr 0x09)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C2VOL7 | C2VOL6 | C2VOL5 | C2VOL4 | C2VOL3 | C2VOL2 | C2VOL1 | C2VOL0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

### 6.2.5 Channel 3 / line output volume (addr 0x0A)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C3VOL7 | C3VOL6 | C3VOL5 | C3VOL4 | C3VOL3 | C3VOL2 | C3VOL1 | C3VOL0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**Table 52. Channel volume as a function of CxVOL**

| CxVOL[7:0] | Volume |
|---|---|
| 00000000 (0x00) | +48 dB |
| 00000001 (0x01) | +47.5 dB |
| 00000010 (0x02) | +47 dB |
| … | … |
| 01011111 (0x5F) | +0.5 dB |
| 01100000 (0x60) | 0 dB |
| 01100001 (0x61) | -0.5 dB |
| … | … |
| 11010111 (0xD7) | -59.5 dB |
| 11011000 (0xD8) | -60 dB |
| 11011001 (0xD9) | -61 dB |
| 11011010 (0xDA) | -62 dB |
| … | … |
| 11101100 (0xEC) | -80 dB |
| 11101101 (0xED) | Hard channel mute |
| … | … |
| 11111111 (0xFF) | Hard channel mute |

## 6.3 Audio preset registers (addr 0x0B and 0x0C)

### 6.3.1 Audio preset register 1 (addr 0x0B)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | AMGC[1] | AMGC[0] | Reserved | Reserved | Reserved | Reserved |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Using AMGC[1:0] bits, attack and release thresholds and rates are automatically configured to properly fit application specific configurations. They are defined below in *Table 53*.

**Table 53. Audio preset gain compression / limiters selection for AMGC[3:2] = 00**

| AMGC[1:0] | Mode |
|---|---|
| 00 | User programmable GC |
| 01 | AC no clipping 2.1 |
| 10 | AC limited clipping (10%) 2.1 |
| 11 | DRC night-time listening mode 2.1 |

### 6.3.2 Audio preset register 2 (addr 0x0C)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| XO3 | XO2 | XO1 | XO0 | AMAM2 | AMAM1 | AMAM0 | AMAME |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

#### AM interference frequency switching

**Table 54. AM interference frequency switching bits**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 0 | R/W | 0 | AMAME | Audio preset AM enable<br>0: switching frequency determined by PWMS setting<br>1: switching frequency determined by AMAM settings |

**Table 55. Audio preset AM switching frequency selection**

| AMAM[2:0] | 48 kHz / 96 kHz input fs | 44.1 kHz / 88.2 kHz input fs |
|---|---|---|
| 000 | 0.535 MHz - 0.720 MHz | 0.535 MHz - 0.670 MHz |
| 001 | 0.721 MHz - 0.900 MHz | 0.671 MHz - 0.800 MHz |
| 010 | 0.901 MHz - 1.100 MHz | 0.801 MHz - 1.000 MHz |
| 011 | 1.101 MHz - 1.300 MHz | 1.001 MHz - 1.180 MHz |
| 100 | 1.301 MHz - 1.480 MHz | 1.181 MHz - 1.340 MHz |
| 101 | 1.481 MHz - 1.600 MHz | 1.341 MHz - 1.500 MHz |
| 110 | 1.601 MHz - 1.700 MHz | 1.501 MHz - 1.700 MHz |

## Bass management crossover

**Table 56. Bass management crossover**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 4 | R/W | 0 | XO0 | Selects the bass-management crossover frequency. A 1st-order hign-pass filter (channels 1 and 2) or a 2nd-order low-pass filter (channel 3) at the selected frequency is performed. |
| 5 | R/W | 0 | XO1 | |
| 6 | R/W | 0 | XO2 | |
| 7 | R/W | 0 | XO3 | |

**Table 57. Bass management crossover frequency**

| XO[3:0] | Crossover frequency |
|---|---|
| 0000 | User-defined (*Section 6.7.8 on page 55*) |
| 0001 | 80 Hz |
| 0010 | 100 Hz |
| 0011 | 120 Hz |
| 0100 | 140 Hz |
| 0101 | 160 Hz |
| 0110 | 180 Hz |
| 0111 | 200 Hz |
| 1000 | 220 Hz |
| 1001 | 240 Hz |
| 1010 | 260 Hz |
| 1011 | 280 Hz |
| 1100 | 300 Hz |
| 1101 | 320 Hz |
| 1110 | 340 Hz |
| 1111 | 360 Hz |

## 6.4 Channel configuration registers (addr 0x0E - 0x10)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1OM1 | C1OM0 | C1LS1 | C1LS0 | C1BO | C1VPB | C1EQBP | C1TCB |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C2OM1 | C2OM0 | C2LS1 | C2LS0 | C2BO | C2VPB | C2EQBP | C2TCB |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C3OM1 | C3OM0 | C3LS1 | C3LS0 | C3BO | C3VPB | Reserved | Reserved |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Tone control bypass

Tone control (bass / treble) can be bypassed on a per channel basis for channels 1 and 2.

**Table 58. Tone control bypass**

| CxTCB | Mode |
|---|---|
| 0 | Perform tone control on channel x - normal operation |
| 1 | Bypass tone control on channel x |

### EQ bypass

EQ control can be bypassed on a per channel basis for channels 1 and 2. If EQ control is bypassed on a given channel the prescale and all filters (high-pass, biquads, de-emphasis, bass, treble in any combination) are bypassed for that channel.

**Table 59. EQ bypass**

| CxEQBP | Mode |
|---|---|
| 0 | Perform EQ on channel x - normal operation |
| 1 | Bypass EQ on channel x |

### Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting has no effect on that channel.

**Table 60. Volume bypass register**

| CxVBP | Mode |
|---|---|
| 0 | Normal volume operations |
| 1 | Volume is by-passed |

### Binary output enable registers

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel is considered the positive output and output B is negative inverse.

**Table 61. Binary output enable registers**

| CxBO | Mode |
|---|---|
| 0 | FFX output operation |
| 1 | Binary output |

### Limiter select

Limiter selection can be made on a per-channel basis according to the channel limiter select bits.

**Table 62. Channel limiter mapping as a function of CxLS bits**

| CxLS[1:0] | Channel limiter mapping |
|---|---|
| 00 | Channel has limiting disabled |
| 01 | Channel is mapped to limiter #1 |
| 10 | Channel is mapped to limiter #2 |

### Output mapping

Output mapping can be performed on a per channel basis according to the CxOM channel output mapping bits. Each input into the output configuration engine can receive data from any of the three processing channel outputs.

**Table 63. Channel output mapping as a function of CxOM bits**

| CxOM[1:0] | Channel x output source from |
|---|---|
| 00 | Channel1 |
| 01 | Channel 2 |
| 10 | Channel 3 |

## 6.5 Tone control register (addr 0x11)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| TTC3 | TTC2 | TTC1 | TTC0 | BTC3 | BTC2 | BTC1 | BTC0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

### Tone control

**Table 64. Tone control boost / cut as a function of BTC and TTC bits**

| BTC[3:0], TTC[3:0] | Boost / Cut |
|---|---|
| 0000 | -12 dB |
| 0001 | -12 dB |
| 0010 | -10 dB |
| … | … |
| 0101 | -4 dB |
| 0110 | -2 dB |
| 0111 | 0 dB |
| 1000 | +2 dB |
| 1001 | +4 dB |
| … | … |
| 1100 | +10 dB |
| 1101 | +12 dB |
| 1110 | +12 dB |
| 1111 | +12 dB |

## 6.6 Dynamic control registers (addr 0x12 - 0x15)

### 6.6.1 Limiter 1 attack / release rate (addr 0x12)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| L1A3 | L1A2 | L1A1 | L1A0 | L1R3 | L1R2 | L1R1 | L1R0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

### 6.6.2 Limiter 1 attack / release threshold (addr 0x13)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| L1AT3 | L1AT2 | L1AT1 | L1AT0 | L1RT3 | L1RT2 | L1RT1 | L1RT0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

### 6.6.3 Limiter 2 attack / release rate (addr 0x14)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| L2A3 | L2A2 | L2A1 | L2A0 | L2R3 | L2R2 | L2R1 | L2R0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

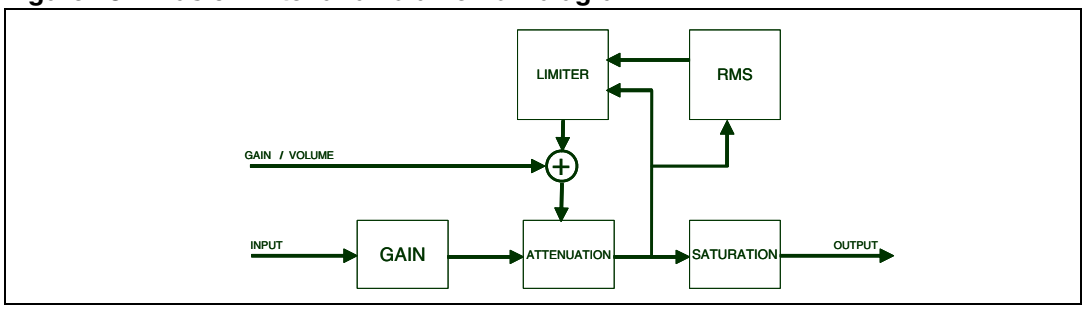
### 6.6.4 Limiter 2 attack / release threshold (addr 0x15)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| L2AT3 | L2AT2 | L2AT1 | L2AT0 | L2RT3 | L2RT2 | L2RT1 | L2RT0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

### 6.6.5 Description

The STA333BW includes two independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anticlipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in *Configuration register E (addr 0x04) on page 31*. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when 0 dBFS is exceeded. Each limiter looks at the present value of each channel that is mapped to it, selects the maximum absolute value of all these channels, performs the limiting algorithm on that value, and then if needed adjusts the gain of the mapped channels in unison.

**Figure 18. Basic limiter and volume flow diagram**




The limiter attack thresholds are determined by the LxAT registers.

It is recommended in anticlipping mode to set this to 0 dBfs, which corresponds to the maximum unclipped output power of a FFX amplifier. Since gain can be added digitally within the STA333BW it is possible to exceed 0 dBfs or any other LxAT setting, when this occurs, the limiter, when active, automatically starts reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. Gain reduction occurs on a peak-detect algorithm.

The limiter release thresholds are determined by the LxRT registers.

The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume / limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the Release Rate register. The gain can never be increased past its set value and, therefore, the release only occurs if the limiter has already

reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over limiting can reduce the dynamic range to virtually zero and cause program material to sound “lifeless”.

In AC mode, the attack and release thresholds are set relative to full-scale. In DRC mode, the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

**Table 65. Limiter attack rate vs LxA bits**

| LxA[3:0] | Attack Rate dB/ms | |
|---|---|---|
| 0000 | 3.1584 | Fast ↓ Slow |
| 0001 | 2.7072 | |
| 0010 | 2.2560 | |
| 0011 | 1.8048 | |
| 0100 | 1.3536 | |
| 0101 | 0.9024 | |
| 0110 | 0.4512 | |
| 0111 | 0.2256 | |
| 1000 | 0.1504 | |
| 1001 | 0.1123 | |
| 1010 | 0.0902 | |
| 1011 | 0.0752 | |
| 1100 | 0.0645 | |
| 1101 | 0.0564 | |
| 1110 | 0.0501 | |
| 1111 | 0.0451 | |

Table 66. Limiter release rate vs LxR bits

| LxR[3:0] | Release Rate dB/ms | |
|---|---|---|
| 0000 | 0.5116 | Fast |
| 0001 | 0.1370 | |
| 0010 | 0.0744 | |
| 0011 | 0.0499 | |
| 0100 | 0.0360 | |
| 0101 | 0.0299 | |
| 0110 | 0.0264 | |
| 0111 | 0.0208 | |
| 1000 | 0.0198 | |
| 1001 | 0.0172 | |
| 1010 | 0.0147 | |
| 1011 | 0.0137 | |
| 1100 | 0.0134 | |
| 1101 | 0.0117 | |
| 1110 | 0.0110 | |
| 1111 | 0.0104 | Slow |

## Anticlipping mode

Table 67. Limiter attack threshold vs LxAT bits (AC mode)

| LxAT[3:0] | AC (dB relative to fs) |
|---|---|
| 0000 | -12 |
| 0001 | -10 |
| 0010 | -8 |
| 0011 | -6 |
| 0100 | -4 |
| 0101 | -2 |
| 0110 | 0 |
| 0111 | +2 |
| 1000 | +3 |
| 1001 | +4 |
| 1010 | +5 |
| 1011 | +6 |
| 1100 | +7 |
| 1101 | +8 |

Table 67. Limiter attack threshold vs LxAT bits (AC mode) (continued)

| LxAT[3:0] | AC (dB relative to fs) |
|---|---|
| 1110 | +9 |
| 1111 | +10 |

Table 68. Limiter release threshold vs LxRT bits (AC mode)

| LxRT[3:0] | AC (dB relative to fs) |
|---|---|
| 0000 | -∞ |
| 0001 | -29 |
| 0010 | -20 |
| 0011 | -16 |
| 0100 | -14 |
| 0101 | -12 |
| 0110 | -10 |
| 0111 | -8 |
| 1000 | -7 |
| 1001 | -6 |
| 1010 | -5 |
| 1011 | -4 |
| 1100 | -3 |
| 1101 | -2 |
| 1110 | -1 |
| 1111 | -0 |

### Dynamic range compression mode

Table 69. Limiter attack threshold vs LxAT bits (DRC mode)

| LxAT[3:0] | DRC (dB relative to Volume) |
|---|---|
| 0000 | -31 |
| 0001 | -29 |
| 0010 | -27 |
| 0011 | -25 |
| 0100 | -23 |
| 0101 | -21 |
| 0110 | -19 |
| 0111 | -17 |
| 1000 | -16 |

Table 69. Limiter attack threshold vs LxAT bits (DRC mode) (continued)

| LxAT[3:0] | DRC (dB relative to Volume) |
|---|---|
| 1001 | -15 |
| 1010 | -14 |
| 1011 | -13 |
| 1100 | -12 |
| 1101 | -10 |
| 1110 | -7 |
| 1111 | -4 |

Table 70. Limiter release threshold vs LxRT bits (DRC mode)

| LxRT[3:0] | DRC (db relative to Volume + LxAT) |
|---|---|
| 0000 | -∞ |
| 0001 | -38 |
| 0010 | -36 |
| 0011 | -33 |
| 0100 | -31 |
| 0101 | -30 |
| 0110 | -28 |
| 0111 | -26 |
| 1000 | -24 |
| 1001 | -22 |
| 1010 | -20 |
| 1011 | -18 |
| 1100 | -15 |
| 1101 | -12 |
| 1110 | -9 |
| 1111 | -6 |

## 6.7 User-defined coefficient control registers (addr 0x16 - 0x26)

### 6.7.1 Coefficient address register (addr 0x16)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | CFA5 | CFA4 | CFA3 | CFA2 | CFA1 | CFA0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 6.7.2 Coefficient b1 data register bits (addr 0x17 - 0x19)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1B23 | C1B22 | C1B21 | C1B20 | C1B19 | C1B18 | C1B17 | C1B16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1B15 | C1B14 | C1B13 | C1B12 | C1B11 | C1B10 | C1B9 | C1B8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C1B7 | C1B6 | C1B5 | C1B4 | C1B3 | C1B2 | C1B1 | C1B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 6.7.3 Coefficient b2 data register bits (addr 0x1A - 0x1C)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C2B23 | C2B22 | C2B21 | C2B20 | C2B19 | C2B18 | C2B17 | C2B16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C2B15 | C2B14 | C2B13 | C2B12 | C2B11 | C2B10 | C2B9 | C2B8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C2B7 | C2B6 | C2B5 | C2B4 | C2B3 | C2B2 | C2B1 | C2B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 6.7.4 Coefficient a1 data register bits (addr 0x1D - 0x1F)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C3B23 | C3B22 | C3B21 | C3B20 | C3B19 | C3B18 | C3B17 | C3B16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C3B15 | C3B14 | C3B13 | C3B12 | C3B11 | C3B10 | C3B9 | C3B8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C3B7 | C3B6 | C3B5 | C3B4 | C3B3 | C3B2 | C3B1 | C3B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 6.7.5 Coefficient a2 data register bits (addr 0x20 - 0x22)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C4B23 | C4B22 | C4B21 | C4B20 | C4B19 | C4B18 | C4B17 | C4B16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C4B15 | C4B14 | C4B13 | C4B12 | C4B11 | C4B10 | C4B9 | C4B8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C4B7 | C4B6 | C4B5 | C4B4 | C4B3 | C4B2 | C4B1 | C4B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 6.7.6 Coefficient b0 data register bits (addr 0x23 - 0x25)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C5B23 | C5B22 | C5B21 | C5B20 | C5B19 | C5B18 | C5B17 | C5B16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C5B15 | C5B14 | C5B13 | C5B12 | C5B11 | C5B10 | C5B9 | C5B8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C5B7 | C5B6 | C5B5 | C5B4 | C5B3 | C5B2 | C5B1 | C5B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 6.7.7 Coefficient read / write control register (addr 0x26)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | RA | R1 | WA | W1 |
| 0 | | | | 0 | 0 | 0 | 0 |

### 6.7.8 Description

Coefficients for user-defined EQ, mixing, scaling, and bass management are handled internally in the STA333BW via RAM. Access to this RAM is available to the user via an $I^2C$ register interface. A collection of $I^2C$ registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the read / write of the coefficient(s) to/from RAM.

*Note: The read and write operation on RAM coefficients works only if LRCKI (pin 29) is switching.*

#### Reading a coefficient from RAM

1. Write 6-bits of address to $I^2C$ register 0x16.
2. Write 1 to R1 bit in $I^2C$ address 0x26.
3. Read top 8-bits of coefficient in $I^2C$ address 0x17.
4. Read middle 8-bits of coefficient in $I^2C$ address 0x18.
5. Read bottom 8-bits of coefficient in $I^2C$ address 0x19.

#### Reading a set of coefficients from RAM

1. Write 6-bits of address to $I^2C$ register 0x16.
2. Write 1 to RA bit in $I^2C$ address 0x26.
3. Read top 8-bits of coefficient in $I^2C$ address 0x17.
4. Read middle 8-bits of coefficient in $I^2C$ address 0x18.
5. Read bottom 8-bits of coefficient in $I^2C$ address 0x19.
6. Read top 8-bits of coefficient b2 in $I^2C$ address 0x1A.
7. Read middle 8-bits of coefficient b2 in $I^2C$ address 0x1B.
8. Read bottom 8-bits of coefficient b2 in $I^2C$ address 0x1C.
9. Read top 8-bits of coefficient a1 in $I^2C$ address 0x1D.
10. Read middle 8-bits of coefficient a1 in $I^2C$ address 0x1E.
11. Read bottom 8-bits of coefficient a1 in $I^2C$ address 0x1F.
12. Read top 8-bits of coefficient a2 in $I^2C$ address 0x20.
13. Read middle 8-bits of coefficient a2 in $I^2C$ address 0x21.
14. Read bottom 8-bits of coefficient a2 in $I^2C$ address 0x22.
15. Read top 8-bits of coefficient b0 in $I^2C$ address 0x23.
16. Read middle 8-bits of coefficient b0 in $I^2C$ address 0x24.
17. Read bottom 8-bits of coefficient b0 in $I^2C$ address 0x25.

#### Writing a single coefficient to RAM

1. Write 6-bits of address to $I^2C$ register 0x16.
2. Write top 8-bits of coefficient in $I^2C$ address 0x17.
3. Write middle 8-bits of coefficient in $I^2C$ address 0x18.
4. Write bottom 8-bits of coefficient in $I^2C$ address 0x19.
5. Write 1 to W1 bit in $I^2C$ address 0x26.

### Writing a set of coefficients to RAM

1. Write 6-bits of starting address to I²C register 0x16.
2. Write top 8-bits of coefficient b1 in I²C address 0x17.
3. Write middle 8-bits of coefficient b1 in I²C address 0x18.
4. Write bottom 8-bits of coefficient b1 in I²C address 0x19.
5. Write top 8-bits of coefficient b2 in I²C address 0x1A.
6. Write middle 8-bits of coefficient b2 in I²C address 0x1B.
7. Write bottom 8-bits of coefficient b2 in I²C address 0x1C.
8. Write top 8-bits of coefficient a1 in I²C address 0x1D.
9. Write middle 8-bits of coefficient a1 in I²C address 0x1E.
10. Write bottom 8-bits of coefficient a1 in I²C address 0x1F.
11. Write top 8-bits of coefficient a2 in I²C address 0x20.
12. Write middle 8-bits of coefficient a2 in I²C address 0x21.
13. Write bottom 8-bits of coefficient a2 in I²C address 0x22.
14. Write top 8-bits of coefficient b0 in I²C address 0x23.
15. Write middle 8-bits of coefficient b0 in I²C address 0x24.
16. Write bottom 8-bits of coefficient b0 in I²C address 0x25.
17. Write 1 to WA bit in I²C address 0x26.

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects. When using this technique, the 6-bit address specifies the address of the biquad b1 coefficient (for example, 0, 5, 10, 20, 35 decimal), and the STA333BW generates the RAM addresses as offsets from this base value to write the complete set of coefficient data.

**Table 71. RAM block for biquads, mixing, scaling, bass management**

| Index (Decimal) | Index (Hex) | Description | Coefficient | Default |
|---|---|---|---|---|
| 0 | 0x00 | Channel 1 - Biquad 1 | C1H10(b1/2) | 0x000000 |
| 1 | 0x01 | | C1H11(b2) | 0x000000 |
| 2 | 0x02 | | C1H12(a1/2) | 0x000000 |
| 3 | 0x03 | | C1H13(a2) | 0x000000 |
| 4 | 0x04 | | C1H14(b0/2) | 0x400000 |
| 5 | 0x05 | Channel 1 - Biquad 2 | C1H20 | 0x000000 |
| … | … | … | … | … |
| 19 | 0x13 | Channel 1 - Biquad 4 | C1H44 | 0x400000 |
| 20 | 0x14 | Channel 2 - Biquad 1 | C2H10 | 0x000000 |
| 21 | 0x15 | | C2H11 | 0x000000 |
| … | … | … | … | … |
| 39 | 0x27 | Channel 2 - Biquad 4 | C2H44 | 0x400000 |

Table 71. RAM block for biquads, mixing, scaling, bass management (continued)

| Index (Decimal) | Index (Hex) | Description | Coefficient | Default |
|---|---|---|---|---|
| 40 | 0x28 | Channel 1 / 2 - Biquad 5 or 8 for XO = 000 High-pass 2nd order filter for XO ≠ 000 | C12H0(b1/2) | 0x000000 |
| 41 | 0x29 | | C12H1(b2) | 0x000000 |
| 42 | 0x2A | | C12H2(a1/2) | 0x000000 |
| 43 | 0x2B | | C12H3(a2) | 0x000000 |
| 44 | 0x2C | | C12H4(b0/2) | 0x400000 |
| 45 | 0x2D | Channel 3 - Biquad for XO = 000 Low-pass 2nd order filter for XO ≠ 000 | C3H0(b1/2) | 0x000000 |
| 46 | 0x2E | | C3H1(b2) | 0x000000 |
| 47 | 0x2F | | C3H2(a1/2) | 0x000000 |
| 48 | 0x30 | | C3H3(a2) | 0x000000 |
| 49 | 0x31 | | C3H4(b0/2) | 0x400000 |
| 50 | 0x32 | Channel 1 - Prescale | C1PreS | 0x7FFFFF |
| 51 | 0x33 | Channel 2 - Prescale | C2PreS | 0x7FFFFF |
| 52 | 0x34 | Channel 1 - Postscale | C1PstS | 0x7FFFFF |
| 53 | 0x35 | Channel 2 - Postscale | C2PstS | 0x7FFFFF |
| 54 | 0x36 | Channel 3 - Postscale | C3PstS | 0x7FFFFF |
| 55 | 0x37 | TWARN / OC - Limit | TWOCL | 0x5A9DF7 |
| 56 | 0x38 | Channel 1 - Mix 1 | C1MX1 | 0x7FFFFF |
| 57 | 0x39 | Channel 1 - Mix 2 | C1MX2 | 0x000000 |
| 58 | 0x3A | Channel 2 - Mix 1 | C2MX1 | 0x000000 |
| 59 | 0x3B | Channel 2 - Mix 2 | C2MX2 | 0x7FFFFF |
| 60 | 0x3C | Channel 3 - Mix 1 | C3MX1 | 0x400000 |
| 61 | 0x3D | Channel 3 - Mix 2 | C3MX2 | 0x400000 |
| 62 | 0x3E | Unused | - | - |
| 63 | 0x3F | Unused | - | - |

## User-defined EQ

The STA333BW can be programmed for four EQ filters (biquads) per each of the two input channels. The biquads use the following equation:

$$Y[n] = 2 * (b_0 / 2) * X[n] + 2 * (b_1 / 2) * X[n-1] + b_2 * X[n-2] - 2 * (a_1 / 2) * Y[n-1] - a_2 * Y[n-2]$$
$$= b_0 * X[n] + b_1 * X[n-1] + b_2 * X[n-2] - a_1 * Y[n-1] - a_2 * Y[n-2]$$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 0x800000 (-1) to 0x7FFFFF (0.9999998808).

Coefficients stored in the user defined coefficient RAM are referenced in the following manner:

CxHy0 = $b_1$ / 2

CxHy1 = $b_2$

CxHy2 = -$a_1$ / 2

CxHy3 = -$a_2$

CxHy4 = $b_0$ / 2

where x represents the channel and the y the biquad number. For example, C2H41 is the $b_2$ coefficient in the fourth biquad for channel 2.

### Crossover and biquad #8

Additionally, the STA333BW can be programmed for a high-pass filter (processing channels 1 and 2) and a low-pass filter (processing channel 3) to be used for bass-management crossover when the XO setting is 000 (user-defined). Both of these filters when defined by the user (rather than using the preset crossover filters) are second order filters that use the biquad equation given above. They are loaded into the C12H0-4 and C3Hy0-4 areas of RAM noted in *Table 71*, addresses 0x28 to 0x31.

By default, all user-defined filters are pass-through where all coefficients are set to 0, except the $b_0$ / 2 coefficient which is set to 0x400000 (representing 0.5)

### Prescale

The STA333BW provides a multiplication for each input channel for the purpose of scaling the input prior to EQ. This pre-EQ scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiply is loaded into RAM. All channels can use the channel-1 prescale factor by setting the Biquad link bit. By default, all prescale factors (RAM addresses 0x32 to 0x33) are set to 0x7FFFFF.

### Postscale

The STA333BW provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel. This postscaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiply is loaded into RAM. This postscale factor can be used in conjunction with an ADC equipped micro-controller to perform power-supply error correction. All channels can use the channel-1 postscale factor by setting the postscale link bit. By default, all postscale factors (RAM addresses 0x34 to 0x36) are set to 0x7FFFFF. When line output is being used, channel-3 postscale affects both channels 3 and 4.

### Thermal warning and overcurrent adjustment (TWOCL)

The STA333BW provides a simple mechanism for reacting to overcurrent or thermal warning detection in the power block. When the warning occurs, the TWOCL value is used to provide output attenuation clipping on all channels.

The amount of attenuation to be applied in this situation can be adjusted by modifying the overcurrent and thermal warning limiting value (RAM addr 0x37). By default, the overcurrent postscale adjustment factor is set to 0x5A9DF7 (that is, -3 dB). Once the limiting is applied, it remains until the device is reset or according to the TWRB and OCRB settings.

## 6.8 Variable max power correction registers (addr 0x27 - 0x28)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MPCC15 | MPCC14 | MPCC13 | MPCC12 | MPCC11 | MPCC10 | MPCC9 | MPCC8 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MPCC7 | MPCC6 | MPCC5 | MPCC4 | MPCC3 | MPCC2 | MPCC1 | MPCC0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

## 6.9 Distortion compensation registers (addr 0x29 - 0x2A)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| DCC15 | DCC14 | DCC13 | DCC12 | DCC11 | DCC10 | DCC9 | DCC8 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| DCC7 | DCC6 | DCC5 | DCC4 | DCC3 | DCC2 | DCC1 | DCC0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

DCC bits determine the 16 MSBs of the distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

## 6.10 Fault detect recovery constant registers (addr 0x2B - 0x2C)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FDRC15 | FDRC14 | FDRC13 | FDRC12 | FDRC11 | FDRC10 | FDRC9 | FDRC8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FDRC7 | FDRC6 | FDRC5 | FDRC4 | FDRC3 | FDRC2 | FDRC1 | FDRC0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

FDRC bits specify the 16-bit fault detect recovery time delay. When FAULT is asserted, the TRISTATE output is immediately asserted low and held low for the time period specified by this constant. A constant value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x000C gives approximately 0.1 ms.

*Note: 0x0000 is a reserved value for these registers.*

## 6.11 Device status register (addr 0x2D)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PLLUL | FAULT | UVFAULT | Reserved | OCFAULT | OCWARN | TFAULT | TWARN |

This read-only register provides fault and thermal-warning status information from the power control block. Logic value 1 for faults or warning means normal state. Logic 0 means a fault or warning detected on power bridge. The PLLUL = 1 means that the PLL is not locked.

**Table 72. Status register bits**

| Bit | R/W | RST | Name | Description |
|---|---|---|---|---|
| 7 | R | - | PLLUL | 0: PLL locked<br>1: PLL not locked |
| 6 | R | - | FAULT | 0: fault detected on power bridge<br>1: normal operation |
| 5 | R | - | UVFAULT | 0: VCCxX internally detected<br>< undervoltage threshold |
| 4 | R | - | Reserved | - |
| 3 | R | - | OCFAULT | 0: overcurrent fault detected |
| 2 | R | - | OCWARN | 0: overcurrent warning |
| 1 | R | - | TFAULT | 0: thermal fault, junction temperature over limit |
| 0 | R | - | TWARN | 0: thermal warning, junction temperature is close to the fault condition |

# 7 Applications

## 7.1 Applications schematic

*Figure 20* below shows the typical applications schematic for STA333BW. Special attention has to be paid to the layout of the PCB. All the decoupling capacitors have to be placed as close as possible to the device to limit spikes on all the supplies.

## 7.2 PLL filter circuit

It is recommended to use the above circuit and values for the PLL loop filter to achieve the best performance from the device in general applications. Note that the ground of this filter circuit has to be connected to the ground of the PLL without any resistive path. Concerning the component values, it must be taken into account that the greater the filter bandwidth, the less is the lock time but the higher is the PLL output jitter.

## 7.3 Typical output configuration

*Figure 19* shows the typical output configuration used for BTL stereo mode. Please contact STMicroelectronics for other recommended output configurations.

**Figure 19. Output configuration for stereo BTL mode ($R_L$ = 8 Ω)**

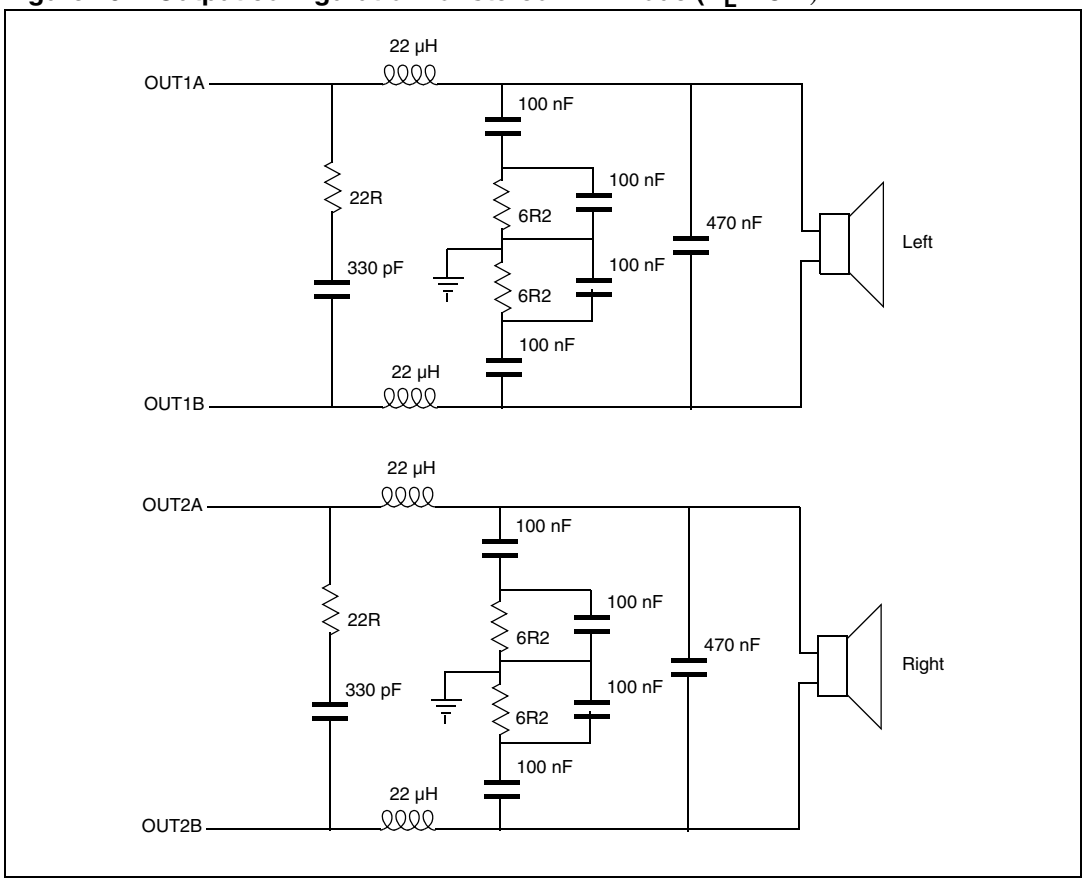
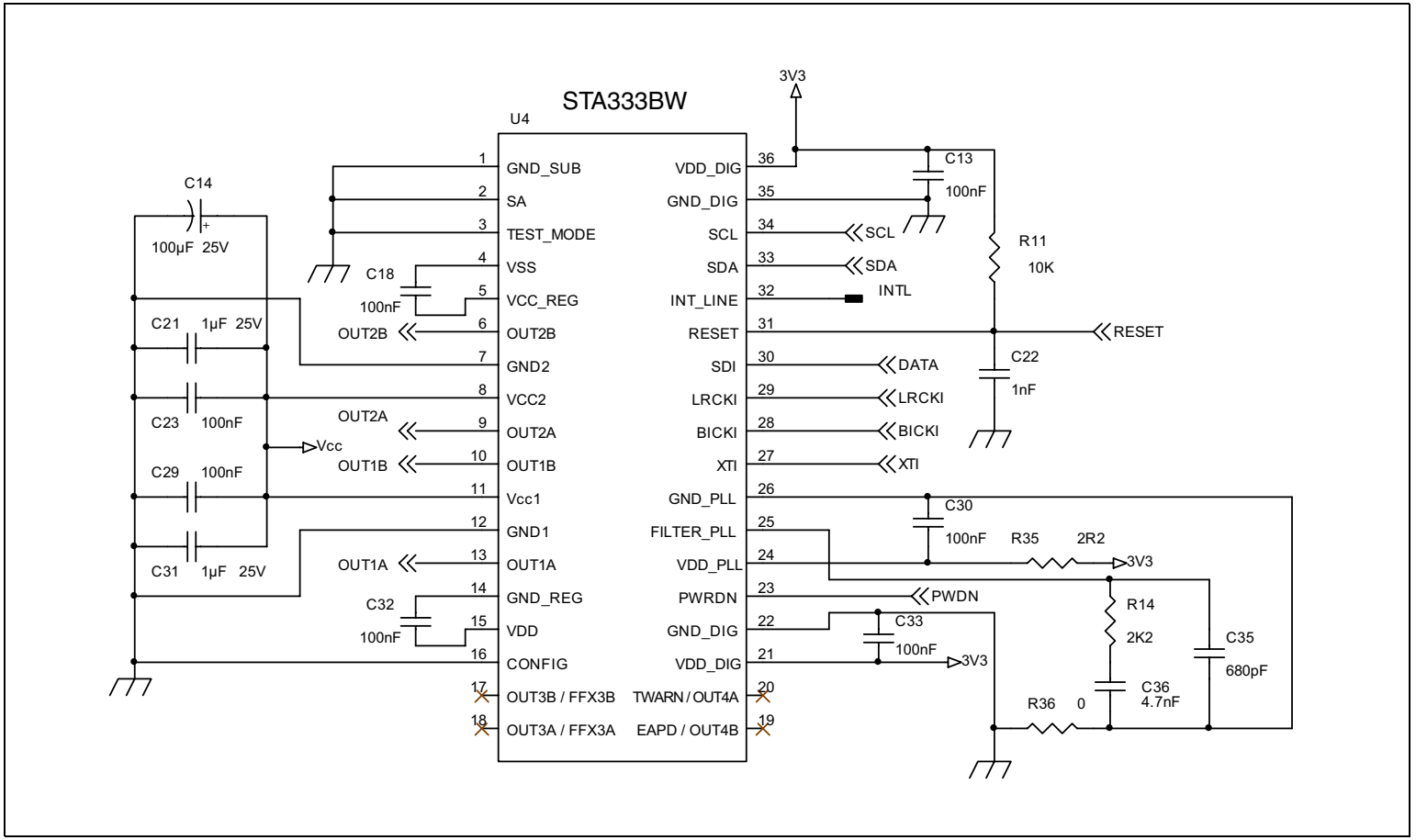


**Figure 20. Applications circuit**



# 8 Package thermal characteristics

Using a double-layer PCB the thermal resistance, junction to ambient, with 2 copper ground areas of 3 x 3 $cm^2$ and with 16 via holes is 24 °C/W in natural air convection.

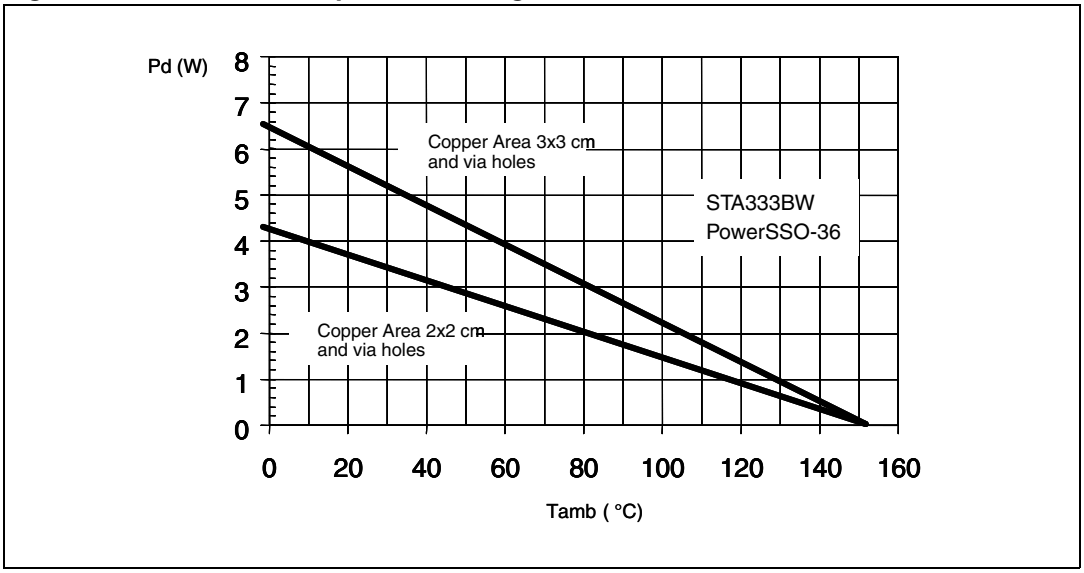
The dissipated power within the device depends primarily on the supply voltage, load impedance and output modulation level.

Thus, the maximum estimated dissipated power for the STA333BW is:

| | |
|---|---|
| 2 x 20 W @ 8 Ω, 18 V | Pd max is approximately 4 W |
| 2 x 9 W + 1 x 20 W @ 4 Ω, 8 Ω, 18 V | Pd max is approximately 5 W |

*Figure 21* shows the power derating curve for the PowerSSO-36 package on PCBs with copper areas of 2 x 2 $cm^2$ and 3 x 3 $cm^2$.

**Figure 21. PowerSSO-36 power derating curve**



# 9 Package mechanical data

*Figure 22* below shows the package outline and *Table 73* gives the dimensions.

**Table 73. PowerSSO-36 EPD dimensions**

| Symbol | Dimensions in mm | | | Dimensions in inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 2.15 | - | 2.47 | 0.085 | - | 0.097 |
| A2 | 2.15 | - | 2.40 | 0.085 | - | 0.094 |
| a1 | 0.00 | - | 0.10 | 0.00 | - | 0.004 |
| b | 0.18 | - | 0.36 | 0.007 | - | 0.014 |
| c | 0.23 | - | 0.32 | 0.009 | - | 0.013 |
| D | 10.10 | - | 10.50 | 0.398 | - | 0.413 |
| E | 7.40 | - | 7.60 | 0.291 | - | 0.299 |
| e | - | 0.5 | - | - | 0.020 | - |
| e3 | - | 8.5 | - | - | 0.335 | - |
| F | - | 2.3 | - | - | 0.091 | - |
| G | - | - | 0.10 | - | - | 0.004 |
| H | 10.10 | - | 10.50 | 0.398 | - | 0.413 |
| h | - | - | 0.40 | - | - | 0.016 |
| k | 0 | - | 8 degrees | 0 | - | 8 degrees |
| L | 0.60 | - | 1.00 | 0.024 | - | 0.039 |
| M | - | 4.30 | - | - | 0.169 | - |
| N | - | - | 10 degrees | - | - | 10 degrees |
| O | - | 1.20 | - | - | 0.047 | - |
| Q | - | 0.80 | - | - | 0.031 | - |
| S | - | 2.90 | - | - | 0.114 | - |
| T | - | 3.65 | - | - | 0.144 | - |
| U | - | 1.00 | - | - | 0.039 | - |
| X | 4.10 | - | 4.70 | 0.161 | - | 0.185 |
| Y | 6.50 | - | 7.10 | 0.256 | - | 0.280 |

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

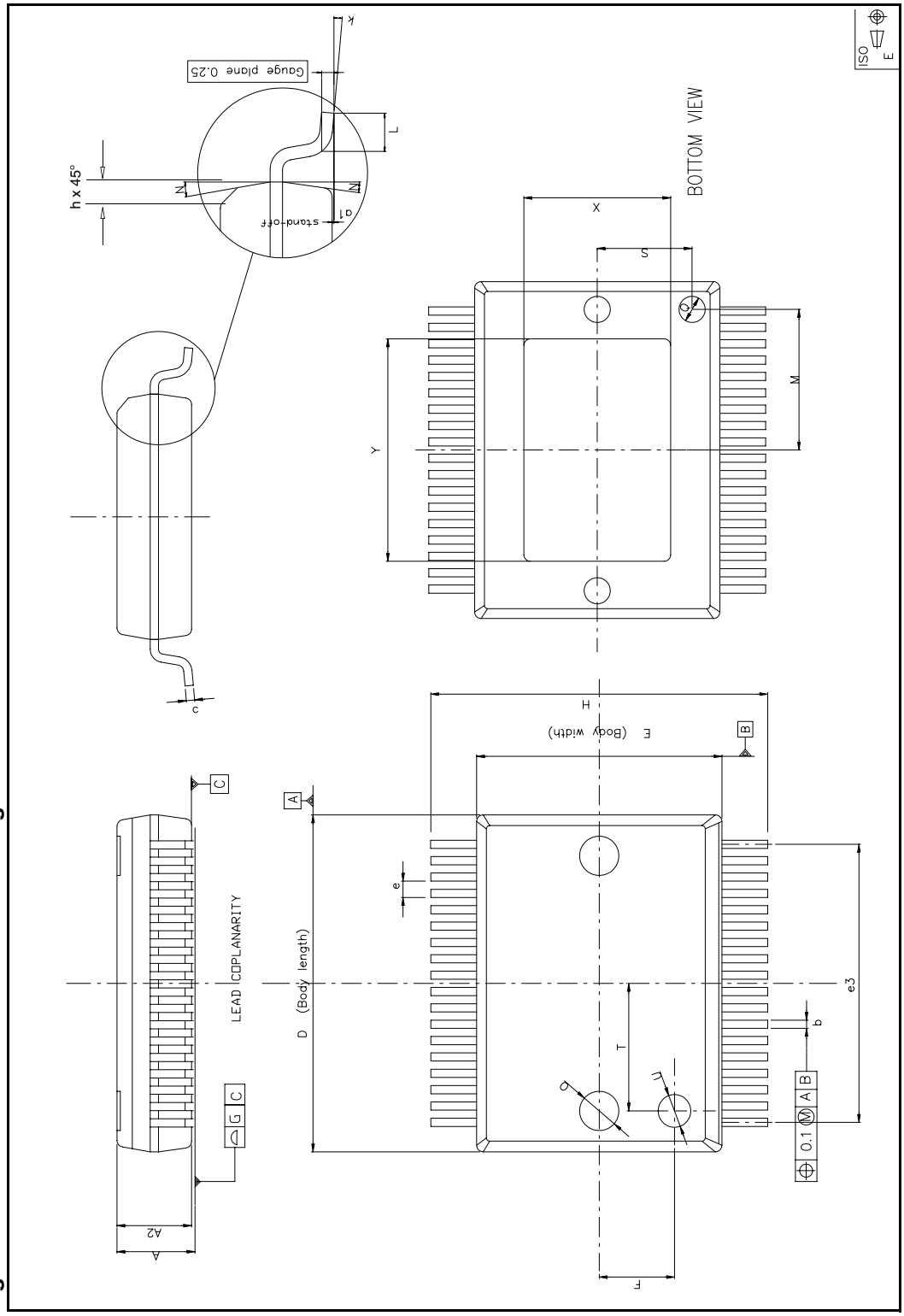



Figure 22. PowerSSO-36 EPD outline drawing

# 10 Revision history

Table 74. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 11-Apr-2006 | 1 | Initial release. |
| 26-Jul-2007 | 2 | Added:<br>Electrical specifications, digital section<br>Power on sequence<br>Processing data path<br>Application<br>Improved:<br>Pin description<br>Absolute maximum ratings<br>Recommended operative conditions<br>Output configuration<br>Device status register |
| 26-Jan-2011 | 3 | Updated presentation<br>Document status updated to Datasheet<br>Modified layout of chapter *Chapter 1: Description*<br>Removed master mute from *Section 6.2 on page 40*<br>Improved presentation of applications circuit in *Figure 20 on page 62* |

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