1.25 Gb Multimode and Single Mode Small Form Factor (SFF) Transceivers

Application Note 1184

Introduction

This document details the recommended circuit connections for Avago's duplex single mode and multimode Small Form Factor (SFF) Gigabit Ethernet transceiver products.

The HFCT-591xE is a single mode receptacled 2 x 5 pinout transceiver. The HFBR-591xE is a multimode receptacled 2 x 5 pinout transceiver. Both are designed to be compliant with the IEEE Gigabit Ethernet 1000 Base-LX requirements. Figure 15 shows the pin assignment diagram and additional pinout information is provided in Table 1.

The relevant data sheet should be read in conjunction with this document.

Product Description

Transmitter Section

The HFBR-591xE transmitter section comprises an 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) in an optical subassembly (OSA), which mates to the fiber optic cable via an MT-RJ connector. The HFCT-591xE transmitter section utilizes a 1300 nm Strained Multi-Quantum Well (SMQW) laser in the same configuration.

Both OSA's are driven by a custom IC which accepts differential PECL logic levels and provides laser biasing and modulation control functions.

Receiver Section

The HFBR-591xE receiver section includes a silicon PIN photodiode mounted together with a custom transimpedance preamplifier IC in an OSA. This OSA is mated to a custom IC that provides post-amplification. The HFCT-591xE utilizes an InP PIN photodiode in the same configuration.

The post-amplifier also includes a signal detect (SD) circuit which provides a TTL logic high output upon detection of an input optical signal.

Electrical Characteristics

Transmitter

Supply Voltage

The transceiver modules require a positive power supply in the range of 3.14 V to 3.47 V.

Supply Transients

Care should be taken to avoid supply transients. These products are not recommended for 'hot-plug' applications.

Data Inputs

The Data and /Data inputs are internally biased and 50 Ω terminated. These data inputs will accept standard PECL inputs with signal levels ranging from 300 mV to 900 mV. It is important to ensure data input lines have a 50 Ω characteristic impedance for optimum performance. Refer to the 'Board Layout' section for additional recommended board layout techniques.

Single ended operation is not recommended since data sheet specifications can only be guaranteed when both differential inputs are used. For input termination recommendations refer to the 'Termination Schemes' section.

The laser is designed to operate with a 50% duty cycle or balanced signal, for normal operation. Failure to provide this may cause the optical parameters to move out of specification. Extinction ratio and duty cycle distortion may be affected. In the absence of data the module will emit a mean optical power within the specified limit.

Optical Output

Figure 1a shows a typical HFBR-591xE transmitter output waveform using the Gbe mask and optical filter.

Figure 1b shows a typical HFCT-591xE transmitter output waveform using the Gbe mask and optical filter.

Power Supply Filtering

Good power supply filtering is required for optimum transmitter performance. The LC filtering technique illustrated in the circuit diagram of Figure 4 is recommended for the user, when using separated transmitter and receiver power supplies. When using this filter arrangement, supply noise greater than 100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, can be tolerated before the transmitter waveform is compromised. For optimum performance, the power supply filter should be located as close as possible to the supply pin of the transceiver.

Transmitter Disable

In normal operation (transmitter enabled), pin 8 should be left open circuit. The transmitter can be disabled by connecting pin 8 to VCCT via a 500 Ω resistor. This input pin requires a minimum of 50 µA for it to operate.

Receiver

Supply Voltage

The transceiver modules require a positive power supply in the range of 3.14 V to 3.47 V. Care should be taken to avoid supply transients (see receiver 'Power Supply Filtering' section).

Power Supply Filtering

Good power supply filtering is required for optimum receiver performance. The LC filtering technique illustrated in the circuit diagram of Figure 4 is recommended. When using this filter arrangement, supply noise greater than 100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, can be tolerated before a receiver sensitivity penalty of 1.0 dB occurs.

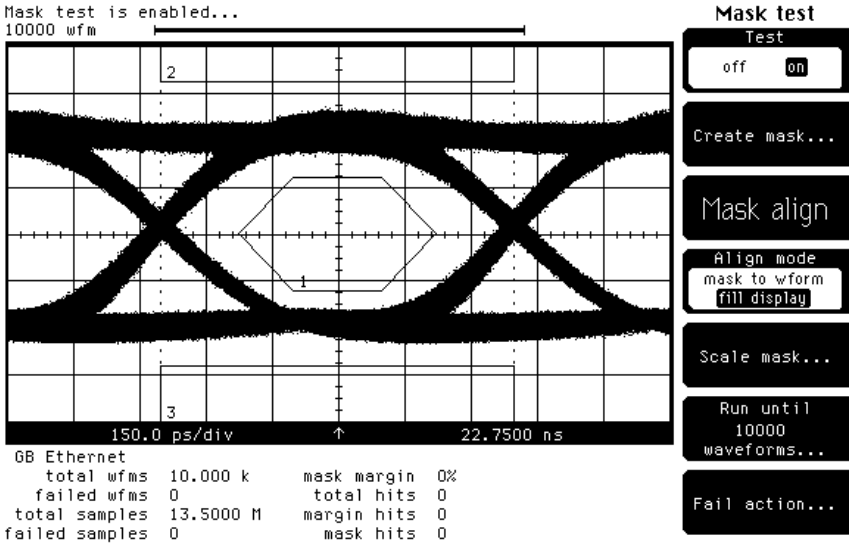


Figure 1a. Typical HFBR-591xE transmitter output showing Gbe mask at +25° C, +3.3 V

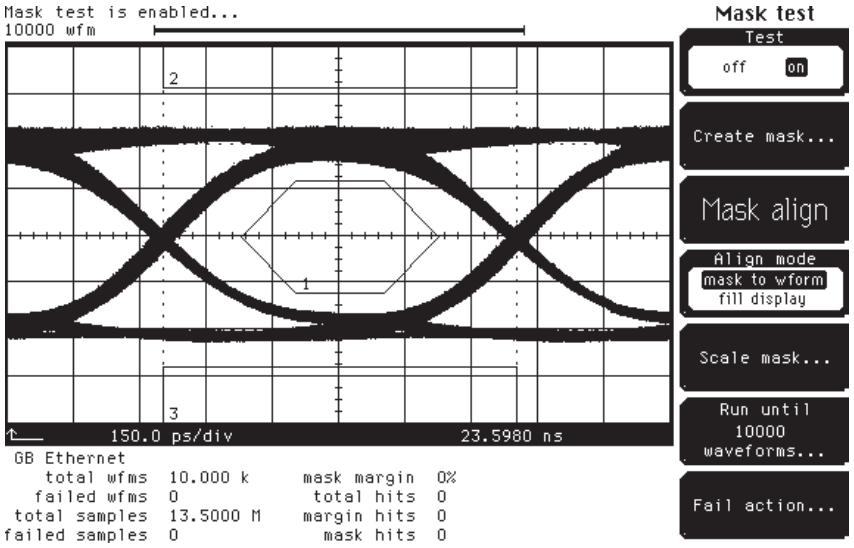


Figure 1b. Typical HFCT-591xE transmitter output showing Gbe mask at +25° C, +3.3 V

Signal Detect

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference level. The signal detect is a single ended output and is compatible with TTL and CMOS levels. No external termination is required.

Data Outputs

The receiver DATA and /DATA provide PECL output levels. These outputs are PECL compatible and are DC coupled. Both outputs should be terminated correctly. Refer to the 'Termination Schemes' section for more detail about recommended termination techniques. Under loss of light conditions the Data outputs will switch randomly.

It is recommended that the Receiver outputs be connected to 50 Ω transmission lines. Refer to the 'Board Layout' section for additional recommended PC board layout techniques.

Figure 2a shows a typical HFBR-591xE receiver data output waveform.

Figure 2b shows a typical HFCT-591xE receiver data output waveform.

Test Fixture

The Small Form Factor (SFF) transceiver test fixture, shown in Figure 3, is available for easy test and evaluation purposes.

It has a four layer FR-4 printed circuit board with ground planes on both sides. It is designed to be footprint compatible for all single and multimode Gigabit Ethernet variants.

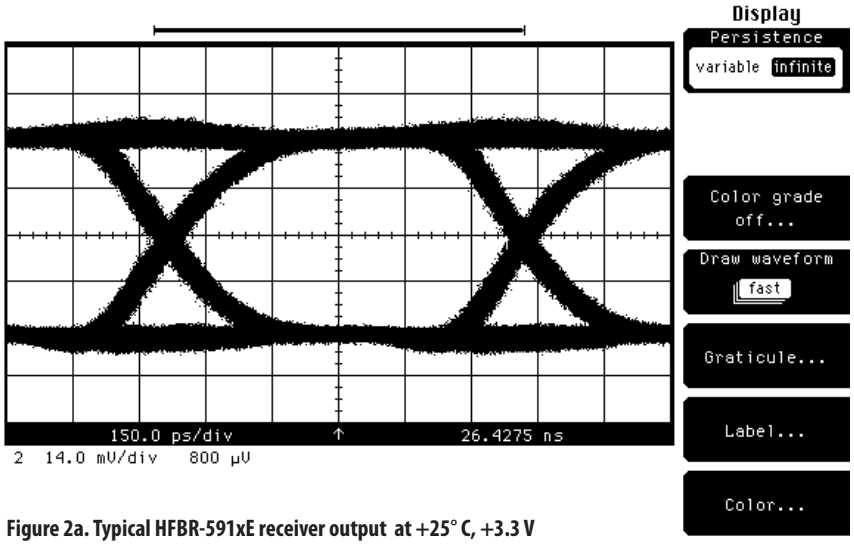


Figure 2a. Typical HFBR-591xE receiver output at +25° C, +3.3 V

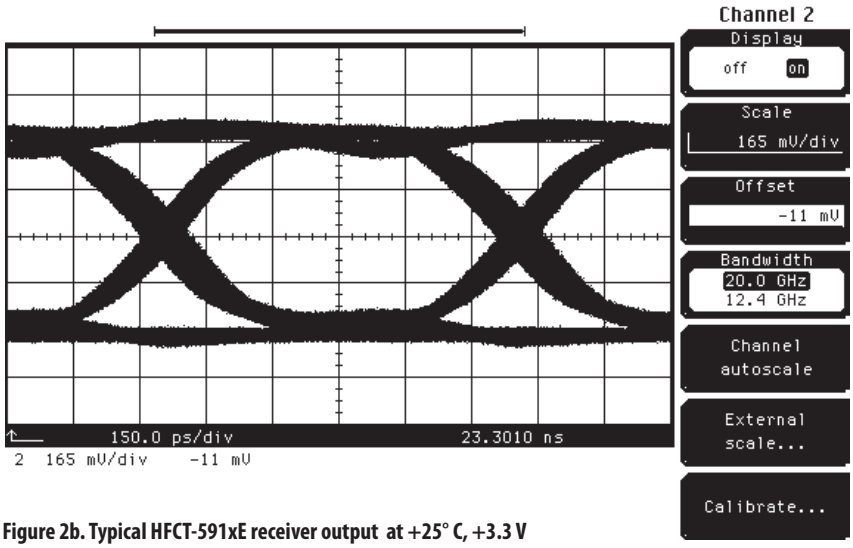


Figure 2b. Typical HFCT-591xE receiver output at +25° C, +3.3 V

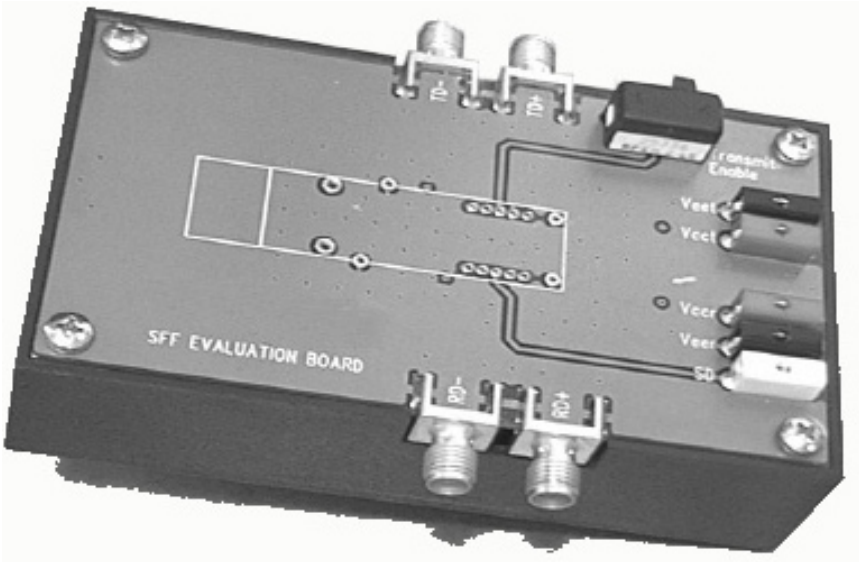


Figure 3. Test fixture

Edge-mounted SMA connectors are provided for data inputs and data outputs. Standard 2 mm sockets are included for easy connection to DC power supplies. A sliding switch is provided for selecting the transmitter disable function. Gold contact pin sockets are used to allow interchangeability between transceiver modules while assuring good connection integrity. Ground tab connection holes are provided on the test fixture for grounding the SFF transceiver body. Grounding the transceiver body is recommended for optimum performance and EMI compliance. Generous grounding is provided around the transceiver footprint using plated through holes.

Figure 4 shows the circuit schematic for the test fixture. Separate power supplies are provided to the transmitter and receiver sections, and the recommended filtering arrangements are also shown.

The signal detect (SD) function is provided for the user. No terminations are required when monitoring TTL levels.

The test fixture requires +3.3 V supply at both V_{CCT} and V_{CCR}. The transmitter enable/disable switch needs to be in position 2 for normal operation and position 1 disables optical data transmission. The test fixture is rated for repeated temperature evaluation from 0° C to +70° C.

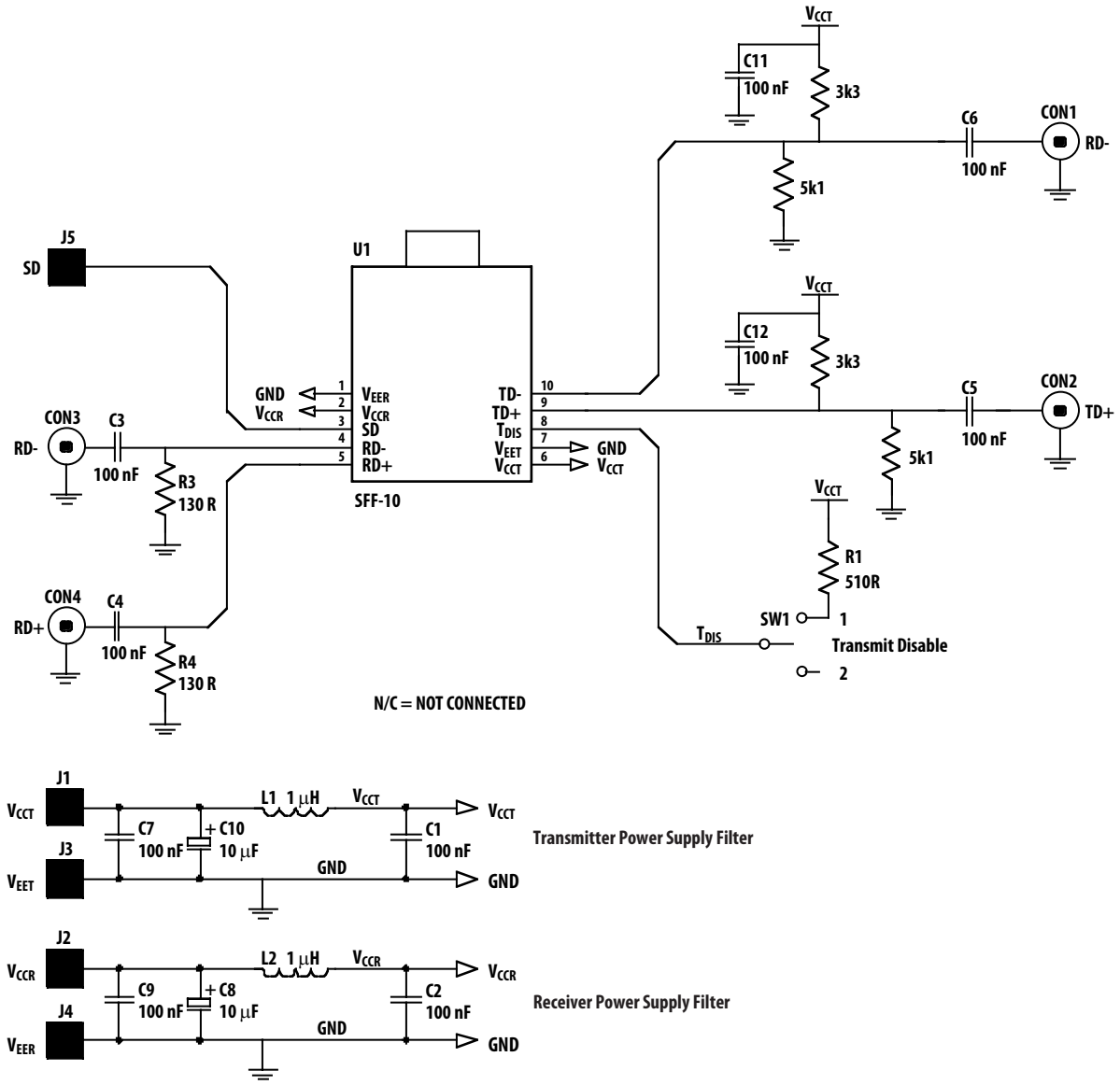
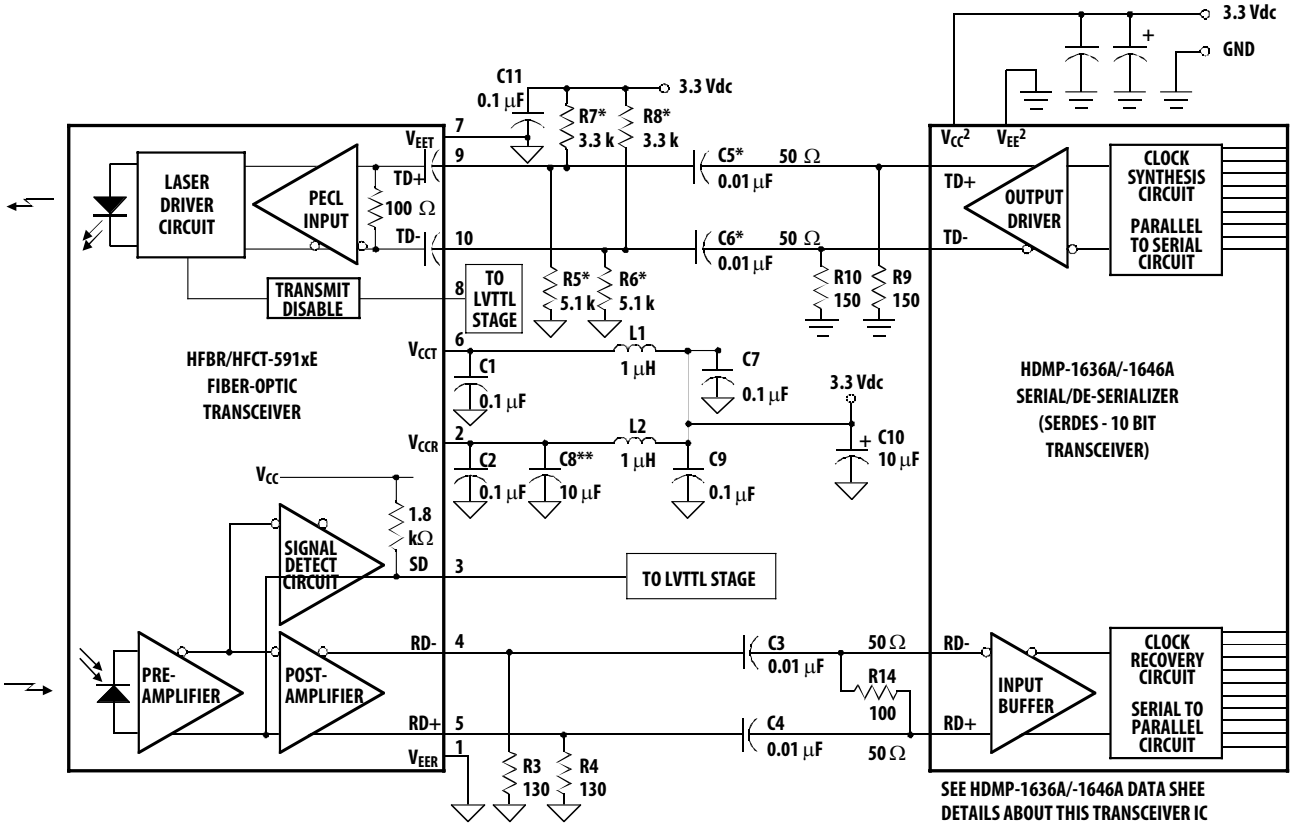


Figure 4. Test fixture circuit schematic

Interfacing/Termination Schemes

Figure 5 shows the recommended interface termination scheme for 1.25 Gb/s SFF transceivers to Avago Gigabit Ethernet SerDes ICs, the HDMP-1636A/1646A. It assumes that the 3.3 V power supply is common to both the fiber optic transmitter and receiver so that the alternative power supply filter shown in Figure 5 can be implemented.

The transmitter input stage is 50 Ω terminated so that the +3.3 kΩ/+5.1 kΩ resistors provide bias only. These termination resistors should be positioned as close as possible to the device pin.



Notes:
Use surface-mount components for optimum high-frequency performance.
Use 50 Ω microstrip or stripline for signal paths.
Locate 50 Ω terminations at the inputs of receiving units.

* In order to eliminate required external passive components, agilent has included the equivalent of resistors C5 and C6 within the module. R5 - R8, C5 and C6 are included as part of the application circuit to accommodate vendors' modules. the HFBR/HFCT-591XE will operate in both configurations.

** C8 is a recommended bypass capacitor for additional low frequency noise filtering. The signal detect output on the HFBR-591XE contains an internal 1.8 kΩ pull up resistor. The output stage on the HFCT-591XE is a PU pull configuration and therefore does not require an external pull up resistor.

Figure 5. Recommended Gigabit/sec Ethernet HFBR/HFCT-591xE Fiber Optic transceiver and HDMP-1636A/1646A SERDES integrated circuit transceiver interface and power supply filter circuits

Board Layout Considerations

The partners in the MT-RJ alliance have agreed that all SFF transceiver products will have the same physical PCB footprint and connector panel opening as documented in the Multi-Source Agreement (MSA). The MSA does not define all SFF physical parameters, such as the overall length, in order to give the partners latitude in their designs. For this reason, exactly what parameters are defined by the MSA will be emphasized in the text reviewing the Avago SFF dimensions. Note that the MSA does not require shield ground tabs on SFF products even though the MSA includes ground pads on the recommended PCB layout. The shield grounding differences in the various Avago SFF products will be discussed during the presentation of both the PCB layout and panel opening drawings. Also described are elements not controlled by the MSA such as the SFF housing material and color.

Shown in Figure 6 is the multimode 2 x 5 SFF 1.25 Gb: HFBR-5912E transceiver. The metal housing includes ground tabs that are connected to signal ground via the recommended PCB layout. The metal nose shield over the MT-RJ connector is connected to chassis ground via the spring contact fingers. The two front standoffs are un-metallized. The two rear standoffs are metallized and connected to signal ground. The metal nose shield and metal housing are electrically isolated from each other.

Shown in Figure 7 is the single mode 2 x 5 SFF 1.25 Gb/s HFCT-5912E transceiver. Similar to the HFBR-5912E, these transceivers also have ground tabs on the metal housing shield, spring contact fingers on the metal nose shield and electrical isolation between these shields. Ground tabs must be connected to signal ground for optimum performance of the transceiver. The two front standoffs are metallized and at chassis ground. The two rear standoffs are at signal ground.

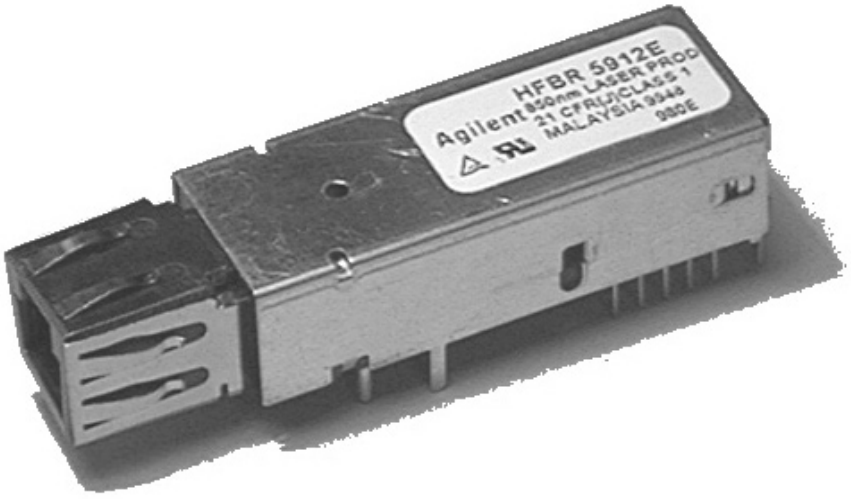


Figure 6. HFBR-5912E 2 x 5 1.25 Gb multimode SFF

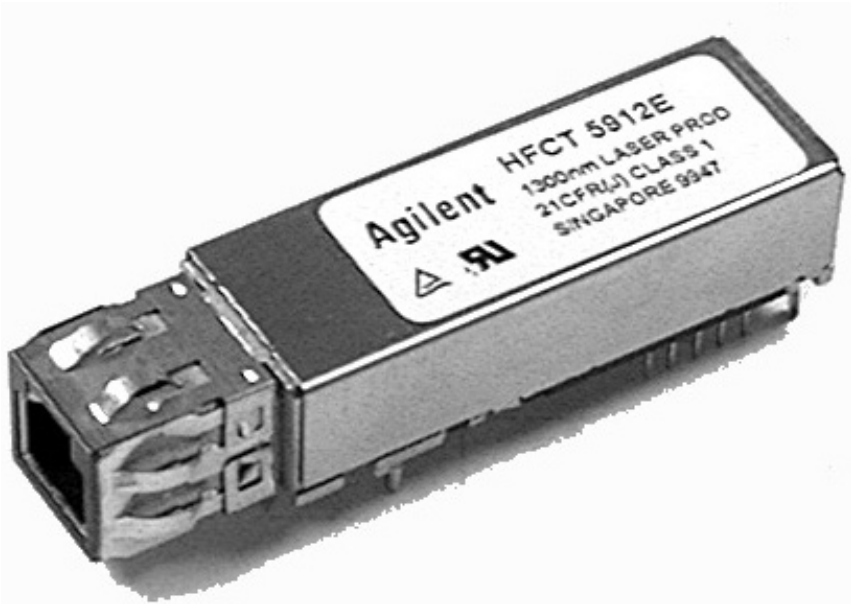


Figure 7. HFCT-5912E 2 x 5 1.25 Gb/s single mode SFF

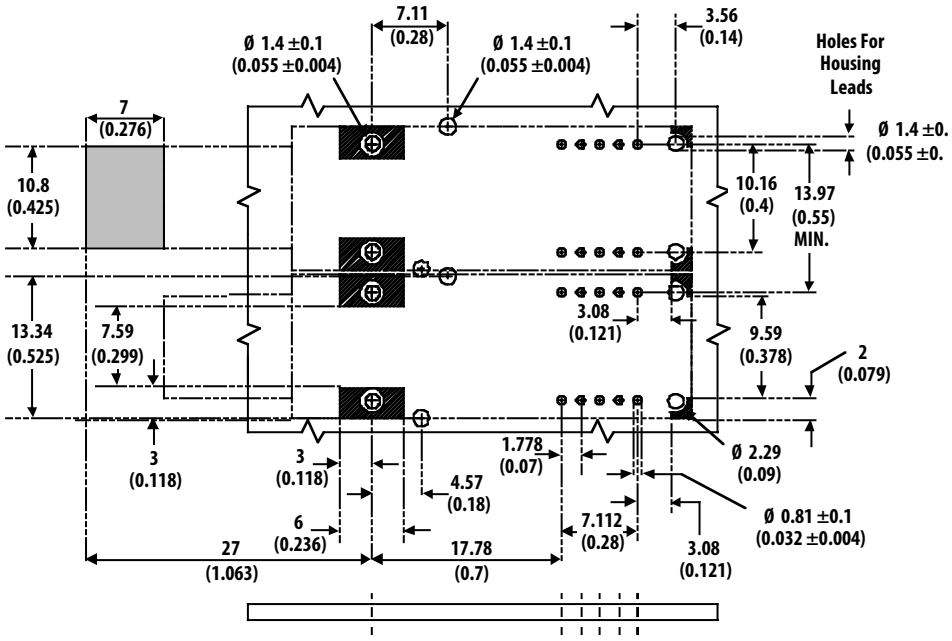
PCB Footprint and Mechanical Outline

All dimensions on the circuit board layout and MT-RJ front panel layout were taken directly or indirectly from the joint MSA.

Shown in Figure 8 is the recommended PCB layout for the HFBR/HFCT-591xE.

The distance from solder posts to front panel is critical in ensuring that the nose shield fits correctly in the front panel. An important note is that there is no dimension that controls the distance from the solder posts to the edge of the PCB. This distance is a function of the PCB material and PCB layout rules. As long as the solder posts are properly soldered to the PCB, there is enough strength in the transceiver port for repeated connections.

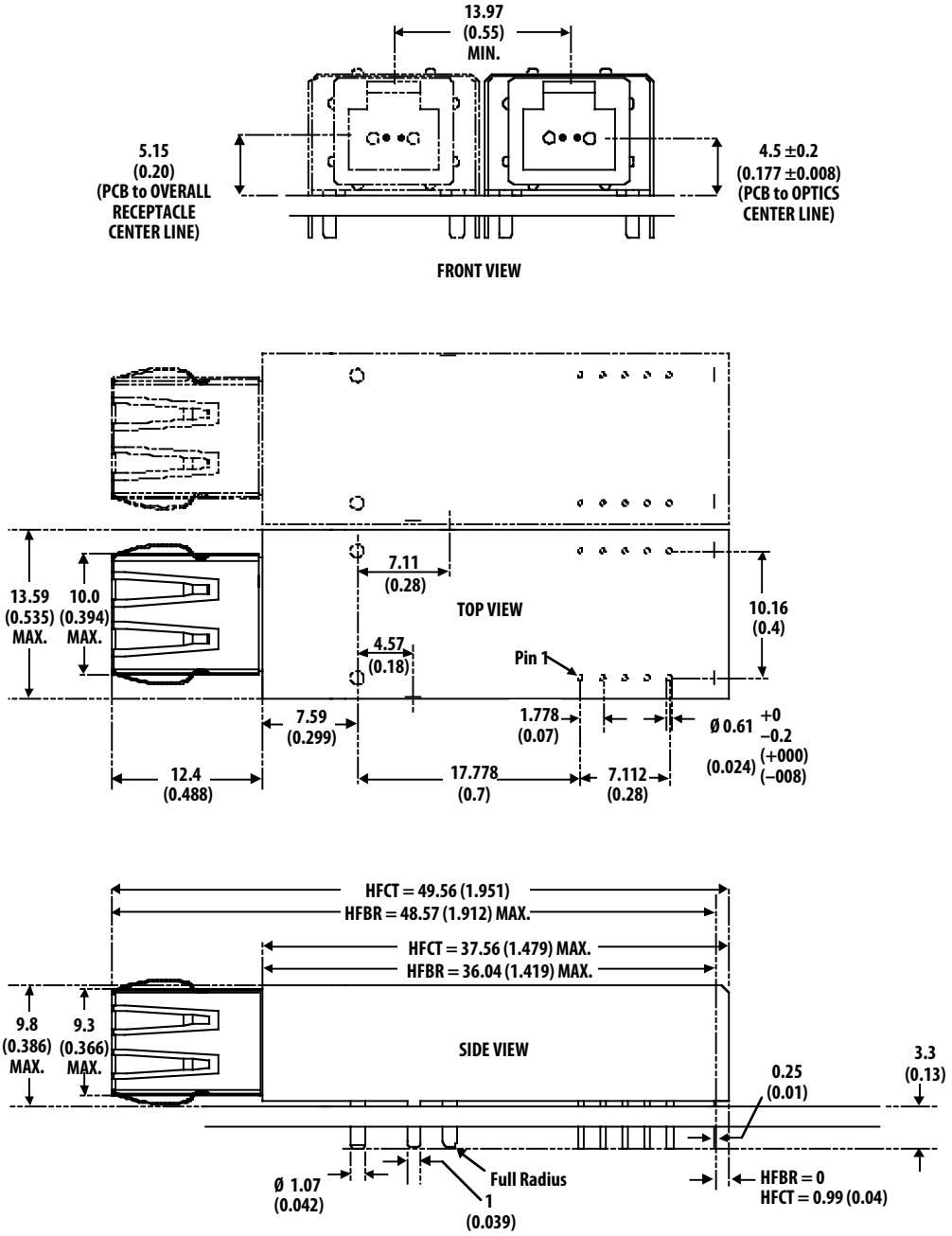
Figure 9 is the package outline drawing for the HFBR/HFCT-591xE.



Dimensions in millimeters (inches)

Notes:
1. This figure describes the recommended circuit board layout for the MT-RJ transceiver pla
   0.550 spacing.
2. The hatched areas are keep-out areas reserved for housing standoffs. No metal traces o
   connection in keep-out areas.
3. 2 x 5 transceiver module requires 16 PCB holes (10 I/O pins, 2 solder posts and 4 package
   tabs).
   Package grounding tabs should be connected to signal ground.
4. Solder posts should be soldered to PCB for mechanical integrity and the holes in the cir
   connected to chassis ground.

Figure 8. Recommended board layout hole pattern



Dimensions in millimeters (inches)

Notes:
1. This page describes the maximum package outline, mounting studs, pins and their relationships to
2. Toleranced to accommodate round or rectangular leads.
3. The 10 I/O pins, 2 solder posts and 4 package grounding tabs are to be treated as a single patter
   (See fFgure 5 PCB layout).
4. The MT-RJ has a 750 μm fiber spacing.
5. The MT-RJ alignment pins are in the module.
6. See MT-RJ transceiver pin out diagram for details.

Figure 9. Package outline drawing of HFBR/HFCT-591xE

MT-RJ SFF Panel Opening

Figure 10 shows the recommended panel mounting for all Avago SFF transceivers. This drawing precisely follows the MSA's drawing "Front Panel Opening for MT-RJ". All Avago SFF transceivers, together with the metal nose shield over the MT-RJ connector port, will conform to this front panel layout. The PCB must be mounted perpendicular to the front panel in order for the nose shield chassis 'fingers' to fit correctly. Care must be taken to slide the PCB horizontally through the panel opening and to avoid excessive pressure on the nose of the transceiver.

The HFBR/HFCT-591xE transceivers meet eye safety requirements, thus avoiding the need for blocking the optical ports when unconnected. The port plugs supplied with SFF transceivers are for protecting the optics from contamination.

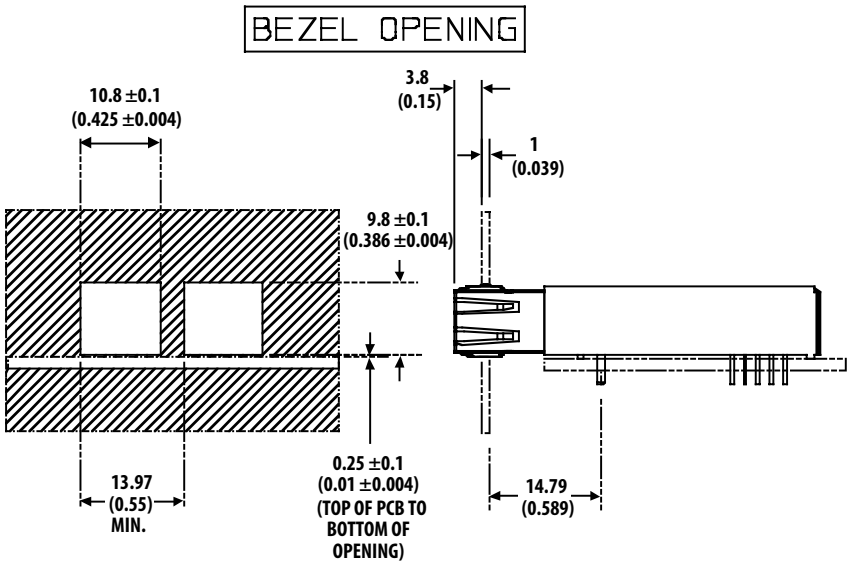
Optimum EMI performance requires low impedance contact between the MT-RJ metal nose shield and system chassis. The edges of the panel opening should be free from any nonconductive paints or adhesives. In addition metals that can build up insulating oxides, such as aluminium, should be avoided.

The SFF grounding scheme is described in the relevant data sheets. It is important to note that the HFBR/HFCT-591xE transceivers have separate V_{CC} planes but common ground planes for the transmitter and receiver sections.

PCB Design Guideline

High-speed PCB design guidelines and rules are well documented in many references but are outlined below as a brief guide for the new fiber optic designer.

1. Make data lines transmission lines of fixed impedance, such as microstrip or stripline. This should be done even if these trace lengths are so short that the propagation delay of the line is small relative to the transition time of the signal. In general, microstrip lines of 50 Ω impedance should be used to help dominate parasitic effects of the board and devices on the signal quality (reflections, ringing, distortion) and minimize unwanted electrical noise.
2. Keep data lines as short as possible and of equal length to minimize pulse-width distortion of the differential data lines. Load the differential lines symmetrically to prevent pulse-width distortion.
3. Keep differential data lines in the same approximate location to prevent unbalanced crosstalk coupling. Use differential signals to interconnect components. Single-ended operation is not recommended since data sheet specifications can only be guaranteed when both differential inputs are used.
4. Place power supply filter circuits as close as possible to the V_{CC} pins of the fiber optic transceiver for best power supply conductive noise filtering.
5. Place data line terminations at the load end of the transmission line where the input of the receiving circuit is located.
6. Use a wide-area, continuous ground plane to provide a low-inductive impedance return path for the power supply ground currents. Minimize holes in the ground plane to allow ground currents to take direct paths to the return point, and to form a shielding plane and reference plane for microstrip transmission lines. It is possible to provide a cut in the ground plane underneath the fiber optic transceiver (along the centerline of the length of the device) from the front of the transceiver to the rear end of the transceiver. This cut does not disconnect the ground plane into independent sub-portions; the ground plane is still one plane. This cut merely causes logic ground currents not to flow under the sensitive receiver section of the transceiver.



Dimensions in millimeters (inches)

Note: Nose shield should be connected to chassis ground.

Figure 10. Recommended panel mounting

7. If possible, distribute V_{CC} power via a plane rather than by traces. This helps minimize the inductive effect of traces on the switching logic currents supplied from V_{CC}.
8. Place V_{CC} bypass capacitors as close as possible to the V_{CC} locations that require bypassing.
9. Use high-quality, high-frequency surface-mount components for best high-frequency performance. Surface mount coil inductors should have < 0.7 Ω series resistance and a high self-resonant frequency. Ferrite beads can be substituted for coil inductors if the power supply noise is fairly quiet. The 0.1 μF capacitors should be monolithic, ceramic type capacitors and the 10 μF capacitor should be a tantalum.

EMI Radiation/Susceptibility

Radiated emissions for the HFBR-591xE and HFCT-591xE have been tested successfully in several environments. Data sheet values will normally describe emissions behavior in a worst-case, open air, unshielded environment. While this number is important for system designers in terms of emissions levels inside a system, Avago recognizes that the performance of most interest to our customers is the emissions levels which could be expected to radiate from a typical system chassis. In their application, SFF transceivers are intended for use inside an enclosed system, protruding through the specified panel opening at the specified protrusion depth. (See the Board Layout Considerations section for appropriate dimensions and layout information). For more detailed information on fiber optic and system EMI and testing, see also AN 1166.

Given that the emissions from one transceiver is L (dBμV/m) we can theoretically scale multiple transceiver performance using 10log(N)+L, where N is the number of transceivers. For example, if we have a reading of 20 dBμV/m for a single transceiver, we would theoretically expect for 100 of the same transceivers, an increase of 10log(N), or 20 dB, to 40 dBμV/m. We have measured some systems which follow this curve quite closely. Repeatability of the measurement setup and repeatability in reassembling the system for different configurations can have a large impact on actual results. The radiation patterns produced by dense arrays of SFF transceivers can be very complex and difficult to accurately characterize or predict. The 10 log(N) relationship should only be used as a rough guideline.

The evaluation board used for EMI testing contains just one SFF transceiver and the specified terminations. Layout is per the recommendations in this application note with the exception of mounting holes, which are slightly larger to accommodate pin sockets that allow easy installation and removal of the transceiver. For testing, 1010 optical data running at 1250 Mb/s is fed to the Rx side. Rx signals are looped back directly to Tx electrically through 50 Ω stripline transmission lines.

For simulated chassis measurements, the evaluation board is screwed into a small, RF tight metal box with just the recommended panel opening for the transceiver port. A +3.3 V DC bias is brought in through the wall using a bulkhead connector mated to an SMA semi-rigid cable. Open air measurements are with the lid removed, exposing the entire top surface of the evaluation board and transceiver. The transceiver and RF box were manipulated 360° over all three axes to determine maximum available emissions.

EMI response for both multimode and single mode transceivers was measured under open air and simulated chassis conditions. Figures 11 to 14 show the worst EMI response when measured from 30 MHz to 7 GHz.

Clearly, the transceiver passes FCC-B under open air conditions, indicating that it should be feasible from an emissions standpoint to use the parts in quantities of over 100. Simulated chassis measurements are at or near the measurement floor. Indicating that with careful enclosure and PCB layout design, high port density may be possible. Careful attention must be paid to the locations of high-speed clocks or gigabit circuitry with respect to these apertures. While our measurements and experiences do not indicate any specific transceiver emissions issues, Avago recognizes that the transceiver aperture is often the weakest link in system enclosure integrity. Avago has designed the modules to minimize emissions and, if necessary, contain the internal system emissions by shielding the aperture.

To that end, our gigabit MT-RJ transceivers (HFCT-591xE & HFBR-591xE) have “metal nose” shields that provide a convenient chassis ground connection to the nose of the transceiver. This metal nose shield improves the EMI performance of the transceiver and improves system EMI performance by minimizing the MT-RJ aperture. Localized shielding is also improved by connecting metal housing solder pins to signal ground on the PCB. Though not obvious by inspection, the nose clip and metal housing are electrically separated for users that do not wish to directly tie chassis and signal grounds together. The recommended transceiver position, PCB layout and panel opening for both the HFBR-591xE and HFCT-591xE are the same, making them physically compatible.

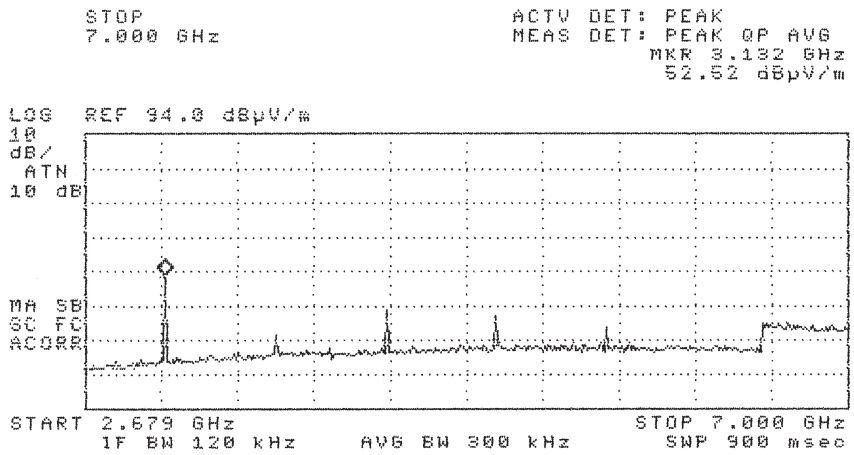


Figure 11. HFBR-591xE open air radiation

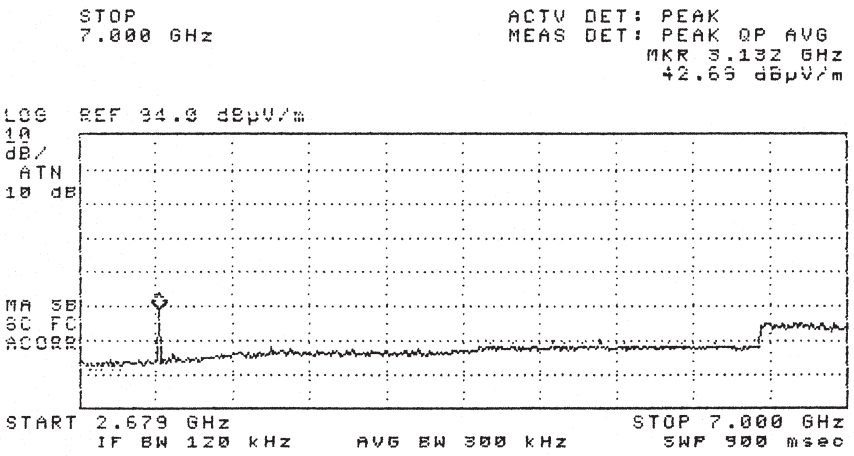


Figure 12. HFBR-591xE simulated chassis radiation

Handling

Process Plug

The HFBR-591xE and HFCT-591xE SFF transceivers are supplied with a process plug for protection of optical ports. This process plug prevents contamination during solder and aqueous rinse as well as during handling, shipping or storage. It is made of high temperature, moulded material containing an insert that forms a seal around the optical port. The multimode (black) and single mode process plugs (blue) are not interchangeable. The process plug is capable of withstanding +80° C and a rinse pressure of 110 psi.

Optical Path Cleanliness

To ensure optimum product performance, the optical light path must not be obscured by any contamination. The following cleaning procedure is suggested:

1) Use a nitrogen air gun, or similar, to blow clean the MT ferrule inside the housing each time before inserting the MT-RJ patchcord.
2) Use a nitrogen air gun, or similar, to blow clean the MT ferrule in the MT-RJ patchcord each time before mating with the module or another patchcord.
3) Wipe the ferrule gently with IPA using lint free material no less than once every 25 matings.
4) Use a nitrogen air gun, or similar, to blow clean the ferrule each time after wiping the ferrule with HFE 7100 to ensure that no debris is left on the MT endface.
5) Put modules and patchcords on a dry and clean surface after demating to avoid contamination.
6) Use the modules process plug and the patchcords dust cap whenever they are not in use.

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the SFF fiber optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA and 100 Flux from Alpha metals of Jersey City, NJ.

Recommended cleaning and degreasing chemicals for the SFF are alcohol's (methyl, isopropyl, isobutyl) and aliphates (hexane, heptane). Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1 trichloroethane, ketones (such as MEK), acetate, chloroform, ethyl acetate, methylene dichloride, phenaol, methylene chloride or N-methylpyrolldone.

Thermal Analysis/Considerations

The HFCT-591xE single mode SFF transceiver consumes a typical 600 mW of power. The case temperature is approximately +5° C higher than ambient temperature and the metal shield of the transceiver enables efficient power dissipation.

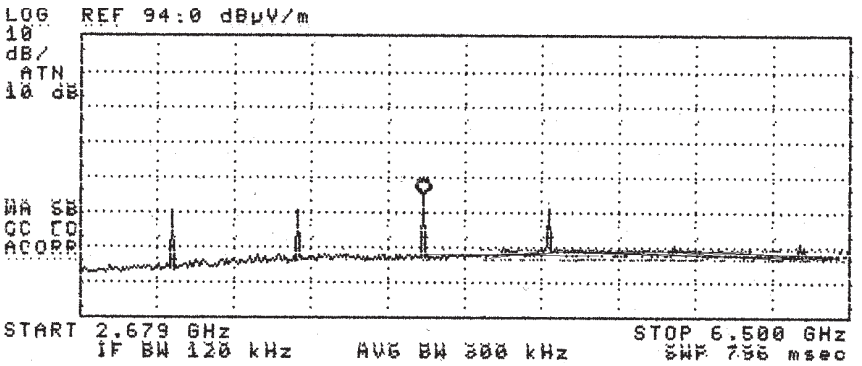


Figure 13. HFCT-591xE open air radiation. Maximum emission up to 6.5 GHz is 51.2 dBmV/m.

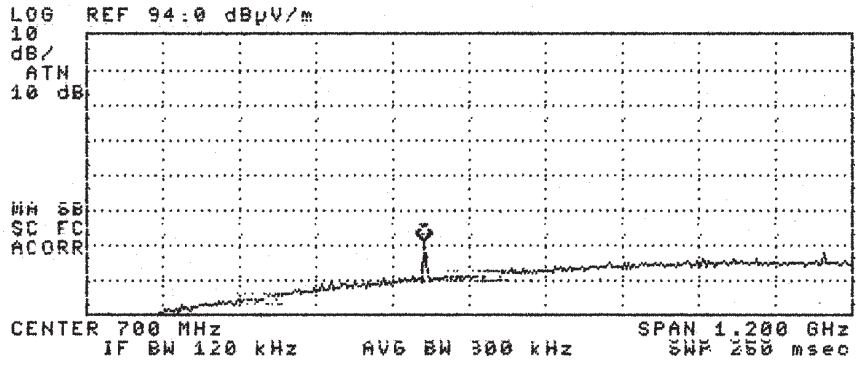


Figure 14. HFCT-591xE simulated chassis radiation. Maximum emission below 960 MHz is 33.3 dBmV/m.

Regulatory Notes

Laser Safety – European Union

The HFCT-591xE transceiver contains a 1300 nm FP laser. The HFBR-591xE transceiver contains a 850 nm VCSEL laser. These transceivers are classified as "Class 1 Laser Products" per EN 60825-1(+A11), Safety of Laser Products; and per Radiation Control for the Health & Safety Act of 1968 of the US. Dept. of Health & Human Services. Class 1 lasers are considered "eye safe" and do not pose a biological hazard if used within the data sheet limits and instructions.

Caution:

Use of controls, adjustments or performance procedures other than those specified may result in hazardous radiation exposure. There are no user serviceable parts nor any maintenance required for the HFCT-591xE and HFBR-591xE transceivers. All adjustments are made at the factory before shipment to our customers. Tampering with or modifying the circuitry by prying open the enclosure may result in improper operation and overstress of the laser source. The person(s) performing such an act is required by law to recertify and reidentify the laser product under the provisions of 21 CFR (US Code of Federal Regulations - Subchapter J).

Safety certificates can be found at the following URL:

http://www.avagotech.com.

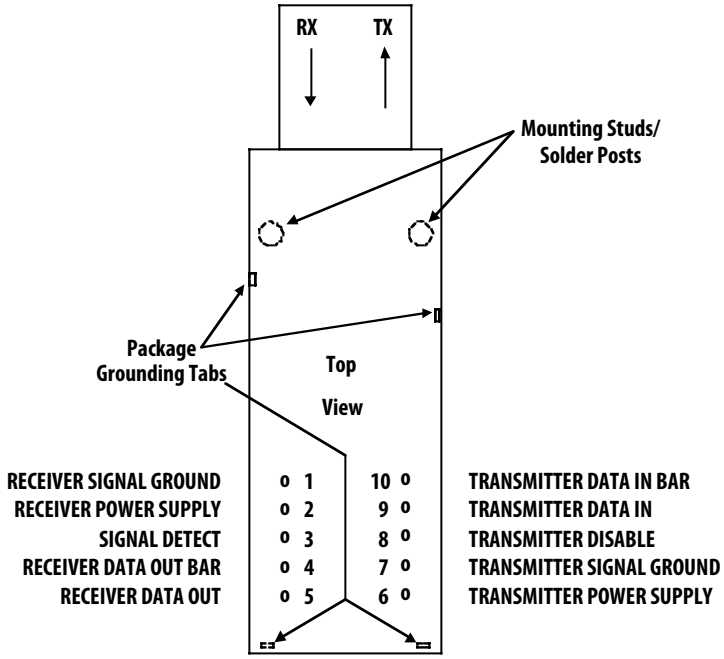


Figure 15. Pin assignment diagram

Table 1. Pinout Table

Pin	Symbol	Functional Description
Two Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground. Note: The holes in the circuit board must be tied to chassis ground.
Four Package Grounding Tabs		Connect to signal ground. Note: Grounding tabs must be connected to signal ground for optimum EMI perfornance.
1	V_{EER}[1]	Receiver Signal Ground. Directly connect this pin to receiver signal ground plane.
2	V_{CCR}	Receiver Power Supply
3	SD	Signal Detect Normal Operation: Logic '1' Output Fault Condition: Logic '0' Output
4	RD-	Received Data Out Bar
		No internal terminations provided.
5	RD+	Received Data Out
		No internal terminations provided.
6	V_{CCT}	Transmitter Power Supply
7	V_{EET}[1]	Transmitter Signal Ground
8	TDis	Transmitter Disable:
		Transmitter Disabled: (V_{CCT} - 1.3 V) < V < V_{CCT}) Transmitter Enabled: V_{EET} < V < (V_{EET} + 0.8 V) or open circuit.
9	TD+	Transmitter Data In
10	TD-	Transmitter Data In Bar

Note:

1. The Transmitter and Receiver V_{EE} connections are commoned within the module.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

5968-7908E - August 23, 2010

AVAGO
TECHNOLOGIES

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru