



## P-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Low threshold (-2.0V max.)
- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

### Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

### General Description

This low threshold enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package Option	BV <sub>DSS</sub> / BV <sub>DGS</sub> (max) (V)	R <sub>DS(ON)</sub> (max) (Ω)	V <sub>GS(th)</sub> (max) (V)	I <sub>D(ON)</sub> (min) (A)
	TO-92				
TP2635	TP2635N3-G	-350	15	-2.0	-0.7

-G indicates package is RoHS compliant ('Green')



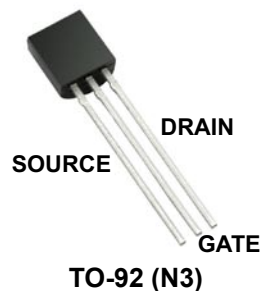
### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV <sub>DSS</sub>
Drain-to-gate voltage	BV <sub>DGS</sub>
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

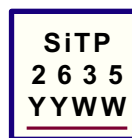
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Pin Configuration



### Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

### Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (A)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{ja}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}$ <sup>†</sup> (mA)	$I_{DRM}$ (A)
TO-92	-180	-0.8	1.0	125	170	-180	-0.8

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

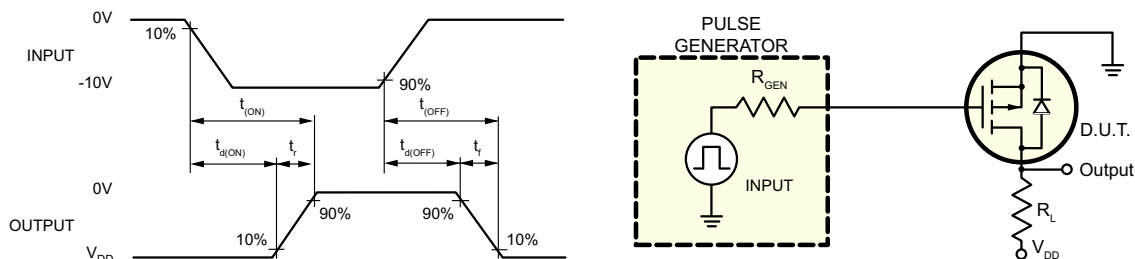
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	-350	-	-	V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	Gate threshold voltage	-0.8	-	-2.0	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
$I_{GSS}$	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero gate voltage drain current	-	-	-1.0	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = -100V$
				-10.0		$V_{GS} = 0V, V_{DS} = \text{Max rating}$
				-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-0.7	-	-	A	$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	12	$\Omega$	$V_{GS} = -2.5V, I_D = -20mA$
				11		$V_{GS} = -4.5V, I_D = -150mA$
				11		$V_{GS} = -10V, I_D = -300mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -300mA$
$G_{FS}$	Forward transconductance	200	-	-	mmho	$V_{DS} = -25V, I_D = -300mA$
$C_{ISS}$	Input capacitance	-	-	300	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	-	50		
$C_{RSS}$	Reverse transfer capacitance	-	-	12		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = -25V, I_D = -300mA, R_{GEN} = 25\Omega$
$t_r$	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	60		
$t_f$	Fall time	-	-	40		
$V_{SD}$	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -200mA$
$t_{rr}$	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -200mA$

**Notes:**

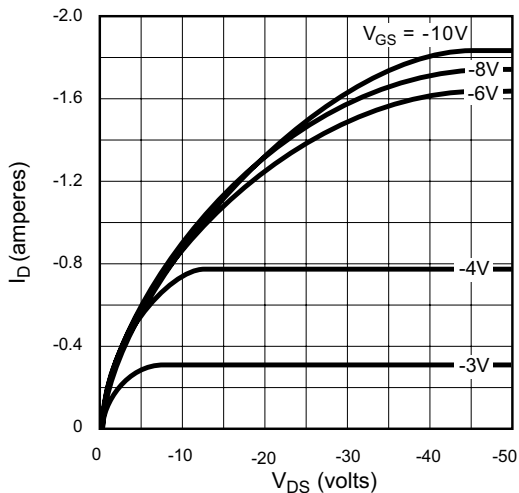
1. All D.C. parameters 100% tested at 25C unless otherwise stated. (Pulse test: 300s pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

### N- Channel Switching Waveforms and Test Circuit

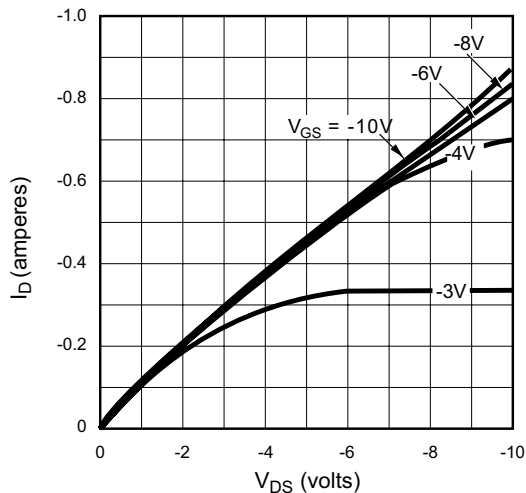


# Typical Performance Curves

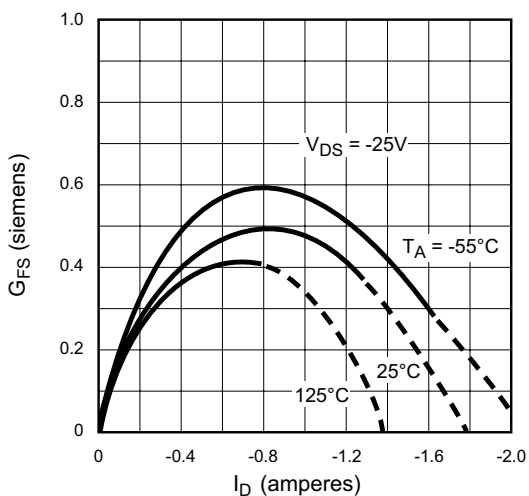
Output Characteristics



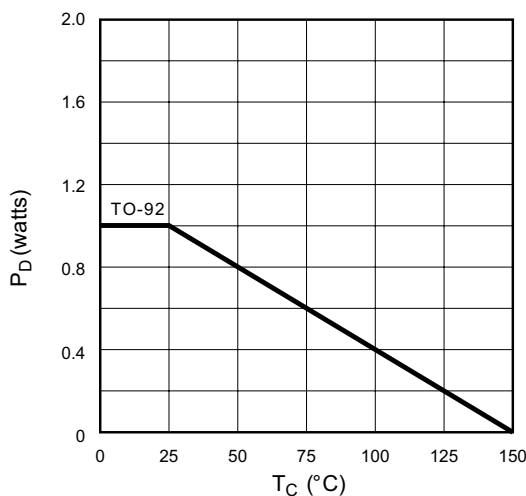
Saturation Characteristics



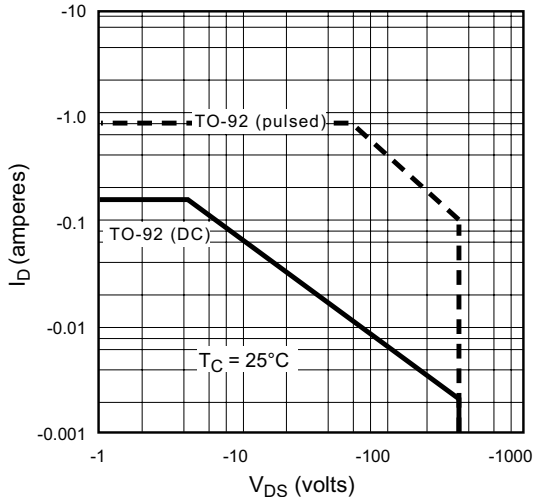
Transconductance vs. Drain Current



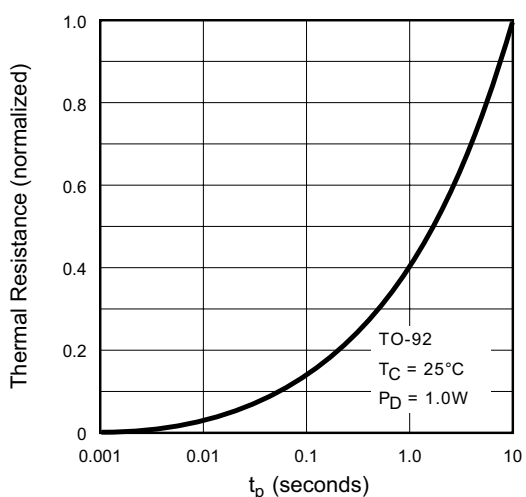
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

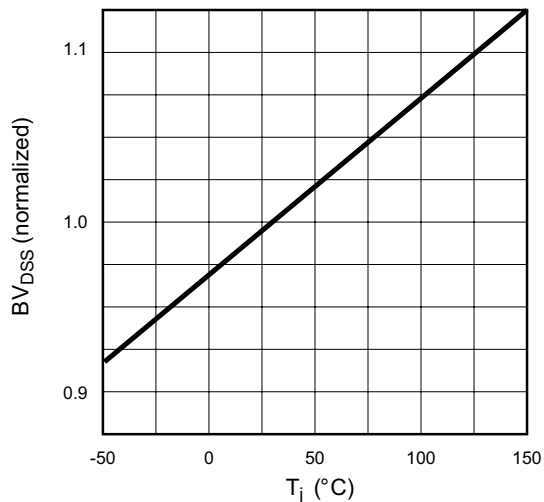


Thermal Response Characteristics

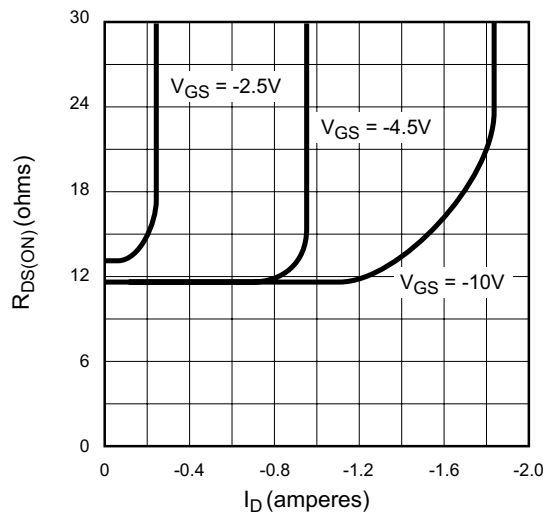


Typical Performance Curves (cont.)

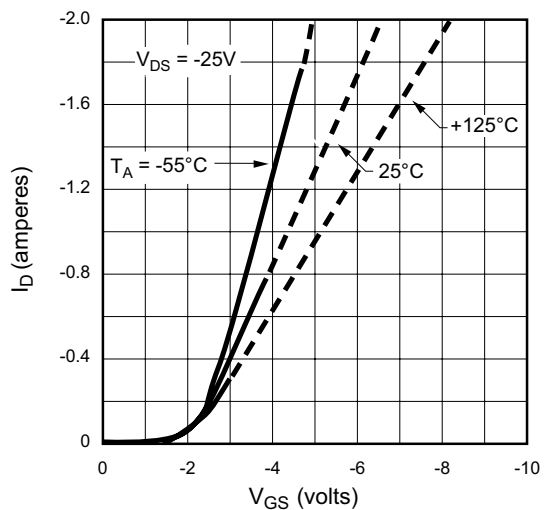
BV<sub>DSS</sub> Variation with Temperature



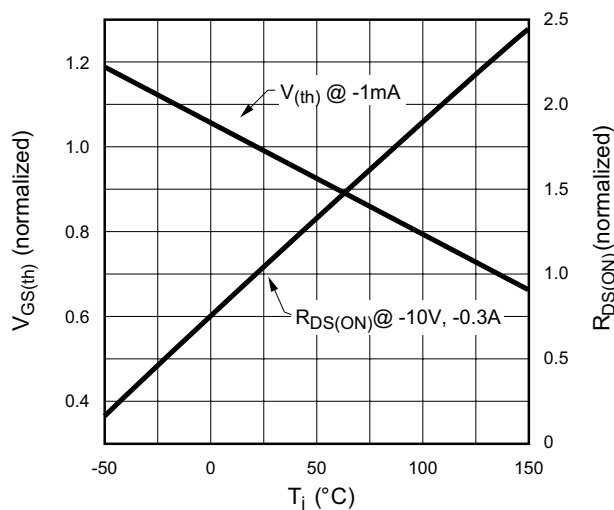
On-Resistance vs. Drain Current



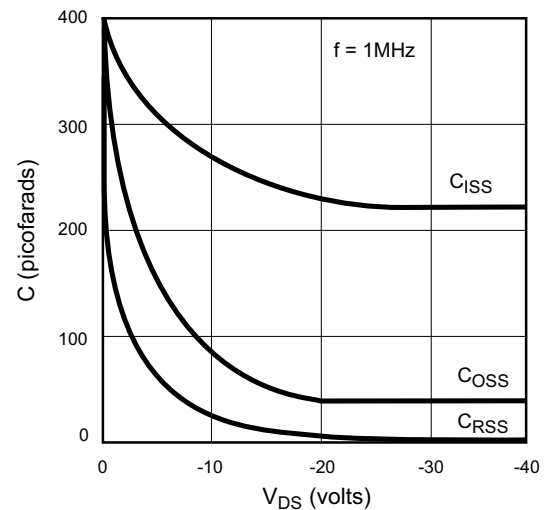
Transfer Characteristics



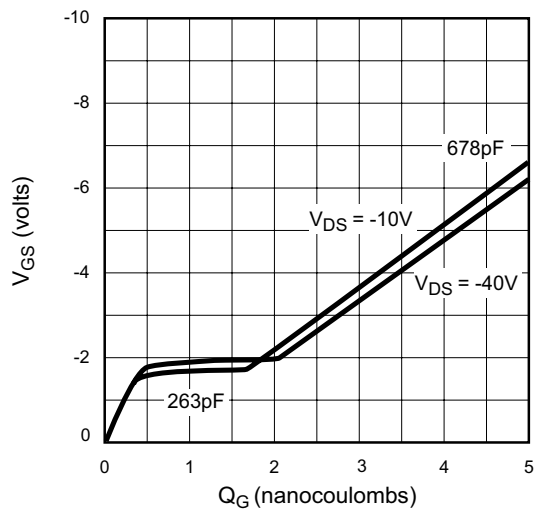
V<sub>TH</sub> and R<sub>DS</sub> Variation with Temperature



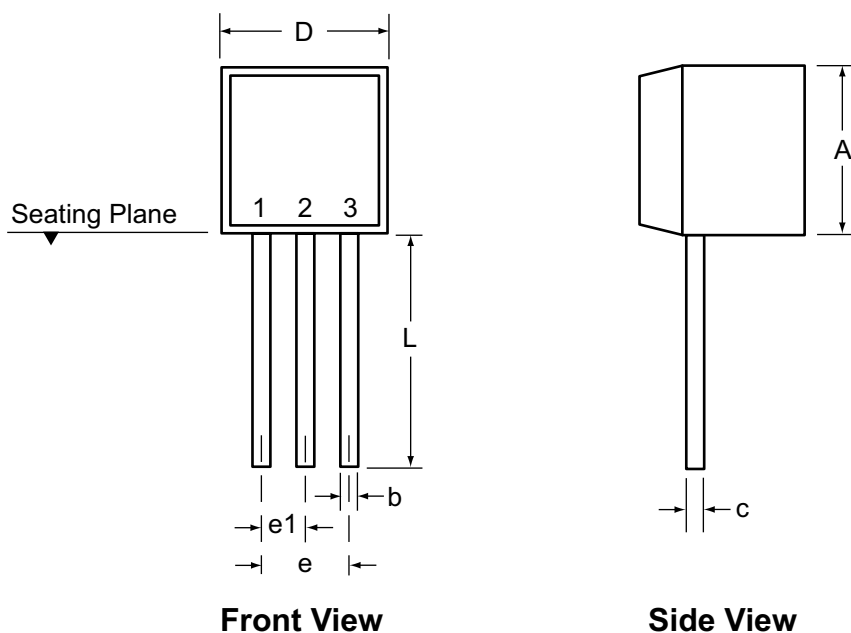
Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



### 3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc.#:** DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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