# PSoC® 4: PSoC 4200D Family Datasheet

## Programmable System-on-Chip (PSoC®)

## General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an ARM® Cortex™-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4200D product family, based on this platform architecture, is a combination of a microcontroller with digital programmable logic, programmable interconnect, and standard communication and timing peripherals. The PSoC 4200D products will be fully compatible with members of the PSoC 4 platform for new applications and design needs. The programmable digital subsystem allows flexibility and in-field tuning of the design.

## Features

### 32-bit MCU Subsystem

- 48 MHz ARM Cortex-M0 CPU with single-cycle multiply
- Up to 64 kB of flash with Read Accelerator
- Up to 8 kB of SRAM
- DMA engine

### Programmable Digital

- Four programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Programmable I/O block (PRGIO) provides the ability to perform Boolean functions in the I/O signal path
- Cypress-provided peripheral component library, user-defined state machines, and Verilog input

### Low Power 1.71 to 5.5 V Operation

- Low-power Deep Sleep Mode with GPIO pin wakeup

### Serial Communication

- Three independent run-time reconfigurable serial communication blocks (SCBs) with reconfigurable $I^2C$, SPI, or UART functionality

### Timing and Pulse-Width Modulation

- Four 16-bit timer/counter pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

### Packages

- 25-ball CSP package 2.07 mm × 2.11 mm, 28-SSOP package.
- Up to 21 programmable GPIOs
- GPIO drive modes, strengths, and slew rates are programmable

### PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API component) for all fixed-function and programmable peripherals

### Industry-Standard Tool Compatibility

- After schematic entry, development can be done with ARM-based industry-standard development tools

## More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

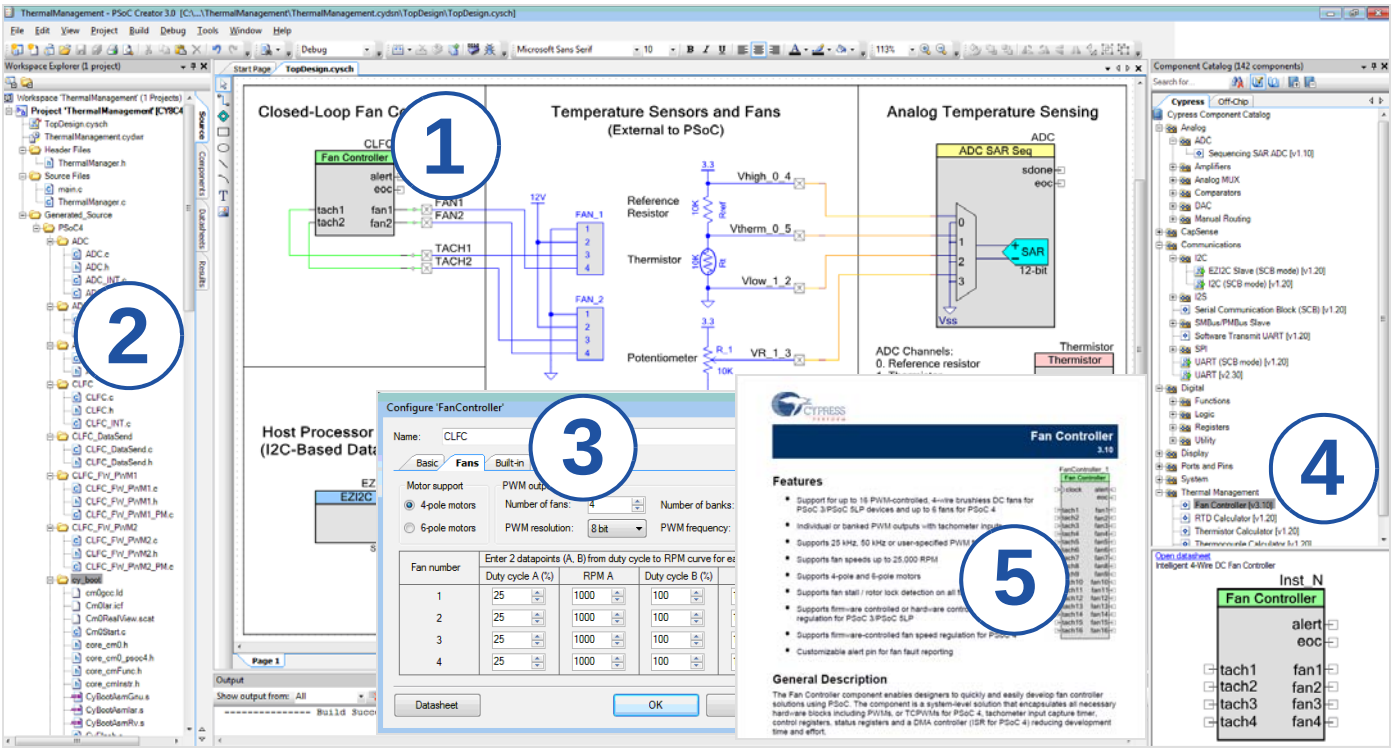
The MiniProg3 device provides an interface for flash programming and debug.

## PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



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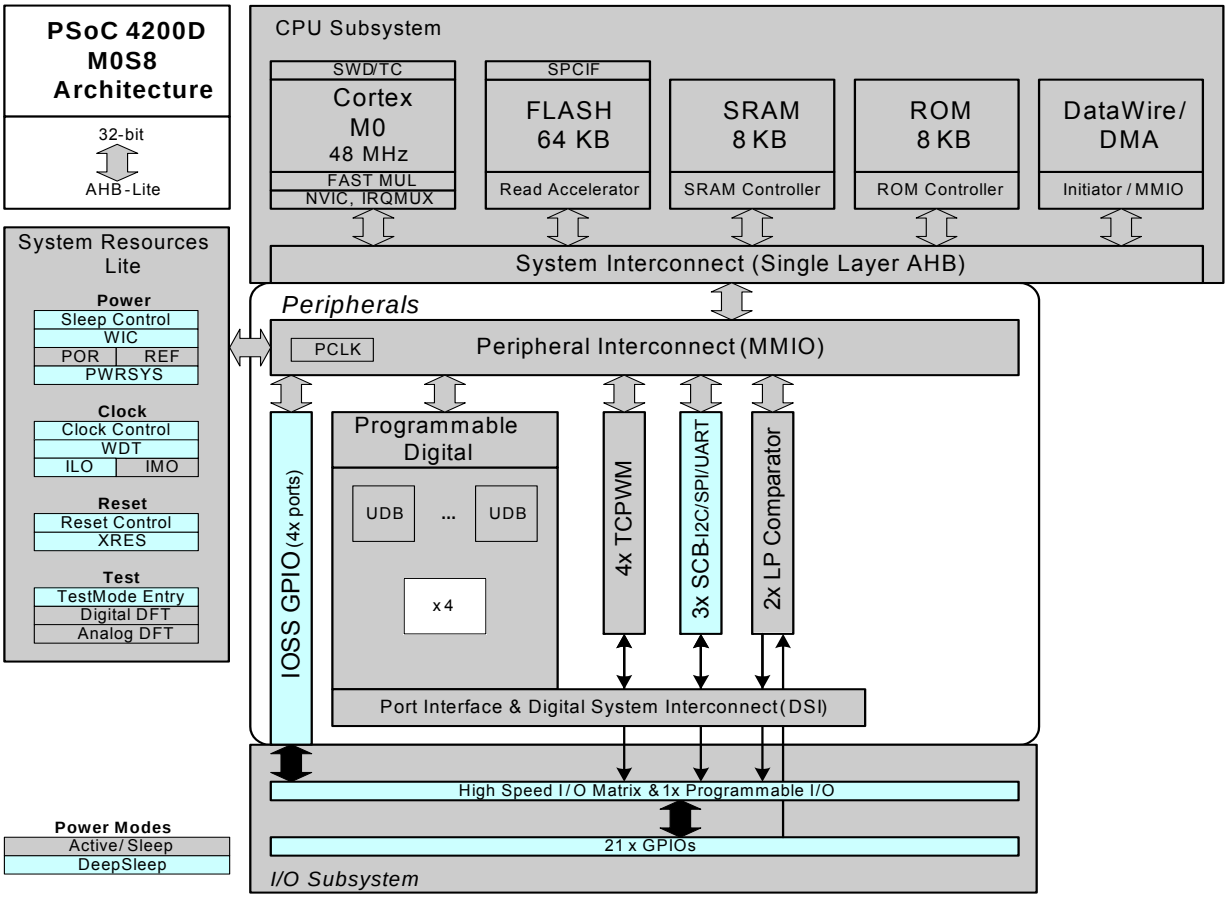
## PSoC 4200D Block Diagram




The PSoC 4200D devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4200D devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4200D family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200D with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200D allows the customer to make.

# Functional Definition

## CPU and Memory Subsystem

### *CPU*

The Cortex-M0 CPU in the PSoC 4200D is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200D has four break-point (address) comparators and two watchpoint (data) comparators.

### *Flash*

The PSoC 4200D has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

### *SRAM*

8K of SRAM memory is provided.

### *SROM*

A supervisory ROM that contains boot and configuration routines is provided.

### *DMA*

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

## System Resources

### *Power System*

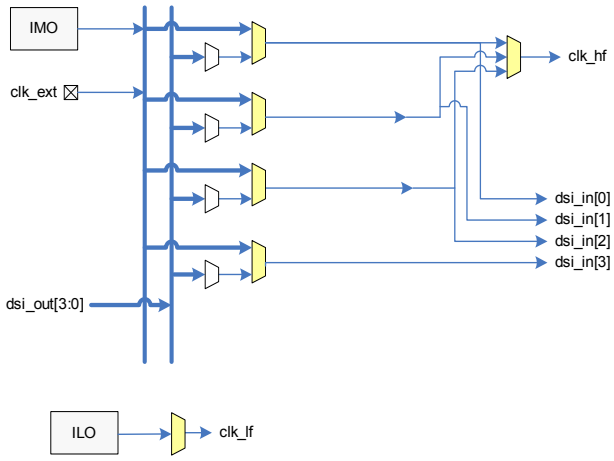
The power system is described in detail in the section Power on page 10. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4200D operates with a single external supply over the range of 1.71 V to 5.5 V and has three different power modes, transitions between which are managed by the power system. The PSoC 4200D provides Active, Sleep, and Deep Sleep modes.

### *Clock System*

The PSoC 4200D clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200D consists of the IMO (3 to 48 MHz) and the ILO (40-kHz nominal) internal oscillators, and provision for an external clock.

**Figure 2. PSoC 4200D MCU Clocking Architecture**




The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of six clock dividers for the PSoC 4200D, each with 16-bit divide capability, two of which support fractional baud-rate generation. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

### *IMO Clock Source*

The IMO is the primary source of internal clocking in the PSoC 4200D. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between the range of 24 to 48 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%. An IMO post-divider with possible divide values of 2, 4, or 8 can be used to divide the clock down to 3 MHz if required.

### *ILO Clock Source*

The ILO is a very low power oscillator, nominally 40 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### *Watchdog Timer*

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

*Reset*

The PSoC 4200D can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

## Analog Block

*Low-power Comparators*

The PSoC 4200D has a pair of low-power comparators, with two different power modes allowing trade-off of power versus response time.

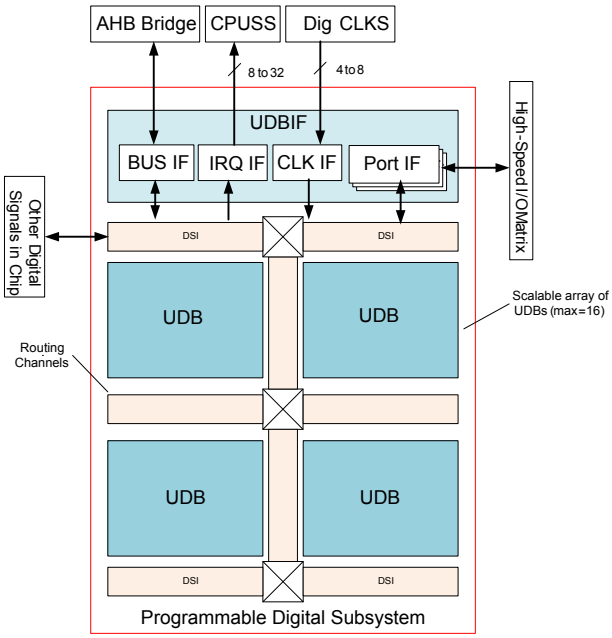
## Programmable Digital

*Universal Digital Blocks (UDBs) and Port Interfaces*

The PSoC 4200D has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

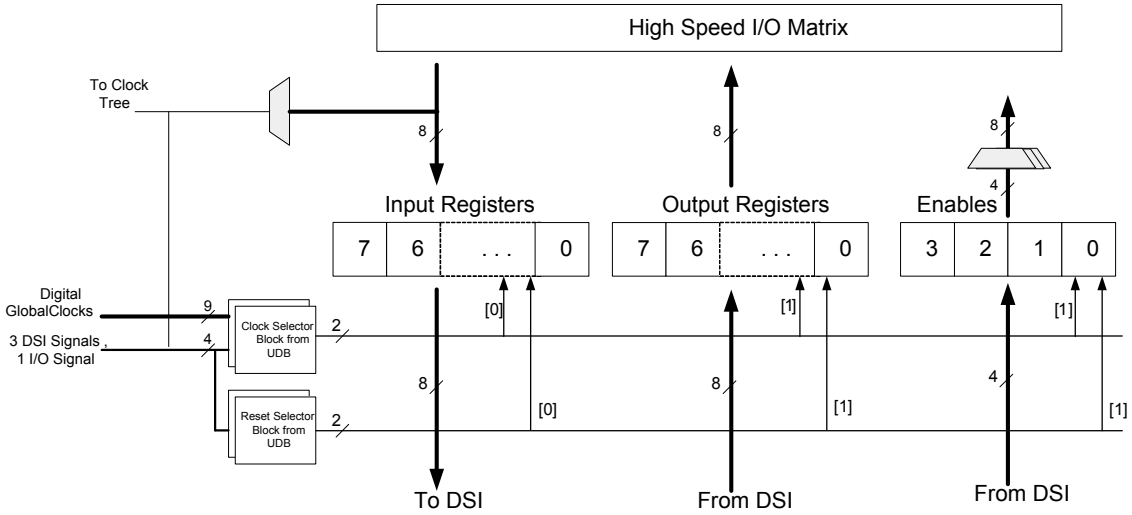
**Figure 3. UDB Array**




A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in Figure 4.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

**Figure 4. Port Interface**



## Fixed Function Digital

*Timer/Counter/PWM (TCPWM) Block*

The TCPWM block uses a16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The PSoC 4200D has four TCPWM blocks.

*Serial Communication Blocks (SCB)*

The PSoC 4200D has three SCBs, which can each implement an $I^2C$, UART, or SPI interface.

$I^2C$ Mode: The hardware $I^2C$ block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports Ez$I^2C$ that creates a mailbox address range in the memory of the PSoC 4200D and effectively reduces $I^2C$ communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The $I^2C$ peripheral is compatible with the $I^2C$ Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP $I^2C$-bus specification and user manual (UM10204). The $I^2C$ bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO to buffer transfers.

## GPIO

The PSoC 4200D has 21 GPIOs in the 25-ball CSP package. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for the PSoC 4200D).

## Pinouts

The following is the pin list for the PSoC 4200D. Pins 16, 17, and 18 are No-Connects in the 28-SSOP package.

**Table 1. PSoC 4200D Pin Description**

| 28-Pin SSOP | | 25-Ball CSP | | Alternate Functions for Pins | | | | | | Pin Description |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Analog | PRGIO | Alt 1 | Alt 2 | Alt 3 | Alt 4 | |
| 19 | P0.0 | E4 | P0.0 | lpcomp.in_p[0] | | tcpwm.line[2] | | | scb[0].spi_select1 | P0.0, LPC0, TCPWM2, SCB0 |
| 20 | P0.1 | E3 | P0.1 | lpcomp.in_n[0] | | tcpwm.line_compl[2] | | | scb[0].spi_select2 | P0.1, LPC0, TCPWM2, SCB0 |
| 21 | P0.2 | D3 | P0.2 | | | tcpwm.line[3] | | | scb[0].spi_select3 | P0.2, TCPWM3, SCB0 |
| 22 | P0.4 | E2 | P0.4 | | | | scb[1].uart_rx | scb[1].i2c_scl | scb[1].spi_mosi | P0.4, SCB1 |
| 23 | P0.5 | C4 | P0.5 | | | | scb[1].uart_tx | scb[1].i2c_sda | scb[1].spi_miso | P0.5, SCB1 |
| 24 | P0.6 | C3 | P0.6 | | | ext_clk | scb[1].uart_cts | | scb[1].spi_clk | P0.6, Ext Clock, SCB1 |
| 25 | XRES | D2 | XRES | | | | | | | XRES |
| 26 | VCCD | E1 | VCCD | | | | | | | Regulator Output |
| 28 | VSSD | D1 | VSSD | | | | | | | Power Supply |
| 27 | VDDD | C1 | VDDD | | | | | | | Ground |
| 1 | P1.0 | C2 | P1.0 | | | tcpwm.line[2] | scb[0].uart_rx | scb[0].i2c_scl | scb[0].spi_mosi | P1.0, TCPWM2, SCB0 |
| 2 | P1.1 | B2 | P1.1 | | | tcpwm.line_compl[2] | scb[0].uart_tx | scb[0].i2c_sda | scb[0].spi_miso | P1.1, TCPWM2, SCB0 |
| 3 | P1.2 | B1 | P1.2 | | | tcpwm.line[3] | scb[0].uart_cts | | scb[0].spi_clk | P1.2, TCPWM3, SCB0 |
| 4 | P1.3 | A1 | P1.3 | | | tcpwm.line_compl[3] | scb[0].uart_rts | | scb[0].spi_select0 | P1.3, TCPWM3, SCB0 |
| 5 | P2.2 | B3 | P2.2 | | prgio[0].io[2] | | scb[2].uart_rx | scb[2].i2c_scl | scb[2].spi_mosi | P2.2, PRG, SCB2 |
| 6 | P2.3 | A2 | P2.3 | | prgio[0].io[3] | | scb[2].uart_tx | scb[2].i2c_sda | scb[2].spi_miso | P2.3, PRG. SCB2 |
| 7 | P2.4 | B4 | P2.4 | | prgio[0].io[4] | tcpwm.line[0] | scb[2].uart_cts | lpcomp.comp[0] | scb[2].spi_clk | P2.4, PRG, TCPWM0, SCB2, LPC0 |
| 8 | P2.5 | A4 | P2.5 | | prgio[0].io[5] | tcpwm.line_compl[0] | scb[2].uart_rts | | scb[2].spi_select0 | P2.5, PRG, TCPWM0, SCB2 |
| 9 | P2.6 | A3 | P2.6 | | prgio[0].io[6] | tcpwm.line[1] | | | scb[2].spi_select1 | P2.6, PRG, TCPWM1, SCB2 |
| 10 | P2.7 | A5 | P2.7 | | prgio[0].io[7] | tcpwm.line_compl[1] | | | scb[2].spi_select2 | P2.7, PRG, TCPWM1, SCB2 |

**Table 1. PSoC 4200D Pin Description** *(continued)*

| 28-Pin SSOP | | 25-Ball CSP | | Alternate Functions for Pins | | | | | | Pin Description |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Analog | PRGIO | Alt 1 | Alt 2 | Alt 3 | Alt 4 | |
| 11 | P3.0 | D5 | P3.0 | | | tcpwm.line[0] | scb[1].uart_rx | scb[1].i2c_scl | scb[1].spi_mosi | P3.0, TCPWM0, SCB1 |
| 12 | P3.1 | C5 | P3.1 | | | tcpwm.line_compl[0] | scb[1].uart_tx | scb[1].i2c_sda | scb[1].spi_miso | P3.1, TCPWM0, SCB1 |
| 13 | P3.2 | E5 | P3.2 | | | tcpwm.line[1] | scb[1].uart_cts | swd_data | scb[1].spi_clk | P3.2, TCPWM1, SCB1, SWD_IO |
| 14 | P3.3 | B5 | P3.3 | | | tcpwm.line_compl[1] | scb[1].uart_rts | swd_clk | scb[1].spi_select0 | P3.3, TCPWM1, SCB1, SWD_CLK |
| 15 | P3.4 | D4 | P3.4 | | | | | | scb[1].spi_select1 | P3.4, SCB1 |

**Descriptions of the power pin functions are as follows:**

**VDDD**: Power supply for the chip.

**VSSD**: Ground pin.

**VCCD**: Regulated digital supply (1.8 V ±5% if supplied externally).

## Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

The PSoC 4200D family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

### Unregulated External Supply

In this mode, the PSoC 4200D is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4200D supplies the internal logic and the VCCD output of the PSoC 4200D must be bypassed to ground via an external capacitor.

Bypass capacitors must be used from VDDD to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

| Power Supply | Typical Bypass Capacitors |
|---|---|
| VDDD–VSS | 0.1-µF ceramic at each pin plus bulk capacitor 1 to 10 µF. |
| VCCD–VSS | 0.1-µF ceramic capacitor at the VCCD pin |

### Regulated External Supply

In this mode, the PSoC 4200D is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple. In this mode, VCCD and VDDD pins are shorted together and bypassed. The internal regulator should be disabled in firmware.

## Development Support

The PSoC 4200D family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4200D family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200D family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

# Electrical Specifications

## Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings**[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID1 | $V_{DD_ABS}$ | Analog or digital supply relative to $V_{SS}$ ($V_{SSD}$ = $V_{SSA}$) | –0.5 | – | 6 | V | Absolute maximum |
| SID2 | $V_{CCD_ABS}$ | Direct digital core voltage input relative to $V_{SSD}$ | –0.5 | – | 1.95 | V | Absolute maximum |
| SID3 | $V_{GPIO_ABS}$ | GPIO voltage; $V_{DDD}$ or $V_{DDA}$ | –0.5 | – | $V_{DD}$+0.5 | V | Absolute maximum |
| SID4 | $I_{GPIO_ABS}$ | Current per GPIO | –25 | – | 25 | mA | Absolute maximum |
| SID5 | $I_{G\text{-}PIO_injection}$ | GPIO injection current per pin | –0.5 | – | 0.5 | mA | Absolute maximum |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | V | |
| BID46 | LU | Pin current for latch-up | –140 | – | 140 | mA | |

## Device Level Specifications

All specifications are valid for -40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 3. DC Specifications**

| Spec Id# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID53 | $V_{DDD}$ | Power supply input voltage unregulated | 1.8 | – | 5.5 | V | With on-chip internal regulator enabled |
| SID255 | $V_{DDD}$ | Power supply input voltage externally regulated | 1.71 | 1.8 | 1.89 | V | Externally regulated within this range |
| SID54 | $V_{CCD}$ | Output voltage (for core logic) | – | 1.8 | – | V | |
| SID55 | $C_{EFC}$ | External regulator voltage bypass | – | 0.1 | – | µF | X5R ceramic or better |
| SID56 | $C_{EXC}$ | Power supply decoupling capacitor | – | 1 | – | µF | X5R ceramic or better |
| **Active Mode** | | | | | | | |
| SID6 | $I_{DD1}$ | Execute from flash; CPU at 6 MHz | – | 2.1 | 2.85 | mA | |
| SID7 | $I_{DD2}$ | Execute from flash; CPU at 12 MHz | – | 3.6 | 4 | mA | |
| SID8 | $I_{DD3}$ | Execute from flash; CPU at 24 MHz | – | 5.3 | 6 | mA | |
| SID9 | $I_{DD4}$ | Execute from flash; CPU at 48 MHz | – | 9.8 | 13 | mA | |
| **Sleep Mode** | | | | | | | |
| SID21 | $I_{DD16}$ | $I^2C$ wakeup, WDT, and comparators on. Regulator off. | – | 1.45 | 1.65 | mA | $V_{DD}$ = 1.71 to 1.89, 6 MHz |
| SID22 | $I_{DD17}$ | $I^2C$ wakeup, WDT, and comparators on. | – | 1.8 | 2.45 | mA | $V_{DD}$ = 1.8 to 5.5, 6 MHz |
| SID23 | $I_{DD18}$ | $I^2C$ wakeup, WDT, and comparators on. Regulator off. | – | 1.6 | 1.9 | mA | $V_{DD}$ = 1.71 to 1.89, 12 MHz |

**Note**
1. Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 3. DC Specifications** *(continued)*

| Spec Id# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID24 | $I_{DD19}$ | $I^2C$ wakeup, WDT, and comparators on. | – | 2 | 2.7 | mA | $V_{DD}$ = 1.8 to 5.5, 12 MHz |
| **Deep Sleep Mode, -40 °C to + 60 °C (Guaranteed by characterization)** | | | | | | | |
| SID30 | $I_{DD25}$ | $I^2C$ wakeup and WDT on. Regulator off. | – | 2 | 15 | µA | $V_{DD}$ = 1.71 to 1.89 |
| SID31 | $I_{DD26}$ | $I^2C$ wakeup and WDT on. | – | 2 | 15 | µA | $V_{DD}$ = 1.8 to 3.6 |
| SID32 | $I_{DD27}$ | $I^2C$ wakeup and WDT on. | – | 2 | 15 | µA | $V_{DD}$ = 3.6 to 5.5 |
| **Deep Sleep Mode, +85 °C (Guaranteed by characterization)** | | | | | | | |
| SID33 | $I_{DD28}$ | $I^2C$ wakeup and WDT on. Regulator off. | – | 4 | 45 | µA | $V_{DD}$ = 1.71 to 1.89 |
| SID34 | $I_{DD29}$ | $I^2C$ wakeup and WDT on. | – | 4 | 45 | µA | $V_{DD}$ = 1.8 to 3.6 |
| SID35 | $I_{DD30}$ | $I^2C$ wakeup and WDT on. | – | 4 | 45 | µA | $V_{DD}$ = 3.6 to 5.5 |
| **XRES current** | | | | | | | |
| SID307 | $I_{DD_XR}$ | Supply current while XRES (Active Low) asserted | – | 2 | 5 | mA | |

**Table 4. AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID48 | $F_{CPU}$ | CPU frequency | DC | – | 48 | MHz | $1.71 \le V_{DD} \le 5.5$ |
| SID49 | $T_{SLEEP}$ | Wakeup from sleep mode | – | 0 | – | µs | Guaranteed by characterization |
| SID50 | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | – | 35 | µs | Guaranteed by characterization |
| SID52 | $T_{RESETWIDTH}$ | External reset pulse width | 1 | – | – | µs | Guaranteed by characterization |

*GPIO*

**Table 5. GPIO DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID57 | $V_{IH}$[2] | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID58 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | V | CMOS Input |
| SID241 | $V_{IH}$[2] | LVTTL input, $V_{DDD}$ < 2.7 V | 0.7× $V_{DDD}$ | – | – | V | |
| SID242 | $V_{IL}$ | LVTTL input, $V_{DDD}$ < 2.7 V | – | – | 0.3 × $V_{DDD}$ | V | |
| SID243 | $V_{IH}$[2] | LVTTL input, $V_{DDD} \ge$ 2.7 V | 2.0 | – | – | V | |
| SID244 | $V_{IL}$ | LVTTL input, $V_{DDD} \ge$ 2.7 V | – | – | 0.8 | V | |
| SID59 | $V_{OH}$ | Output voltage high level | $V_{DDD}$ –0.6 | – | – | V | $I_{OH}$ = 4 mA at 3 V $V_{DDD}$ |
| SID60 | $V_{OH}$ | Output voltage high level | $V_{DDD}$ –0.5 | – | – | V | $I_{OH}$ = 1 mA at 1.8 V $V_{DDD}$ |
| SID61 | $V_{OL}$ | Output voltage low level | – | – | 0.6 | V | $I_{OL}$ = 4 mA at 1.8 V $V_{DDD}$ |

**Note**
2. $V_{IH}$ must not exceed $V_{DDD}$ + 0.2 V.

**Table 5. GPIO DC Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID62 | $V_{OL}$ | Output voltage low level | – | – | 0.6 | V | $I_{OL}$ = 8 mA at 3 V $V_{DDD}$ |
| SID62A | $V_{OL}$ | Output voltage low level | – | – | 0.4 | V | $I_{OL}$ = 3 mA at 3 V $V_{DDD}$ |
| SID63 | $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID65 | $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DDD}$ = 3.0 V |
| SID66 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | |
| SID67 | $V_{HYSTTL}$ | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DDD} \geq 2.7$ V |
| SID68 | $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.05 × $V_{DDD}$ | – | – | mV | |
| SID69 | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/Vss | – | – | 100 | µA | Guaranteed by characterization |
| SID69A | $I_{TOT_GPIO}$ | Maximum Total Source or Sink Chip Current | – | – | 200 | mA | Guaranteed by characterization |

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization)[3]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID70 | $T_{RISEF}$ | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID71 | $T_{FALLF}$ | Fall time in fast strong mode | 2 | – | 12 | ns | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID72 | $T_{RISES}$ | Rise time in slow strong mode | 10 | – | 60 | ns | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID73 | $T_{FALLS}$ | Fall time in slow strong mode | 10 | – | 60 | ns | 3.3 V $V_{DDD}$, Cload = 25 pF |
| SID74 | $F_{GPIOUT1}$ | GPIO Fout;3.3 V ≤ $V_{DDD}$ ≤ 5.5 V. Fast strong mode. | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOUT2}$ | GPIO Fout;1.7 V≤ $V_{DDD}$≤ 3.3 V. Fast strong mode. | – | – | 16.7 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOUT3}$ | GPIO Fout;3.3 V ≤ $V_{DDD}$ ≤ 5.5 V. Slow strong mode. | – | – | 7 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOUT4}$ | GPIO Fout;1.7 V ≤ $V_{DDD}$ ≤ 3.3 V. Slow strong mode. | – | – | 3.5 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | $F_{GPIOIN}$ | GPIO input operating frequency; 1.71 V ≤ $V_{DDD}$ ≤ 5.5 V | – | – | 48 | MHz | 90/10% $V_{IO}$ |

**Note**
3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

*XRES*

**Table 7. XRES DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID77 | $V_{IH}$ | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID78 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | V | CMOS Input |
| SID79 | $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | |
| SID80 | $C_{IN}$ | Input capacitance | – | 3 | – | pF | |
| SID81 | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | Guaranteed by characterization |
| SID82 | $I_{DIODE}$ | Current through protection diode to $V_{DDD}/V_{SS}$ | – | – | 100 | µA | Guaranteed by characterization |

**Table 8. XRES AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID83 | $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | µs | Guaranteed by characterization |

## Analog Peripherals

*Comparator*

**Table 9. Comparator DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID85 | $V_{OFFSET2}$ | Input offset voltage, Common Mode voltage range from 0 to $V_{DD}$-1 | – | – | ±4 | mV | |
| SID86 | $V_{HYST}$ | Hysteresis when enabled, Common Mode voltage range from 0 to $V_{DD}$ -1. | – | 10 | 35 | mV | Guaranteed by characterization |
| SID87 | $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$ – 0.1 | V | Modes 1 and 2. |
| SID247 | $V_{ICM2}$ | Input common mode voltage in low-power mode | 0 | – | $V_{DDD}$ | V | |
| SID88 | CMRR | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD} \geq 2.7$ V. Guaranteed by characterization |
| SID88A | CMRR | Common mode rejection ratio | 42 | – | – | dB | $V_{DDD} < 2.7$ V. Guaranteed by characterization |
| SID89 | $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | Guaranteed by characterization |
| SID248 | $I_{CMP2}$ | Block current, low power mode | – | – | 100 | µA | Guaranteed by characterization |
| SID90 | $Z_{CMP}$ | DC input impedance of comparator | 35 | – | – | MΩ | Guaranteed by characterization |

**Table 10. Comparator AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID91 | $T_{RESP1}$ | Response time, normal mode | – | – | 110 | ns | 50-mV overdrive |
| SID258 | $T_{RESP2}$ | Response time, low power mode | – | – | 200 | ns | 50-mV overdrive |

## Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

*Timer/Counter/PWM*

**Table 11. TCPWM Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | – | – | 45 | µA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 12 MHz | – | – | 155 | µA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 48 MHz | – | – | 650 | µA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.3 | TCPWMFREQ | Operating frequency | – | – | Fc | MHz | Fc max = Fcpu. Maximum = 48 MHz |
| SID.TCPWM.4 | TPWMENEXT | Input Trigger Pulse Width for all Trigger Events | 2/Fc | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. |
| SID.TCPWM.5 | TPWMEXT | Output Trigger Pulse widths | 2/Fc | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs |
| SID.TCPWM.5A | TCRES | Resolution of Counter | 1/Fc | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWMRES | PWM Resolution | 1/Fc | – | – | ns | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | QRES | Quadrature inputs resolution | 1/Fc | – | – | ns | Minimum pulse width between Quadrature phase inputs. |

*$I^2C$*

**Table 12. Fixed $I^2C$ DC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID149 | $I_{I2C1}$ | Block current consumption at 100 kHz | – | – | 50 | µA | |
| SID150 | $I_{I2C2}$ | Block current consumption at 400 kHz | – | – | 135 | µA | |
| SID151 | $I_{I2C3}$ | Block current consumption at 1 Mbps | – | – | 310 | µA | |
| SID152 | $I_{I2C4}$ | $I^2C$ enabled in Deep Sleep mode | – | – | 1.4 | µA | |

**Table 13. Fixed $I^2C$ AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID153 | $F_{I2C1}$ | Bit rate | – | – | 1 | Mbps | |

**Table 14. Fixed UART DC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID160 | $I_{UART1}$ | Block current consumption at 100 Kbits/sec | – | – | 55 | µA | |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 Kbits/sec | – | – | 312 | µA | |

**Table 15. Fixed UART AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | |

*SPI Specifications*

**Table 16. Fixed SPI DC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID163 | $I_{SPI1}$ | Block current consumption at 1 Mbits/sec | – | – | 360 | µA | |
| SID164 | $I_{SPI2}$ | Block current consumption at 4 Mbits/sec | – | – | 560 | µA | |
| SID165 | $I_{SPI3}$ | Block current consumption at 8 Mbits/sec | – | – | 600 | µA | |

**Table 17. Fixed SPI AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID166 | $F_{SPI}$ | SPI operating frequency (master; 6X oversampling) | – | – | 8 | MHz | |

**Table 18. Fixed SPI Master mode AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SID167 | $T_{DMO}$ | MOSI valid after Sclock driving edge | – | – | 15 | ns |
| SID168 | $T_{DSI}$ | MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used | 20 | – | – | ns |
| SID169 | $T_{HMO}$ | Previous MOSI data hold time with respect to capturing edge at Slave | 0 | – | – | ns |

**Table 19. Fixed SPI Slave mode AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SID170 | $T_{DMI}$ | MOSI valid before Sclock capturing edge | 40 | – | – | ns |
| SID171 | $T_{DSO}$ | MISO valid after Sclock driving edge | – | – | 42 + 3 × (1/FCPU) | ns |
| SID171A | $T_{DSO_ext}$ | MISO valid after Sclock driving edge in Ext. Clock mode | – | – | 48 | ns |
| SID172 | $T_{HSO}$ | Previous MISO data hold time | 0 | – | – | ns |
| SID172A | $T_{SSELSCK}$ | SSEL Valid to first SCK Valid edge | 100 | – | – | ns |

## Memory

**Table 20. Flash DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID173 | $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | |

**Table 21. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID174 | $T_{ROWWRITE}$ | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 256 bytes |
| SID175 | $T_{ROWERASE}$ | Row erase time | – | – | 13 | ms | |
| SID176 | $T_{ROWPROGRAM}$ | Row program time after erase | – | – | 7 | ms | |
| SID178 | $T_{BULKERASE}$ | Bulk erase time (64 KB) | – | – | 35 | ms | |
| SID180 | $T_{DEVPROG}$ | Total device program time | – | – | 15 | seconds | Guaranteed by characterization |
| SID181 | $F_{END}$ | Flash endurance | 100 K | – | – | cycles | Guaranteed by characterization |
| SID182 | $F_{RET}$ | Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles | 20 | – | – | years | Guaranteed by characterization |
| SID182A | | Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles | 10 | – | – | years | Guaranteed by characterization |

## System Resources

*Power-on-Reset and Brown-out Detect (BOD) Specifications*

**Table 22. Power On Reset**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up |
| SID185 | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.45 | V | Guaranteed by characterization |
| SID186 | $V_{FALLIPOR}$ | Falling trip voltage | 0.75 | – | 1.4 | V | Guaranteed by characterization |
| BID51 | Twupo | Initialization after Power-On | – | – | 3 | ms | |

**Table 23. Brown-out Detect (BOD) for $V_{CCD}$**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID190 | $V_{FALLPPOR}$ | BOD trip voltage in active and sleep modes | 1.48 | - | 1.62 | V | Guaranteed by characterization |
| SID192 | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.11 | - | 1.5 | V | Guaranteed by characterization |

*SWD Interface*

**Table 24. SWD Interface Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID213 | F_SWDCLK1 | $3.3\ V \le V_{DD} \le 5.5\ V$ | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID214 | F_SWDCLK2 | $1.71\ V \le V_{DD} \le 3.3\ V$ | – | – | 7 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID215 | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25*T | – | – | ns | Guaranteed by characterization |
| SID216 | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25*T | – | – | ns | Guaranteed by characterization |
| SID217 | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5*T | ns | Guaranteed by characterization |
| SID217A | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | ns | Guaranteed by characterization |

*Internal Main Oscillator*

**Table 25. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID218 | $I_{IMO1}$ | IMO operating current at 48 MHz | – | – | 250 | µA | |
| SID219 | $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 180 | µA | |

**Table 26. IMO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation | – | – | ±2 | % | |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 7 | µs | |
| SID228 | $T_{JITRMSIMO2}$ | RMS Jitter at 24 MHz | – | 145 | – | ps | |

*Internal Low-Speed Oscillator*

**Table 27. ILO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID231 | $I_{ILO1}$ | ILO operating current | – | 0.3 | 1.05 | µA | Guaranteed by Characterization |

**Table 28. ILO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID234 | $T_{STARTILO1}$ | ILO startup time | – | – | 2 | ms | Guaranteed by characterization |
| SID236 | $T_{ILODUTY}$ | ILO duty cycle | 40 | 50 | 60 | % | Guaranteed by characterization |
| SID237 | $F_{ILOTRIM1}$ | Operating frequency | 20 | 40 | 80 | kHz | |

**Table 29. External Clock Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID305 | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | Guaranteed by characterization |
| SID306 | ExtClkDuty | Duty cycle; Measured at $V_{DD/2}$ | 45 | – | 55 | % | Guaranteed by characterization |

**Table 30. UDB AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| **Datapath performance** | | | | | | | |
| SID249 | $F_{MAX-TIMER}$ | Max frequency of 16-bit timer in a UDB pair | – | – | 48 | MHz | |
| SID250 | $F_{MAX-ADDER}$ | Max frequency of 16-bit adder in a UDB pair | – | – | 48 | MHz | |
| SID251 | $F_{MAX_CRC}$ | Max frequency of 16-bit CRC/PRS in a UDB pair | – | – | 48 | MHz | |
| **PLD Performance in UDB** | | | | | | | |
| SID252 | $F_{MAX_PLD}$ | Max frequency of 2-pass PLD function in a UDB pair | – | – | 48 | MHz | |
| **Clock to Output Performance** | | | | | | | |
| SID253 | $T_{CLK_OUT_UDB1}$ | Prop. delay for clock in to data out at 25 °C, Typ. | – | 15 | – | ns | |
| SID254 | $T_{CLK_OUT_UDB2}$ | Prop. delay for clock in to data out, Worst case. | – | 25 | – | ns | |

**Table 31. Block Specs**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID256* | $T_{WS48}$* | Number of wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | $T_{WS24}$* | Number of wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |
| * Tws48 and Tws24 are guaranteed by Design | | | | | | | |

## Ordering Information

The PSoC 4200D family part numbers and features are listed in the following table.

**Table 32. PSoC 4200D Ordering Information**

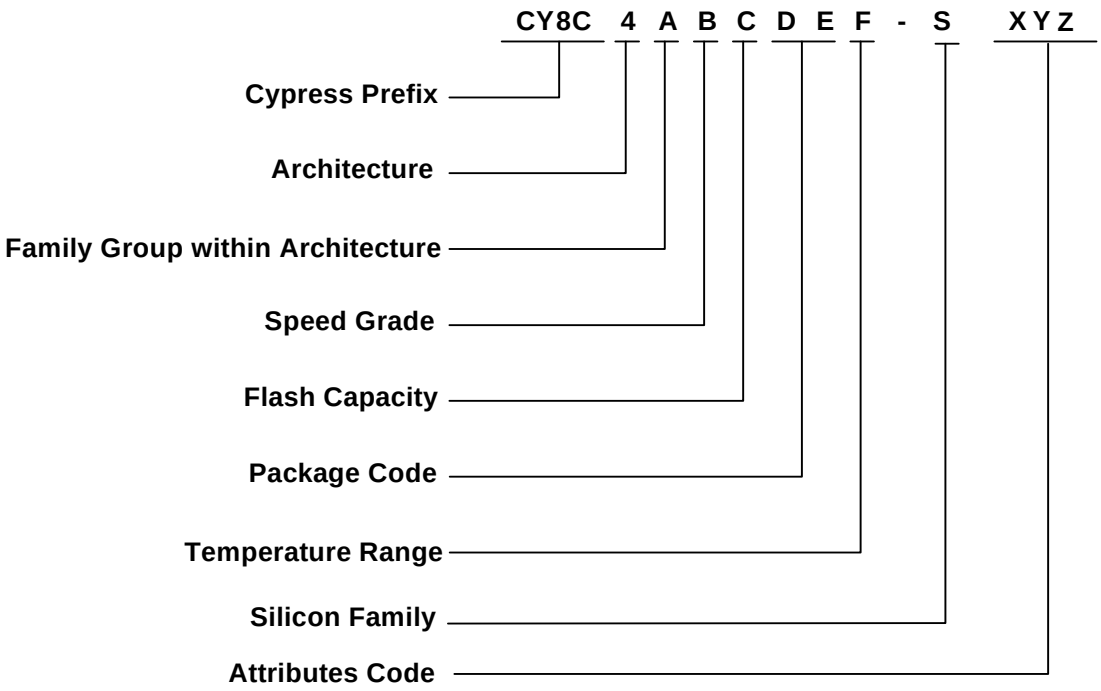
| Category | Marketing Part Number (MPN) | MAX. CPU Speed (MHz) | No. of DMA Channels | Flash (KB) | SRAM (KB) | Low-power Comparators | No. of Universal Digital Blocks (UDB) | Timer/Counter/PWM Blocks (TCPWM) | No. of Serial Communication Blocks (SCB) | PRGIO | No. of GPIOs | Package Type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4045 | CY8C4045PVI-DS402 | 48 | 8 | 32 | 4 | 2 | - | 4 | 3 | 1 | 21 | 28-pin SSOP |
| | CY8C4045FNI-DS402 | 48 | 8 | 32 | 4 | 2 | - | 4 | 3 | 1 | 21 | 25-ball WLCSP |
| 4245 | CY8C4245PVI-DS402 | 48 | 8 | 32 | 4 | 2 | 4 | 4 | 3 | 1 | 21 | 28-pin SSOP |
| | CY8C4245FNI-DS402 | 48 | 8 | 32 | 4 | 2 | 4 | 4 | 3 | 1 | 21 | 25-ball WLCSP |
| 4246 | CY8C4246PVI-DS402 | 48 | 8 | 64 | 8 | 2 | 4 | 4 | 3 | 1 | 21 | 28-pin SSOP |
| | CY8C4246FNI-DS402 | 48 | 8 | 64 | 8 | 2 | 4 | 4 | 3 | 1 | 21 | 25-ball WLCSP |

The nomenclature used in the preceding table is based on the following part numbering convention:

| Field | Description | Values | Meaning |
|---|---|---|---|
| CY8C | Cypress Prefix | | |
| 4 | Architecture | 4 | PSoC 4 |
| A | Family | 2 | 4200 Family |
| B | CPU Speed | 4 | 48 MHz |
| C | Flash Capacity | 5 | 32 KB |
| | | 6 | 64 KB |
| DE | Package Code | PV | SSOP |
| | | FN | CSP |
| F | Temperature Range | I | Industrial |
| S | Silicon Family | D | PSoC 4D |
| XYZ | Attributes Code | 000-999 | Code of feature set in the specific family |

### Part Numbering Conventions

The part number fields are defined as follows.



## Packaging

The description of the PSoC 4200D package dimensions follows.

| Spec Id# | Package | Description | Package Dwg # |
|---|---|---|---|
| PKG_1 | 28-pin SSOP | 28-pin SSOP, 8 mm × 10 mm × 2.0 mm height with 0.65-mm pitch | 51-85079 |
| PKG_2 | 25-ball CSP | 25-ball CSP, 2.07 mm × 2.11 mm × 0.55 mm height with 0.4-mm pitch | 001-97945 |

**Table 33. Package Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ (28-pin SSOP) | | – | 67 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (28-pin SSOP) | | – | 26 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (25-ball CSP) | | – | 48 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (25-ball CSP) | | – | 0.47 | – | °C/Watt |

**Table 34. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| All packages | 260 °C | 30 seconds |

**Table 35. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 28-SSOP | MSL 3 |
| 25-ball CSP | MSL 1 |

**Figure 5. 28-Pin SSOP Package Outline**

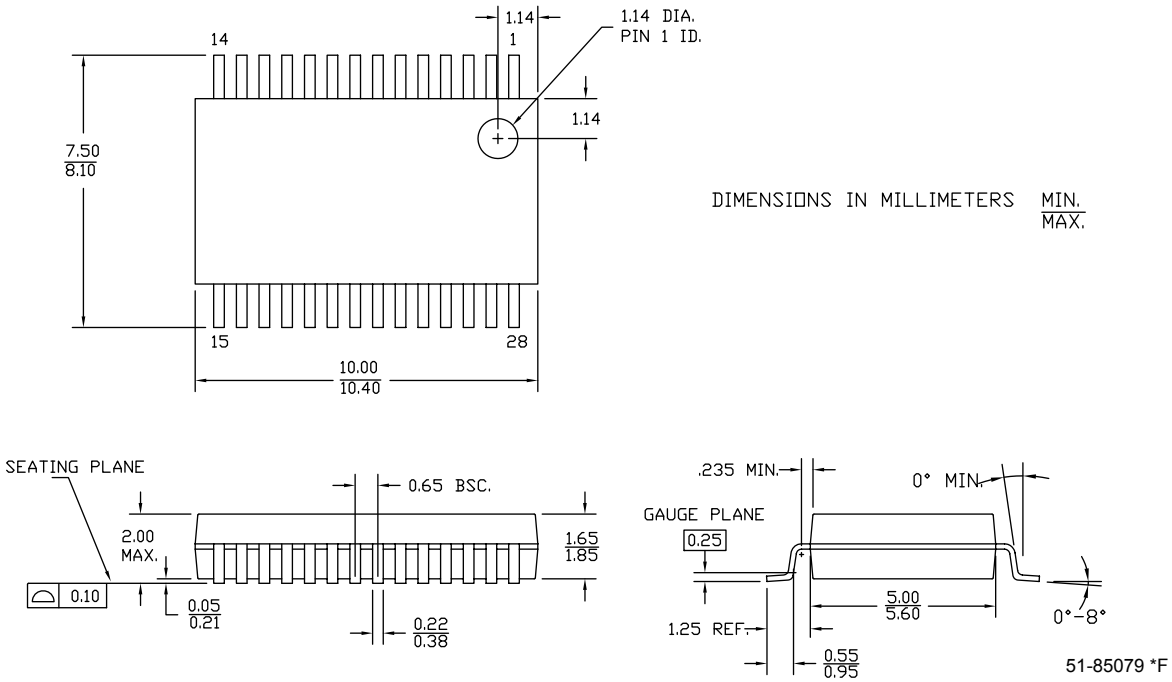
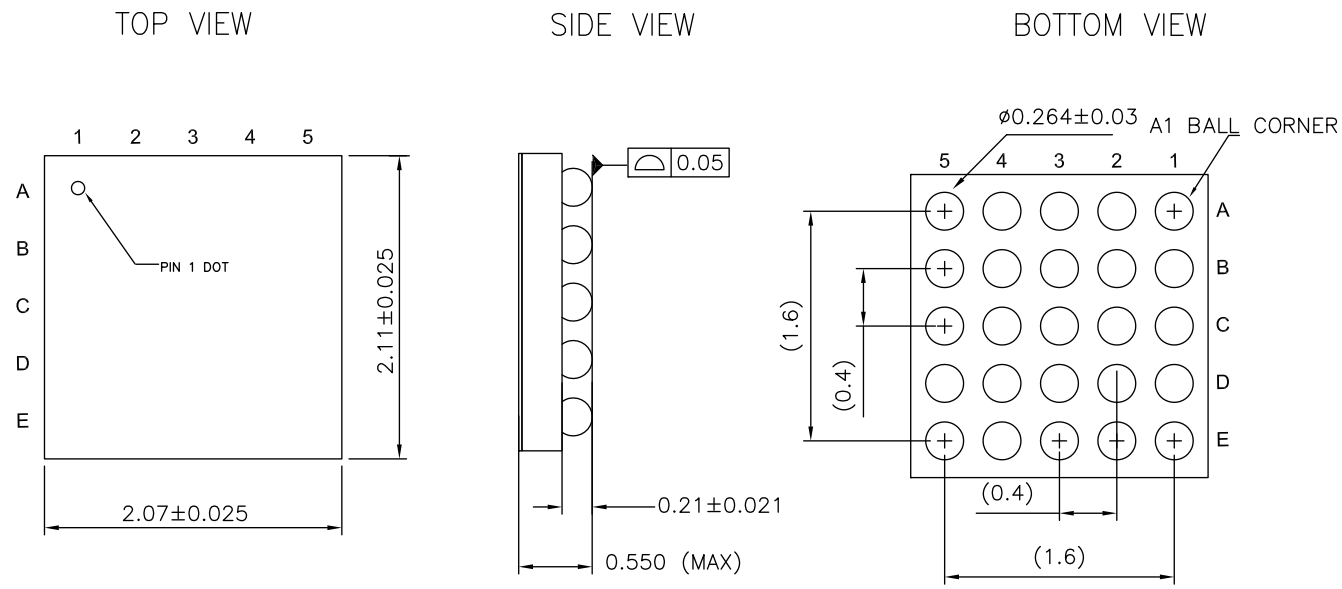



**Figure 6. 25-ball CSP 2.07 × 2.11 × 0.55 mm**




Note: 1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETER

001-97945 **

## Acronyms

**Table 36. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

**Table 36. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |

**Table 36. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |

**Table 36. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

## Document Conventions

### Units of Measure

**Table 37. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Revision History

| Description Title: PSoC® 4: PSoC 4200D Family Datasheet Programmable System-on-Chip (PSoC®)<br>Document Number: 001-98044 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 4795389 | WKA | 06/23/2015 | New datasheet |
| *A | 4931127 | WKA | 09/23/2015 | Removed 28-pin SSOP package.<br>Updated Pinouts.<br>Updated DC Specifications.<br>Removed SID85A, SID247A, SID259, and SID92.<br>Added BID51. |
| *B | 4958966 | WKA | 10/12/2015 | Updated package dimensions.<br>Updated bulk erase time to 64 KB.<br>Changed SID226 max to 7.<br>Updated $T_{JA}$ typ to 48 and $T_{JC}$ typ to 0.47. |
| *C | 5759255 | WKA | 05/31/2017 | Added 28-pin SSOP package.<br>Updated Cypress logo, copyright notice, and Sales, Solutions, and Legal Information based on the template. |

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