

Low-Power, 1.62V to 3.63V, 1MHz to 150MHz, 1:3 Fanout Buffer IC

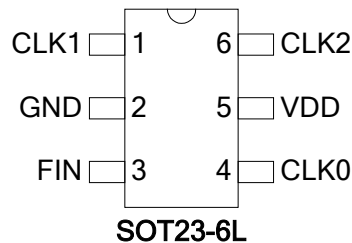
FEATURES

- 3 LVCMOS Outputs
- 12mA Output Drive Strength
- Input/Output Frequency:
 - Reference Clock: 1MHz to 150MHz
- Supports LVCMOS or Sine Wave Input Clock
- Very Low Jitter and Phase Noise
- Low Current Consumption
- Single 1.8V, 2.5V, or 3.3V, $\pm 10\%$ Power Supply
- Operating Temperature Range
 - 0°C to 70°C (Commercial)
 - -40°C to 85°C (Industrial)
- Available in SOT23-6L GREEN/RoHS Compliant Packages

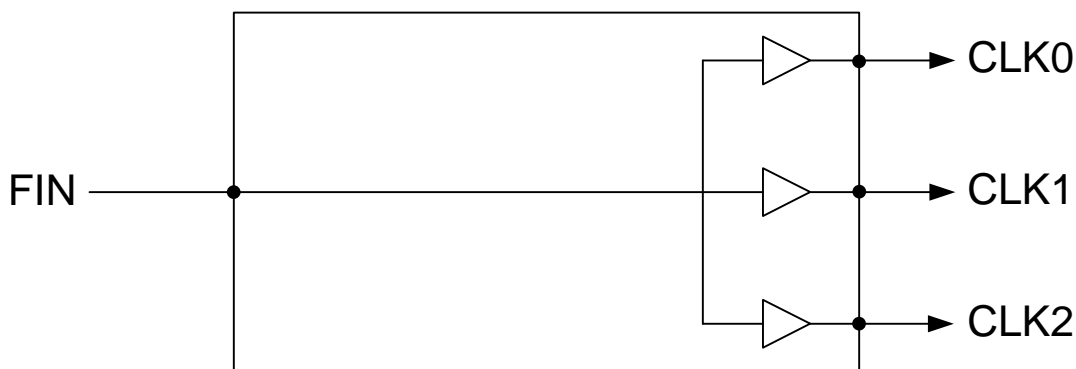
DESCRIPTION

The PL133-37 is an advanced fanout buffer design for high performance, low-power, small form-factor applications. The PL133-37 accepts a reference clock input of 1MHz to 150MHz and produces three outputs of the same frequency. Reference clock inputs may be LVCMOS or sine-wave signals (the inputs are internally AC-coupled). Offered in a small 3mm x 3mm SOT23, the PL133-37 offers the best phase noise and jitter performance and lowest power consumption of any comparable IC.

PACKAGE PIN CONFIGURATION



BLOCK DIAGRAM



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PIN DESCRIPTION

| Name | Package Pin # | Type | Description |
|------|---------------|------|-----------------------|
| | SOT23-6L | | |
| CLK1 | 1 | O | Output clock |
| GND | 2 | P | Ground connection |
| FIN | 3 | I | Reference clock input |
| CLK0 | 4 | O | Output clock |
| VDD | 5 | P | Power supply |
| CLK2 | 6 | O | Output clock |

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

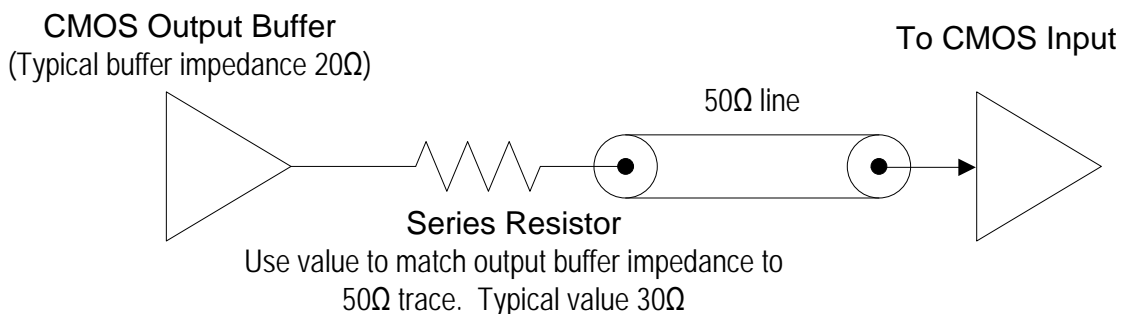
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as "striplines" or "microstrips" with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply
- Multiple V_{DD} pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical value to use is $0.1\mu F$.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



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ELECTRICAL SPECIFICATIONS
ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|--------------------------------|----------|------|--------------|-------|
| Supply Voltage Range | V_{DD} | -0.5 | 4.6 | V |
| Input Voltage Range | V_I | -0.5 | $V_{DD}+0.5$ | V |
| Output Voltage Range | V_O | -0.5 | $V_{DD}+0.5$ | V |
| Storage Temperature | T_S | -65 | 150 | °C |
| Ambient Operating Temperature* | | -40 | 85 | °C |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------|-----------------------------------------------------------------------------------|------|------|----------|----------|
| Input (FIN) Frequency | 2.5V and 3.3V operation | 1 | | 150 | MHz |
| | 1.8V operation | 1 | | 100 | MHz |
| Input (FIN) Signal Amplitude | Internally AC coupled, ≤ 150 MHz, $V_{DD}=2.5$ V and 3.3V. | 0.8 | | V_{DD} | V_{PP} |
| | Internally AC coupled, ≤ 100 MHz, all VDDs | 0.5 | | V_{DD} | V_{PP} |
| | Internally AC coupled, 3.3V ≤ 50 MHz, 2.5V ≤ 40 MHz, 1.8V ≤ 15 MHz | 0.1 | | V_{DD} | V_{PP} |
| Output Enable Time | OE Function; $T_a=25^\circ$ C, 15pF Load | | | 10 | ns |
| Output Rise Time | 15pF Load, 10/90% V_{DD} , 3.3V | | 2 | 3 | ns |
| Output Fall Time | 15pF Load, 90/10% V_{DD} , 3.3V | | 2 | 3 | ns |
| Duty Cycle | Input Duty Cycle is 50% | 45 | 50 | 55 | % |
| Output to Output Skew | All outputs equally loaded | | | 250 | ps |

DC SPECIFICATIONS

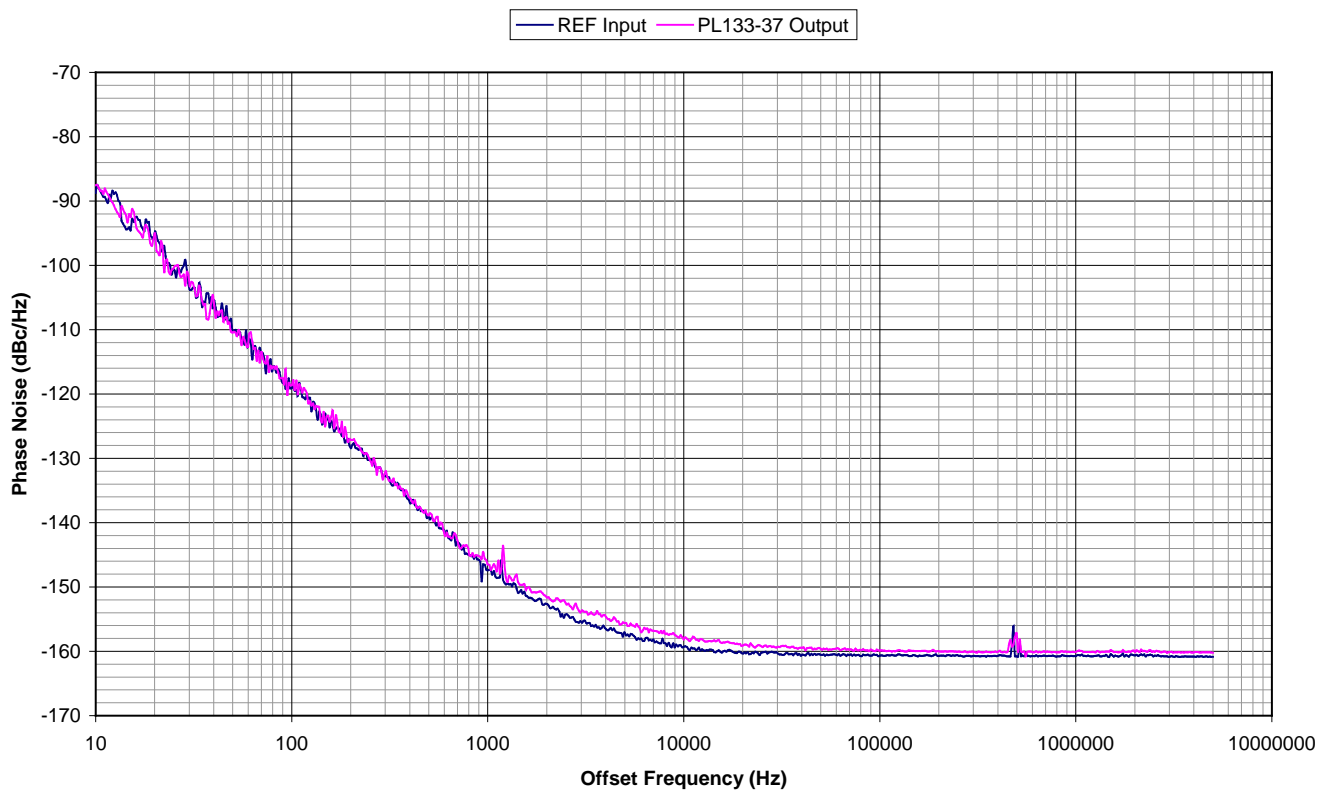
| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|--------------|------------------------------------------------------|------|-----|------|-------|
| Supply Current, Dynamic | I_{DD} | $V_{DD} = 3.3$ V, 25MHz, No Load | | 1.2 | | mA |
| | | $V_{DD} = 2.5$ V, 25MHz, No Load | | 0.9 | | mA |
| | | $V_{DD} = 1.8$ V, 25MHz, No Load | | 0.6 | | mA |
| Supply Current, Standby | I_{DD_SB} | OE Pin Pulled Low, $V_{DD} = 3.3$ V | | 0.3 | | mA |
| Operating Voltage | V_{DD} | | 1.62 | | 3.63 | V |
| Output Low Voltage | V_{OL} | $I_{OL} = +12$ mA, $V_{DD} = 3.3$ V | | | 0.4 | V |
| Output High Voltage | V_{OH} | $I_{OH} = -12$ mA, $V_{DD} = 3.3$ V | 2.4 | | | V |
| Output Current | I_{OSD} | $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V, $V_{DD} = 3.3$ V | 12 | | | mA |

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NOISE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------|-----------------------------------------------------------------|-----|-----|-----|------|
| Additive Phase Jitter | | V _{DD} =3.3V, Frequency=26MHz Offset=12kHz ~ 5MHz | | 70 | | fs |
| | | V _{DD} =3.3V, Frequency=100MHz Offset=12kHz ~ 20MHz | | 80 | | fs |

PL133-37 Additive Phase Jitter:
V_{DD}=3.3V, CLK=26MHz, Integration Range 12KHz to 5MHz: 0.072ps typical.



When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

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