## FEATURES

- No write delays
- Unlimited write endurance
- Data retention greater than 20 years
- Automatic data protection on power loss
- Block write protection
- Fast, simple SPI interface with up to 40 MHz clock rate
- 2.7 to 3.6 Volt power supply range
- Low current sleep mode
- Industrial and Automotive temperatures
- Available in 8-pin DFN Small Flag RoHS-compliant package.
- Direct replacement for serial EEPROM, Flash, FeRAM
- Industrial Grade and AEC-Q100 Grade 1 and Grade 3 options
- Moisture Sensitivity MSL-3

Small Flag DFN

## INTRODUCTION

The **MR25H128A** is a 128Kbit magnetoresistive random access memory (MRAM) device organized as 16,384 words of 8 bits. The **MR25H128A** offers serial EEPROM and serial Flash compatible read/write timing with no write delays and unlimited read/write endurance.

Unlike other serial memories, both reads and writes can occur randomly in memory with no delay between writes. The **MR25H128A** is the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of I/O pins.

The **MR25H128A** is available in a 5 mm x 6 mm 8-pin DFN Small Flag package compatible with serial EEPROM, Flash, and FeRAM products.

The **MR25H128A** provides highly reliable data storage over a wide range of temperatures. The product is offered with industrial (-40° to +85 °C) and AEC-Q100 Grade 1 (-40°C to +125 °C) and AEC-Q100 Grade 3 (-40° to +85 °C) operating temperature range options.

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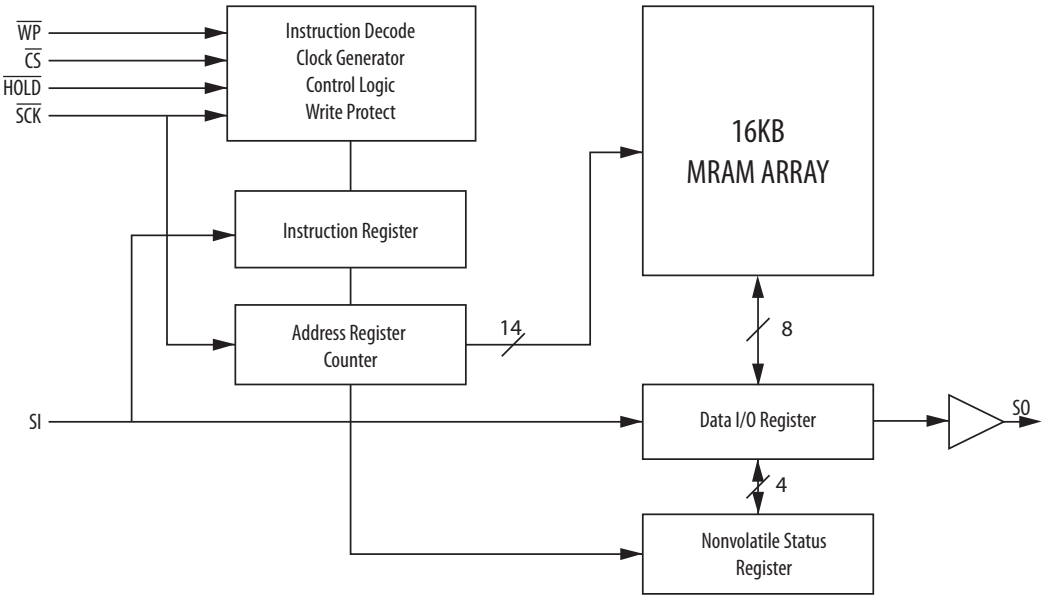
## 1. DEVICE PIN ASSIGNMENT

### Overview

The MR25H128A is a serial MRAM with memory array logically organized as 16Kx8 using the four pin interface of chip select (CS), serial input (SI), serial output (SO) and serial clock (SCK) of the serial peripheral interface (SPI) bus. Serial MRAM implements a subset of commands common to today's SPI EEPROM and Flash components allowing MRAM to replace these components in the same socket and interoperate on a shared SPI bus. Serial MRAM offers superior write speed, unlimited endurance, low standby & operating power, and more reliable data retention compared to available serial memory alternatives.

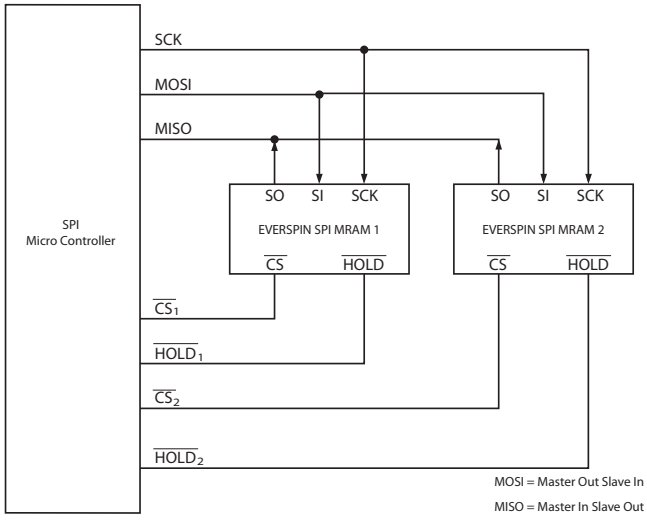
**Figure 1.1 Block Diagram**




### System Configuration

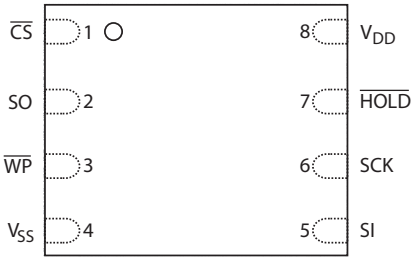
Single or multiple devices can be connected to the bus as shown in Figure 1.2. Pins SCK, SO and SI are common among devices. Each device requires $\overline{CS}$ and $\overline{HOLD}$ pins to be driven separately.

**Figure 1.2 System Configuration**



*DEVICE PIN ASSIGNMENT*

**Figure 1.3 Pin Diagrams (Top View)**




**8-Pin DFN Small Flag Package**

**Table 1.1 Pin Functions**

| Signal Name | Pin | I/O | Function | Description |
|---|---|---|---|---|
| $\overline{CS}$ | 1 | Input | Chip Select | An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory. |
| SO | 2 | Output | Serial Output | The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when $\overline{HOLD}$ is low. Data transitions on the data output occur on the falling edge of SCK. |
| $\overline{WP}$ | 3 | Input | Write Protect | A low on the write protect input prevents write operations to the Status Register. |
| $V_{SS}$ | 4 | Supply | Ground | Power supply ground pin. |
| SI | 5 | Input | Serial Input | All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired. |
| SCK | 6 | Input | Serial Clock | Synchronizes the operation of the MRAM. The clock can operate up to 40 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time. |
| $\overline{HOLD}$ | 7 | Input | Hold | A low on the Hold pin interrupts a memory operation for another task. When $\overline{HOLD}$ is low, the current operation is suspended. The device will ignore transitions on the $\overline{CS}$ and SCK when $\overline{HOLD}$ is low. All transitions of $\overline{HOLD}$ must occur while $\overline{CS}$ is low. |
| $V_{DD}$ | 8 | Supply | Power Supply | Power supply voltage from +2.7 to +3.6 volts. |

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## 2. SPI COMMUNICATIONS PROTOCOL

MR25H128A can be operated in either SPI Mode 0 (CPOL=0, CPHA =0) or SPI Mode 3 (CPOL=1, CPHA=1). For both modes, inputs are captured on the rising edge of the clock and data outputs occur on the falling edge of the clock. When not conveying data, SCK remains low for Mode 0; while in Mode 3, SCK is high. The memory determines the mode of operation (Mode 0 or Mode 3) based upon the state of the SCK when $\overline{CS}$ falls.

All memory transactions start when $\overline{CS}$ is brought low to the memory. The first byte is a command code. Depending upon the command, subsequent bytes of address are input. Data is either input or output. There is only one command performed per $\overline{CS}$ active period. $\overline{CS}$ must go inactive before another command can be accepted. To ensure proper part operation according to specifications, it is necessary to terminate each access by raising $\overline{CS}$ at the end of a byte (a multiple of 8 clock cycles from $\overline{CS}$ dropping) to avoid partial or aborted accesses.

**Table 2.1 Command Codes**

| Instruction | Description | Binary Code | Hex Code | Address Bytes | Data Bytes |
|---|---|---|---|---|---|
| WREN | Write Enable | 0000 0110 | 06h | 0 | 0 |
| WRDI | Write Disable | 0000 0100 | 04h | 0 | 0 |
| RDSR | Read Status Register | 0000 0101 | 05h | 0 | 1 |
| WRSR | Write Status Register | 0000 0001 | 01h | 0 | 1 |
| READ | Read Data Bytes | 0000 0011 | 03h | 2 | 1 to ∞ |
| WRITE | Write Data Bytes | 0000 0010 | 02h | 2 | 1 to ∞ |
| SLEEP | Enter Sleep Mode | 1011 1001 | B9h | 0 | 0 |
| WAKE | Exit Sleep Mode | 1010 1011 | ABh | 0 | 0 |

### Status Register and Block Write Protection

The status register consists of the 8 bits listed in table 2.2. Status register bits BP0 and BP1 define the memory block arrays that are protected as described in table 2.3. The Status Register Write Disable bit (SRWD) is used in conjunction with bit 1 (WEL) and the Write Protection pin ($\overline{WP}$) as shown in table 2.4 to enable writes to status register bits. The fast writing speed of MR25H128A does not require write status bits. The state of bits 6,5,4, and 0 can be user modified and do not affect memory operation. All bits in the status register are pre-set from the factory to the "0" state.

**Table 2.2 Status Register Bit Assignments**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| SRWD | Don't Care | Don't Care | Don't Care | BP1 | BP0 | WEL | Don't Care |

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**Table 2.3 Block Memory Write Protection**

| Status Register | | Memory Contents | |
|---|---|---|---|
| **BP1** | **BP0** | **Protected Area** | **Unprotected Area** |
| 0 | 0 | None | All Memory |
| 0 | 1 | Upper Quarter | Lower Three-Quarters |
| 1 | 0 | Upper Half | Lower Half |
| 1 | 1 | All | None |

**Table 2.4 Memory Protection Modes**

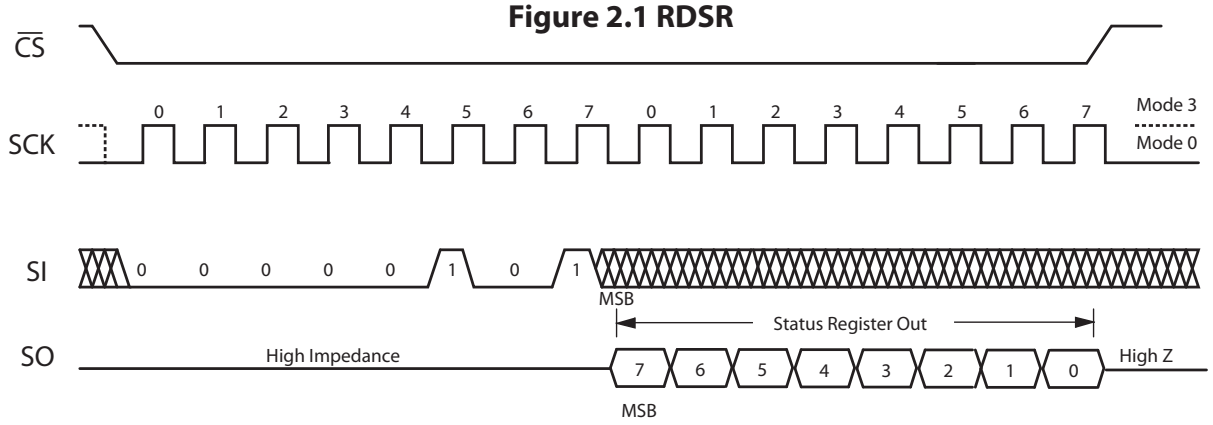
| WEL | SRWD | $\overline{WP}$ | Protected Blocks | Unprotected Blocks | Status Register |
|---|---|---|---|---|---|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Protected | Writable | Writable |
| 1 | 1 | Low | Protected | Writable | Protected |
| 1 | 1 | High | Protected | Writable | Writable |

When WEL is reset to 0, writes to all blocks and the status register are protected. When WEL is set to 1, BP0 and BP1 determine which memory blocks are protected. While SRWD is reset to 0 and WEL is set to 1, status register bits BP0 and BP1 can be modified. Once SRWD is set to 1, $\overline{WP}$ must be high to modify SRWD, BP0 and BP1.

### Read Status Register (RDSR)

The Read Status Register (RDSR) command allows the Status Register to be read. The Status Register can be read at any time to check the status of write enable latch bit, status register write protect bit, and block write protect bits. For MR25H128A, the write in progress bit (bit 0) is not written by the memory because there is no write delay. The RDSR command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

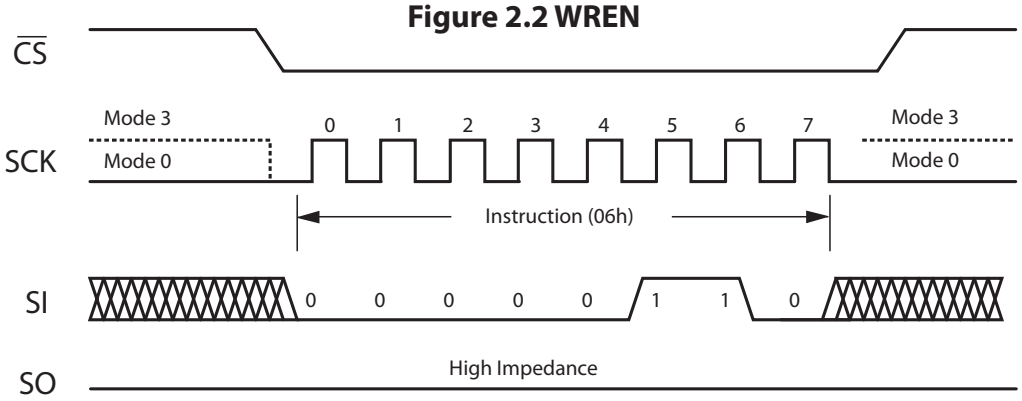
**Figure 2.1 RDSR**



### Write Enable (WREN)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit in the status register to 1. The WEL bit must be set prior to writing in the status register or the memory. The WREN command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

**Figure 2.2 WREN**

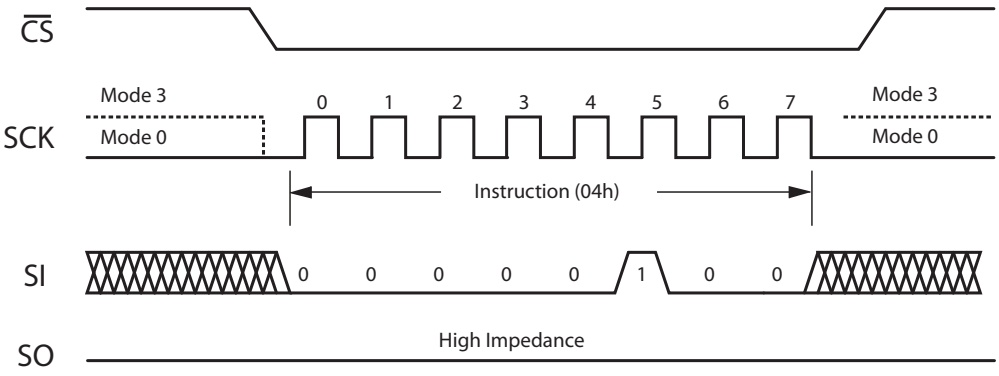



### Write Disable (WRDI)

The Write Disable (WRDI) command resets the WEL bit in the status register to 0. This prevents writes to status register or memory. The WRDI command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

The WEL bit is reset to 0 on power-up or completion of WRDI.

**Figure 2.3 WRDI**




### Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. The WRSR command is not executed unless the Write Enable Latch (WEL) has been set to 1 by executing a WREN command while pin $\overline{WP}$ and bit SRWD correspond to values that make the status register writable as seen in table 2.4. Status Register bits are non-volatile with the exception of the WEL which is reset to 0 upon power cycling.

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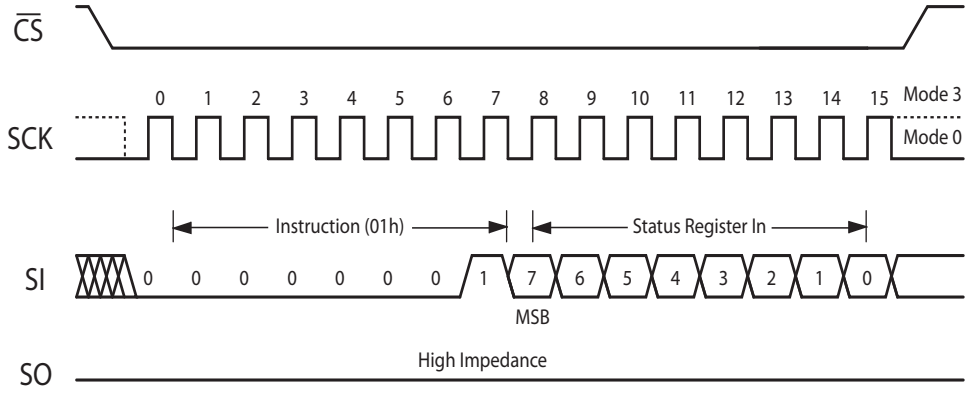
The WRSR command is entered by driving $\overline{CS}$ low, sending the command code and status register write data byte, and then driving $\overline{CS}$ high.

**Figure 2.4 WRSR**

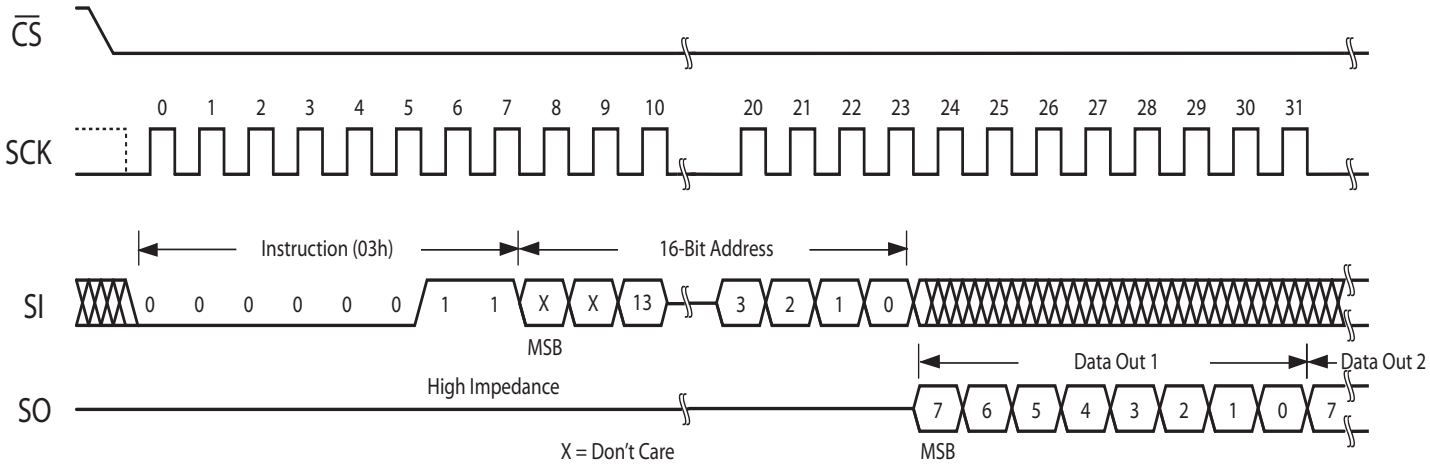



**Read Data Bytes (READ)**

The Read Data Bytes (READ) command allows data bytes to be read starting at an address specified by the 16-bit address. Only address bits 0-13 are decoded by the memory. The data bytes are read out sequentially from memory until the read operation is terminated by bringing $\overline{CS}$ high The entire memory can be read in a single command. The address counter will roll over to 0000h when the address reaches the top of memory.

The READ command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. The command is terminated by bring $\overline{CS}$ high.

**Figure 2.5 READ**



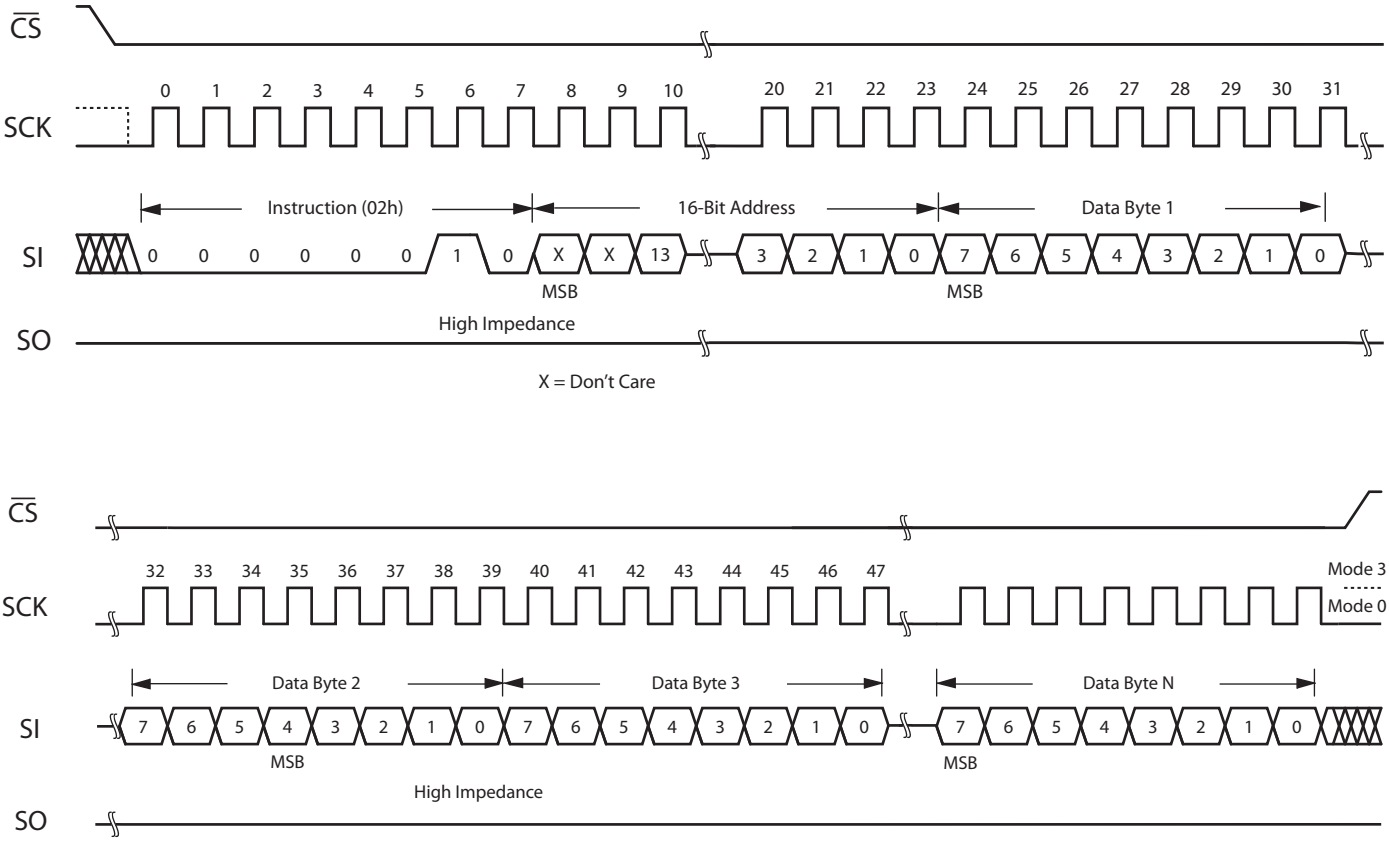
**Write Data Bytes (WRITE)**

The Write Data Bytes (WRITE) command allows data bytes to be written starting at an address specified by the 16-bit address. Only address bits 0-13 are decoded by the memory. The data bytes are written sequentially in memory until the write operation is terminated by bringing $\overline{CS}$ high. The entire memory can be written in a single command. The address counter will roll over to 0000h when the address reaches the top of memory.

Unlike EEPROM or Flash Memory, MRAM can write data bytes continuously at its maximum rated clock speed without write delays or data polling. Back to back WRITE commands to any random location in memory can be executed without write delay. MRAM is a random access memory rather than a page, sector, or block organized memory making it ideal for both program and data storage.

The WRITE command is entered by driving $\overline{CS}$ low, sending the command code, and then sequential write data bytes. Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

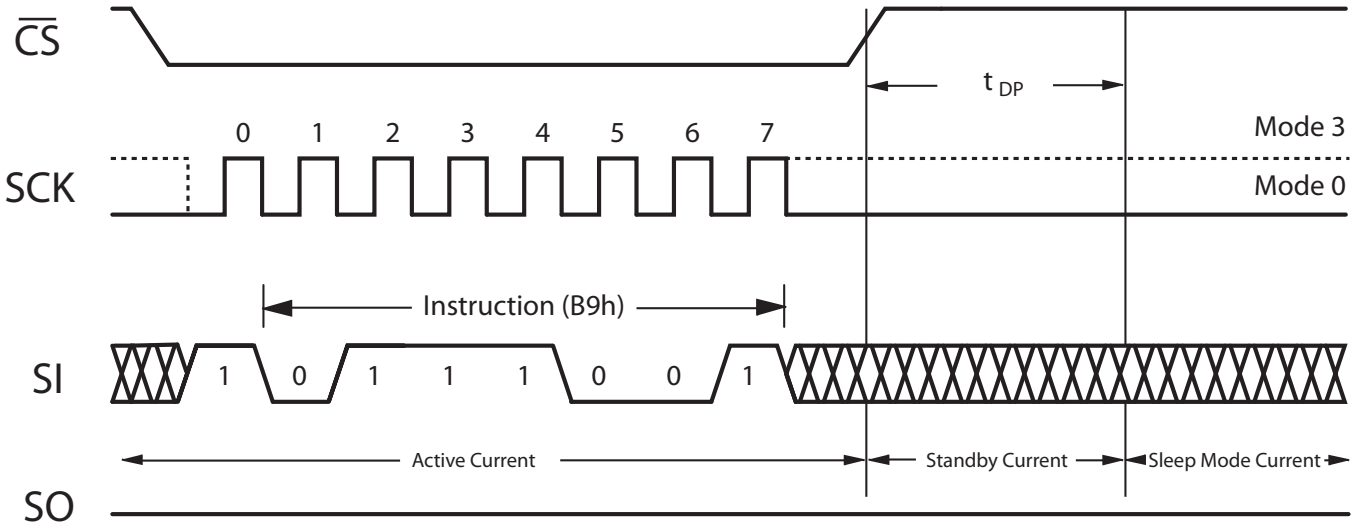
**Figure 2.6 WRITE**



**Enter Sleep Mode (SLEEP)**

The Enter Sleep Mode (SLEEP) command turns off all MRAM power regulators in order to reduce the overall chip standby power to 3 µA typical. The SLEEP command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The standby current is achieved after time, $t_{DP}$. If power is removed when the part is in sleep mode, upon power restoration, the part enters normal standby. The only valid command following SLEEP mode entry is a WAKE command.

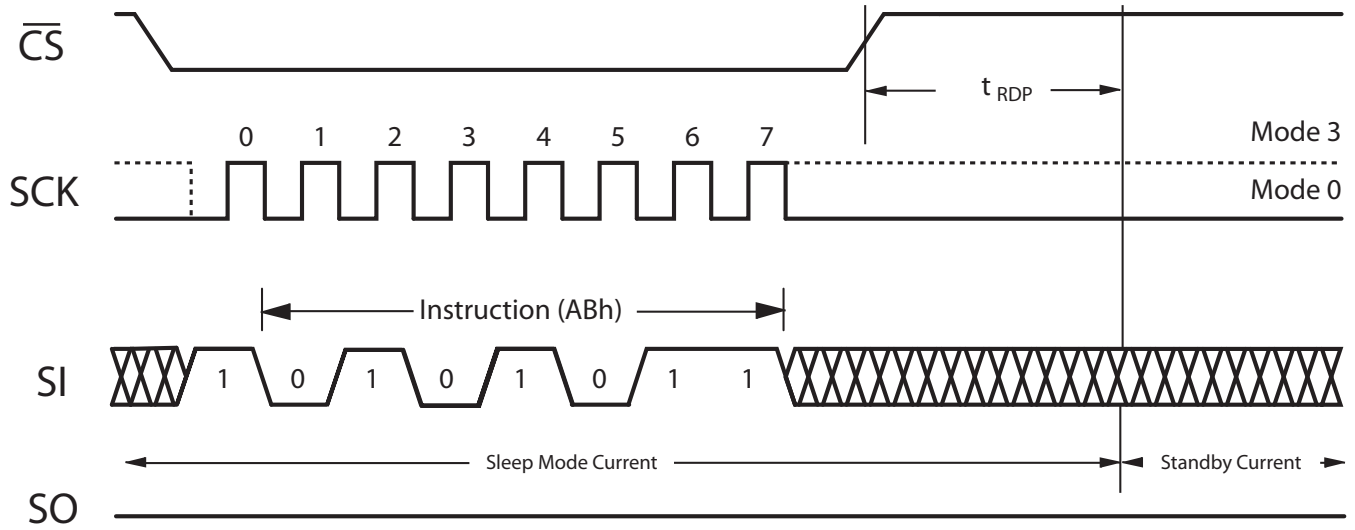
**Figure 2.7 SLEEP**




**Exit Sleep Mode (WAKE)**

The Exit Sleep Mode (WAKE) command turns on internal MRAM power regulators to allow normal operation. The WAKE command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The memory returns to standby mode after $t_{RDP}$. The $\overline{CS}$ pin must remain high until the $t_{RDP}$ period is over.

**Figure 2.8 WAKE**



## 3. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the field intensity specified in the maximum ratings.

**Table 3.1 Absolute Maximum Ratings [1]**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage [2] | All | -0.5 to 4.0 | V |
| $V_{IN}$ | Voltage on any pin [2] | All | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_{OUT}$ | Output current per pin | All | ±20 | mA |
| $P_D$ | Package power dissipation [3] | All | 0.600 | W |
| $T_{BIAS}$ | Temperature under bias | Industrial | -45 to 95 | °C |
| | | AEC-Q100 Grade 3 | -45 to 95 | °C |
| | | AEC-Q100 Grade 1 | -45 to 135 | °C |
| $T_{stg}$ | Storage Temperature | All | -55 to 150 | °C |
| $T_{Lead}$ | Lead temperature during solder (3 minute max) | All | 260 | °C |
| $H_{max_write}$ | Maximum magnetic field (Write) | During Write | 12,000 | A/m |
| $H_{max_read}$ | Maximum magnetic field (Read or Standby) | During Read or Standby | 12,000 | A/m |

[1] Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

[2] All voltages are referenced to $V_{SS}$. The DC value of $V_{IN}$ must not exceed actual applied $V_{DD}$ by more than 0.5V. The AC value of $V_{IN}$ must not exceed applied $V_{DD}$ by more than 2V for 10ns with $I_{IN}$ limited to less than 20mA.

[3] Power dissipation capability depends on package characteristics and use environment.

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*ELECTRICAL SPECIFICATIONS*

**Table 3.2 Operating Conditions**

| Symbol | Parameter | Grade | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | Industrial | 2.7 | - | 3.6 | V |
| | | AEC-Q100 Grade 3 | 2.7 | - | 3.6 | |
| | | AEC-Q100 Grade1 | 3.0 | - | 3.6 | V |
| $V_{IH}$ | Input high voltage | All | 2.2 | - | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input low voltage | All | -0.5 | - | 0.8 | V |
| $T_A$ | Temperature under bias | Industrial | -40 | - | 85 | °C |
| | | AEC-Q100 Grade 3 | -40 | - | 85 | °C |
| | | AEC-Q100 Grade 1 [1] | -40 | - | 125 | °C |

Note 1: AEC-Q100 Grade 1 temperature profile assumes 10 percent duty cycle at maximum temperature (2 years out of 20-year life.)

**Table 3.3 DC Characteristics**

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | All | - | - | ±1 | µA |
| $I_{LO}$ | Output leakage current | All | - | - | ±1 | µA |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = +4 mA | - | - | 0.4 | V |
| | | $I_{OL}$ = +100 µA | - | - | $V_{SS}$ + 0.2v | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -4 mA | 2.4 | - | - | V |
| | | $I_{OH}$ = -100 µA | $V_{DD}$ - 0.2 | - | - | V |

**Table 3.4 Power Supply Characteristics**

| Symbol | Parameter | Conditions | Typical | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDR}$ | Active Read Current | @ 1 MHz | 2.5 | 3 | mA |
| | | @ 40 MHz | 6 | 10 | mA |
| $I_{DDW}$ | Active Write Current | @ 1 MHz | 8 | 13 | mA |
| | | @ 40 MHz | 23 | 27 | mA |
| $I_{SB}$ | Standby Current | $\overline{CS}$ High [1] | 90 | 115 | µA |
| $I_{ZZ}$ | Standby Sleep Mode Current | $\overline{CS}$ High | 7 | 30 | µA |

[1] $I_{SB}$ current is specified with $\overline{CS}$ high and the SPI bus inactive.

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## 4. TIMING SPECIFICATIONS

**Table 4.1 Capacitance[1]**

| Symbol | Parameter | Typical | Max | Unit |
|---|---|---|---|---|
| $C_{In}$ | Control input capacitance | - | 6 | pF |
| $C_{I/O}$ | Input/Output capacitance | - | 8 | pF |

[1] $f$ = 1.0 MHz, dV = 3.0 V, $T_A$ = 25 °C, periodically sampled rather than 100% tested.

**Table 4.2 AC Measurement Conditions**

| Parameter | Value | Unit |
|---|---|---|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 4.1 | |
| Output load for all other timing parameters | See Figure 4.2 | |

**Figure 4.1 Output Load for Impedance Parameter Measurements**

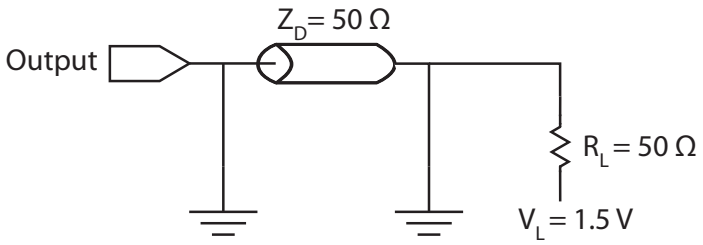
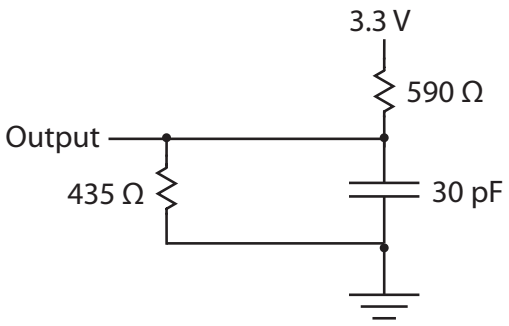



**Figure 4.2 Output Load for all Other Parameter Measurements**



*TIMING SPECIFICATIONS*

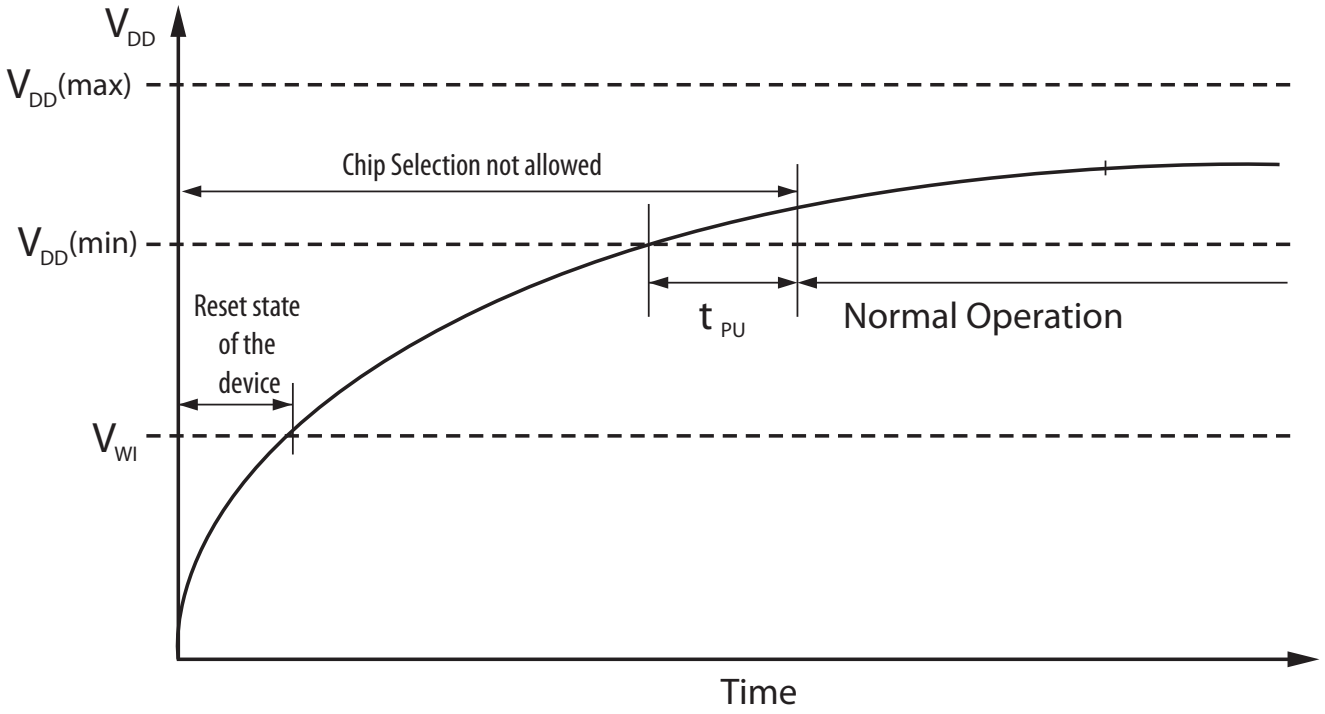
**Power-Up Timing**

The MR25H128A is not accessible for a start-up time, $t_{PU}$ = 400 µs after power up. Users must wait this time from the time when $V_{DD}$ (min) is reached until the first $\overline{CS}$ low to allow internal voltage references to become stable. The $\overline{CS}$ signal should be pulled up to $V_{DD}$ so that the signal tracks the power supply during power-up sequence.

**Table 4.3 Power-Up**

| Symbol | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| $V_{WI}$ | Write Inhibit Voltage | 2.2 | - | 2.7 | V |
| $t_{PU}$ | Startup Time | 400 | - | - | µs |

**Figure 4.3 Power-Up Timing**



*TIMING SPECIFICATIONS*

**Synchronous Data Timing**

**Table 4.4 AC Timing Parameters**

| Over the Operating Temperature Range and $C_L$ = 30 pF | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | | **Min** | **Max** | **Unit** |
| $f_{SCK}$ | SCK Clock Frequency | | | 0 | 40 | MHz |
| $t_{RI}$ | Input Rise Time | | | - | 50 | ns |
| $t_{RF}$ | Input Fall Time | | | - | 50 | ns |
| $t_{WH}$ | SCK High Time | | | 11 | - | ns |
| $t_{WL}$ | SCK Low Time | | | 11 | - | ns |
| Synchronous Data Timing (See figure 4.4) | | | | | | |
| $t_{CS}$ | $\overline{CS}$ High Time | | | 40 | - | ns |
| $t_{CSS}$ | $\overline{CS}$ Setup Time | | | 10 | - | ns |
| $t_{CSH}$ | $\overline{CS}$ Hold Time | | | 10 | - | ns |
| $t_{SU}$ | Data In Setup Time | | | 5 | - | ns |
| $t_H$ | Data In Hold Time | | | 5 | - | ns |
| $t_V$ | Output Valid | Industrial Grade | $V_{DD}$ = 2.7 to 3.6v. | 0 | 10 | ns |
| | | | $V_{DD}$ = 3.0 to 3.6v. | 0 | 9 | ns |
| | | AEC Q-100 Grade 3 | $V_{DD}$ = 2.7 to 3.6v. | 0 | 10 | ns |
| | | | $V_{DD}$ = 3.0 to 3.6v. | 0 | 9 | ns |
| | | AEC Q-100 Grade 1 | $V_{DD}$ = 3.0 to 3.6v. | 0 | 10 | ns |

Table continues next page.

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**Table 4.4 (Cont'd) AC Timing Parameters**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{HO}$ | Output Hold Time | 0 | - | ns |
| $\overline{HOLD}$ Timing (See figure 4.5) | | | | |
| $t_{HD}$ | $\overline{HOLD}$ Setup Time | 10 | - | ns |
| $t_{CD}$ | $\overline{HOLD}$ Hold Time | 10 | - | ns |
| $t_{LZ}$ | $\overline{HOLD}$ to Output Low Impedance | - | 20 | ns |
| $t_{HZ}$ | $\overline{HOLD}$ to Output High Impedance | - | 20 | ns |
| Other Timing Specifications | | | | |
| $t_{WPS}$ | $\overline{WP}$ Setup To $\overline{CS}$ Low | 5 | - | ns |
| $t_{WPH}$ | $\overline{WP}$ Hold From $\overline{CS}$ High | 5 | - | ns |
| $t_{DP}$ | Sleep Mode Entry Time | 3 | - | µs |
| $t_{RDP}$ | Sleep Mode Exit Time | 400 | - | µs |
| $t_{DIS}$ | Output Disable Time | 12 | - | ns |

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**Figure 4.4 Synchronous Data Timing**

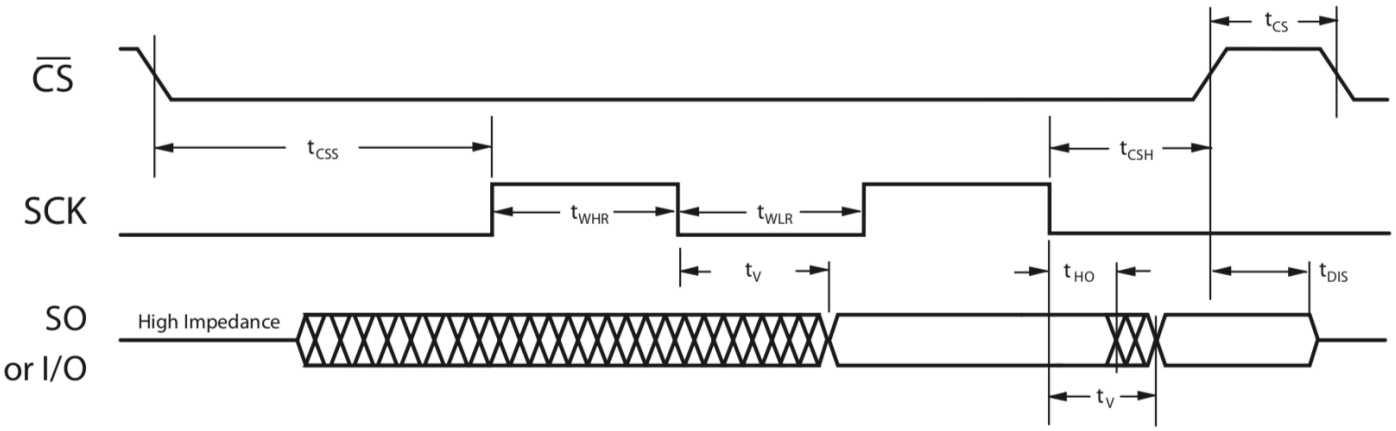
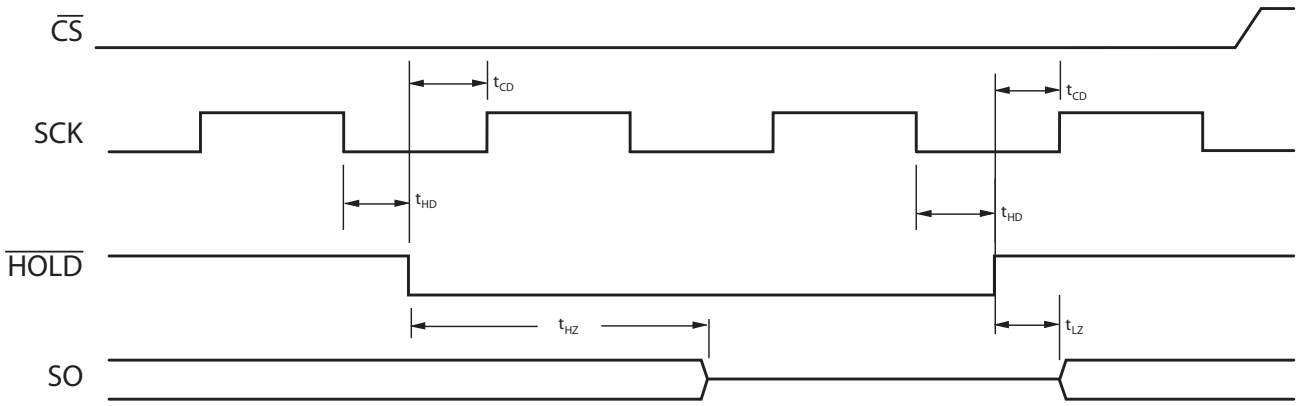



**Figure 4.5 $\overline{HOLD}$ Timing**



## 5. ORDERING INFORMATION

**Figure 5.1 Product Part Number Decoder Table**

| | | | Memory | Speed | Voltage | Density | Revision | Temp | Package | Ship | Grade |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Example Ordering Part Number** | | | MR | 25 | H | 128 | A | P | DF | R | ES |
| Everspin MRAM | | MR | | | | | | | | | |
| 40 MHz | | 25 | | | | | | | | | |
| 3.0v. Vdd | | H | | | | | | | | | |
| 128 Kb | | 128 | | | | | | | | | |
| Revision A | | A | | | | | | | | | |
| Industrial | -40 to 85°C | C | | | | | | | | | |
| AEC-Q100 Grade 3 | -40 to 85°C | P | | | | | | | | | |
| AEC-Q100 Grade 1 | -40 to 125°C | M | | | | | | | | | |
| 8-pin DFN Small Flag | | DF | | | | | | | | | |
| Tray | | Blank | | | | | | | | | |
| Tape and Reel | | R | | | | | | | | | |
| Mass Production | | Blank | | | | | | | | | |
| Customer Samples | | CS | | | | | | | | | |
| Engineering Samples | | ES | | | | | | | | | |

**Table 5.1 Ordering Part Numbers**

| Grade | Temperature | Package | Shipping Container | Order Part Number |
|---|---|---|---|---|
| Industrial | -40 to +85 C | 8-DFN Small Flag | Trays | MR25H128ACDF |
| | | | Tape and Reel | MR25H128ACDFR |
| AEC-Q100 Grade 3 | -40 to +85 C | 8-DFN Small Flag | Trays | MR25H128APDF |
| | | | Tape and Reel | MR25H128APDFR |
| AEC-Q100 Grade 1 | -40 to +125 C | 8-DFN Small Flag | Trays | MR25H128AMDF |
| | | | Tape and Reel | MR25H128AMDFR |

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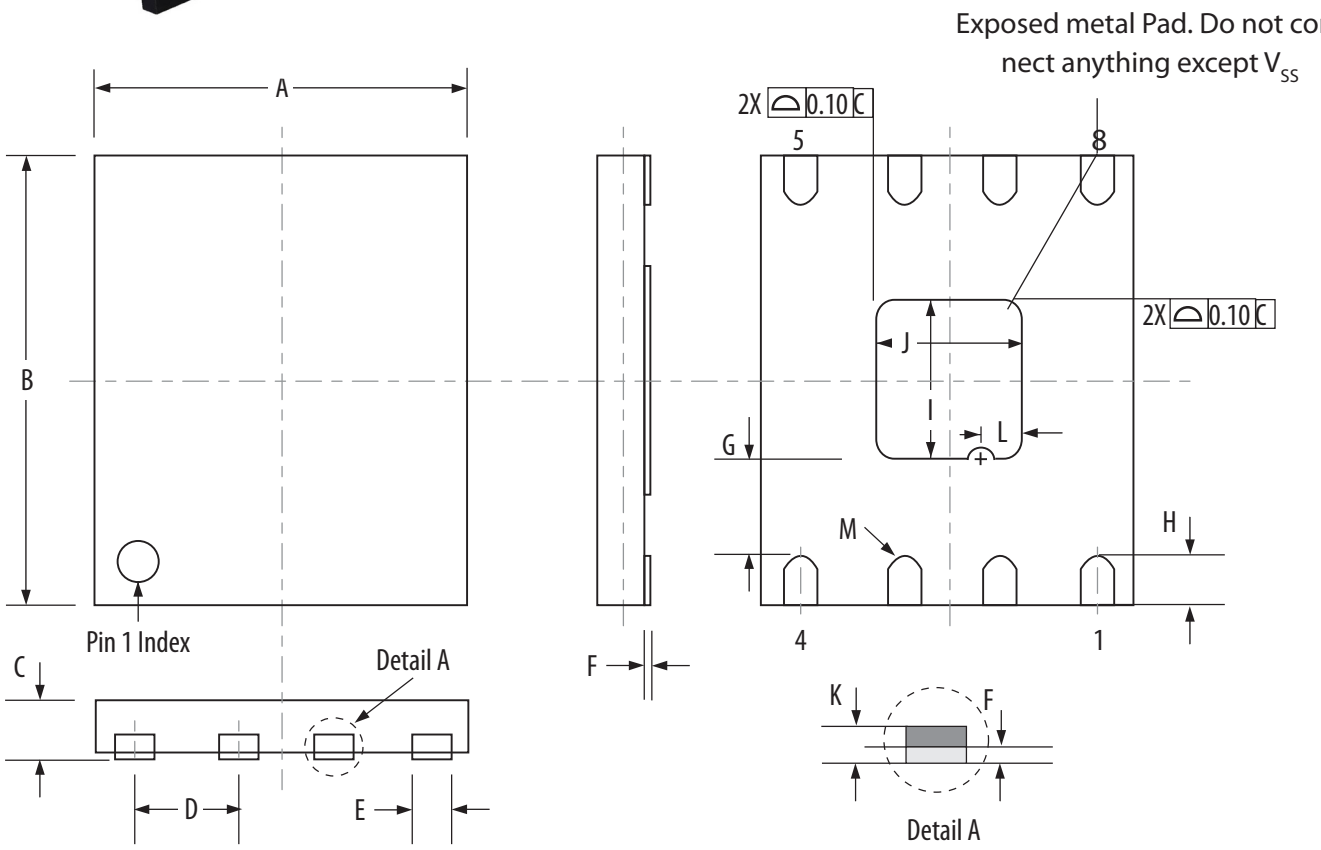
## 6. MECHANICAL DRAWINGS

**Figure 6.1 DFN Small Flag Package**




| Dimension | A | B | C | D | E | F | G | H | I | J | K | L | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max | 5.10 | 6.10 | 0.90 | - | 0.45 | 0.05 | 1.54 | 0.70 | 2.10 | 2.10 | 0.210 | - | - |
| Nominal | 5.00 | 6.00 | 0.85 | 1.27 BSC | 0.40 | - | 1.40 | 0.60 | 2.00 | 2.00 | 0.200 | C0.45 | R0.20 |
| Min | 4.90 | 5.90 | 0.80 | - | 0.35 | 0.00 | 1.26 | 0.50 | 1.90 | 1.90 | 0.190 | - | - |

NOTE:

1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
3. Refer to JEDEC MO-229-E

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## 7. REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| 0.1 | June 1, 2015 | First Draft |
| 0.2 | September 29, 2015 | Corrected address range and timing diagrams for READ and WRITE to Address bits 0-13. Added Grade 3 parameters to Table 4.4 and reformatted the Table. |
| 0.3 | November 2, 2015 | Revised Part Number Decoder Table. |
| 1.0 | October 1, 2016 | Production release. Removed all Preliminary status statements and indications. Added nominal values to DFN package outline dimensions table. |
| 1.1 | February 1, 2017 | Added $^{t}$HO and $^{t}$V relationship to Synchronous Data Timing |
| 1.2 | March 23, 2018 | Updated the Contact Us table |

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