# BT138Y-600E

## 4Q Triac

15 September 2018 Product data sheet

## 1. General description

Planar passivated sensitive gate four quadrant triac in an internally insulated SOT78D (TO-220AB) plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac can be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits. The internally insulated mounting base gives good thermal performance combined with ease of handling and assembly by the user.

## 2. Features and benefits

- 2500 V RMS isolation voltage capability
- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- Industry standard TO-220 package for ease of handling
- Isolated mounting base
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Triggering in all four quadrants

## 3. Applications

- 230 V lamp dimmers
- General purpose switching and phase control

## 4. Quick reference data

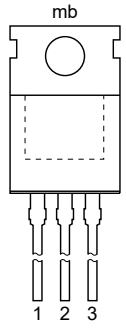
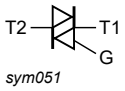
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 85$ °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 12 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | - | 95 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms | | - | - | 105 | A |
| $T_j$ | junction temperature | | | - | - | 125 | °C |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | - | - | 10 | mA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | - | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 7 | | - | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | - | - | 25 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 30 | mA |
| $V_T$ | on-state voltage | $I_T$ = 15 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.4 | 1.65 | V |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 402 V; $T_j$ = 125 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | - | 50 | - | V/µs |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | T1 | main terminal 1 |  **TO-220AB (SOT78D)** |  |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| mb | n.c. | mounting base; isolated | | |

## 6. Ordering information

**Table 3. Ordering information**

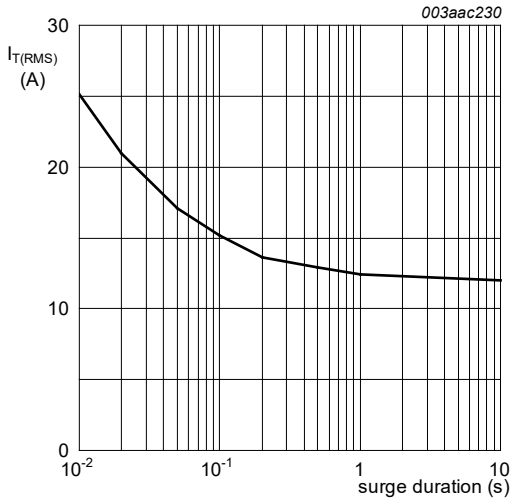
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BT138Y-600E | TO-220AB | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 | SOT78D |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 85$ °C; Fig. 1; Fig. 2; Fig. 3 | | - | 12 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5 | | - | 95 | A |
| | | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms | | - | 105 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p = 10$ ms; SIN | | - | 45 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_G = 100$ mA; T2+ G+ | | - | 50 | A/µs |
| | | $I_G = 100$ mA; T2+ G- | | - | 50 | A/µs |
| | | $I_G = 100$ mA; T2- G- | | - | 50 | A/µs |
| | | $I_G = 100$ mA; T2- G+ | | - | 10 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 2 | A |
| $P_{GM}$ | peak gate power | | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.5 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | - | 125 | °C |




f = 50 Hz; $T_{mb}$ = 85 °C

**Fig. 1. RMS on-state current as a function of surge duration; maximum values**

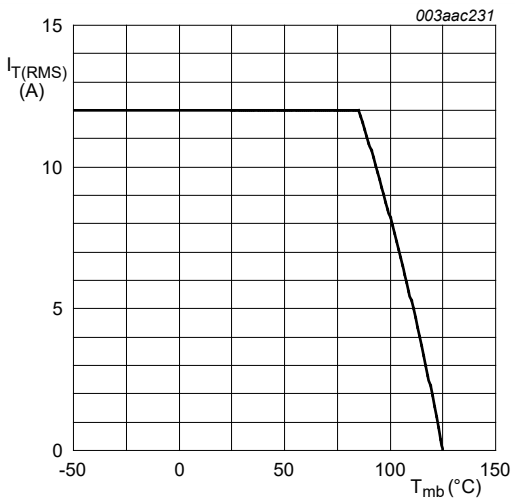
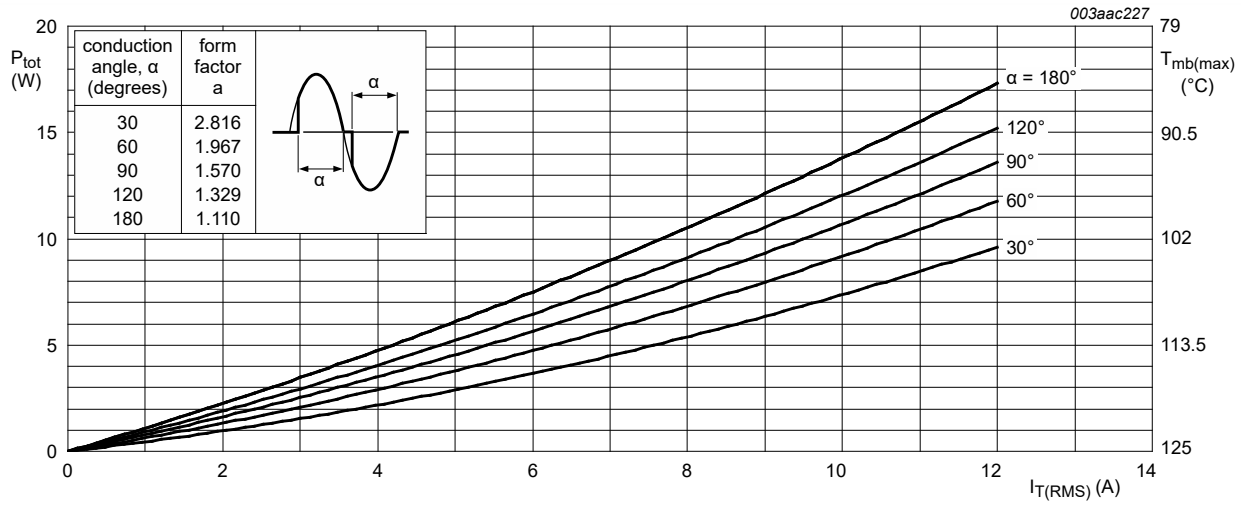


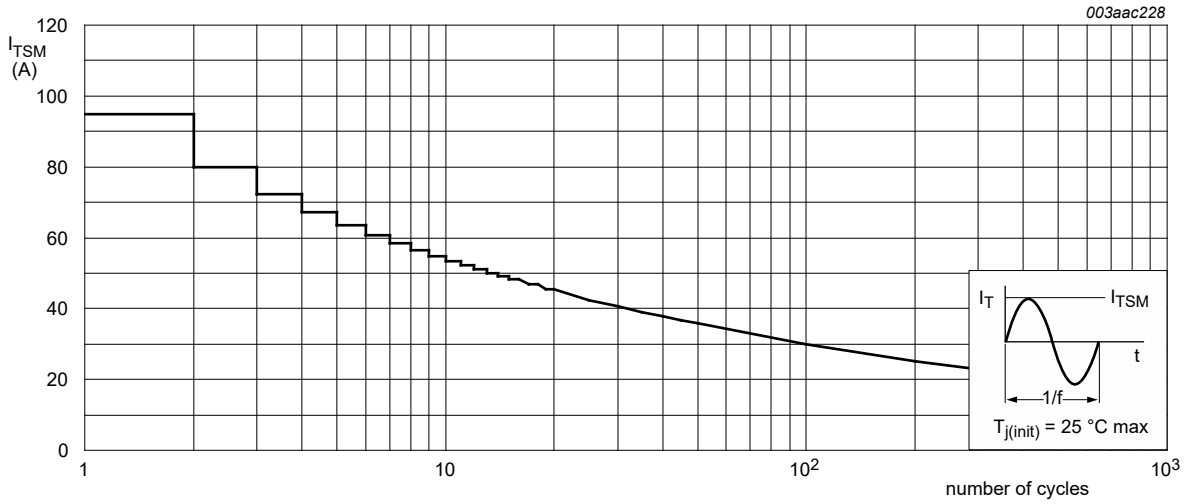

**Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values**




α = conduction angle

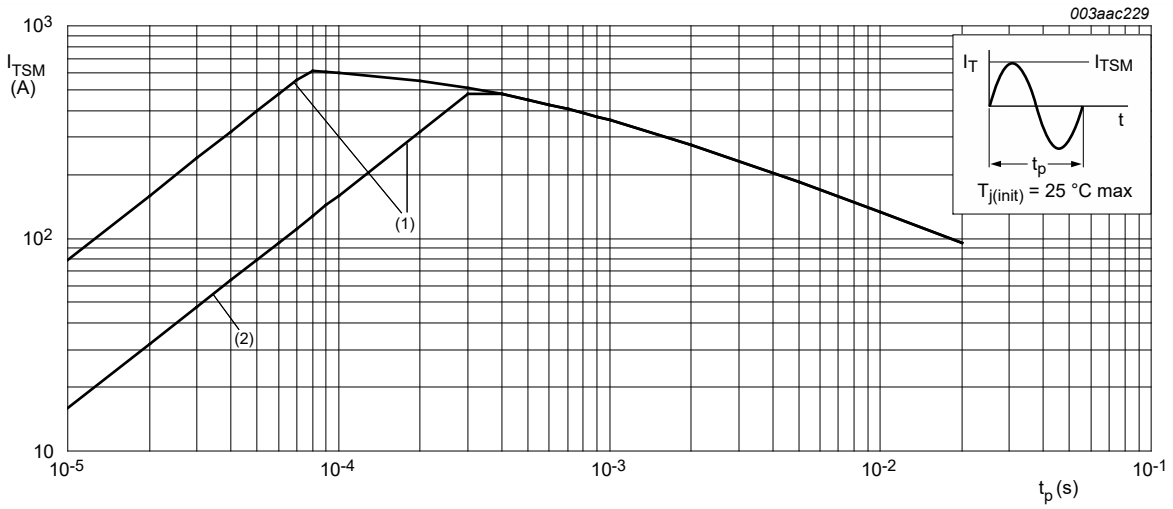
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 20$ ms
(1) $dI_T/dt$ limit
(2) T2- G+ quadrant limit

**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

# 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | full cycle; Fig. 6 | | - | - | 2.3 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | full cycle; in free air | | - | 60 | - | K/W |

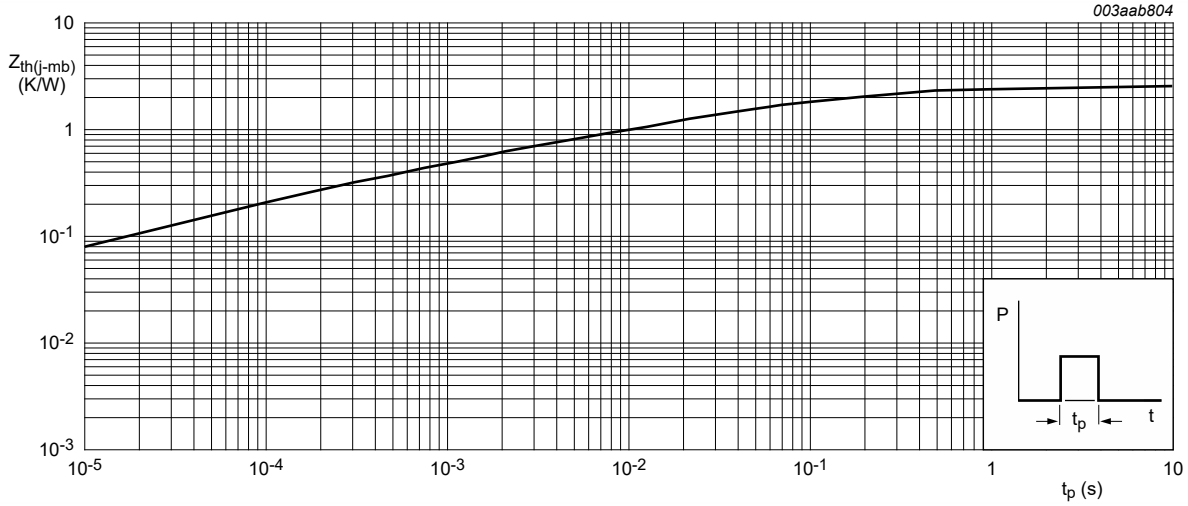



**Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 9. Isolation characteristics

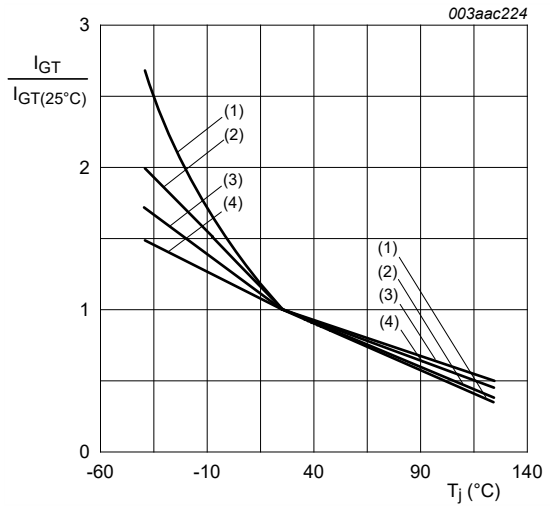
**Table 6. Isolation characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{isol(RMS)}$ | RMS isolation voltage | from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; $T_{mb}$ = 25 °C | | - | - | 2500 | V |
| $C_{isol}$ | isolation capacitance | from main terminal 2 to external heatsink; f = 1 MHz; $T_{mb}$ = 25 °C | | - | 10 | - | pF |

# 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | - | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | - | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 7 | | - | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | - | - | 25 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 8 | | - | - | 30 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 40 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 30 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 8 | | - | - | 40 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 30 | mA |
| $V_T$ | on-state voltage | $I_T$ = 15 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.4 | 1.65 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 0.7 | 1 | V |
| | | $V_D$ = 600 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11 | | 0.25 | 0.4 | - | V |
| $I_D$ | off-state current | $V_D$ = 600 V; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 402 V; $T_j$ = 125 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | - | 50 | - | V/µs |
| $t_{gt}$ | gate-controlled turn-on time | $I_{TM}$ = 16 A; $V_D$ = 600 V; $I_G$ = 100 mA; $dI_G/dt$ = 5 A/µs | | - | 2 | - | µs |




(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

**Fig. 7. Normalized gate trigger current as a function of junction temperature**

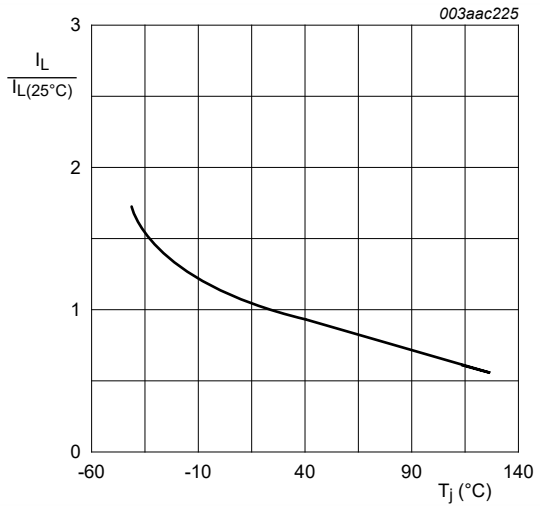



**Fig. 8. Normalized latching current as a function of junction temperature**

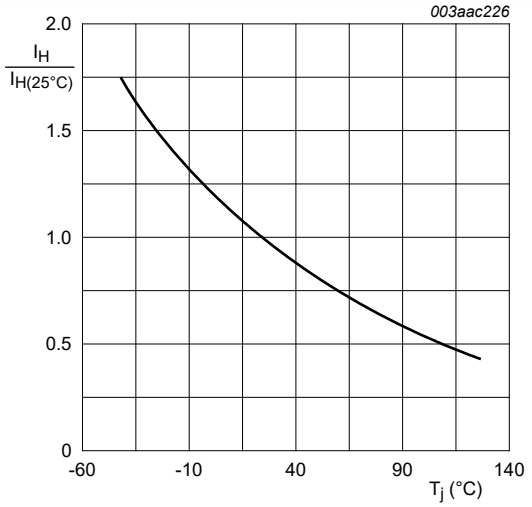
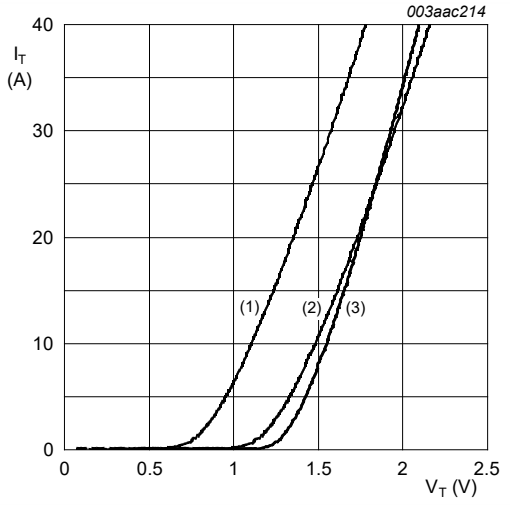



**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.175 V; $R_s$ = 0.032 Ω
(1) $T_j$ = 125 °C; typical values
(2) $T_j$ = 125 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**

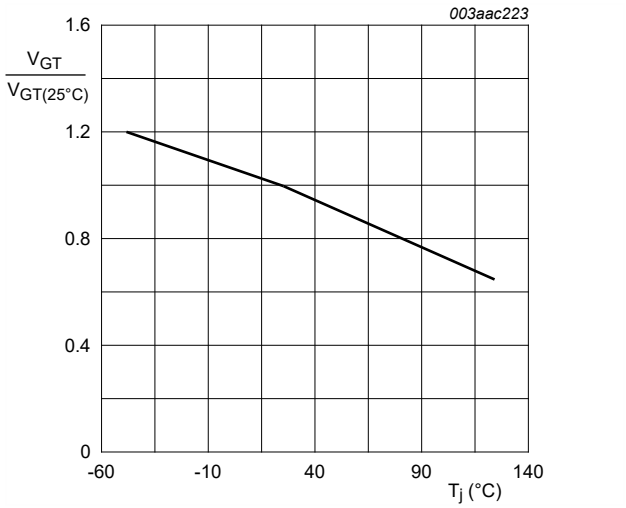
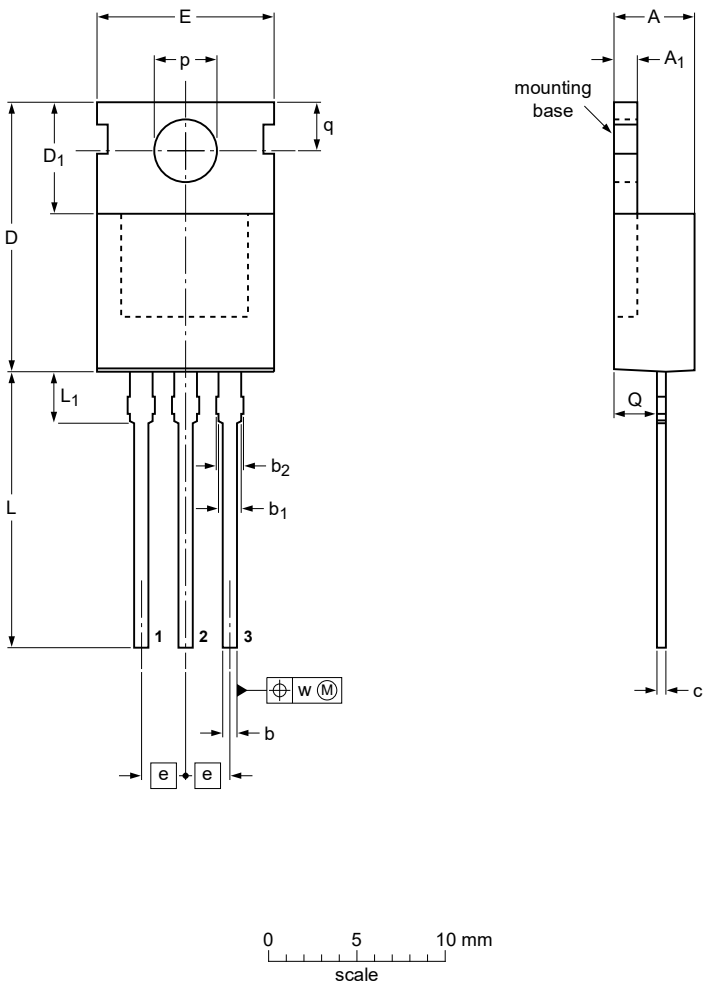



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**

# 11. Package outline

**Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220** **SOT78D**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | D | $D_1$ ref | E | e | L | $L_1$ ref | p | Q | q | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7<br>4.3 | 1.40<br>1.25 | 0.9<br>0.6 | 1.4<br>1.1 | 1.72<br>1.32 | 0.6<br>0.4 | 16.0<br>15.2 | 6.5 | 10.3<br>9.7 | 2.54 | 14.0<br>12.8 | 3.0 | 3.7<br>3.5 | 2.6<br>2.2 | 3.0<br>2.7 | 0.2 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT78D | | TO-220 | | | | ~~07-04-04~~<br>07-07-10 |

**Fig. 12. Package outline TO-220AB (SOT78D)**

# 12. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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# 13. Contents





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**Date of release: 15 September 2018**

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