EZR32LG Wireless MCUs
EZR32LG230 Data Sheet

EZR32LG230 Wireless MCU family with ARM Cortex-M3 CPU and sub-GHz Radio

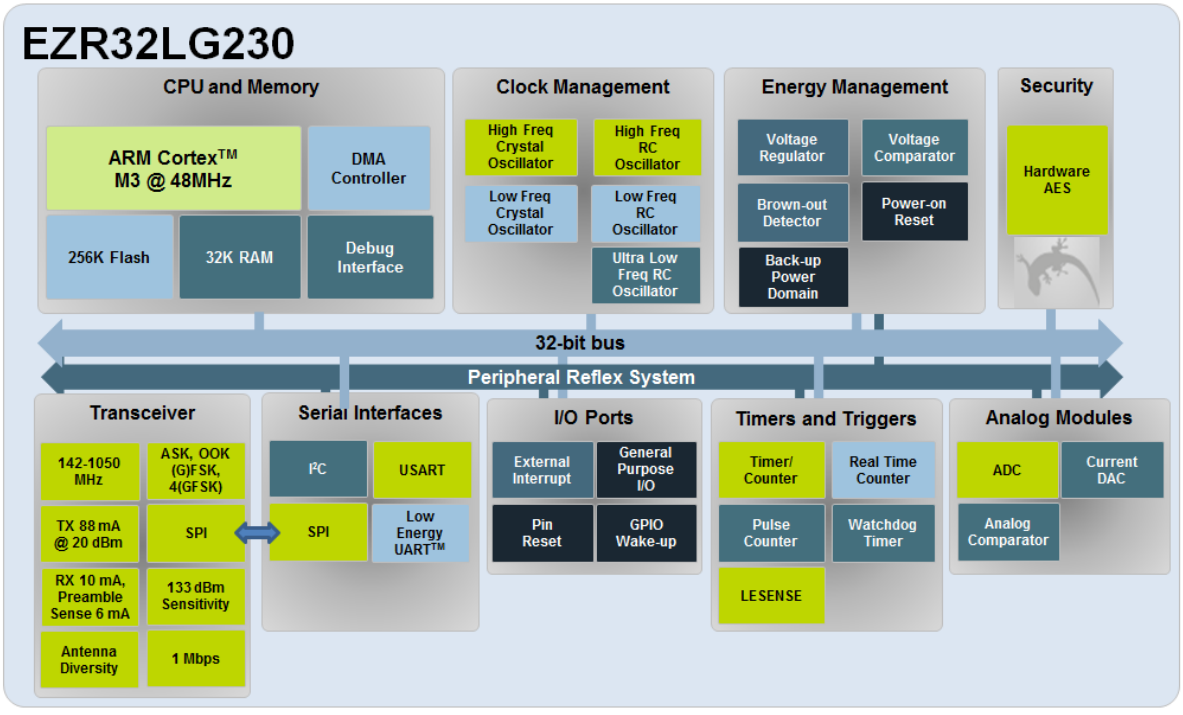
The EZR32LG Wireless MCUs are the latest in Silicon Labs family of wireless MCUs delivering a high performance, low energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit MCU, the EZR32LG family provides designers the ultimate in flexibility with a family of pin-compatible devices that scale with 64/128/256 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times of the Silicon Labs energy friendly 32-bit MCUs, combined with the low transmit and receive power consumption of the sub-GHz radio, result in a solution optimized for battery powered applications.

32-Bit ARM Cortex wireless MCUs applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Consumer electronics
- Alarm and security systems
- Building and home automation

KEY FEATURES

- Silicon Labs' first 32-bit Wireless MCUs
- Based on ARM Cortex M3 (LG) and M4 (WG) CPU cores with 256 kB of flash and 32 kB RAM
- Best-in-class RF performance with EZradio and EZRadioPro transceivers
- Ultra-low power wireless MCU
  - Low transmit and receive currents
  - Ultra-low power standby and sleep modes
  - Fast wake-up time
- Low Energy sensor interface (LESENSE)
- Rich set of peripherals including 12-bit ADC and DAC, multiple communication interfaces (USB, UART, SPI, I2C), multiple GPIO and timers
- AES Accelerator with 128/256-bit keys



1. Feature List

The LG highlighted features are listed below.

MCU Features

- ARM Cortex-M3 CPU platform
  - Up to 48 MHz
  - 64/128/256 kB Flash w/32 kB RAM
  - Hardware AES with 128/256-bit keys
- Flexible Energy Management System
  - 40 nA @ 3 V Shutoff Mode
  - 0.65 µA @ 3 V Stop Mode
  - 211 µA/MHz @ 3 V Run Mode
- Timers/Counters
  - 4× Timer/Counter
  - 4×3 Compare/Capture/PWM channels
  - Low Energy Timer
  - Real-Time Counter
  - 16/8-bit Pulse Counter
  - Watchdog Timer
- Communication interfaces
  - 2× USART (UART/SPI)
  - 2× UART
  - 2× Low Energy UART
  - 2× I2C Interface with SMBus support
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s ADC
  - On-chip temperature sensor
  - 12-bit 500 ksamples/s DAC
  - 2× Analog Comparator
  - 3x Operational Amplifier
- Low Energy Sensor Interface (LESENSE)
- Up to 41 General Purpose I/O pins

RF Features

- RF Features Frequency Range
  - 142-1050 MHz
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK, OOK
- Receive sensitivity up to -133 dBm
- Up to +20 dBm max output power
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm
  - 6 mA @ 1.2 Kbps (Preamble Sense)
- Data rate = 100 bps to 1 Mbps
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- IEEE 802.15.4g compliant

System Features

- Power-on Reset and Brown-Out Detector
- Debug Interface
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- QFN64 package

2. Ordering Information

The table below shows the available EZR32LG230 devices.

Table 2.1. Ordering Information

Ordering	Radio	Flash (kB)	RAM (kB)	Power Amplifier (dBm)	Max Sensitivity (dBm)	Supply Voltage (V)	Package
EZR32LG230Fx55G	EZRadio	64-256	32	+13	-116	1.98 - 3.8	QFN64
EZR32LG230Fx60G	EZRadioPro	64-256	32	+13	-129	1.98 - 3.8	QFN64
EZR32LG230Fx61G	EZRadioPro	64-256	32	+16	-129	1.98 - 3.8	QFN64
EZR32LG230Fx63G	EZRadioPro	64-256	32	+20	-129	1.98 - 3.8	QFN64
EZR32LG230Fx67G	EZRadioPro	64-256	32	+13	-133	1.98 - 3.8	QFN64
EZR32LG230Fx68G	EZRadioPro	64-256	32	+20	-133	1.98 - 3.8	QFN64
EZR32LG230Fx69G	EZRadioPro	64-256	32	+13 & 20	-133	1.98 - 3.8	QFN64

Table 2.2. Flash Sizes

Example Part Number	Flash Size
EZR32LG230FE55G	64 kB
EZR32LG230FF55G	128 kB
EZR32LG230FG55G	256 kB

Note: Add an "(R)" at the end of the device part number to denote tape and reel option.

Visit www.silabs.com for information on global distributors and representatives.

3. System Overview

3.1 Introduction

The EZR32LG230 Wireless MCUs are the latest in Silicon Labs family of wireless MCUs delivering a high performance, low energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit ARM Cortex-M3, , the EZR32LG family provides designers with the ultimate in flexibility with a family of pin-compatible parts that scale from 64 to 256 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times combined with the low transmit and receive power consumption of the sub-GHz radio, results in a solution optimized for low power and battery powered applications. For a complete feature set and in-depth information on the modules, the reader is referred to the EZR32LG Reference Manual.

The EZR32LG230 block diagram is shown below.

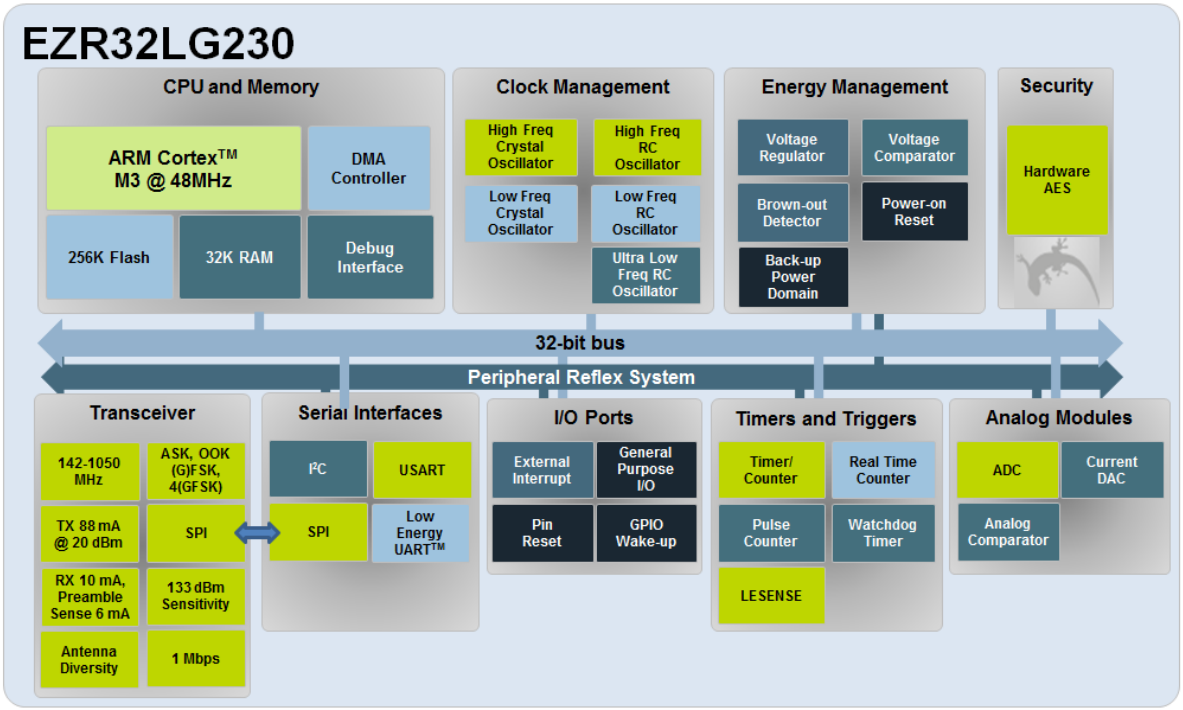


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EZR32 implementation of the Cortex-M3 is described in detail in *EZR32 Cortex-M3 Reference Manual*.

3.1.2 Debugging

These devices include hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EZR32LG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EZR32LG.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EZR32LG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EZR32LG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and I2S devices.

3.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

3.1.13 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

3.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.17 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

3.1.18 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

3.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

3.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

3.1.24 Operational Amplifier (OPAMP)

The EZR32LG230 features 2 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors, etc.

3.1.25 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.1.26 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EZR32LG230 to keep track of time and retain data, even if the main power source should drain out.

3.1.27 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations (i.e., 8- or 16-bit operations are not supported).

3.1.28 General Purpose Input/Output (GPIO)

In the EZR32LG230, there are 41 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.29 EZRadio® and EZRadioPro® Transceivers

The EZR32LG family of devices is built using high-performance, low-current EZRadio and EZRadioPro RF transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. These devices offer outstanding sensitivity of upto –133 dBm (using EZRadioPro) while achieving extremely low active and standby current consumption. The EZR32LG devices using the EZRadioPro transceiver offer frequency coverage in all major bands and include optimal phase noise, blocking, and selectivity performance for narrow band and licensed band applications, such as FCC Part 90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times is optimized for extended battery life in the most demanding applications. The EZR32LG devices can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be programmed and configured via Simplicity Studio, available at www.silabs.com.

Communication between the radio and MCU are done over USART, PRS and IRQ, which requires the pins to be configured in the following way:

Table 3.1. Radio MCU Communication Configuration

EZR32LG Pin	Radio Assignment	EZR32LG Function Assignment
PE8	SDN	GPIO Output
PE9	$_{n}$SEL	Bit-Banged SPI.CS (GPIO Output)
PE10	SDI	US0_TX #0
PE11	SDO	US0_RX #0
PE12	SCLK	US0_CLK #0
PE13	$_{n}$IRQ	GPIO_EM4WU5 (GPIO Input with IRQ enabled)
PE14	GPIO1	PRS Input
PA15	GPIO0	PRS Input

3.2 Configuration Summary

The features of the EZR32LG230 is a subset of the feature set described in the *EZR32LGReference Manual*. The table below describes device specific implementation of the features.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]

Module	Configuration	Pin Connections
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	41 pins	Available pins are shown in 5.4 GPIO Pinout Overview

3.3 Memory Map

The EZR32LG230 memory map is shown below with RAM and flash sizes for the largest memory configuration.

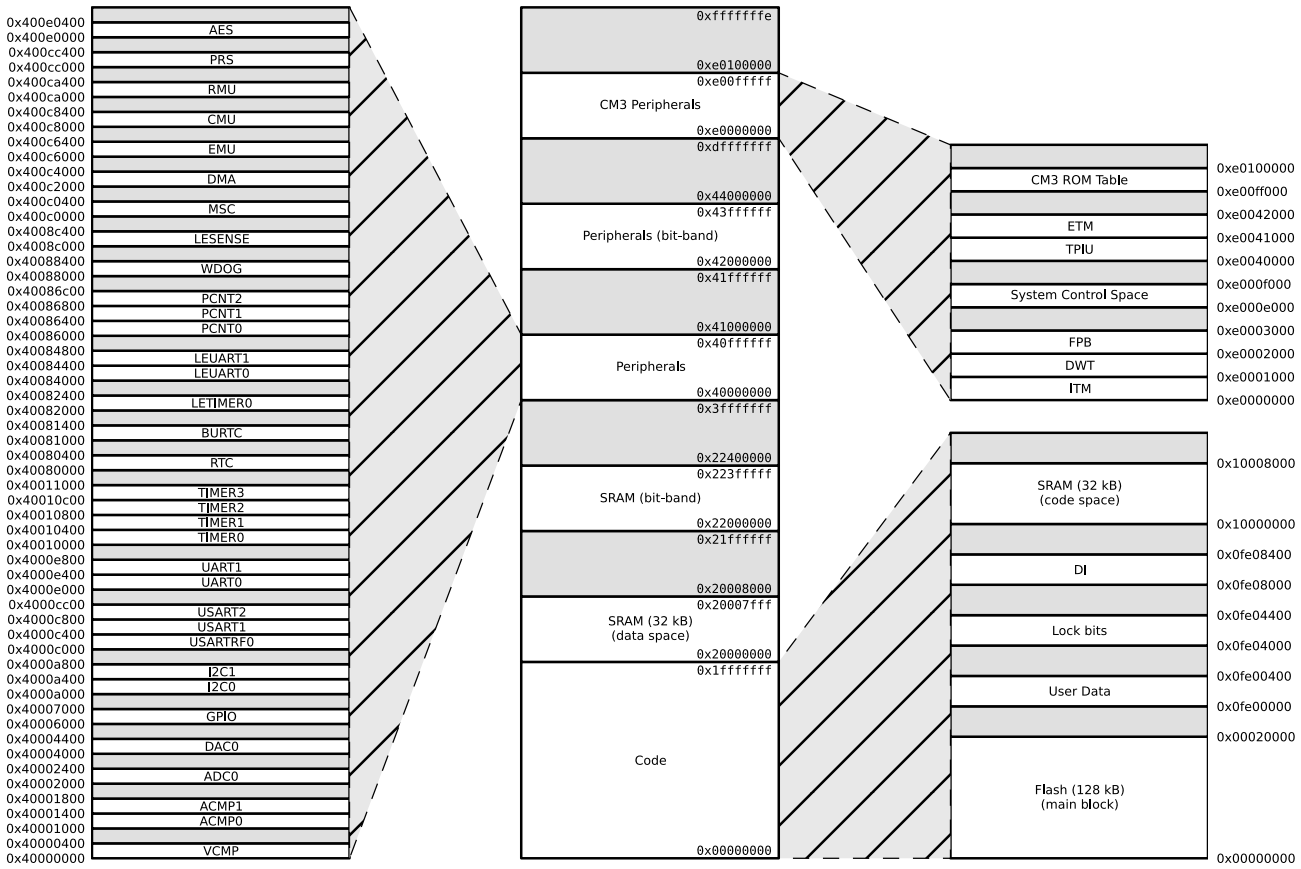


Figure 3.2. EZR32LG230 Memory Map with Largest RAM and Flash Sizes

4. Electrical Specifications

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB}=25 °C and V_{DD}=3.0 V, as defined in Table 4.3 General Operating Conditions on page 11, by simulation and/or technology characterisation unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 4.3 General Operating Conditions on page 11, by simulation and/or technology characterisation unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the table below may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 4.3 General Operating Conditions on page 11.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-55	—	150[1]	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V

Note:

1. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.3 Thermal Characteristics

Table 4.2. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}		-40	—	85	°C
Junction temperature value	T_J		—	—	105[1]	°C
Thermal impedance junction to ambient	TI_{JA}	+13/+16 dBm on 2-layer board	—	—	61.8	°C/W
		+20 dBm on 4-layer board	—	—	20.7[2]	°C/W
Storage temperature range	T_{STG}		-55	—	150	°C

Note:

1. Values are based on simulations run on 2 layer and 4 layer PCBs at 0m/s airflow.
2. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.4 General Operating Conditions

Table 4.3. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	
Ambient temperature range	T_{AMB}	-40	—	85	°C	
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V	
Internal APB clock frequency	f_{APB}	—	—	48	MHz	
Internal AHB clock frequency	f_{AHB}	—	—	48	MHz	

Table 4.4. Environmental

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ESD (Human Body Model HBM)	V_{ESDHBM}	T_{AMB}=25 °C	—	—	2000	V
ESD (Charged Device Model, CDM)	V_{ESDCDM}	T_{AMB}=25 °C	—	—	500	V

Latch-up sensitivity passed: ±100 mA/1.5 × V_{SUPPLY}(max) according to JEDEC JESD 78 method Class II, 85 °C.

4.5 Current Consumption

Table 4.5. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	211	225	µA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	211	230	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	212	220	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	213	223	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	214	224	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	215	226	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	216	231	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	217	237	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	218	239	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	219	239	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	224	242	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	224	250	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	257	285	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	261	293	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM1 current (Production test condition = 14 MHz)	I_{EM1}	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	63	75	µA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	65	76	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	64	75	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	65	77	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	65	76	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	66	78	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	67	79	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	68	82	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	68	81	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	70	83	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	74	87	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	76	89	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	106	120	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	112	129	µA/MHz
EM2 current	I_{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	0.95[1]	1.7	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	3.0[1]	4.0[1]	µA
EM3 current	I_{EM3}	V_{DD}= 3.0 V, T_{AMB}=25 °C	—	0.65	1.3	µA
		V_{DD}= 3.0 V, T_{AMB}=85 °C	—	2.65	4.0	µA
EM4 current	I_{EM4}	V_{DD}= 3.0 V, T_{AMB}=25 °C	—	0.02	0.055	µA
		V_{DD}= 3.0 V, T_{AMB}=85 °C	—	0.44	0.9	µA

Note:
1. Using backup RTC.

4.6 Transitions between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CP.

Table 4.6. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	µs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	µs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	µs

4.7 Power Management

The EZR32LG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002: EFM32 Hardware Design Considerations*.

Table 4.7. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$		1.74	—	1.96	V
BOD threshold on falling internally regulated supply voltage	$V_{BODintthr-}$		1.57	—	1.7	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$		—	1.85	1.98	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	t_{RESET}	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	µs
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	µF

4.8 Flash

Table 4.8. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 °C	10000	—	—	h
		T_{AMB}<85 °C	10	—	—	years
		T_{AMB}<70 °C	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time	t_{PERASE}		20	20.4	20.8	ms
Device erase time	t_{DERASE}		40	40.8	41.6	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

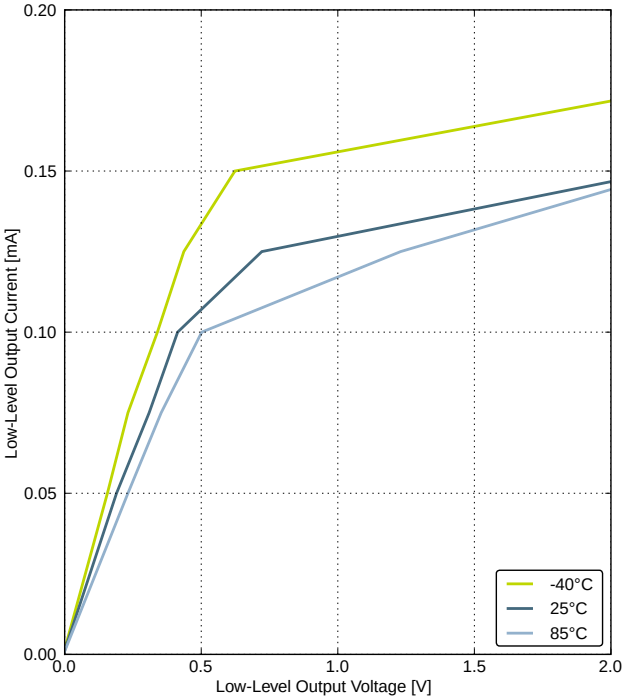
Note:
1. Measured at 25 ºC.

4.9 General Purpose Input Output

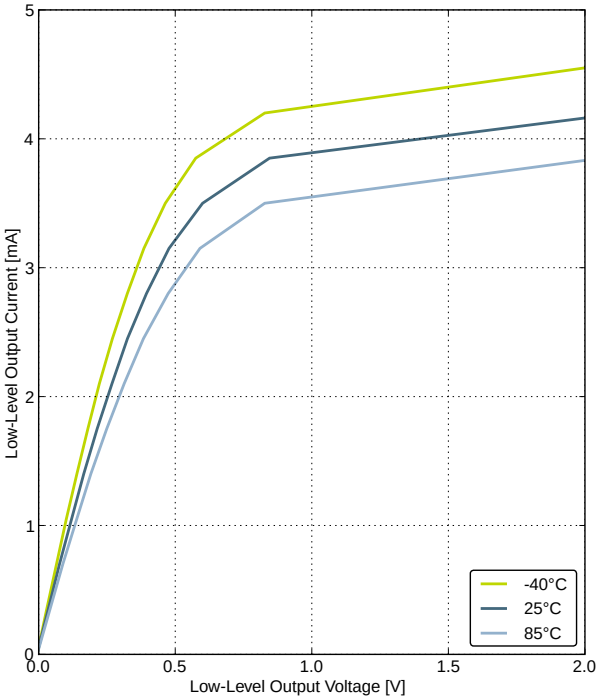
Table 4.9. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	0.30 V_{DD}	V
Input high voltage	V_{IOIH}		0.70 V_{DD}	—	—	V
Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.80 V_{DD}	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.90 V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.85 V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.90 V_{DD}	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75 V_{DD}	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80 V_{DD}	—	—	V

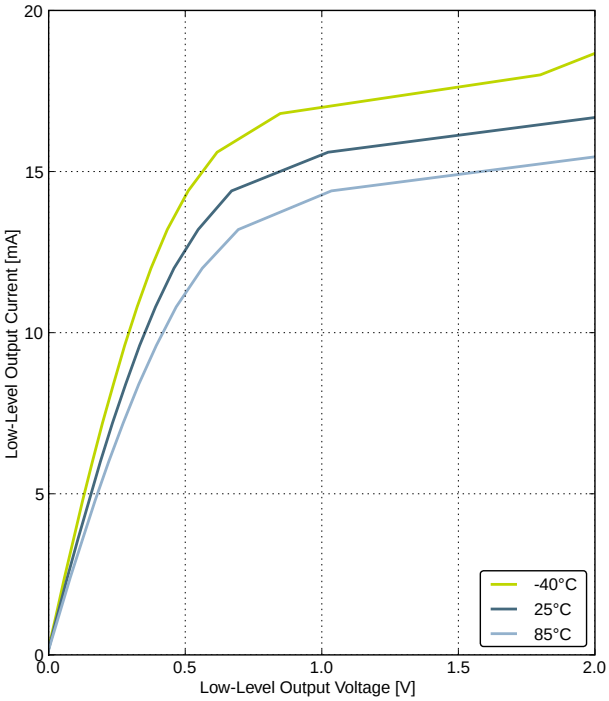
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output low voltage (Production test condition = 3.0 V, DRIVEMODE = STANDARD)	V_{IOOL}	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.20 V_{DD}	—	V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.05 V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.30 V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.20 V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.35 V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.25 V_{DD}	V
Input leakage current	I_{IOLEAK}	High Impedance IO connected to GROUND or Vdd	—	±0.1	±100	nA
I/O pin pull-up resistor	R_{PU}		—	40	—	kOhm
I/O pin pull-down resistor	R_{PD}		—	40	—	kOhm
Internal ESD series resistor	R_{IOESD}		—	200	—	Ohm
Pulse width of pulses to be removed by the glitch suppression filter	$t_{IOGLITCH}$		10	—	—	ns
Output fall time	t_{IOOF}	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25 pF.	20+0.1 C_L	—	250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600 pF	20+0.1 C_L	—	250	ns
I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{IOHYST}	V_{DD} = 1.98 - 3.8 V	0.10 V_{DD}	—	—	V



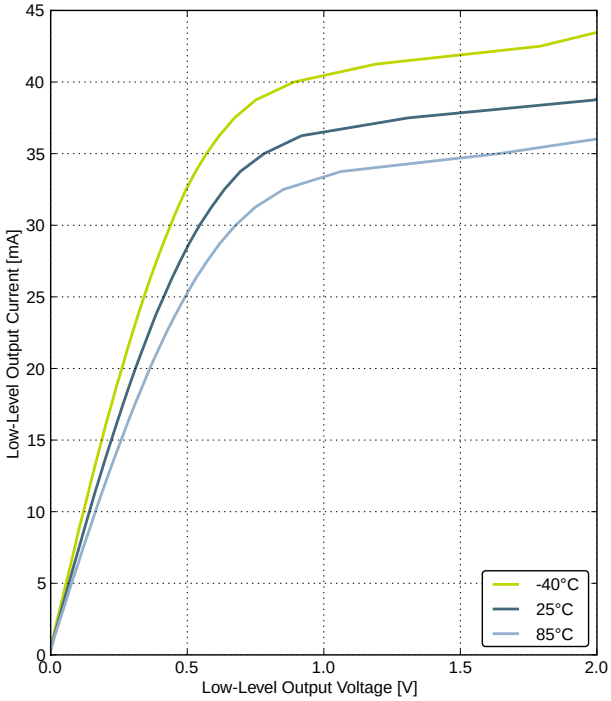
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

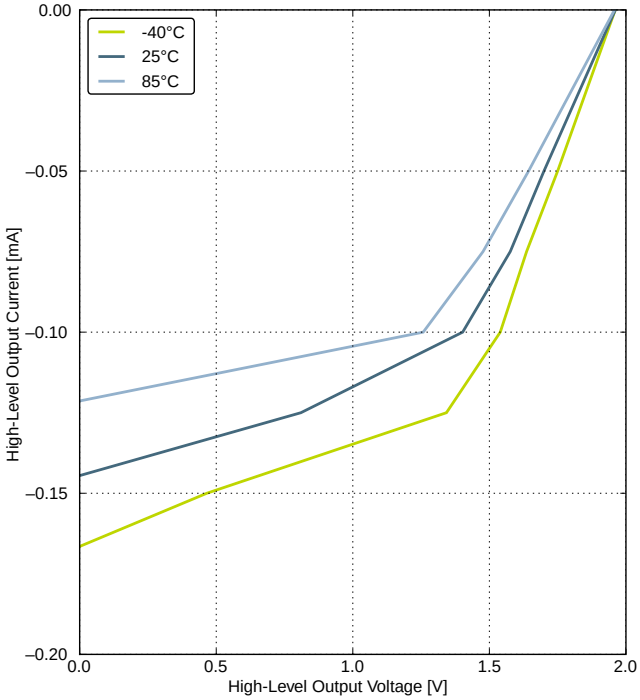


GPIO_Px_CTRL DRIVEMODE = STANDARD

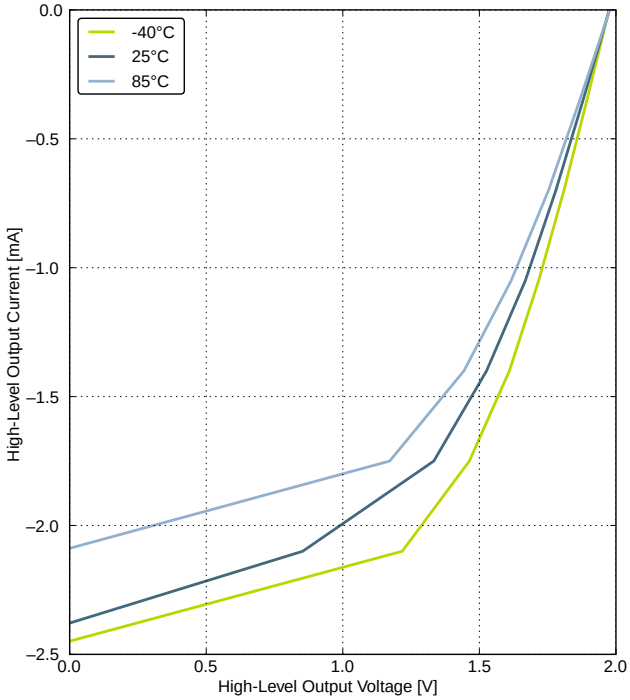


GPIO_Px_CTRL DRIVEMODE = High

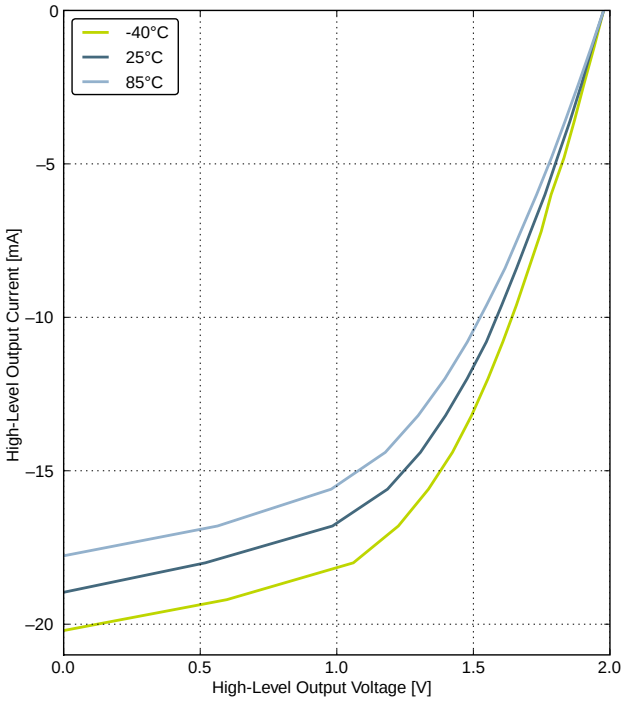
Figure 4.1. Typical Low-Level Output Current, 2 V Supply Voltage



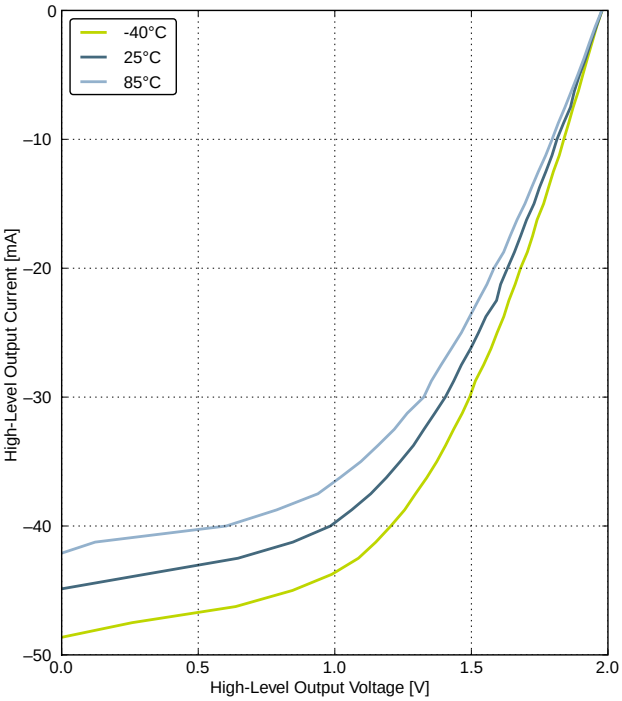
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

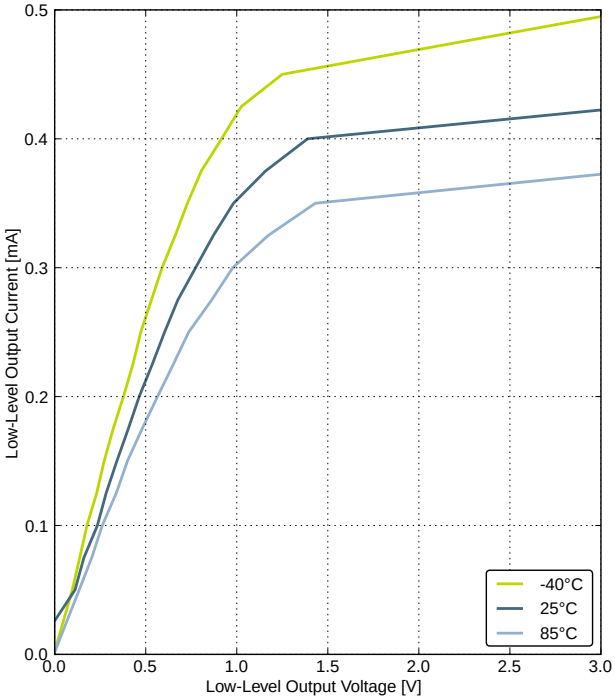


GPIO_Px_CTRL DRIVEMODE = STANDARD

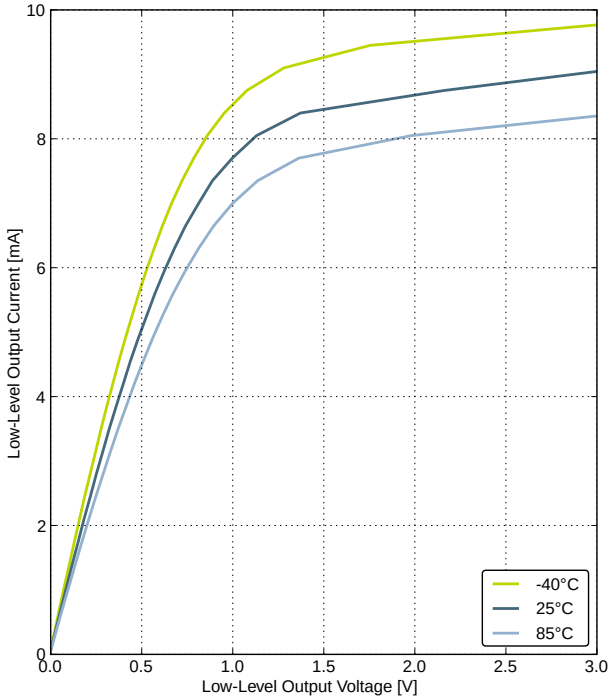


GPIO_Px_CTRL DRIVEMODE = High

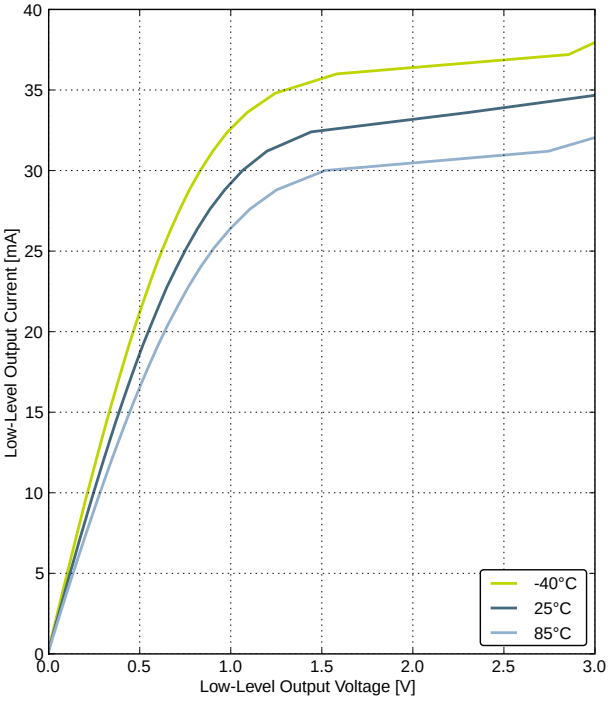
Figure 4.2. Typical High-Level Output Current, 2 V Supply Voltage



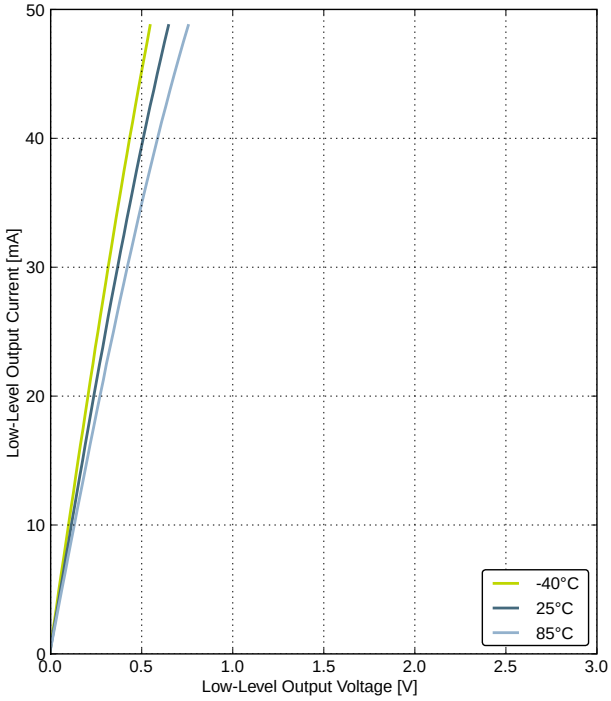
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

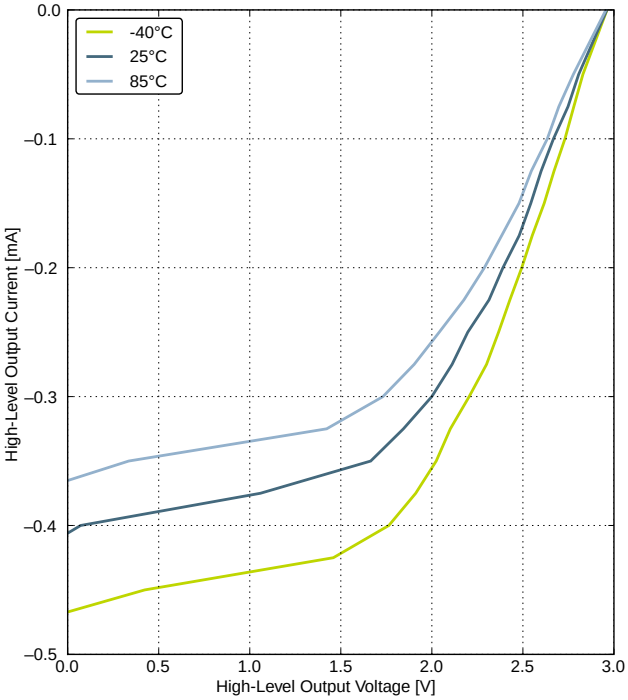


GPIO_Px_CTRL DRIVEMODE = STANDARD

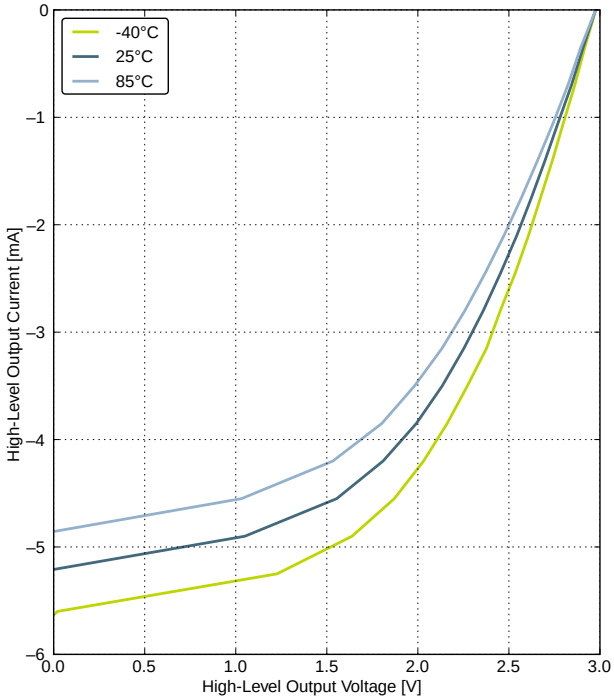


GPIO_Px_CTRL DRIVEMODE = High

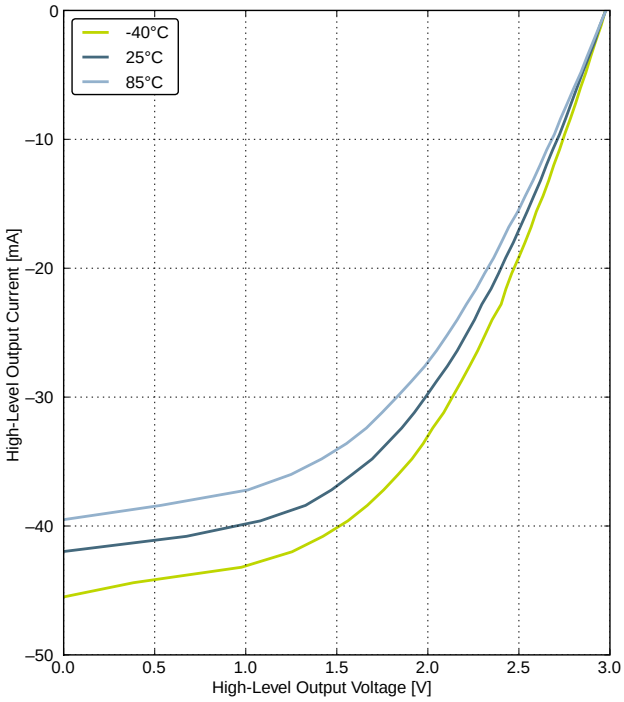
Figure 4.3. Typical Low-Level Output Current, 3 V Supply Voltage



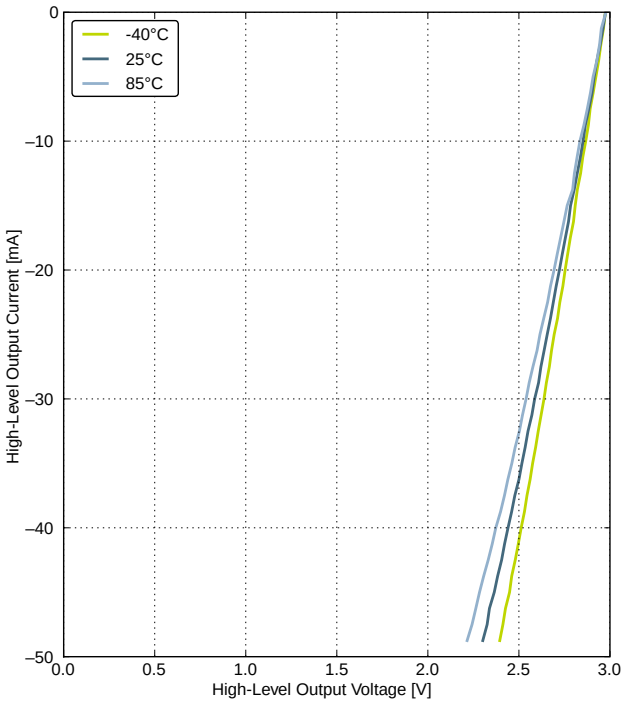
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

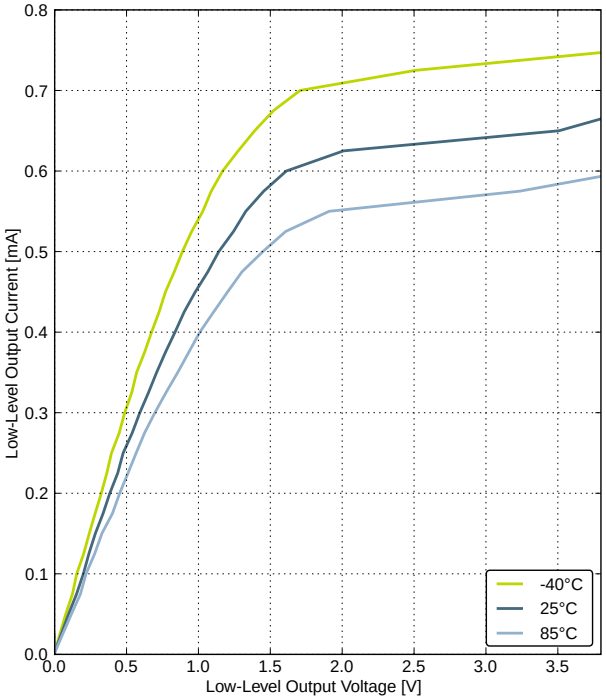


GPIO_Px_CTRL DRIVEMODE = STANDARD

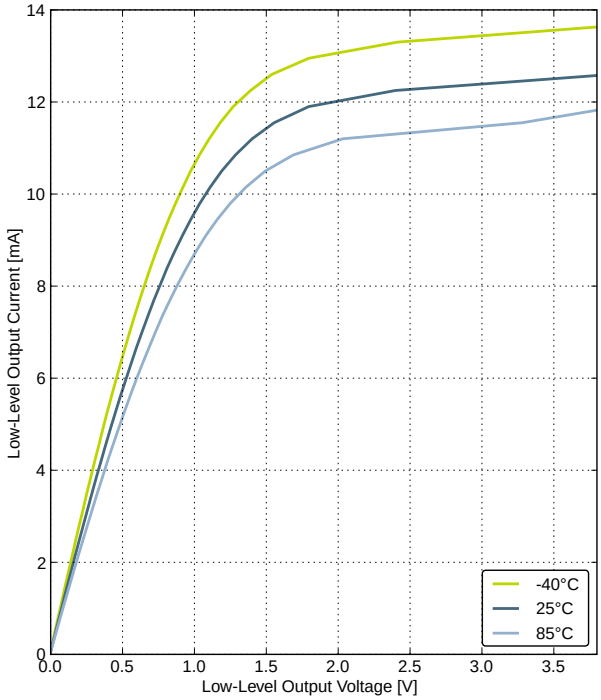


GPIO_Px_CTRL DRIVEMODE = High

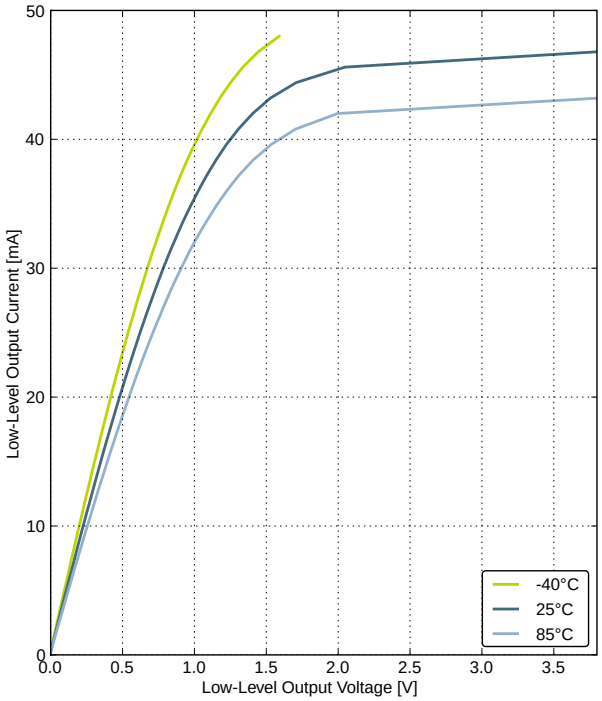
Figure 4.4. Typical High-Level Output Current, 3 V Supply Voltage



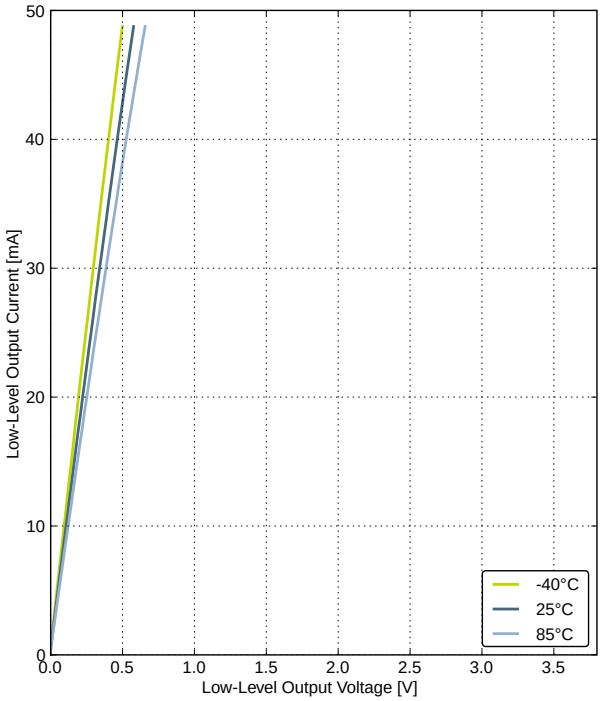
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

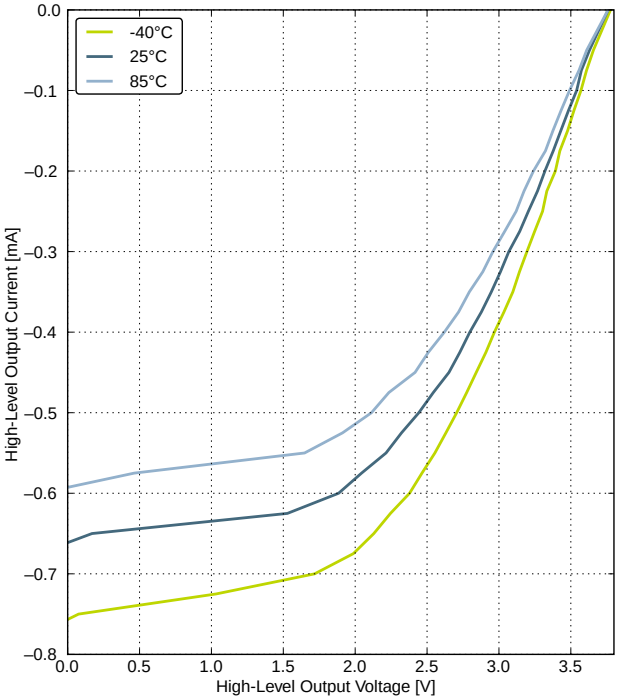


GPIO_Px_CTRL DRIVEMODE = STANDARD

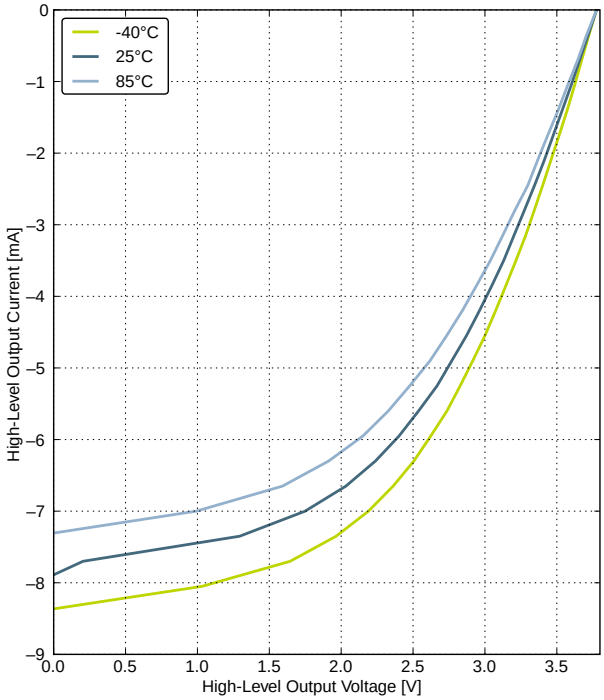


GPIO_Px_CTRL DRIVEMODE = High

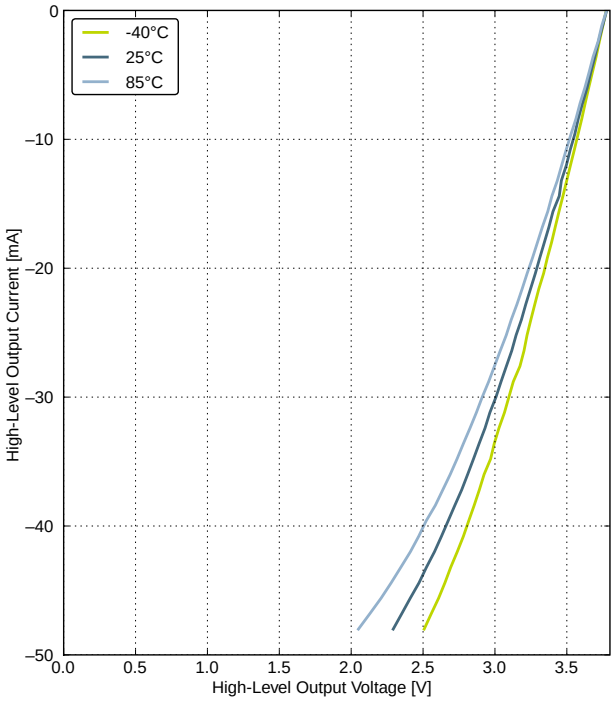
Figure 4.5. Typical Low-Level Output Current, 3.8 V Supply Voltage



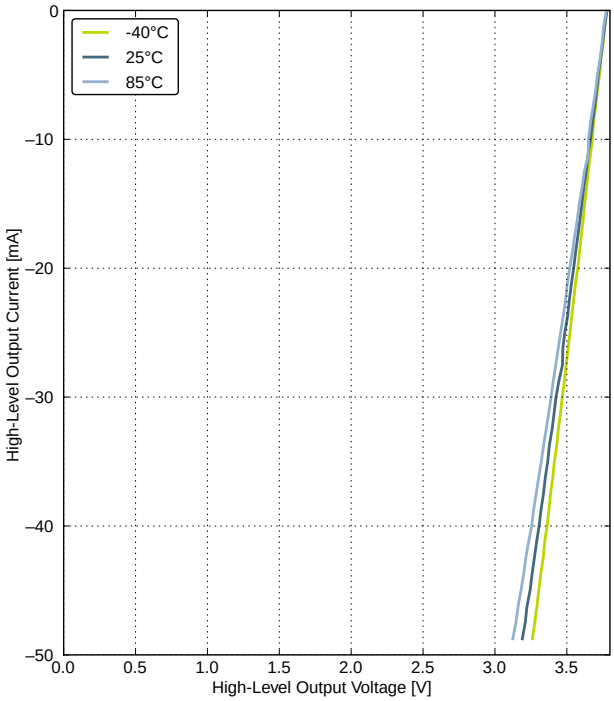
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = High

Figure 4.6. Typical High-Level Output Current, 3.8 V Supply Voltage

4.10 Oscillators

4.10.1 LXFO

Table 4.10. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	30	120	kΩ
Supported crystal external load range	C_{LFXOL}		X[1]	—	25	pF
Duty cycle	DC_{LFXO}		48	50	53.5	%
Current consumption for core and buffer after startup	I_{LFXO}	ESR=30 kΩ, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1	—	190	—	nA
Start- up time	t_{LFXO}	ESR=30 kΩ, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1	—	400	—	ms

Note:
1. See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio.

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note *AN0016: EFM32 Oscillator Design Consideration*.

4.10.2 HFXO

Table 4.11. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal Frequency	f_{HFXO}		4	—	48	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 48 MHz	—	—	50	Ω
		Crystal frequency 32 MHz	—	30	60	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	ms
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Duty cycle	DC_{HFXO}		46	50	54	%
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	µA
Startup time	t_{HFXO}	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	400	—	µs

4.10.3 LFRCO

Table 4.12. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25 °C	f_{LFRCO}		31.29	32.768	34.28	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	µs
Current consumption	I_{LFRCO}		—	300	—	nA
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	1.5	—	%

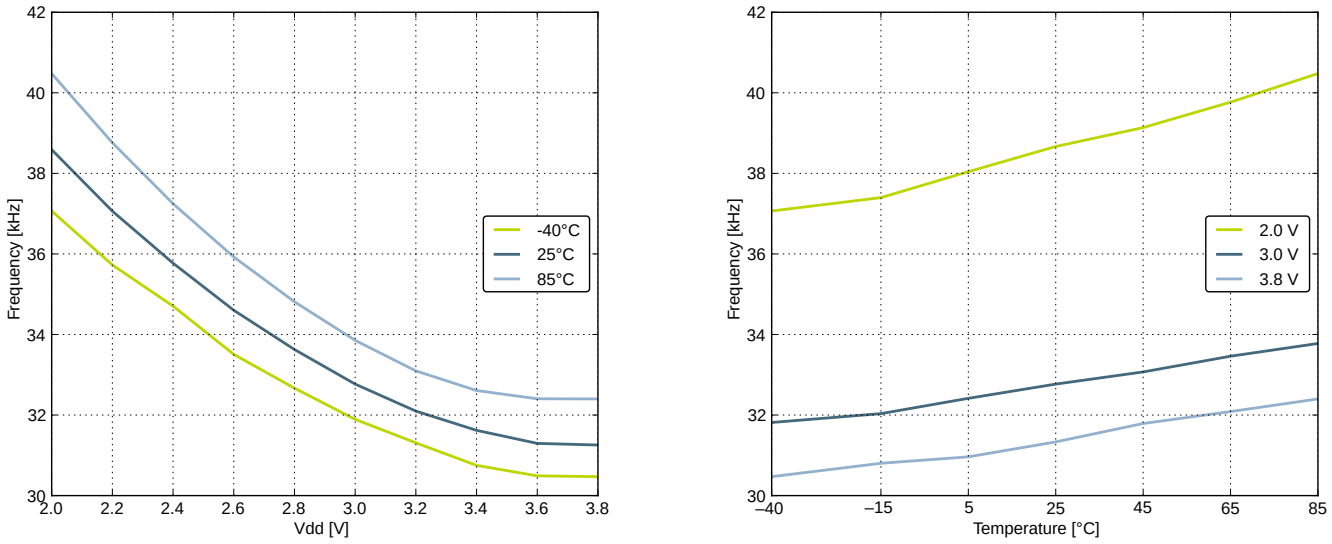


Figure 4.7. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

4.10.4 HFRCO

Table 4.13. HFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25 °C	f_{HFRCO}	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48	6.60	6.72	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
Settling time after start-up	$t_{HFRCO\_settling}$	f_{HFRCO} = 14 MHz	—	0.6	—	Cycles
Current consumption	I_{HFRCO}	f_{HFRCO} = 28 MHz	—	165	215	µA
		f_{HFRCO} = 21 MHz	—	134	175	µA
		f_{HFRCO} = 14 MHz	—	106	140	µA
		f_{HFRCO} = 11 MHz	—	94	125	µA
		f_{HFRCO} = 6.6 MHz	—	77	105	µA
		f_{HFRCO} = 1.2 MHz	—	25	40	µA
Duty cycle	DC_{HFRCO}	f_{HFRCO} = 14 MHz	48.5	50	51	%
Frequency step for LSB change in TUNING value	$TUNESTEP_{HFRCO}$		—	0.3[1]	—	%

Note:

1. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

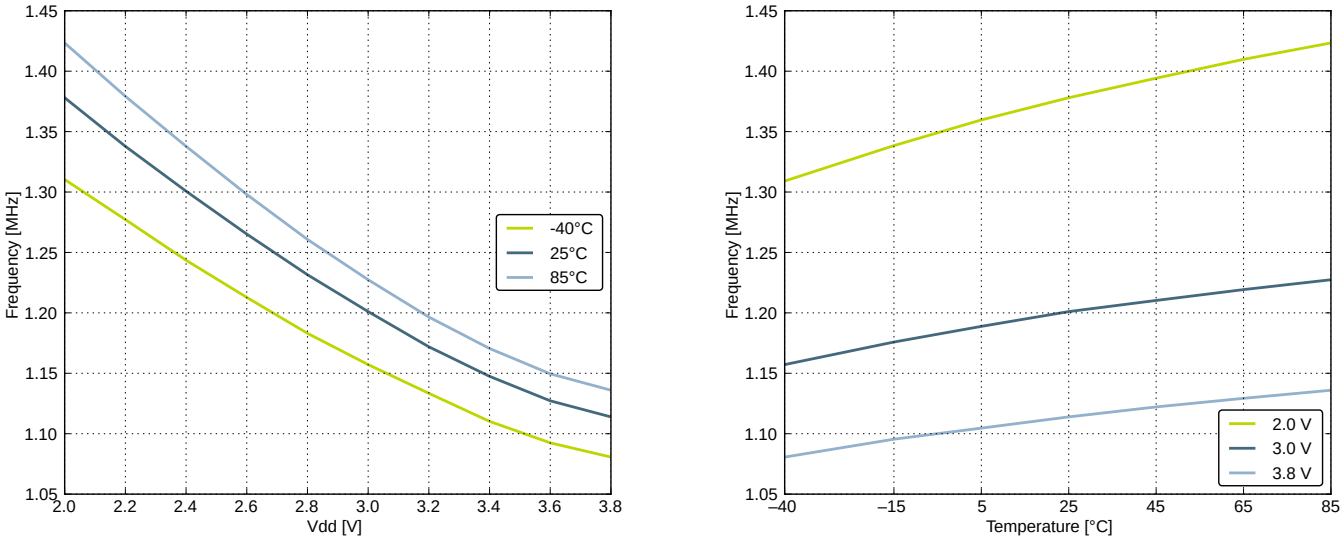


Figure 4.8. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

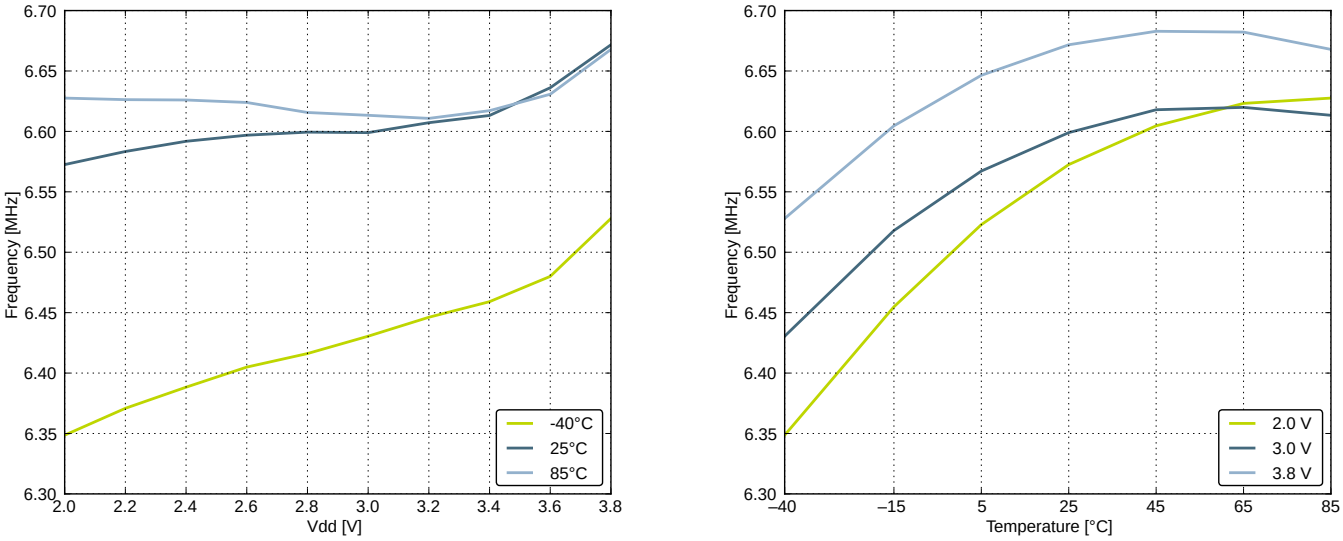


Figure 4.9. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

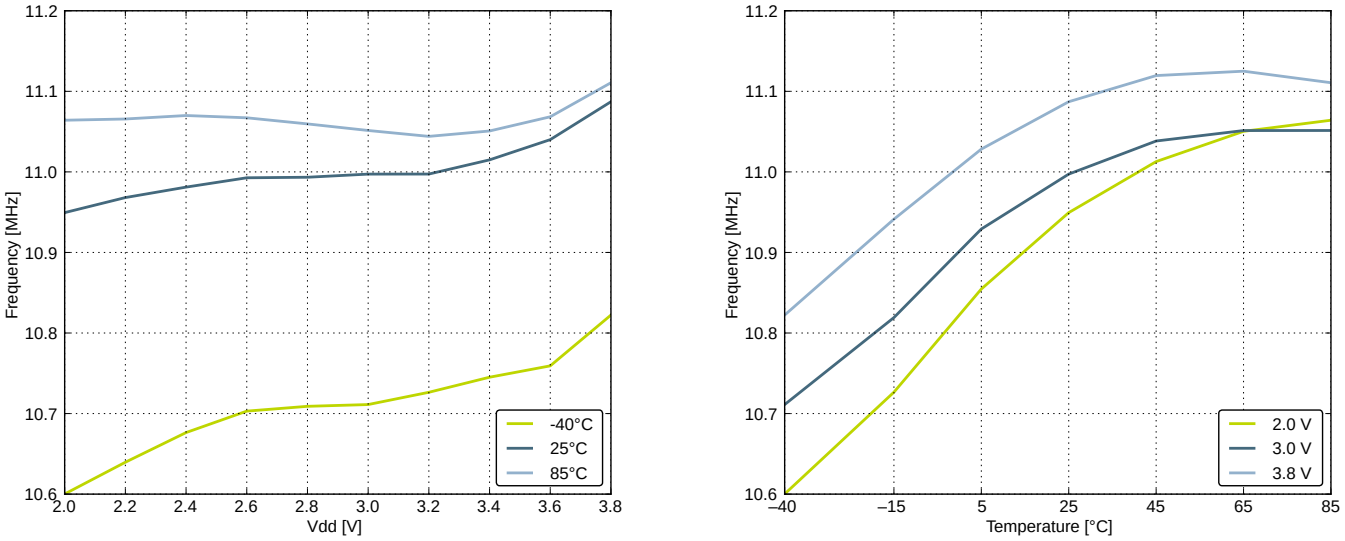


Figure 4.10. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

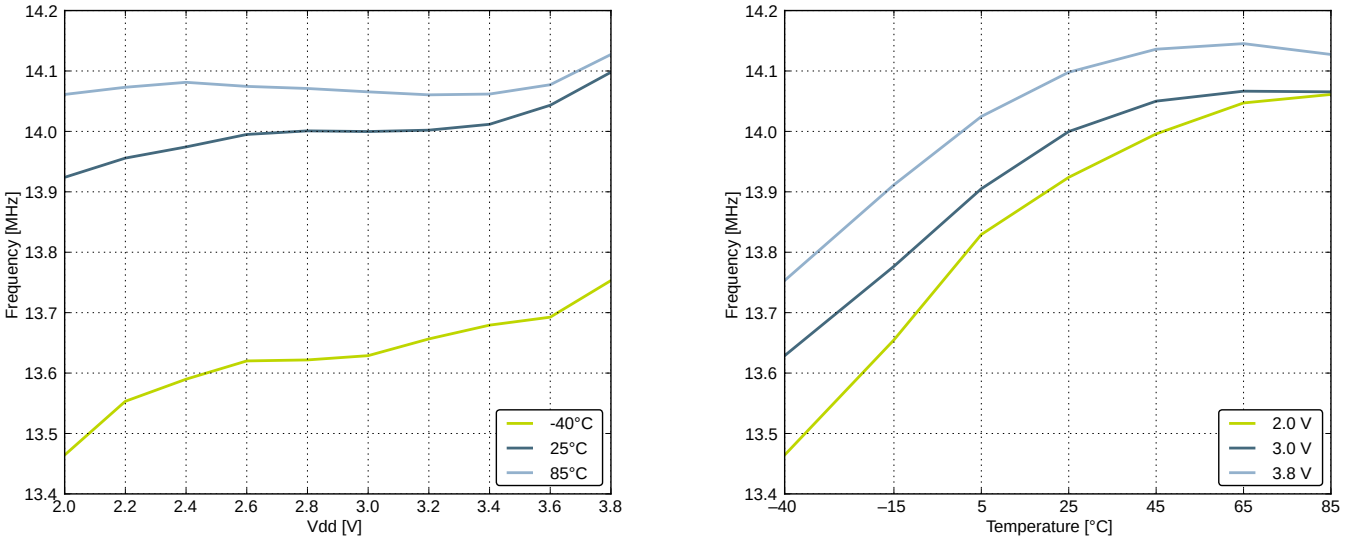


Figure 4.11. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

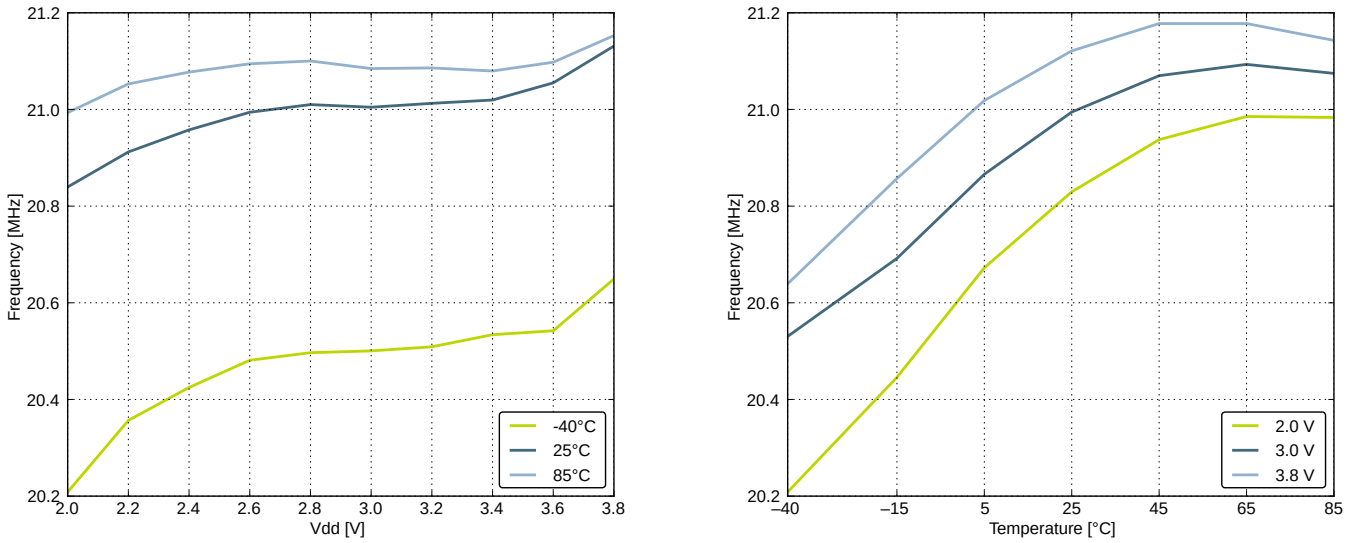


Figure 4.12. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

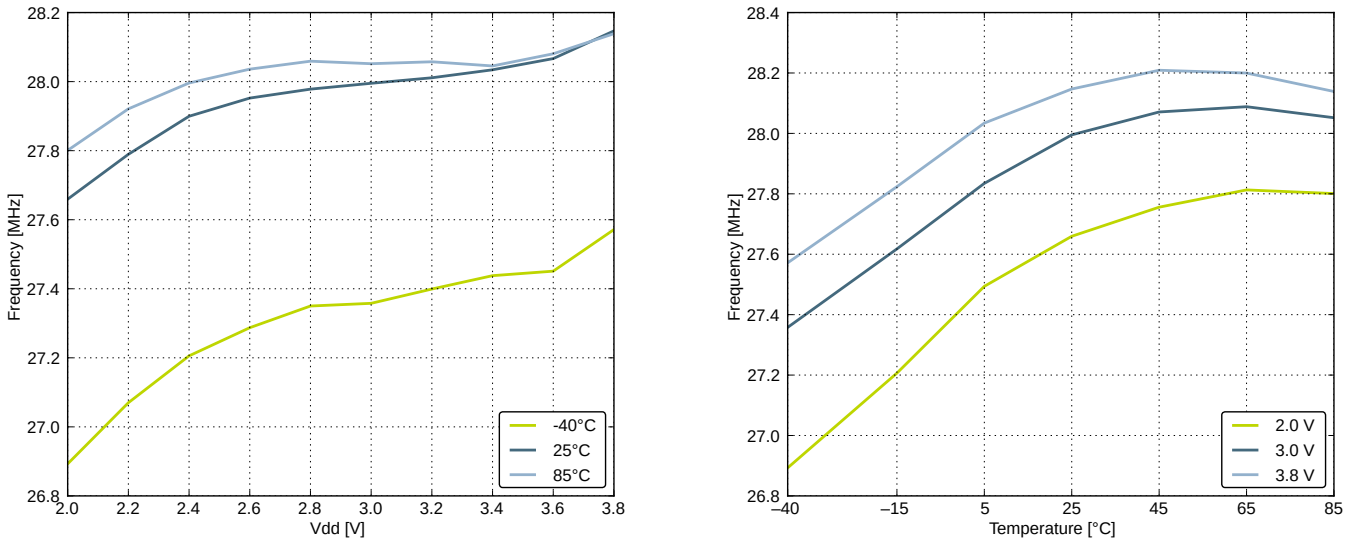


Figure 4.13. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

4.10.5 AUXHFRCO

Table 4.14. AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25 °C	$f_{AUXHFRCO}$	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48[1]	6.60[1]	6.72[1]	MHz
		1 MHz frequency band	1.15[2]	1.20[2]	1.25[2]	MHz
Settling time after start-up	$t_{AUXHFRCO\_settling}$	$f_{AUXHFRCO}$ = 14 MHz	—	0.6	—	Cycles
Frequency step for LSB change in TUNING value	$TUNESTEP_{AUXHFRCO}$		—	0.3[3]	—	%

Note:

1. For devices with prod. rev. < 19, Typ = 7 MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1 MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

4.10.6 ULFRCO

Table 4.15. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}	25 °C, 3 V	0.7		1.75	kHz
Temperature coefficient	TC_{ULFRCO}		—	0.05	—	%/°C
Supply voltage coefficient	VC_{ULFRCO}		—	-18.2	—	%/V

4.11 Analog Digital Converter (ADC)

Table 4.16. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN}$		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{ADCREFIN\_CH7}$	See $V_{ADCREFIN}$	0	—	V_{DD} - 1.1	V
Input range of external positive reference voltage on channel 6	$V_{ADCREFIN\_CH6}$	See $V_{ADCREFIN}$	0.625	—	V_{DD}	V
Common mode input range	$V_{ADCCMIN}$		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	$CMRR_{ADC}$		—	65	—	dB
Average active current	I_{ADC}	1 MSamples/s, 12 bit, external reference	—	351	—	µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00	—	67	—	µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01	—	63	—	µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10	—	64	—	µA
Current consumption of internal voltage reference	I_{ADCREF}	Internal voltage reference	—	65	—	µA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		1	—	—	MOhm
Input RC filter resistance	$R_{ADCFILT}$		—	10	—	kOhm
Input RC filter/decoupling capacitance	$C_{ADCFILT}$		—	250	—	fF
ADC Clock Frequency	f_{ADCCLK}		—	—	13	MHz
Conversion time	$t_{ADCCONV}$	6 bit	7	—	—	ADCCLK Cycles
		8 bit	11	—	—	ADCCLK Cycles
		12 bit	13	—	—	ADCCLK Cycles
Acquisition time	t_{ADCACQ}	Programmable	1	—	256	ADCCLK Cycles

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Required acquisition time for VDD/3 reference	$t_{AD-CACQVDD3}$		2	—	—	µs
Startup time of reference generator and ADC core in NORMAL mode	$t_{ADCSTART}$		—	5	—	µs
Startup time of reference generator and ADC core in KEEPADCWARM mode			—	1	—	µs
Signal to Noise Ratio (SNR)	SNR_{ADC}	1 MSamples/s, 12 bit, single ended, internal 1.25 V reference	—	59	—	dB
		1 MSamples/s, 12 bit, single ended, internal 2.5 V reference	—	63	—	dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference	—	65	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference	—	60	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference	—	65	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference	—	54	—	dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference	—	67	—	dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference	—	69	—	dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference	—	62	—	dB
		200 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	63	—	dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	—	67	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5 V reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	63	66	—	dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference	—	70	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SIgnal-to-Noise And Distortion-ratio (SINAD)	$SINAD_{ADC}$	1 MSamples/s, 12 bit, single ended, internal 1.25 V reference	—	58	—	dB
		1 MSamples/s, 12 bit, single ended, internal 2.5 V reference	—	62	—	dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference	—	64	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference	—	60	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference	—	64	—	dB
		1 MSamples/s, 12 bit, differential, 5V reference	—	54	—	dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference	—	66	—	dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference	—	68	—	dB
		200 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	61	—	dB
		200 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	65	—	dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5V reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66	—	dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference	—	69	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 12 bit, single ended, internal 1.25 V reference	—	64	—	dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5 V reference	—	76	—	dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference	—	73	—	dBc
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference	—	66	—	dBc
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference	—	77	—	dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference	—	76	—	dBc
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference	—	75	—	dBc
		1 MSamples/s, 12 bit, differential, 5V reference	—	69	—	dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	75	—	dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	75	—	dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	—	76	—	dBc
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, 5 V reference	—	78	—	dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79	—	dBc
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference	—	79	—	dBc
Offset voltage	$V_{ADCOFFSET}$	After calibration, single ended	-3.5	0.3	3	mV
		After calibration, differential	—	0.3	—	mV
Thermometer output gradient	$TGRAD_{ADCTH}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/°C
Differential non-linearity (DNL)	DNL_{ADC}		-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL_{ADC}		—	±1.2	±3	LSB
No missing codes	MC_{ADC}		11.999[1]	12	—	bits
Gain error drift	$GAIN_{ED}$	1.25 V reference	—	0.01[2]	0.033[3]	%/°C
		2.5 V reference	—	0.01[2]	0.03[3]	%/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset error drift	$OFFSET_{ED}$	1.25 V reference	—	0.2[2]	0.7[3]	LSB/°C
		2.5 V reference	—	0.2[2]	0.62[3]	LSB/°C

Note:

1. On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78 dBc for a full scale input for chips that have the missing code issue.
2. Typical numbers given by abs(Mean) / (85 - 25).
3. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.14 (p. 33) and Figure 3.15 (p. 33) , respectively.

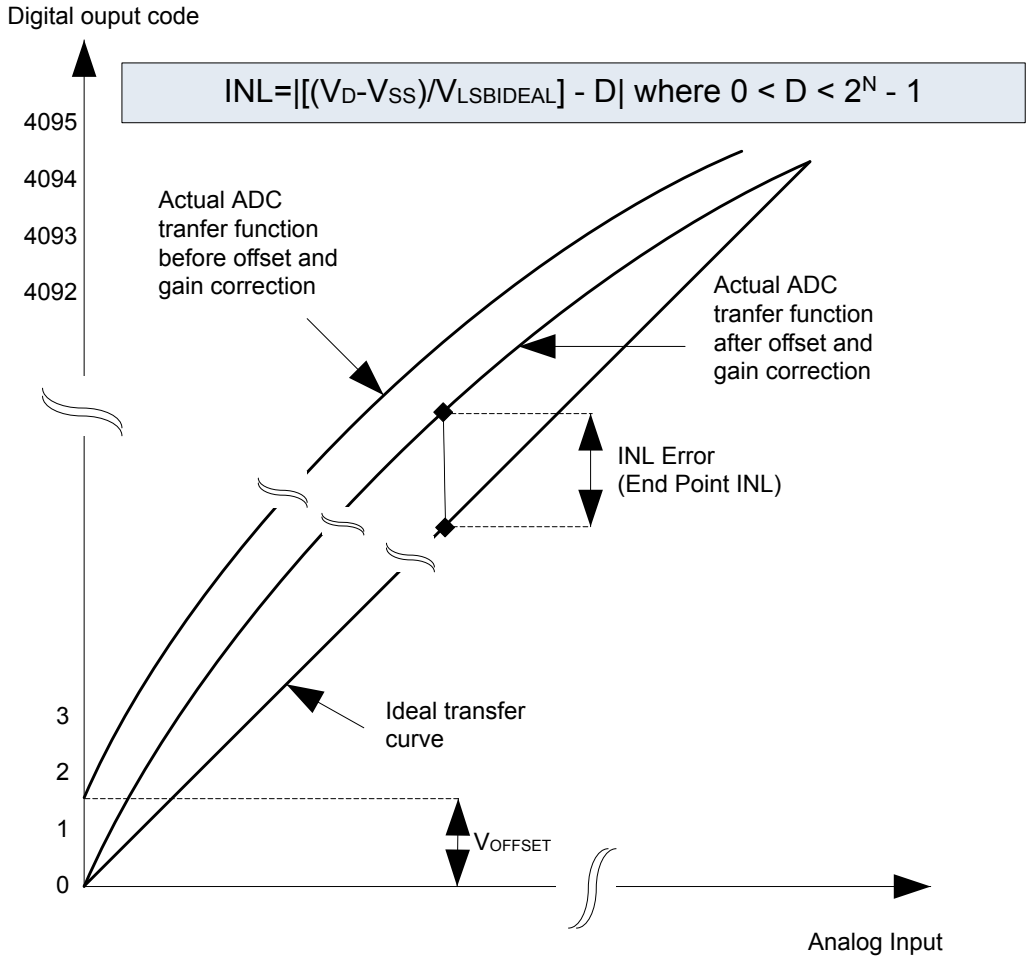


Figure 4.14. Integral Non-Linearity (INL)

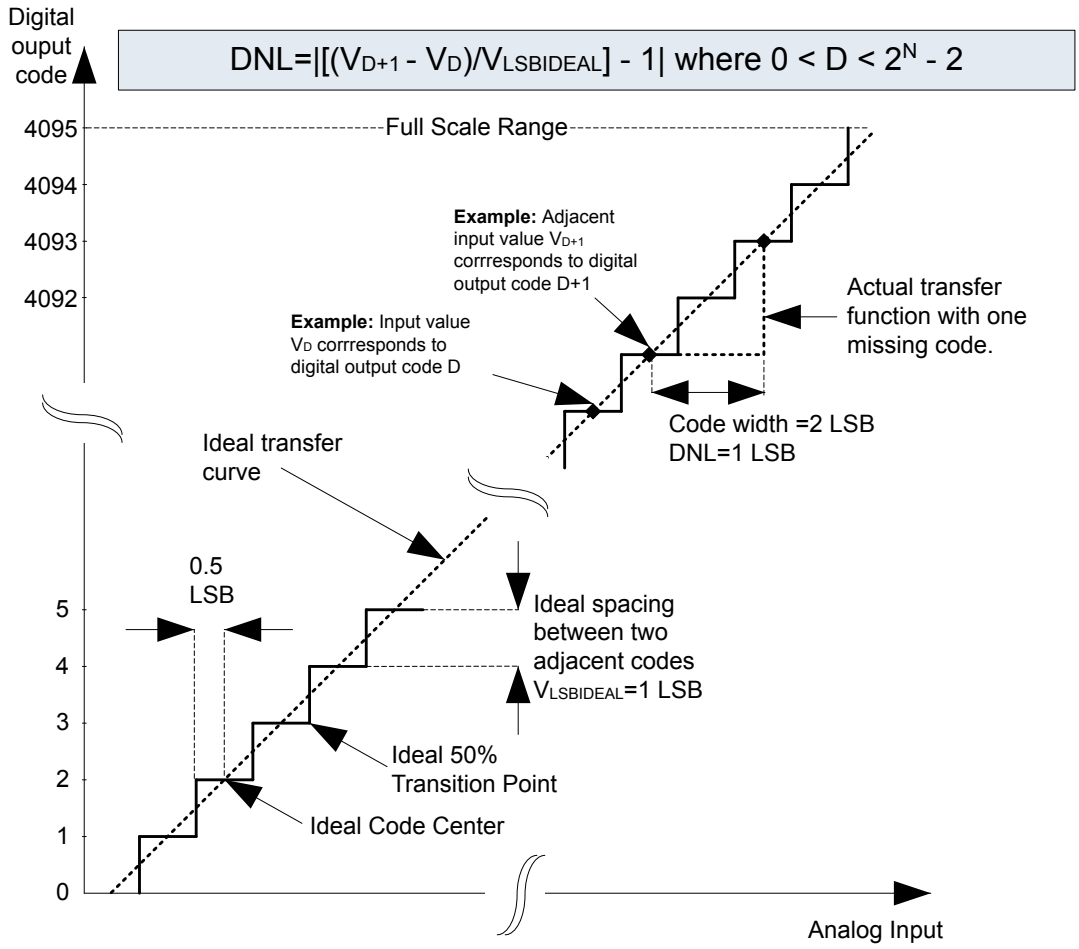
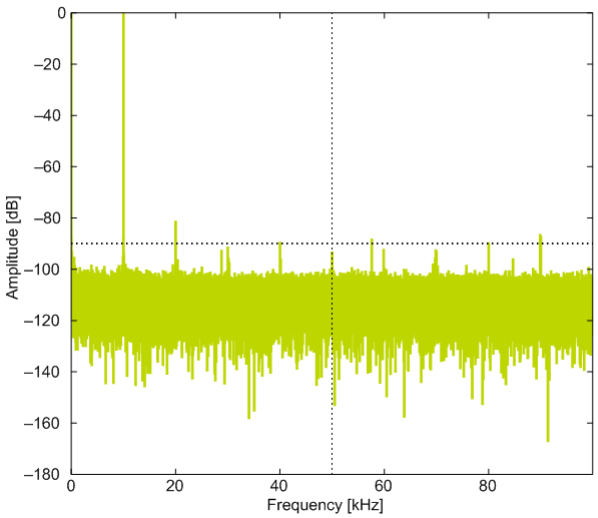
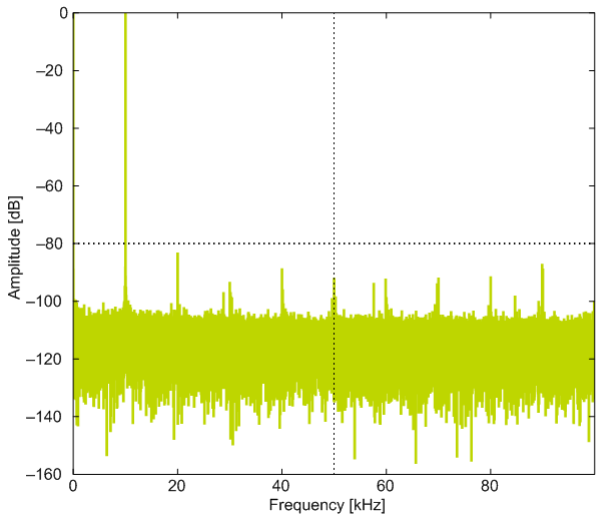


Figure 4.15. Differential Non-Linearity (DNL)

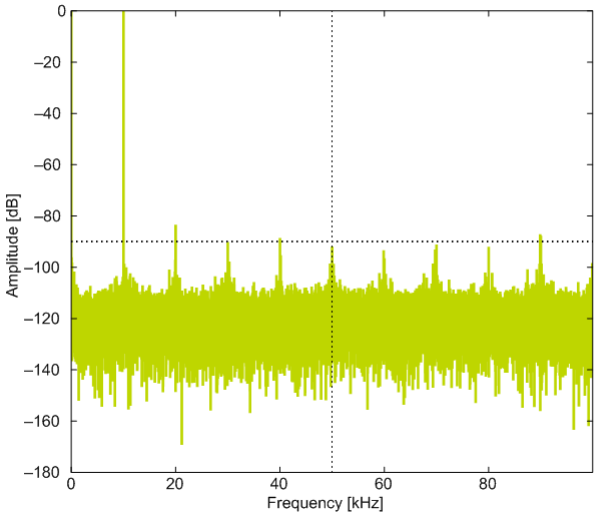
4.11.1 Typical Performance



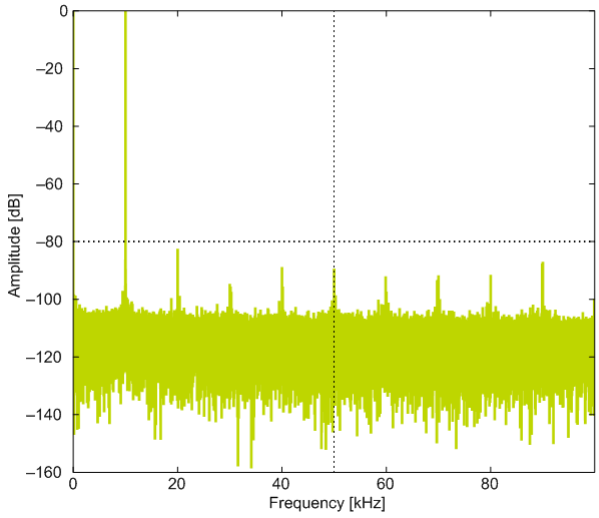
1.25V Reference



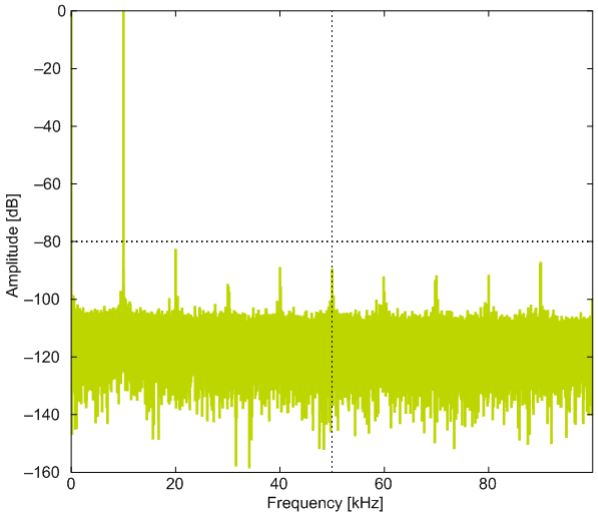
2.5V Reference



2XVDDVSS Reference

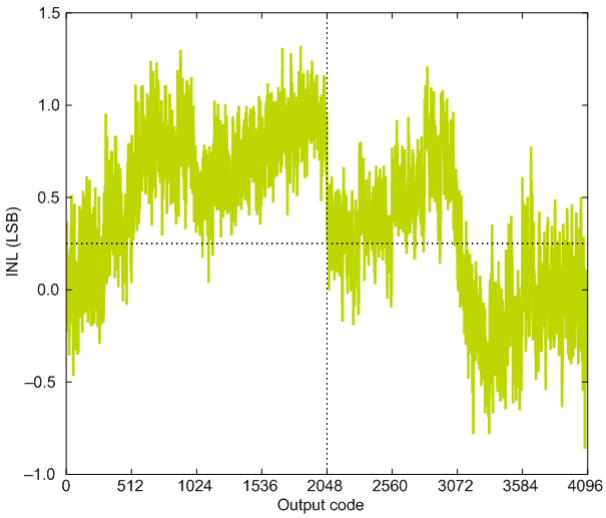


5VDIFF Reference

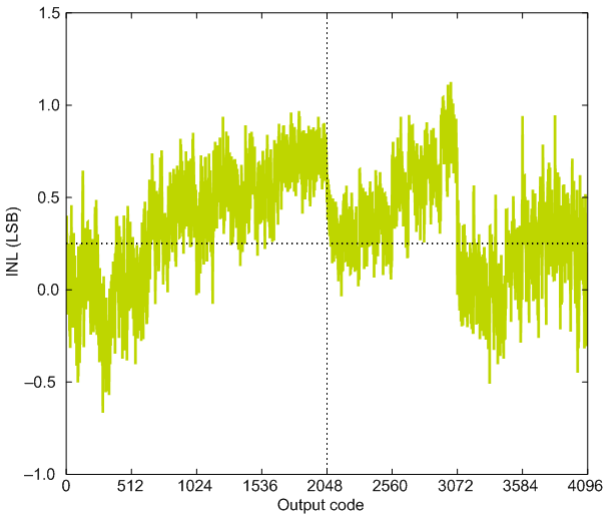


V_{DD} Reference

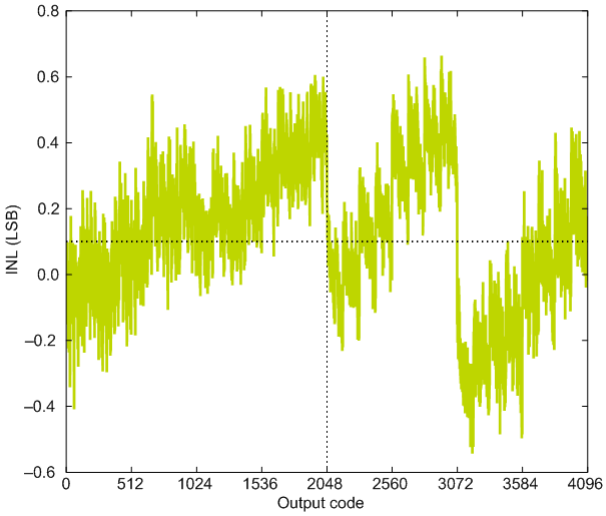
Figure 4.16. ADC Frequency Spectrum, V_{DD} = 3 V, Temp = 25 °C



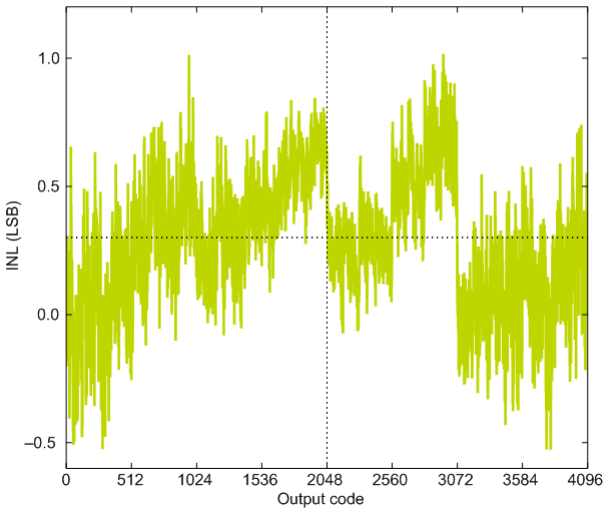
1.25V Reference



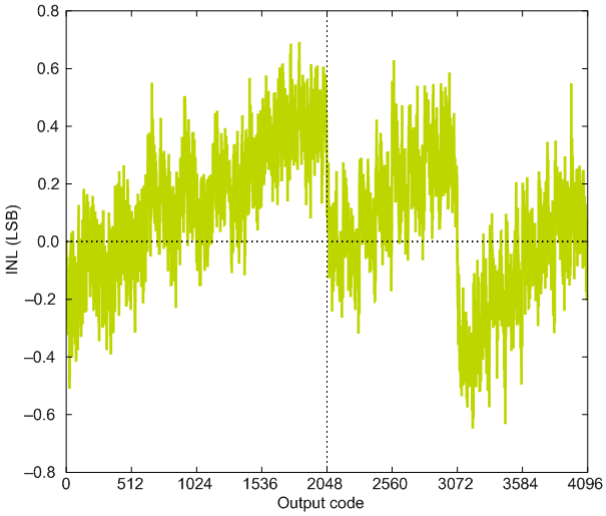
2.5V Reference



2XVDDVSS Reference

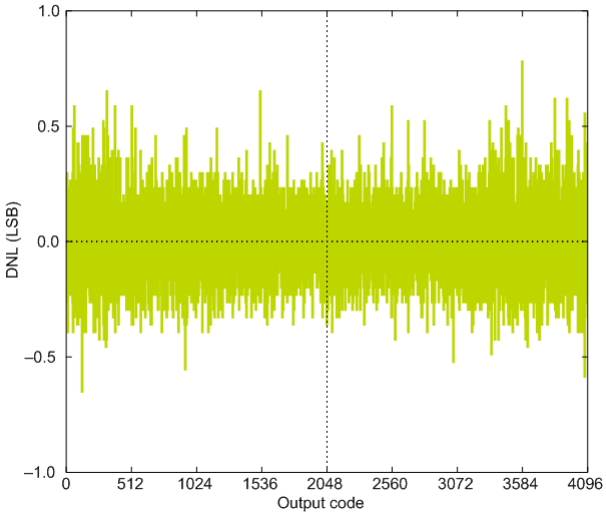


5VDIFF Reference

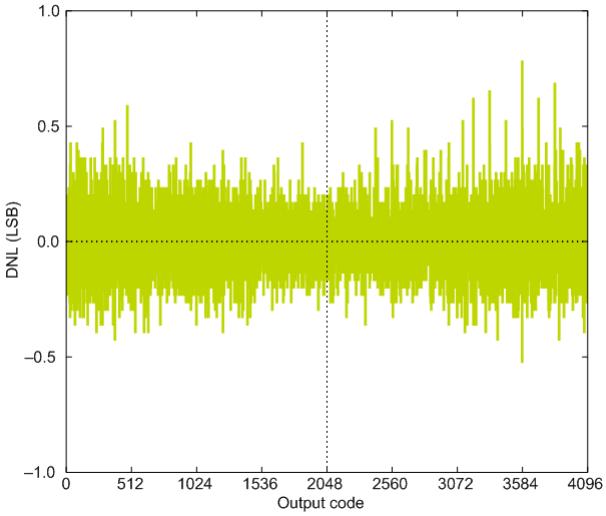


VDD Reference

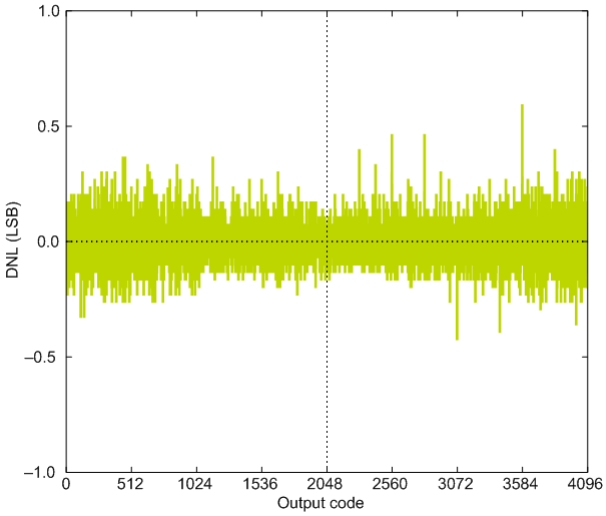
Figure 4.17. ADC Integral Linearity Error vs Code, V_{DD} = 3 V, Temp = 25 °C



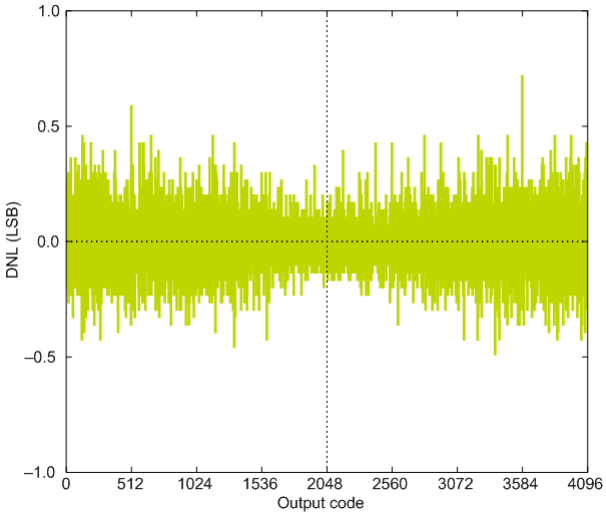
1.25V Reference



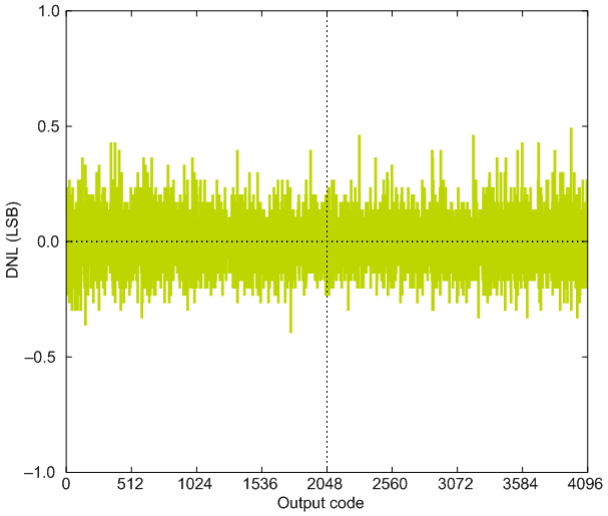
2.5V Reference



2XVDDVSS Reference

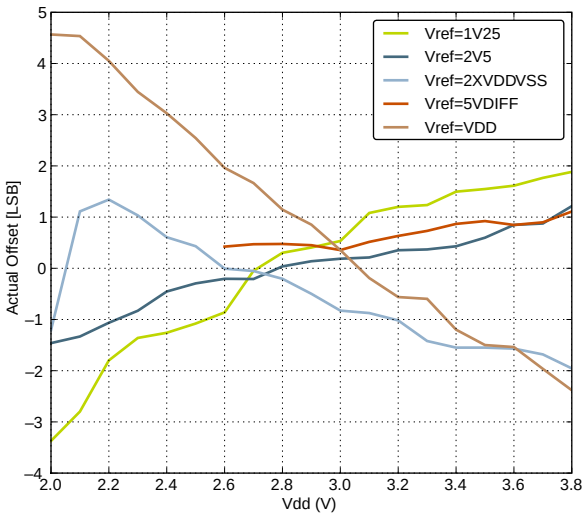


5VDIFF Reference

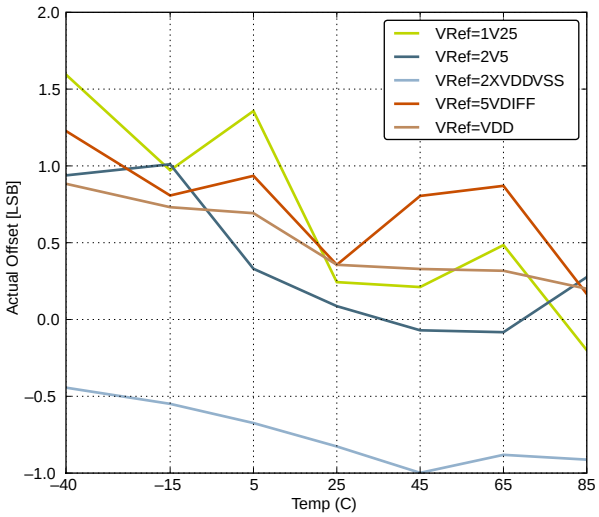


V_{DD} Reference

Figure 4.18. ADC Differential Linearity Error vs Code, V_{DD} = 3 V, Temp = 25 °C

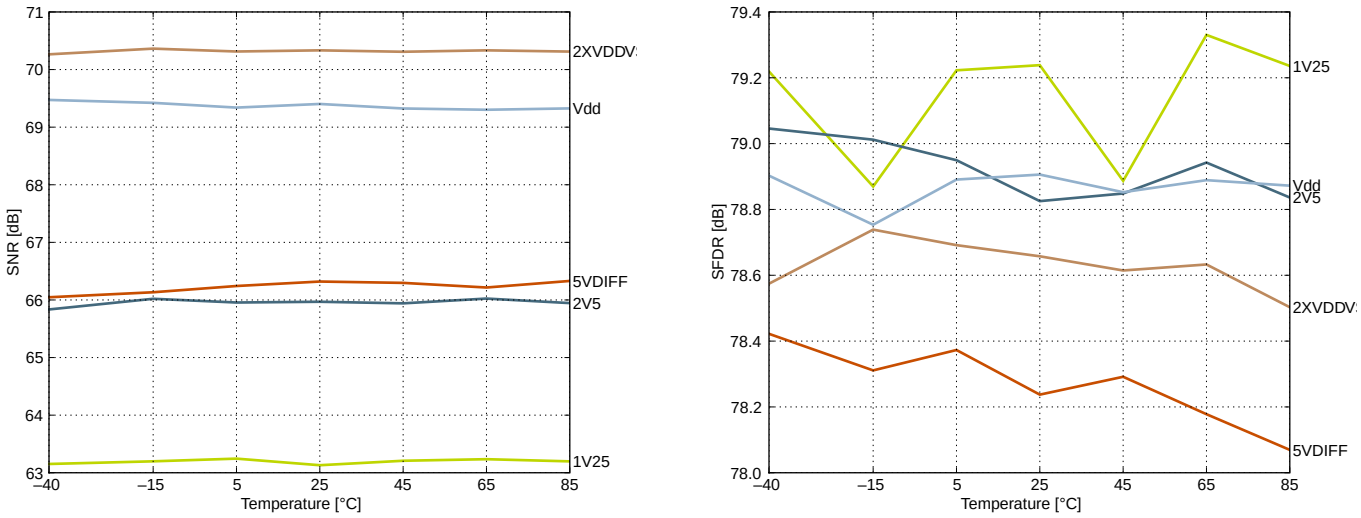


Offset vs Supply Voltage, Temp = 25 °C



Offset vs Temperature, V_{DD} = 3 V

Figure 4.19. ADC Absolute Offset, Common Mode = V_{DD}/2



Signal to Noise Ratio (SNR) **Spurious-Free Dynamic Range (SFDR)**

Figure 4.20. ADC Dynamic Performance vs Temperature for all ADC References, V_{DD} = 3 V

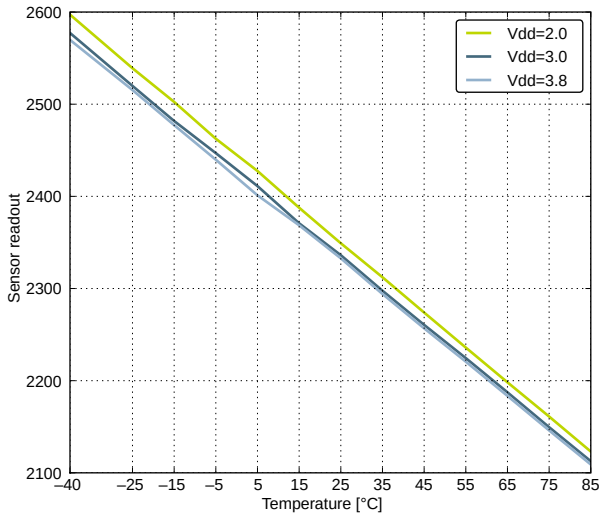


Figure 4.21. ADC Temperature Sensor Readout

4.12 Digital Analog Converter (DAC)

Table 4.17. DAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage range	V_{DACOUT}	VDD voltage reference, single ended	0	—	V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$	—	V_{DD}	V
Output common mode voltage range	V_{DACCM}		0	—	V_{DD}	V
Active current including references for 2 channels	I_{DAC}	500 kSamples/s, 12 bit	—	400[1]	—	µA
		100 kSamples/s, 12 bit	—	200	—	µA
		1 kSamples/s 12 bit NORMAL	—	17	—	µA
Sample rate	SR_{DAC}		—	—	500	ksamples/s
DAC clock frequency	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode	—	—	250	kHz
		Sample/Off Mode	—	—	250	kHz
Clock cyckles per conversion	$CYC_{DAC-CONV}$		—	2	—	
Conversion time	$t_{DACCONV}$		2	—	—	µs
Settling time	$t_{DACSETTLE}$		—	5	—	µs
Signal to Noise Ratio (SNR)	SNR_{DAC}	500 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	59	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	58	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	59	—	dB
Signal to Noise-pulse Distortion Ratio (SNDR)	$SNDR_{DAC}$	500 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	57	—	dB
		500 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	54	—	dB
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	56	—	dB
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	53	—	dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	55	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range(SFDR)	$SFDR_{DAC}$	500 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	62	—	dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	56	—	dBc
		500 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	61	—	dBc
		500 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	55	—	dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference	—	60	—	dBc
Offset voltage	$V_{DACOFF-SET}$	After calibration, single ended	—	2	9	mV
		After calibration, differential	—	2	—	mV
Differential non-linearity	DNL_{DAC}		—	±1	—	LSB
Integral non-linearity	INL_{DAC}		—	±5	—	LSB
No missing codes	MC_{DAC}		—	12	—	bits

Note:

1. Measured with a static input code and no loading on the output.

4.13 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 4.18. OPAMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active Current	I_{OPAMP}	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain	—	370	460	µA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain	—	95	135	µA
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain	—	13	25	µA
Open Loop Gain	G_{OL}	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0	—	101	—	dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1	—	98	—	dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1	—	91	—	dB
Gain Bandwidth Product	GBW_{OPAMP}	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0	—	6.1	—	MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1	—	1.8	—	MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1	—	0.25	—	MHz
Phase Margin	PM_{OPAMP}	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C_L=75 pF	—	64	—	°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C_L=75 pF	—	58	—	°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C_L=75 pF	—	58	—	°
Input Resistance	R_{INPUT}		—	100	—	MΩ
Load Resistance	R_{LOAD}		200	—	—	Ω
DC Load Current	I_{LOAD_DC}		—	—	11	mA
Input Voltage	V_{INPUT}	OPAxHCMDIS=0	V_{SS}	—	V_{DD}	V
		OPAxHCMDIS=1	V_{SS}	—	V_{DD}-1.2	V
Output Voltage	V_{OUTPUT}		V_{SS}	—	V_{DD}	V
Input Offset Voltage	V_{OFFSET}	Unity Gain, V_{SS}<V_{in}<V_{DD}, OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, V_{SS}<V_{in}<V_{DD}-1.2, OPAxHCMDIS=1	—	1	—	mV
Input Offset Voltage Drift	V_{OFFSET_DRIFT}		—	—	0.02	mV/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew Rate	SR_{OPAMP}	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0	—	3.2	—	V/µs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1	—	0.8	—	V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1	—	0.1	—	V/µs
Voltage Noise	N_{OPAMP}	V_{out}=1 V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0	—	101	—	μV_{RMS}
		V_{out}=1 V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1	—	141	—	μV_{RMS}
		V_{out}=1 V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0	—	196	—	μV_{RMS}
		V_{out}=1 V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1	—	229	—	μV_{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0	—	1230	—	μV_{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1	—	2130	—	μV_{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0	—	1630	—	μV_{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1	—	2590	—	μV_{RMS}

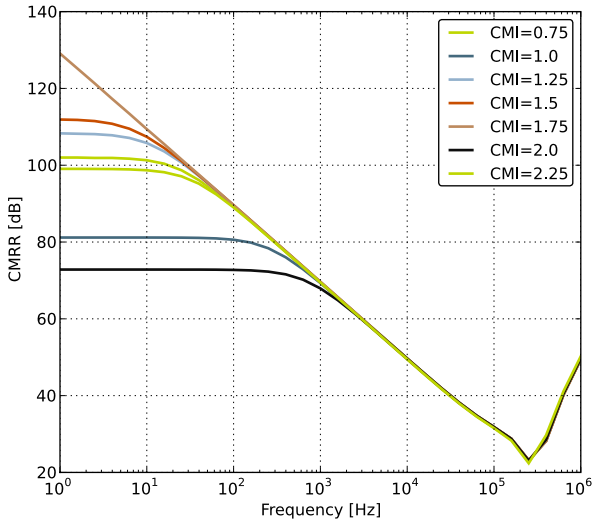


Figure 4.22. OPAMP Common Mode Rejection Ratio

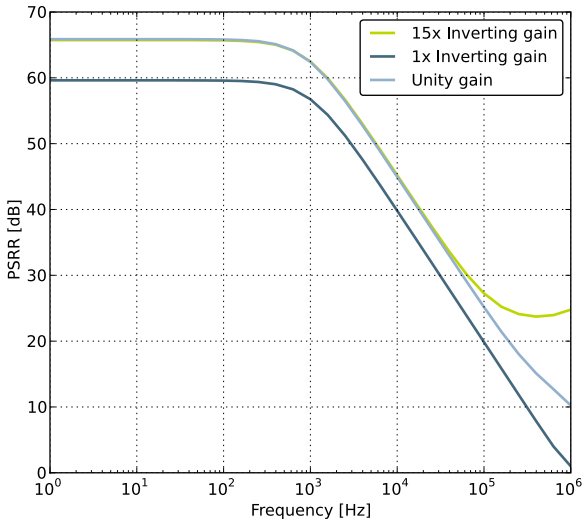


Figure 4.23. OPAMP Positive Power Supply Rejection Ratio

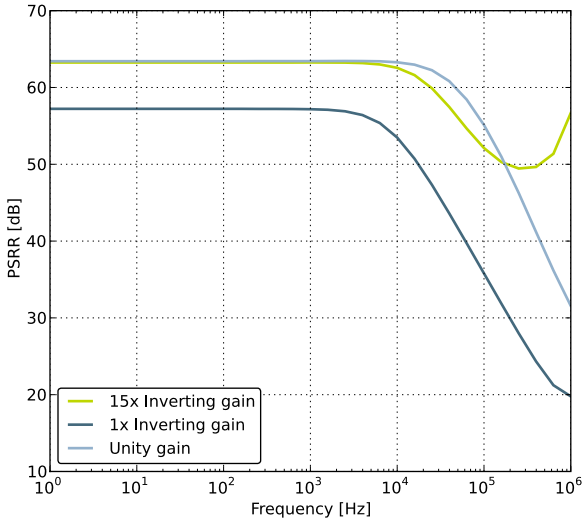


Figure 4.24. OPAMP Negative Power Supply Rejection Ratio

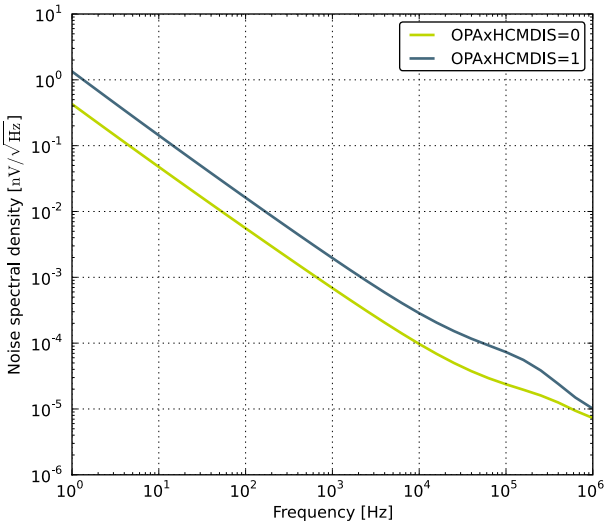


Figure 4.25. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out} = 1 V

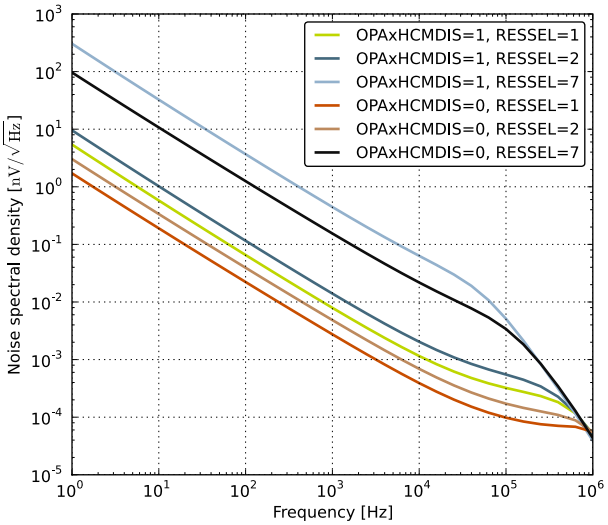


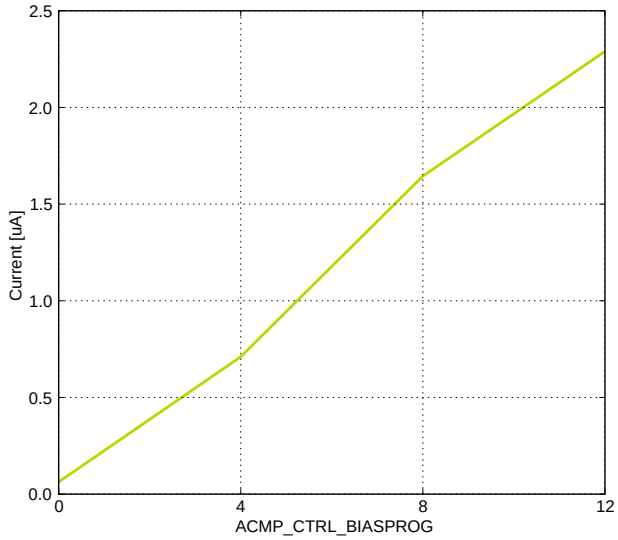
Figure 4.26. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)

4.14 Analog Comparator (ACMP)

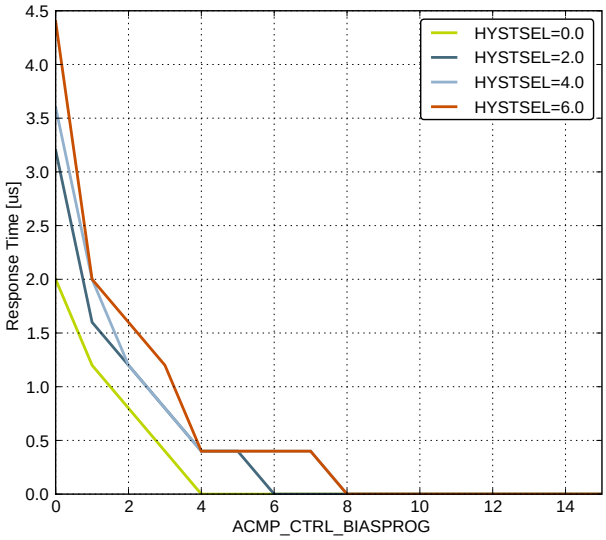
Table 4.19. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}		0	—	V_{DD}	V
ACMP Common Mode voltage range	V_{ACMPCM}		0	—	V_{DD}	V
Active current	I_{ACMP}	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register	—	0.1	0.4	µA
	$I_{ACMPREF}$	BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	—	2.87	15	µA
	$V_{ACMPOFFSET}$	BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register	—	195	520	µA
Current consumption of internal voltage reference	$V_{ACMPHYST}$	Internal voltage reference off. Using external voltage reference	—	0	—	µA
	R_{CSRES}	Internal voltage reference	—	5	—	µA
Offset voltage	$t_{ACMPSTART}$	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
ACMP hysteresis		Programmable	—	17	—	mV
Capacitive Sense Internal Resistance		CSRESSEL=0b00 in ACMPn_INPUTSEL	—	39	—	kΩ
		CSRESSEL=0b01 in ACMPn_INPUTSEL	—	71	—	kΩ
		CSRESSEL=0b10 in ACMPn_INPUTSEL	—	104	—	kΩ
		CSRESSEL=0b11 in ACMPn_INPUTSEL	—	136	—	kΩ
Startup time			—	—	10	µs

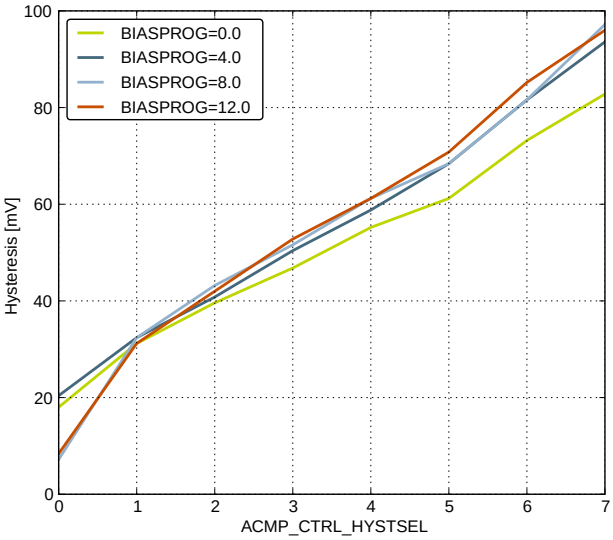
The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given below. $I_{ACMPREF}$ is zero if an external voltage reference is used: $I_{ACMPTOTAL} = I_{ACMP} = I_{ACMPREF}$



Current Consumption, HYSTEL = 4



Response Time



Hysteresis

Figure 4.27. CMP Characteristics, Vdd = 3 V, Temp = 25 °C, FULLBIAS = 0, HALFBIAS = 1

4.15 Voltage Comparator (VCMP)

Table 4.20. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{VCMPIN}		—	V_{DD}	—	V
VCMP Common Mode voltage range	V_{VCMPCM}		—	V_{DD}	—	V
Active current	I_{VCMP}	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register	—	0.3	0.6	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.	—	22	35	µA
Startup time reference generator	$t_{VCMPREF}$	NORMAL	—	10	—	µs
Offset voltage	$V_{VCMPOFFSET}$	Single ended	—	10	—	mV
		Differential	—	10	—	mV
VCMP hysteresis	$V_{VCMPHYST}$		—	61	210	mV
Startup time	$t_{VCMPSTART}$		—	—	10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation: $V_{DD\ Trigger\ Level}$=1.667 V+0.034 ×TRIGLEVEL

4.16 I2C

Table 4.21. I2C Standard-Mode (Sm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	100 [1]	kHz
SCL clock low time	t_{LOW}	4.7	—	—	µs
SCL clock high time	t_{HIGH}	4.0	—	—	µs
SDA set-up time	$t_{SU,DAT}$	250	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	3450 [2, 3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	4.0	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	4.0	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	4.7	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the *EZR32LG Reference Manual*.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450 * 10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 4.22. I2C Fast-Mode (Fm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	400[1]	kHz
SCL clock low time	t_{LOW}	1.3	—	—	µs
SCL clock high time	t_{HIGH}	0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$	100	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	900[2 , 3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.6	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	1.3	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the *EZR32LG Reference Manual*.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900 * 10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 4.23. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000[1]	kHz
SCL clock low time	t_{LOW}	0.5	—	—	µs
SCL clock high time	t_{HIGH}	0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the *EZR32LG Reference Manual*.

4.17 Radio

All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. The data was collected while running off the internal RC oscillator (HFRCO).

4.17.1 EZRadioPRO (R6x) DC Electrical Characteristics

Measured on direct-tie RF evaluation board.

Table 4.24. EZRadioPro DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Saving Modes	$I_{shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	4000	nA
	$I_{standby}$	Register values maintained and RC oscillator/WUT OFF	—	40	9000	nA
	$I_{SleepRC}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	740	10000	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal	—	1.7	—	µA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
Preamble Sense Mode Current	I_{psm}	Duty cycing during preamble search, 1.2 kbps, 4 byte preamble	—	6	—	mA
		Fixed 1s wakeup interval, 50 kbps, 5 byte preamble	—	10	—	µA
TUNE Mode Current	I_{TuneRX}	RX Tune, High Performance Mode	—	7.6	—	mA
	I_{TuneTX}	TX Tune, High Performance Mode	—	7.8	—	mA
RX Mode Current	I_{RXH}	High Performance Mode, 868 MHz, 40 kbps	—	13.7	22	mA
	I_{RXL}	Low Power Mode, 868 MHz, 40 kbps	—	11.1	—	mA
TX Mode Current (R63, R68)	I_{TX+20}	+20 dBm output power, class-E match, 915 MHz, 3.3 V	—	88	108	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	69	80	mA
		+13 dBm output power, class-E match, 915 MHz, 3.3 V	—	44.5	60	mA
TX Mode Current (R60, R67)	I_{TX+10}	+10 dBm output power, class-E match, 868/915 MHz, 3.3 V	—	19.7	—	mA
	I_{TX_+10}	+10 dBm output power, class-E match, 169 MHz, 3.3 V	—	18	—	mA
	I_{TX_+13}	+13 dBm output power, class-E match, 868/915 MHz, 3.3 V	—	22	—	mA
TX Mode Current (R61)	I_{TX_+16}	+16 dBm output power, class-E match, 868 MHz, 3.3 V	—	43	55	mA
	I_{TX_+13}	+13 dBm output power, switched-current match, 868 MHz, 3.3 V	—	33.5	40	mA

4.17.2 EZRadioPRO (R6x) Synthesizer AC Electrical Characteristics

Table 4.25. EZRadioPro Synthensizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Resolution	$F_{RES-1050}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	µs
Phase Noise	$L_{(fM)}$	ΔF = 10 kHz, 169 MHz, High Perf Mode	—	–117	–108	dBc/Hz
		ΔF = 100 kHz, 169 MHz, High Perf Mode	—	–120	–115	dBc/Hz
		ΔF = 1 MHz, 169 MHz, High Perf Mode	—	–138	–135	dBc/Hz
		ΔF = 10 MHz, 169 MHz, High Perf Mode	—	–148	–143	dBc/Hz
		ΔF = 10 kHz, 915 MHz, High Perf Mode	—	–102	–94	dBc/Hz
		ΔF = 100 kHz, 915 MHz, High Perf Mode	—	–105	–97	dBc/Hz
		ΔF = 1 MHz, 915 MHz, High Perf Mode	—	–125	–122	dBc/Hz
		ΔF = 10 MHz, 915 MHz, High Perf Mode	—	–138	–135	dBc/Hz

4.17.3 EZRadioPRO (R6x) Receiver AC Electrical Characteristics

For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.

Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 4.26. EZRadioPro Receiver AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		850	—	1050	MHz
			350	—	525	MHz
			284		350	MHz
			142	—	175	MHz
RX Sensitivity 169 MHz (R68, R67)3	$P_{RX\_0.1}$	(BER < 0.1%) (100 bps, GFSK, BT = 0.5, Δf = ±100 Hz)	—	–133	—	dBm
RX Sensitivity 169 MHz (R60, R61, R63)3	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250 Hz)	—	–129	—	dBm
RX Sensitivity 169 MHz (R60, R61, R63, R67, R68)3	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–110.7	–108	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–106	–104	dBm
	P_{RX_125}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–99	–96	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–89	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–110	–107	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–103	–100	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–97	–93	dBm
RX Sensitivity 915/868 MHz (R68, R67)3	$P_{RX\_0.1}$	(BER < 0.1%) (100 bps, GFSK, BT = 0.5, Δf = ±100 Hz)	—	–132	—	dBm
RX Sensitivity 915/868 MHz (R60, R61, R63)3	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250 Hz)	—	–127	—	dBm
RX Sensitivity 868 MHz (R60, R61, R63, R67, R68)3	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109.9	—	dBm
RX Sensitivity 915 MHz (R60, R61, R63, R67, R68)3		(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109.4	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity 915/868 MHz (R60, R61, R63, R67, R68)3	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–104	–102	dBm
	P_{RX_125}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–97	–92	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110.6	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–88.7	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–108	–104	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–101	–97	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–96	–91	dBm
RX Channel Bandwidth (R60, R61, R63)	BW		1.1	—	850	kHz
RX Channel Bandwidth (R68, R67)			0.2	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from –110 dBm to -90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity, 169 MHz	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz, channel spacing = 12.5 kHz	—	–69	–59	dB
±1-Ch Offset Selectivity, 450 MHz			—	–60	–50	dB
±1-Ch Offset Selectivity, 868 / 915 MHz			—	–52.5	–45	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz	—	–79	–68	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	–86	–75	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image Rejection (IF = 468.75 kHz)	Im_{REJ}	No image rejection calibration. Rejection at the image frequency. RF = 460 MHz	30	40	—	dB
		With image rejection calibration. Rejection at the image frequency. RF = 460 MHz	40	55	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 915 MHz	30	45	—	dB
		With image rejection calibration. Rejection at the image frequency. RF = 915 MHz	40	52	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 169 MHz	35	45	—	dB
		With image rejection calibration. Rejection at the image frequency. RF = 169 MHz	45	60	—	dB

4.17.4 EZRadioPRO (R6x) Transmitter AC Electrical Characteristics

The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).

Default API setting for modulation deviation resolution is double the typical value specified.

Output power is dependent on matching components and board layout.

Table 4.27. EZRadioPro Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
(G)FSK Data Rate	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{420}	350–420 MHz	—	600	—	kHz
	Δf_{350}	283–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Resolution	$F_{RES-1050}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Output Power Range (R63)	P_{TX63}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+20	dBm
Typical Output Power Range (R61)	P_{TX61}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–40		+16	dBm
Typical Output Power Range at (R60)	P_{TX60}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+12.5	dBm
Typical Output Power Range at (R68)	P_{TX68}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+20	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Typical Output Power Range at (R67)	P_{TX67}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+12.5	dBm
Output Power Variation (R63, R68)		At 20 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	19	20	21	dBm
Output Power Variation (R60, R67)		At 10 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	9	10	11	dBm
Output Power Variation (R63, R68)		At 20 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	18.5	20	21	dBm
Output Power Variation (R60, R67)		At 10 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	9.5	10	10.5	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.25	0.4	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2.3	3	dB
TX RF Output Level Variation vs. Frequency	$\Delta P\text{-}RF_{FREQ}$	Measured across 902–928 MHz	—	0.6	1.7	dB
Transmit Modulation Filtering	B×T	Gaussian Filtering Bandwith Time Product	—	0.5	—	

4.17.5 EZRadioPRO (R6x) Radio Auxillary Block Specifications

Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested by bench characterization.

XTAL Range tested in production using an external clock source (similar to using a TCXO).

Table 4.28. EZRadioPro Auxiliary Block Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XTAL Range	$XTAL_{RANGE}$		25	—	32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	300	—	uS
30 MHz XTAL Cap Resolution	$30M_{RES}$		—	70	—	fF
32 kHz XTAL Start-Up Time	t_{32K}		—	2	—	sec
32 kHz Accuracy using Internal RC Oscillator	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	—	6	ms

4.17.6 EZRadio (R55) DC Electrical Characteristics

Table 4.29. EZRadio DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Saving Modes	$I_{shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	—	nA
	$I_{standby}$	Register values maintained	—	40	—	nA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
	$I_{SPIActive}$	SPI active state	—	1.5	—	mA
TUNE Mode Current	I_{TuneRX}	RX Tune	—	6.8	—	mA
	I_{TuneTX}	TX Tune	—	7.1	—	mA
RX Mode Current	I_{RX}	Measured at 40 kbps, 20 kHz deviation, 315 MHz	—	10.9	—	mA
TX Mode Current	I_{TX}	+10 dBm output power, measured on direct tie RF evaluation board at 868 MHz	—	19	—	mA
		+13 dBm output power, measured on direct tie RF evaluation board at 868 MHz	—	24	—	mA

4.17.7 EZRadio (R55) Synthesizer AC Electrical Characteristics

Table 4.30. EZRadio Synthensizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		284	—	350	MHz
			350	—	525	MHz
			850	—	960	MHz
Synthesizer Frequency Resolution	$F_{RES-960}$	850-960 MHz	—	114.4	—	Hz
	$F_{RES-525}$	420-525 MHz	—	57.2	—	Hz
	$F_{RES-350}$	283-350 MHz	—	38.1	—	Hz
Phase Noise	$L_{(fM)}$	ΔF = 10 kHz, 915 MHz	—	100	—	dBc/Hz
		ΔF = 100 kHz, 915 MHz	—	102.1	—	dBc/Hz
		ΔF = 1 MHz, 915 MHz	—	123.5	—	dBc/Hz
		ΔF = 10 MHz, 915 MHz	—	136.6	—	dBc/Hz

4.17.8 EZRadio (R55) Receiver AC Electrical Characteristics

Table 4.31. EZRadio Receiver AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		284	—	350	MHz
			350	—	525	MHz
			850	—	960	MHz
RX Sensitivity 915 MHz	P_{RX_2}	(BER < 0.1%) (2.4 kbps, GFSK, BT = 0.5, Δf = ±30 kHz, 114 kHz RX BW)	—	-115	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±25 kHz, 114 kHz RX BW)	—	-107.6	—	dBm
	P_{RX_128}	(BER < 0.1%) (128 kbps, GFSK, BT = 0.5, Δf = ±70 kHz, 305 kHz RX BW)	—	-102.4	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 1 kbps, 185 kHz Rx BW, OOK, PN15 data)	—	-113.5	—	dBm
		(BER < 0.1%, 40 kbps, 185 kHz BW, OOK, PN15 data)	—	-102.7	—	dBm
RX Channel Bandwidth	BW		40	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from -110 dBm to -90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, RX channel BW = 58 kHz, channel spacing = 100 kHz	—	-50	—	dB
±2-Ch Offset Selectivity	$C/I_{2\text{-}CH}$		—	-56	—	dB
Blocking 200 kHz−1 MHz	$200K_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, RX channel BW = 58 kHz	—	-56	—	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$		—	-71	—	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	-71	—	dB
Image Rejection	Im_{REJ}	Rejection at the image frequency IF = 468 kHz	—	40	—	dB

4.17.9 EZRadio (R55) Transmitter AC Electrical Characteristics

The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).

Conducted measurements based on RF evaluation board. Output power and emissions specifications are dependent on transmit frequency, matching components, and board layout.

Table 4.32. EZRadio Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		284	—	350	MHz
			350	—	525	MHz
			850	—	960	MHz
(G)FSK Data Rate	DR_{FSK}		1.0	—	500	kbps
OOK Data Rate	DR_{OOK}		0.5	—	120	kbps
Modulation Deviation Range	Δf_{960}	850-960 MHz	—	—	500	kHz
	Δf_{525}	350-525 MHz	—	—	500	kHz
	Δf_{350}	284-350 MHz	—	—	500	kHz
Modulation Deviation Resolution	$F_{RES-960}$	850-960 MHz	—	114.4	—	Hz
	$F_{RES-525}$	420-525 MHz	—	57.2	—	Hz
	$F_{RES-420}$	350-420 MHz	—	45.6	—	Hz
	$F_{RES-350}$	284-350 MHz	—	38.1	—	Hz
Output Power Range	P_{TX}	Measured at 434 MHz, 3.3 V, Class E match	-20	—	+13	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.25	—	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	-40 to +85 °C	—	2.3	—	dB
TX RF Output Level Variation vs. Frequency	$\Delta P\text{-}RF_{FREQ}$	Measured across 902-928 MHz	—	0.6	—	dB
Transmit Modulation Filtering	B×T	Gaussian Filtering Bandwith Time Product	—	0.5	—	

4.17.10 EZRadio (R55) Radio Auxiliary Block Specifications

XTAL Range tested in production using an external clock source (similar to using a TCXO).

Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested by bench characterization.

Table 4.33. EZRadio Auxilliary Block Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XTAL Range	$XTAL_{RANGE}$		25		32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	300	—	us
30 MHz XTAL Cap Resolution	$30M_{RES}$		—	70	—	Ff
POR Reset Time	t_{POR}		—	—	6	ms

4.17.11 EZRadioPRO/EZRadioPRO Digital I/O Specification

6.7 ns is typical for GPIO0 rise time.

Assuming V_{DD} = 3.3 V, drive strength is specified at V_{OH} (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.

2.4 ns is typical for GPIO0 fall time.

Table 4.34. EZRadio/Pro Digital I/O Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2.3	—	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD_RF} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD_RF} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< VDD	-1	—	1	uA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	4	uA
Drive Strength for Output Low Level3	I_{OmaxLL}	DRV[1:0] = LL	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	1.13	—	mA
Drive Strength for Output High Level3	I_{OmaxLL}	DRV[1:0] = LL	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	0.96	—	mA
Drive Strength for Output High Level for GPIO3	I_{OmaxLL}	DRV[1:0] = LL	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	1.7	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD_RF} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD_RF} x 0.2	V

4.18 Digital Peripherals

Table 4.35. Digital Peripherals

Parameter	Symbol	Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	4.0	—	µA/MHz
UART current	I_{UART}	UART idle current, clock enabled	—	3.8	—	µA/MHz
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	194	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	7.6	—	µA/MHz
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	6.5	—	µA/MHz
LETIMER current	$I_{LETIMER}$	LETIMER idle current, clock enabled	—	86	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	91	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	55	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	1.8	—	µA/MHz
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	3.4	—	µA/MHz
PRS current	I_{PRS}	PRS idle current	—	3.9	—	µA/MHz
DMA current	I_{DMA}	Clock enable	—	10.9	—	µA/MHz

5. Pinout and Package

Note: Please refer to the application note *AN0002: EFM32 Hardware Design Considerations* for guidelines on designing Printed Circuit Boards (PCB's) for the EZR32LG230.

5.1 Pinout

The EZR32LG230 pinout is shown in below. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

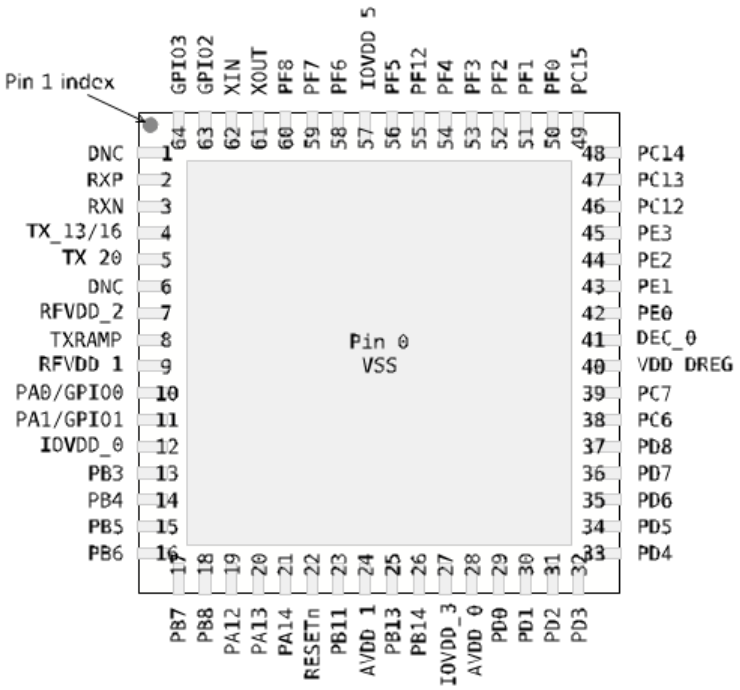


Figure 5.1. Pinout (top view, not to scale)

5.2 Pin Descriptions

Table 5.1. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	NC	No connect.			
2	RXP	Differential RF Input Pin of the LNA. See application schematic for example matching network.			
3	RXN	Differential RF Input Pin of the LNA. See application schematic for example matching network.			
4	TX_13/16	Transmit Output Pin (+13 dBm or +16 dBm) for R55, R60, R61, R67 and R69 variants. The PA output is an open-drain connection, so the L-C match must supply VDD (+3.3 VDC nominal) to this pin. Pin is DNC on the +20 dBm parts.			
5	TX_20	Transmit Output Pin (+20 dBm) for R63, R68 and R69 variants. The PA output is an open-drain connection, so the L-C match must supply VDD (+3.3 VDC nominal) to this pin. Pin is DNC on the +13 dBm parts.			
6	NC	No connect.			
7	RFVDD_2	+1.8 to +3.6 V Supply Voltage Input to Internal Regulators for the Radio. The recommended VDD supply voltage is +3.3 V.			
8	TXRAMP	Programmable Bias Output with Ramp Capability for External FET PA.			
9	RFVDD_1	+1.8 to +3.6 V Supply Voltage Input to Internal Regulators for the Radio. The recommended VDD supply voltage is +3.3 V.			
10	PA0/GPIO0[1]		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0 RF_GPIO0
11	PA1/GPIO1[1]		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0 RF_GPIO1
12	IOVDD_0	Digital IO power supply 0.			
13	PB3		PCNT1_S0IN #1	US2_TX #1	
14	PB4		PCNT1_S1IN #1	US2_RX #1	
15	PB5			US2_CLK #1	
16	PB6			US2_CS #1	
17	PB7	LFXTAL_P	TIM1_CC0 #3	USRF0_TX #4	
18	PB8	LFXTAL_N	TIM1_CC1 #3	USRF0_RX #4	
19	PA12		TIM2_CC0 #1		
20	PA13		TIM2_CC1 #1		
21	PA14		TIM2_CC2 #1		
22	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
23	PB11		TIM1_CC2 #3 LE-TIM0_OUT0 #1		
24	AVDD_1	Analog power supply 1.			
25	PB13	HFXTAL_P		LEU0_TX #1	

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
26	PB14	HFXTAL_N		LEU0_RX #1	
27	IOVDD_3	Digital IO power supply 3.			
28	AVDD_0	Analog power supply 0.			
29	PD0	ADC0_CH0 OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
30	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
31	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	DBG_SWO #3
32	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
33	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
34	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
35	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 BOOT_RX
36	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_AL-TEX1 #0 ACMP1_O #2 ETM_TCLK #0 BOOT_TX
37	PD8	BU_VIN			CMU_CLK1 #1
38	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
39	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
40	VDD_DREG	Power supply for on-chip voltage regulator.			
41	DEC_0	Decouple output for on-chip voltage regulator.			
42	PE0		TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
43	PE1		TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
44	PE2	BU_VOUT	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
45	PE3	BU_STAT		U1_RX #3	ACMP1_O #1
46	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT		U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
47	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
48	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	LES_CH14 #0

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
49	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	LES_CH15 #0 DBG_SWO #1
50	PF0		TIM0_CC0 #5 LE-TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
51	PF1		TIM0_CC1 #5 LE-TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
52	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
53	PF3		TIM0_CDTI0 #2/5		PRS_CH0 #1
54	PF4		TIM0_CDTI1 #2/5		PRS_CH1 #1
55	PF12				
56	PF5		TIM0_CDTI2 #2/5		PRS_CH2 #1
57	IOVDD_5	Digital IO power supply 5.			
58	PF6		TIM0_CC0 #2		
59	PF7		TIM0_CC1 #2		
60	PF8		TIM0_CC2 #2		
61	XOUT	EZRadio peripheral crystal oscillator output. Connect to an external 26/30 MHz crystal or to an external clock source. If using an external clock source with no crystal, dc coupling with a nominal 0.8 VDC level is recommended with a minimum ac amplitude of 700 mVpp. Refer to AN417 for more details about using an external clock source.			
62	XIN	EZRadio peripheral crystal oscillator input. Connect to an external 26/30 MHz crystal or leave floating if driving the XOUT pin with an external signal source.			
63	GPIO2	General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.			
64	GPIO3	General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.			

Note:

1. General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFOStatus, POR, Wake-up Timer, TRSW, AntDiversity control, etc.

5.3 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.
Note: Some functionality, such as analog interfaces, do no have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to the LOCATION 0.

Table 5.2. Alternate functionality overview

Alternate	LOCATION						
Functionality	0	1	2	3	4	5	Description
ACMP0_CH6	PC6						Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7						Analog comparator ACMP0, channel 7.
ACMP0_O		PE2	PD6				Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12						Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13						Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14						Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15						Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7				Analog comparator ACMP1, digital output.
ADC0_CH0	PD0						Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1						Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2						Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3						Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4						Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5						Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6						Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7						Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PD6						Bootloader RX.
BOOT_TX	PD7						Bootloader TX.
BU_STAT	PE3						Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8						Battery input for Backup Power Domain
BU_VOUT	PE2						Power output for Backup Power Domain
CMU_CLK0		PC12	PD7				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1/ GPIO1	PD8					Clock Management Unit, clock output number 1.

Alternate	LOCATION						
Functionality	0	1	2	3	4	5	Description
DAC0_N1 / OPAMP_N1	PD7						Operational Amplifier 1 external negative input.
OPAMP_N2	PD3						Operational Amplifier 2 external negative input.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1		Digital to Analog Converter DAC0_OUT1ALT /OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0					Operational Amplifier 2 output.
DAC0_P1 / OPAMP_P1	PD6						Operational Amplifier 1 external positive input.
OPAMP_P2	PD4						Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6				Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0/ GPIO0						Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1						Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2						Pin can be used to wake the system up from EM4
HFXTAL_N	PB14						High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13						High Frequency Crystal positive pin.
I2C0_SCL	PA1/ GPIO1	PD7	PC7			PF1	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0/ GPIO0	PD6	PC6			PF0	I2C0 Serial Data input / output.
I2C1_SCL			PE1				I2C1 Serial Clock Line input / output.
I2C1_SDA			PE0				I2C1 Serial Data input / output.
LES_ALTEX0	PD6						LESENSE alternate exite output 0.
LES_ALTEX1	PD7						LESENSE alternate exite output 1.
LES_CH6	PC6						LESENSE channel 6.
LES_CH7	PC7						LESENSE channel 7.

Alternate	LOCATION						
Functionality	0	1	2	3	4	5	Description
LES_CH12	PC12						LESENSE channel 12.
LES_CH13	PC13						LESENSE channel 13.
LES_CH14	PC14						LESENSE channel 14.
LES_CH15	PC15						LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14		PF1	PA0/ GPIO0		LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7						LEUART1 Receive input.
LEU1_TX	PC6						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8						Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7						Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0		PD6			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1		PD7			Pulse Counter PCNT0 input number 1.
PCNT1_S0IN		PB3					Pulse Counter PCNT1 input number 0.
PCNT1_S1IN		PB4					Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0/ GPIO0	PF3					Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1/ GPIO1	PF4					Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5					Peripheral Reflex System PRS, channel 2.
RF_GPIO0	PA0/ GPIO0						RF GPIO0.
RF_GPIO1	PA1/ GPIO1						RF GPIO1.
TIM0_CC0	PA0/ GPIO0	PA0/ GPIO0	PF6	PD1	PA0/ GPIO0	PF0	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1/ GPIO1	PA1/ GPIO1	PF7	PD2		PF1	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2			PF8	PD3		PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13	PF3	PC13		PF3	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14	PF4	PC14		PF4	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15	PF5	PC15		PF5	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13			PB7	PD6		Timer 1 Capture Compare input / output channel 0.

Alternate	LOCATION						
Functionality	0	1	2	3	4	5	Description
TIM1_CC1	PC14			PB8	PD7		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15			PB11	PC13		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0		PE0					Timer 3 Capture Compare input / output channel 0.
TIM3_CC1		PE1					Timer 3 Capture Compare input / output channel 1.
TIM3_CC2		PE2					Timer 3 Capture Compare input / output channel 2.
U0_RX		PE1		PC15			UART0 Receive input.
U0_TX		PE0		PC14			UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13			PE3			UART1 Receive input.
U1_TX	PC12			PE2			UART1 Transmit output. Also used as receive input in half duplex communication.
US1_CLK		PD2	PF0				USART1 clock input / output.
US1_CS		PD3	PF1				USART1 chip select input / output.
US1_RX		PD1	PD6				USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX		PD0	PD7				USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK		PB5					USART2 clock input / output.
US2_CS		PB6					USART2 chip select input / output.
US2_RX		PB4					USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX		PB3					USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USRF0_RX					PB8		USARTRF0 Asynchronous Receive. USARTRF0 Synchronous mode Master Input / Slave Output (MISO).
USRF0_TX					PB7		USARTRF0 Asynchronous Transmit.Also used as receive input in half duplex communication. USARTRF0 Synchronous mode Master Output / Slave Input (MOSI).

5.4 GPIO Pinout Overview

The specific GPIO pins available in EZR32LG230 are shown in the GPIO pinout table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A		PA14	PA13	PA12												
Port B		PB14	PB13		PB11			PB8	PB7	PB6	PB5	PB4	PB3			
Port C	PC15	PC14	PC13	PC12					PC7	PC6						
Port D								PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E													PE3	PE2	PE1	PE0
Port F				PF12				PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

5.5 Opamp Pinout Overview

The specific opamp terminals available in EZR32LG230 are shown in Opamp pinout figure.

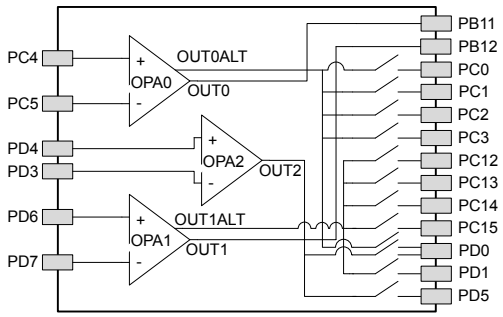


Figure 5.2. Opamp Pinout

5.6 QFN64 Package

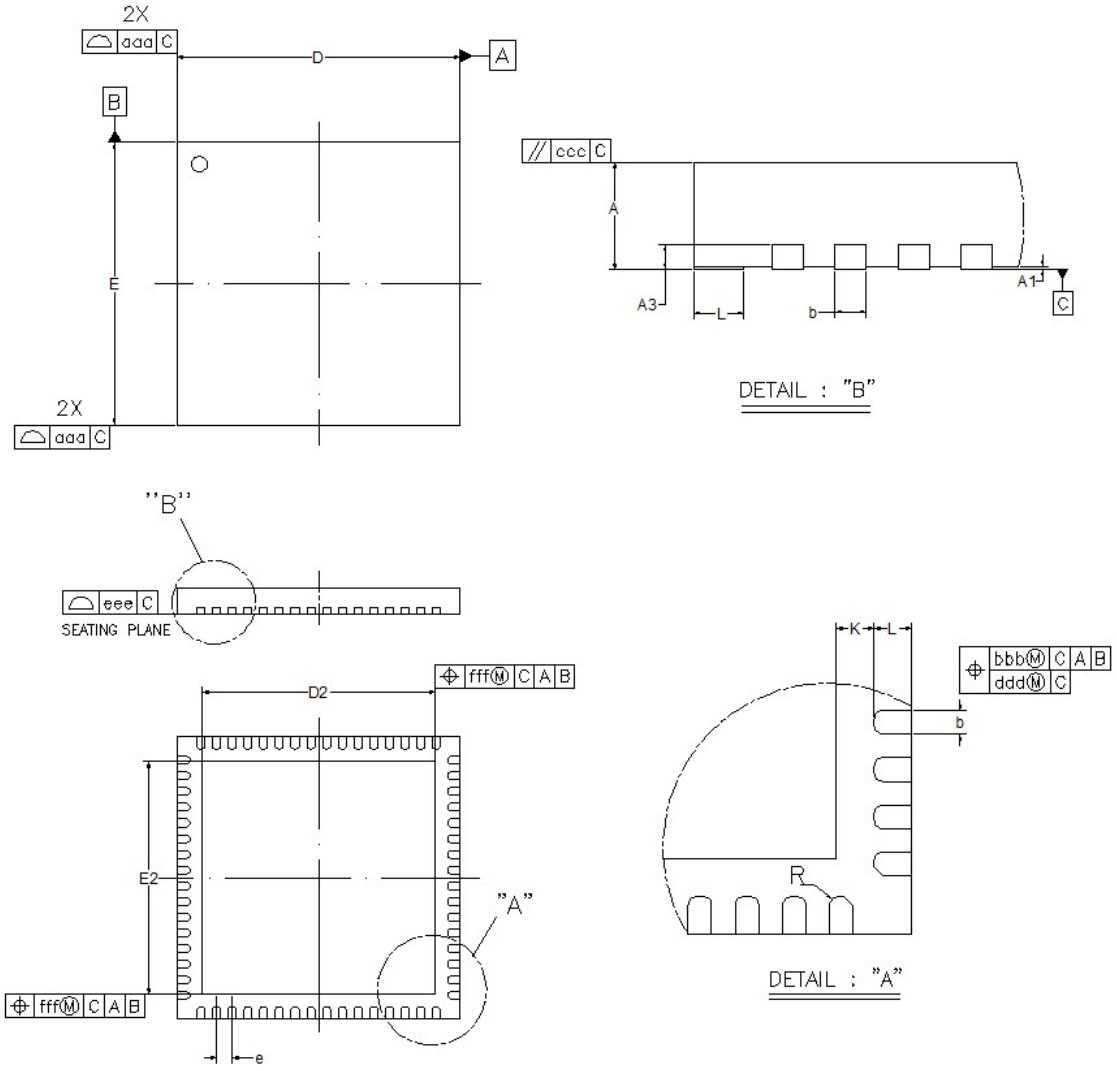


Figure 5.3. QFN64

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220 except for custom features D2, E2, L, Z, and Y which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 5.4. QFN64 (Dimensions in mm)

Symbol	A	A1	A3	b	D/E	D2/E2	e	L	R	K	aaa	bbb	ccc	ddd	eee	fff
Min	0.80	0.00	0.20 REF	0.18	8.9	7.25	0.50 BSC	0.30	0.09	0.20	0.15	0.10	0.10	0.05	0.08	0.10
Nom	0.85	0.02		0.25	9.00	7.40		0.40	—	—						
Max	0.90	0.05		0.30	9.1	7.55		0.50	—	—						

The QFN64 Package uses Matte Tin plated leadframe. All EFR32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

6. PCB Layout and Soldering

6.1 Recommended PCB Layout

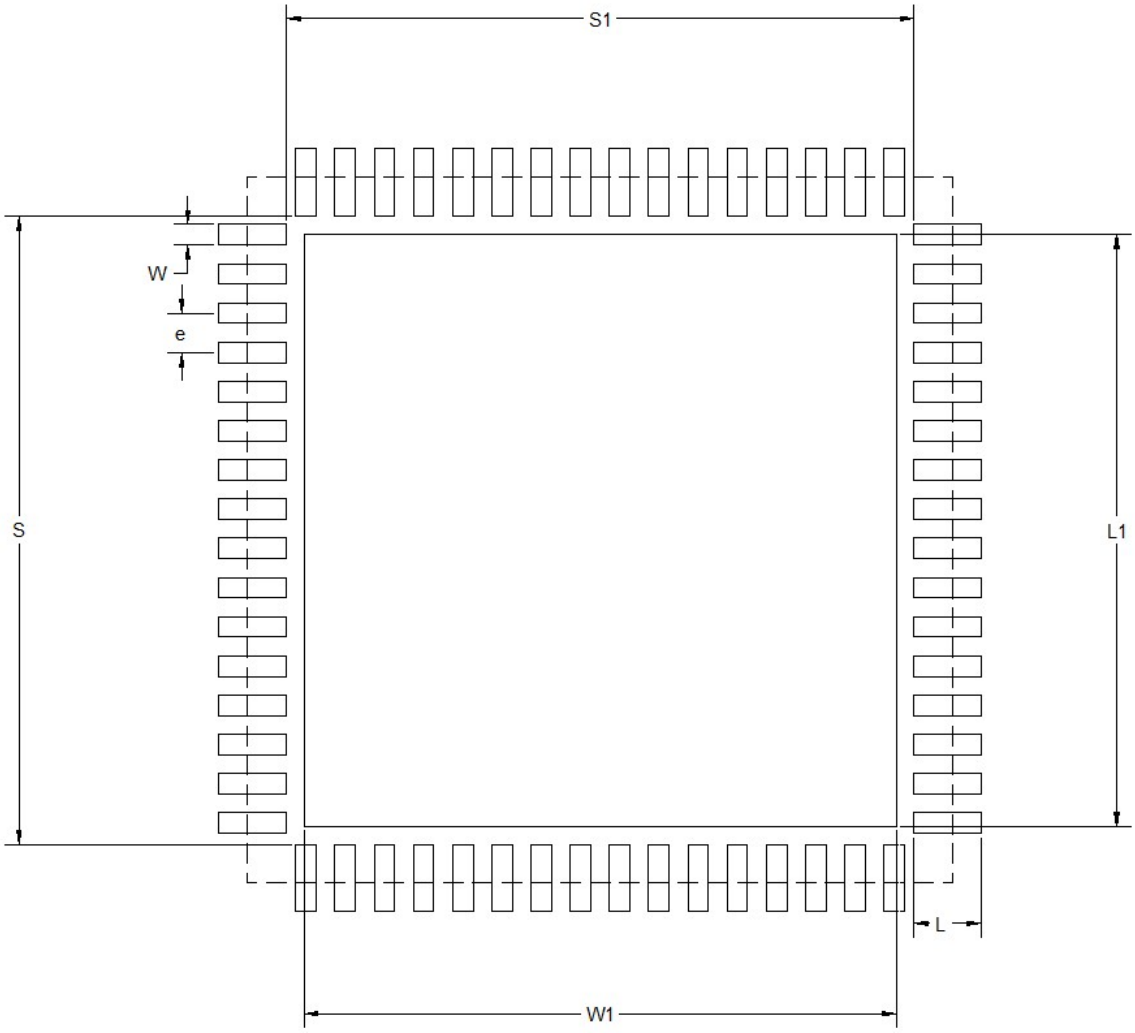


Figure 6.1. PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dimension (mm)
S1	8.01
S	8.01
L1	7.55
W1	7.55
e	0.50
W	0.26
L	0.86

Symbol	Dimension (mm)

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 4x4 array of 1.45 mm square openings on a 1.25 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

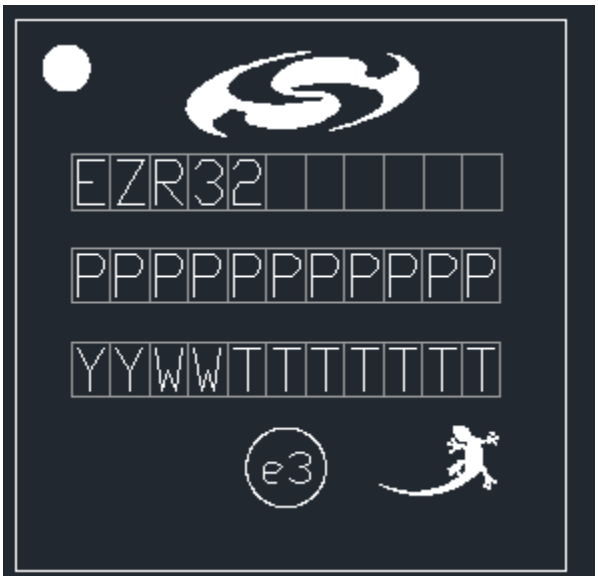
6.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions. Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

7. Top Marking

The top marking is illustrated and explained below.



Mark Method:	Laser	
Logo Size:	Top center	
Font Size:	0.71 mm Left-Justified	
Line 1 Marking:	FFFFFFFFFF = Family Part Number (EZR32)	Refer to the line marking instruction from assembly PO.

Line 2 Marking:	PPPPPPPPPP = Part Number
	• P_1P_2: LG = Leopard Gecko
	• $P_3P_4P_5$: 230 (non USB)
	• P_5P_6: Flash Size
	  • FE = 64
	  • FF = 128
	  • FG = 256
		• P_7P_8: Radio
		  • 55 = EZRadio +13 dBm, -116 sensitivity
		  • 60 = EZRadioPRO +13 dBm, -129 sensitivity
		  • 61 = EZRadioPRO +16 dBm, -129 sensitivity
		  • 63 = EZRadioPRO +20 dBm, -129 sensitivity
		  • 67 = EZRadioPRO +13 dBm, -133 sensitivity
		  • 68 = EZRadioPRO +20 dBm, -133 sensitivity
		  • 69 = EZRadioPRO +13 & 20 dBm, -133 sensitivity
		• P_9: Temperature Range
		  • G = -40 - 85 °C

Line 3 Marking:	YY = Year	Assigned by the Assembly House.
	WW = Work Week	Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order from assembly PO.
Line 4 Marking:	Circle = 1.3 mm diameter; center justified	"e3" Pb-Free Symbol
	Gecko Logo; right justified	Gecko Logo height = 1.90 mm

8. Revision History

8.1 Revision History

Revision 0.5

- Initial preliminary revision

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