Low Power Multi-Rate Two Channel Retimer

Check for Samples: DS110DF111

FEATURES

- **Pin Compatible Retimer Family**
  - **DS125DF111 with DFE : 9.8 to 12.5G**
  - **DS110DF111 with DFE : 8.5 to 11.3G**
- **Adaptive CTLE up to 34 dB Boost at 11.3G**
- **Self Tuning 5-Tap DFE**
- **Raw Equalized and Retimed Data Loopback**
- **Adjustable Transmit V_{OD}: 600 to 1300 mVp-p**
- **Settable Tx De-Emphasis Driver 0 to -12dB**
- **Low Power Consumption: 200mW/Channel**
- **Locks to Half/Quarter/Eighth Data Rates for Legacy Support**
- **On-Chip Eye Monitor (EOM), PRBS Generator**
- **Input Signal Detection, CDR Lock Detection/Indicator**
- **Single 3.3V or 2.5V ±5% Power Supply**
- **SMBus, EEPROM, or Pin Based Configuration**
- **4 mm x 4 mm, 24-Pin QFN Package**
- **Operating Temp Range: -40°C to 85°C**

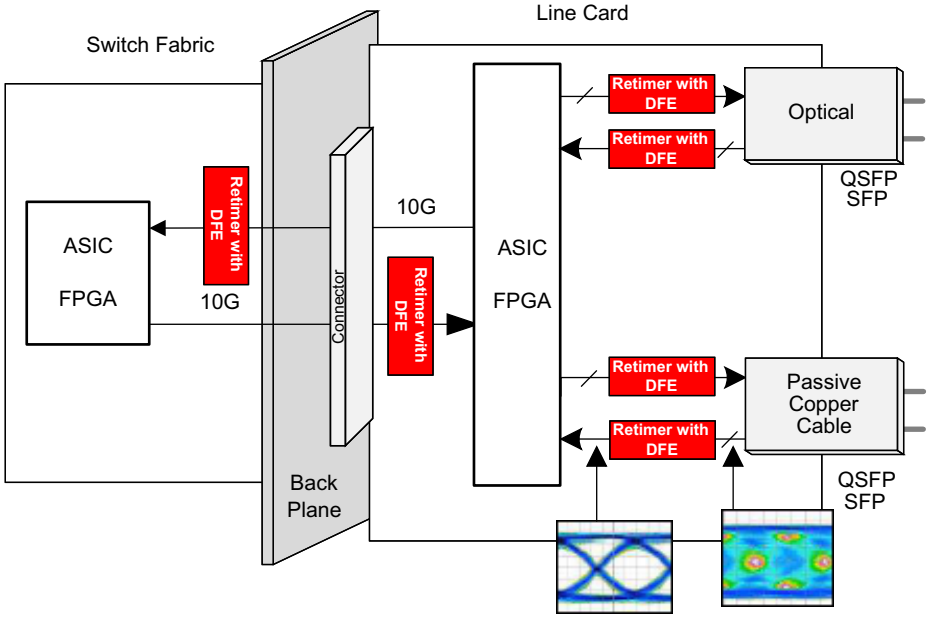
DESCRIPTION

The DS110DF111 is a dual channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR) and transmit driver on each channel.

The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For Less demanding applications/interconnects, the DFE can be switched off and achieve the same BER performance. The DS125 and DS110 devices are pin-compatible.

Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported sub-rate of these data rates. This simplifies system design and lowers overall cost.

Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high speed serial data.



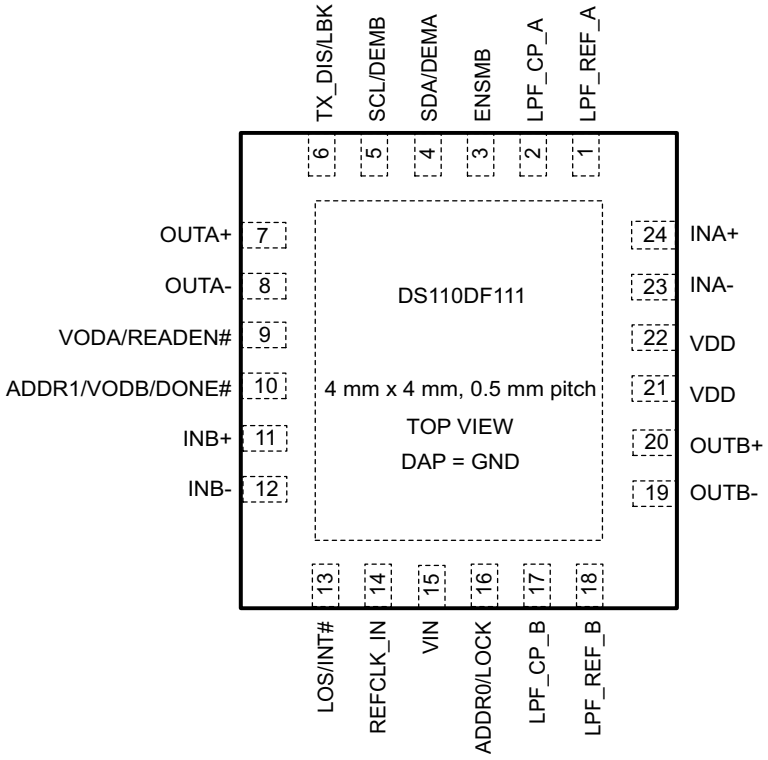
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PRODUCTION CONNECTION DIAGRAM

PIN OUT DIAGRAM (TOP VIEW)



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PIN DESCRIPTIONS

PIN NAME	PIN #	I/O TYPE	DESCRIPTION
HIGH SPEED DIFFERENTIAL I/OS			
OUTA+/-	7, 8	O, CML	Inverting and non-inverting CML-compatible differential outputs. Outputs require AC coupling
OUTB+/-	20, 19	O, CML	Inverting and non-inverting CML-compatible differential outputs. Outputs require AC coupling
INA+/-	24, 23	I, CML	Inverting and non-inverting CML-compatible differential inputs. An on-chip 100 Ohm terminating resistor connects INA+ to INA- Inputs require AC coupling. TI recommends 100 nF capacitors. Note that for SFP+ applications, AC coupling is included as part of the SFP+ module.
INB+/-	11, 12	I, CML	Inverting and non-inverting CML-compatible differential inputs. An on-chip 100 Ohm terminating resistor connects INB+ to INB- Inputs require AC coupling. TI recommends 100 nF capacitors. Note that for SFP+ applications, AC coupling is included as part of the SFP+ module.
LOOP FILTER CONNECTION PIN			
LPF_CP_A, LPF_REF_A	2, 1	I/O, analog	Loop filter connection, place a 22 nF capacitor in series between LPF_CP_A and LPF_REF_A
LPF_CP_B, LPF_REF_B	17, 18	I/O, analog	Loop filter connection, place a 22 nF capacitor in series between LPF_CP_B and LPF_REF_B
Reference Clock I/O			
REFCLK_IN	14	I, LVCMOS	25 MHz ± 100 ppm clock from external osc
INDICATOR PINS			
LOCK	16	O, LVCMOS	Goes high when CDR lock is attained on the corresponding channel. Note that this pin is shared with strap input functions read at startup
LOS/INT#	13	O, OD	Output is driven LOW when a valid signal is present on CH A. Output is released when signal on CH A is lost (LOS). This output can be redefined as an INT# signal which will be driven LOW if the EOM check returns a value below the HEO/VEO interrupt threshold(1)
SMBus MODE PINS			
ENSMB	3	I, 4-Level	System Management Bus (SMBus) enable pin HIGH = Register Access, SMBus Slave mode FLOAT = SMBus Master read from External EEPROM LOW = External Pin Control Mode
SDA	4	I, 4-Level O, OD	Data Input / Open Drain Output External pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant(2)
SCL	5	I, 4-Level O, OD	Clock input in SMBus slave mode. Can also be an open drain output in SMBus master mode Pin is 3.3 V LVCMOS Tolerant(2)
TX_DIS	6	I, 4-Level	Disable the transmitter and put the device in low power mode HIGH = OUTA Enabled/OUTB Disabled LOW = OUTA/OUTB Enabled (normal operation)
ADDR0	16	I, LVCMOS	This pin sets the SMBus address for the retimer. This pin is a strap input. The state is read on power-up to set the SMBus address in SMBus control mode(2)
ADDR1/DONE#	10	IO, LVCMOS	This pin sets the SMBus address for the retimer in SMBus Slave Mode. Goes low to indicate that the SMBus master EEPROM read has been completed in SMBus Master Mode(2)
READEN#	9	I, 4-Level	Initiates SMBus master EEPROM read. When multiple DS110DS111 are connected to a single EEPROM, the READEN# input can be daisychained to the DONE# output. Pull low for proper register operation(2)

(1) The LOS/INT# pin is an open drain output which requires external pull-up resistor to 3.3V to achieve a HIGH level.
(2) This pin is shared with other functions.

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PIN DESCRIPTIONS (continued)

PIN NAME	PIN #	I/O TYPE	DESCRIPTION
PIN CONTROL (ENSMB = LOW) (3)			
DEMA	4	I, 4-Level	Set CHA output de-emphasis level in pin control mode(4)
DEMB	5	I, 4-Level	Set CHB output de-emphasis level in pin control mode(4)
LBK	6	I, 4-Level	HIGH = INA goes to OUTA, INB goes to OUTB LOW = INA goes to OUTB, INB goes to OUTA(4)
VODA	9	I, 4-Level	Set CHA output launch amplitude in pin control mode(4)
VODB	10	I, 4-Level	Set CHB output launch amplitude in pin control mode(4)
POWER			
VDD	21, 22	Power	VDD = 2.5 V +/- 5% 3.3V Mode Operation: VDD Supply Output = 2.5V +/- 5% 2.5V Mode Operation: VDD Supply Input = 2.5V +/- 5%
VIN	15	Power	Regulator Input with Integrated Supply Mode Control 3.3V Mode Operation: VIN Supply Input = 3.3V +/- 10% 2.5V Mode Operation: VIN Supply Input = 2.5V +/- 5%
DAP	PAD	Power	Ground reference The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 vias to lower the ground impedance and improve the thermal performance of the package

(3) When in pin control mode, the production silicon DS110DF111 device operates at 1.25 and 10.3125 Gbps and has limited VOD and De-Emphasis control.
(4) This pin is shared with other functions.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNITS
Supply Voltage (V_{DD})		-0.5	+2.75	V
Supply Voltage (V_{IN})		-0.5	+3.6	V
LVCMOS Input/Output Voltage		-0.5	2.75	V
4-Level Input Voltage (2.5V mode)		-0.5	V_{DD} + 0.5	V
4-Level Input Voltage (3.3V mode)		-0.5	3.6	V
SMBus Input/Output Voltage		-0.5	3.6	V
CML Input Voltage		-0.5	V_{DD} + 0.5	V
CML Input Current		-30	+30	mA
Storage Temperature		-40	+125	°C
ESD Rating	HBM, STD - JESD22-A114F		> 2.5	kV
	CDM, STD - JESD22-C101-D		> 1.0	kV
Package Thermal Resistance	θ_{JA}, No Airflow, 4 Layer		42.0°C/W	
For soldering specifications, see product folder at www.ti.com				

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage	2.5V Mode	2.375	2.5	2.625	V
	3.3V Mode	3.0	3.3	3.6	
Ambient Temperature		-40	25	+85	°C
SMBus (SDA, SCL)		3.0	3.3	3.6	V

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ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
R_baud	Input baud rate	Full Rate: DS110DF111	8.5		11.3	Gbps
F_{SDC}	SMBus Clock Rate		100		400	KHz
REFCLK	Clock Rate	+/- 100 ppm		25.0		MHz
Power Supply Current						
I_{DD}	Current Consumption (Whole Device)	11.3 Gbps : DS110DF111		170		mA
		11.3 Gbps : DS110DF111 DFE Disabled		150		mA
		Maximum Transient Supply Current Default Settings: CHA and CHB valid input signal detected CHA and CHB acquiring LOCK		235	300	mA
NTps	Supply Noise Tolerance	50 Hz to 100 Hz		100		mVp-p
		100 Hz to 10 MHz		40		mVp-p
		10 MHz to 5.0 GHz		10		mVp-p
LVCMOS (LBK, READEN#, DONE#, LOCK)						
V_{IH}	High level input voltage	2.5V or 3.3V Supply Modes	1.7			V
V_{IL}	Low level input voltage	2.5V or 3.3V Supply Modes			0.7	V
V_{OH}	High level output voltage	I_{OH} = -3 mA	2.0			V
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.4	V
I_{IN}	Input leakage current	V_{INPUT} = GND or V_{IN}	-15		+15	uA
4-Level Inputs (ENSMB, DEMA, DEMB, TX_DIS, VODA, VODB)						
I_{IN-R}	Input leakage current	V_{INPUT} = GND or V_{IN}	-160		+80	uA
Open Drain (LOS/INT#)						
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.4	V
SIGNAL DETECT						
SDH	Signal Detect: ON Threshold Level	Default level to assert Signal Detect, 10.3125 Gbps		20		mVp-p
SDL	Signal Detect: OFF Threshold Level	Default level to de-assert Signal Detect, 10.3125 Gbps		15		mVp-p
CML RX Inputs						
R_Rd	DC Input differential Resistance			100		Ω
RL_{RX-IN}	Input Return-Loss	SDD11 10 MHz		-19		dB
		SDD11 2.0 GHz		-14		dB
		SDD11 6.0 - 11.1 GHz		-8		dB
$V_{RX-LAUNCH}$	Source Transmit Signal Level		600		1600	mVp-p
CML TX Outputs						
T_V_{DIFF0}	Output differential voltage	Default setting, PRBS31	400	550	675	mVp-p
T_V_{DIFF7}	Output differential voltage	Maximum setting, PRBS31 Requires SMBus Control	1000	1250		mVp-p
V_{OD_DE}	De-emphasis Level	Maximum setting, VOD and DE Requires SMBus Control Input: 10.3125Gbps, 64T pattern		-12		dB
T_Rd	DC Output Differential Resistance			100		Ω
T_R/T_F	Output Rise/Fall Time	Full Slew Rate 20% - 80% Input: 10.3125 Gbps, 8T Pattern		36		psec
T_{RS}/T_{FS}	Output Rise/Fall Time	Limited Slew Rate (Reg 0x18) 20% - 80% Input: 10.3125 Gbps, 8T Pattern		50		psec

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ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
T_{SDD22}	Output differential mode return loss	SDD22 10 MHz - 2 GHz		-19		dB
		SDD22 5.5GHz		-15		
		SDD22 11.1GHz		-11		
T_{PD}	Propagation Delay	Retimed Data 10.3125 Gbps		350		psec
T_{PD-RAW}	Propagation Delay	Raw Data		200		psec
Transmit Jitter Specs(1)						
T_{TJ}	Total Jitter (1E-12)	PRBS7, 10.3125 Gbps		7.5		ps
T_{RJ}	Random Jitter	PRBS7, 10.3125 Gbps		0.33		ps (RMS)
T_{DJ}	Deterministic Jitter	PRBS7, 10.3125 Gbps		3.6		ps

(1) Rj and Dj Jitter decomposition as reported by TEK DSA8200 Sampling scope using a 80E09 Electrical sampling module, 80A06 Pattern trigger, and 82A04 Phase Reference Module.

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ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Clock and Data Recovery						
BW_{PLL}	PLL Bandwidth -3 dB	Measured at 10.3125 Gbps		5		MHz
J_{TOL}	Total jitter tolerance	Jitter per SFF-8431 Appendix D.11 Combination of Dj, Pj, and Rj		> 0.70		UI
T_{LOCK1}	CDR Lock Time	Standards Based (2)		10 - 30		mS
$TEMP_{LOCK}$	CDR Lock	Lock Temperature Range -40C to 85C operating range		125		^{0}C
Serial Bus Interface Characteristics (3)						
V_{IL}	Data, Clock Input Low Voltage (SDA / SCL)				0.8	V
V_{IH}	Data, Clock Input High Voltage (SDA / SCL)		2.1		3.6	V
V_{HY}	Input Hystersis			>50		mV
V_{OL}	Output Low Voltage	SDA or SCL, IOL = 1.25 mA	0		0.36	V
I_{IN}	Input Current	SDA or SCL, $V_{INPUT} = V_{IN}$, V_{DD}, GND	-15		+15	uA
T_R	SDA Rise Time, Read Operation	SDA, RPU = 10K, Cb < 400 pF		430		ns
T_F	SDA Fall Time, Read Operation	SDA, RPU = 10K, Cb < 400 pF		20		ns
$T_{SU;DAT}$	Setup Time, Read Operation			560		ns
$T_{HD;DAT}$	Hold Time, Read Operation			615		ns
T_{SP}	Input Filter			50		ns
C_{IN}	Input Capacitance	SDA or SCL		< 5		pF
Recommended Timing for the Serial Bus Interface						
F_{SCL}	SCL Clock Frequency				400	KHz
T_{LOW}	SCL Low Period		1.3			us
T_{HIGH}	SCL High Period		0.6			us
$T_{HD;STA}$	Hold Time, Start Operation		0.6			us
$T_{SU;STA}$	Setup Time, Start Operation		0.6			us
$T_{HD;DAT}$	Data Hold Time		0		0.9	us
$T_{SU;DAT}$	Data Set Up Time		100			ns
$T_{SU;STO}$	Set Up Time, Stop Condtion		0.6			us
T_{BUF}	Bus Free Time Between Stop - Start		1.3			us
T_R	SCL and SDA, Rise Time				300	ns
T_F	SCL and SDA, Rise Time				300	ns

(2) The typical LOCK time can vary based on data-rate, input channel, and specific DS110DF111 settings.
(3) EEPROM interface requires 400 KHz capable EEPROM device.

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FUNCTIONAL DESCRIPTION

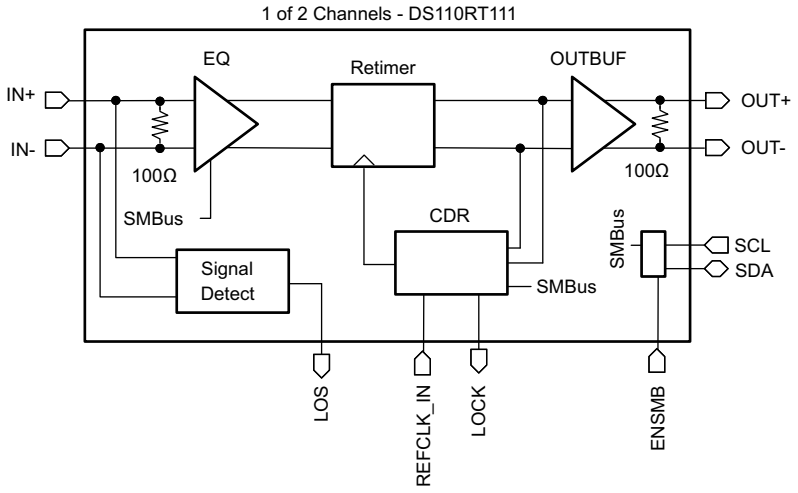


Figure 1. DS110DF111 Data Path Block Diagram

The DS110DF111 is a low-power, multi-rate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the DS110DF111's input. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

DEVICE DATA PATH OPERATION

The data path operation of the DS110DF111 comprises three functional sections as shown in the data path block diagram of Figure 1. The three functional sections are as follows.

- Channel Equalization
- Clock and Data Recovery
- Output Driver

CHANNEL EQUALIZATION

Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium.

To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock.

The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit.

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The DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments.

CLOCK AND DATA RECOVERY

The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system.

OUTPUT DRIVER

Once the input data has been retimed by the DS110DF111 to the recovered, cleaned, clock, it is output to the next device in the signal path using the output driver. The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111.

When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

An idealized transmit waveform with analog de-emphasis applied

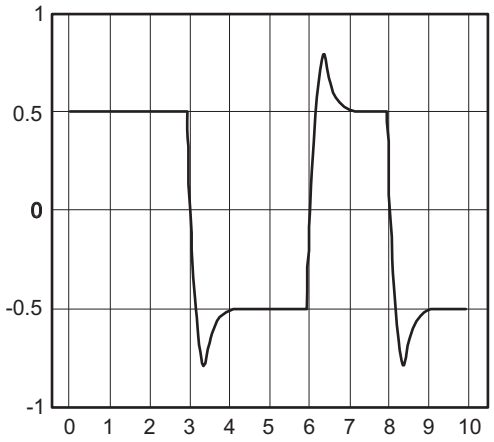


Figure 2. Idealized De-Emphasis Waveform

The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently.

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REFERENCE CLOCK

A 25 MHz +/- 100 ppm reference clock is required for proper device operation. The DS110DF111 uses the reference clock to determine when its VCO is properly phase-locked to the incoming data-rate. The DS110DF111 does not include a crystal driver, so a stand-alone external oscillator is required.

The DS110DF111 is set to phase lock to a constrained set of data-rates, the digital circuitry in the device pre-configures the VCO frequency. This enables the DS110DF111 to detect very quickly that a loss of lock has occurred.

The phase noise of the reference clock is not critical. Any commercially-available 25 MHz oscillator (+/- 100ppm maximum) can provide an acceptable reference clock. The 25 MHz clock high level input voltage must match the VIN level utilized on the DS110DF111.

CONTROL PINS

The 4-level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Table 1. 4-Level Inputs

LEVEL	SETTING	VOLTAGE
0	1K to GND	0.1 V
R	20K to GND	0.33 * VIN
Float	No connection	0.67 * VIN
1	1K to VIN	VIN - 0.05V

In order to minimize the startup current associated with the integrated 2.5V regulator the 1K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1K resistors into a single lower value resistor. As an example; combining two inputs with a single 500 Ohm resistor is a good way to save board space.

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SMBus INTERFACE

ENSMB PIN DESCRIPTION

To select different programming device, the ENSMB pin selects the control modes. The DS110DF111device can be programmed using external pin control, a SMBus controller, or through an EEPROM configuration load.

Table 2. ENSMB Control Description

ENSMB PIN	DESCRIPTION	READEN# Pin
High	SMBus Slave Mode	Pull Low to initiate reading configuration data from the EEPROM
Float	SMBus Master Mode	Tie Low to enable proper address strapping on power up
R	N/A	
Low	Pin Mode Control	Shared with VODA pin control function

SMBus REGISTER MODE CONTROL

SDA and SCL

To select different programming device, the ENSMB pin selects the control modes. The DS110DF111device can be programmed using external pin control, a SMBus controller, or through an EEPROM configuration load.

SMBus Master mode and SMBus Slave Mode

In SMBus master mode the DS110DF111 reads its initial configuration from an external EEPROM upon powerup. Once the DS100DF410 has finished reading its initial configuration from the external EEPROM in SMBus master mode it reverts to SMBus slave mode and can be further configured by an external controller over the SMBus. Two device pins initiate reading the configuration from the external EEPROM and indicate when the configuration read is complete.

- DONE#
- READEN#

These pins are meant to work together. When the DS110DF111 is powered up in SMBus master mode, it reads its configuration from the external EEPROM. This is triggered when the READEN# pin goes low. When the DS110DF111 is finished reading its configuration from the external EEPROM, it drives its DONE# pin low. In this mode, as the name suggests, the DS110DF111 acts as an SMBus master during the time it is reading its configuration from the external EEPROM. After the DS110DF111 has finished reading its configuration from the EEPROM, it releases control of the SMBus and becomes a SMBus slave. In applications where there is more than one DS110DF111 on the same SMBus, bus contention can result if more than one DS110DF111 tries to take command of the SMBus as the SMBus master at the same time. The READEN# and DONE# pins prevent this bus contention.

In a system where the DS110DF111s are meant to operate in SMBus master mode, the READEN# pin of one retimer should be wired to the DONE# pin of the next. The system should be designed so that the READEN# pin of one (and only one) of the DS110DF111s in the system is driven low on power-up. This DS110DF111 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When it is finished reading its configuration, it will set its DONE# pin low. This pin should be connected to the READEN# pin of another DS110DF111. When this DS110DF111 senses its READEN# pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its DONE# pin low. By connecting the DONE# pin of each DS110DF111 to the READEN# pin of the next DS110DF111, each DS110DF111 can read its initial configuration from the EEPROM without causing bus contention.

For SMBus slave mode, the READEN# pin must be tied LOW. Do not leave it Floating or tie it HIGH.

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Address Lines

In either SMBus mode the DS110DF111 must be assigned a SMBus address. A unique address should be assigned to each device on the SMBus.

The SMBus address is latched into the DS110DF111 on power-up. The address is read in from the state of the ADR[1:0] lines upon power-up. A floating address line input will be interpreted as a logic 0.

The DS110DF111 can be configured with any of 4 SMBus addresses. The SMBus addressing scheme uses the least significant bit of the SMBus address as the Write/Read_N address bit. When an SMBus device is addressed for writing, this bit is set to 0; for reading, to 1. Table 3 shows the write address setting for the DS110DF111versus the values latched in on the address line at power-up.

Device Configuration in SMBus Slave Mode

The configurable settings of the DS110DF111 may be set independently for each channel at any time after power up using the SMBus. A register write is accomplished when the controller sends a START condition on the SMBus followed by the Write address of the DS110DF111 to be configured. See Table 3 for the mapping of the address lines to the SMBus Write addresses. After sending the Write address of the DS110DF111, the controller sends the register address byte followed by the register data byte. The DS110DF111 acknowledges each byte written to the controller according to the data link protocol of the SMBus Version 2.0 Specification. See this specification for additional information on the operation of the SMBus.

There are two types of device registers in the DS110DF111. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS110DF111. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers.

The channel registers are used to set all the configuration settings of the DS110DF111. They provide independent control for each channel of the DS110DF111 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS110DF111 on a channel-by-channel basis.

Bit Fields in the Register Set

Many of the registers in the DS110DF111 are divided into bit fields. This allows a single register to serve multiple purposes, which may be unrelated. Often configuring the DS110DF111 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged.

Writing to and Reading From the Control/Shared Registers

Any write operation targeting register 0xff writes to the control/shared register 0xff. This is the only register in the DS110DF111 with an address of 0xff. Bit 2 of register 0xff is used to select either the control/shared register set or a channel register set. If bit 2 of register 0xff is cleared (written with a 0), then all subsequent read and write operations over the SMBus are directed to the control/shared register set. This situation persists until bit 2 of register 0xff is set (written with a 1). There is a register with address 0x00 in the control/shared register set, and there is also a register with address 0x00 in each channel register set. If you read the value in register 0x00 when bit 2 of register 0xff is cleared to 0, then the value returned by the DS110DF111 is the value in register 0x00 of the control/shared register set. If you read the value in register 0x00 when bit 2 of register 0xff is set to 1, then the value returned by the DS110DF111 is the value in register 0x00 of the selected channel register set. The channel register set is selected by bits 1:0 of register 0xff. If bit 3 of register 0xff is set to 1 and bit 2 of register 0xff is also set to 1, then any write operation to any register address will write all the channel register sets in the DS110DF111 simultaneously. This situation will persist until either bit 3 of register 0xff or bit 2 of register 0xff is cleared.

Note that when you write to register 0xff, independent of the current settings in register 0xff, the write operation ALWAYS targets the control/shared register 0xff. This channel select register, register 0xff, is unique in this regard. Table 4 shows the control/shared register set.

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Table 3. SMBus Write Address Assignment(1)

ADDR1	ADDR0	SMBus WRITE ADDRESS	SMBus READ ADDRESS
0	0	0x30	0x31
0	1	0x32	0x33
1	0	0x34	0x35
1	1	0x36	0x37

(1) A floating ADDR[1:0] pin at power-up will be interpreted as a logic 0.

Table 4. Control and Shared Register Space

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x00	00	7:4	0000	R	SMBus Address Strap Observation <3:0>
0x01	40	7:5	011	R	Device Revision
		4:0	0 0000	R	Device ID
0x04	01	6	0	R/W/SC	Self-Clearing Reset for Control/Shared Registers
		5	0	R/W	Reset for SMBus Master Mode
		4	0	R/W	Force EEPROM Configuration
0x05	00	4	0	R	Indicates EEPROM read complete
		3	0	R	Indicates Channel A has interrupted
		2	0	R	Indicates Channel B has interrupted
0x06	00	3:0	0000	R/W	Write to 0xA'h to observe SMBus Address strap in Reg 0x00[7:4]
0x07	04	1	0	R/W	Loopback: Loopback Input of Channel A to output of Channel B
		0	0	R/W	Loopback: Loopback Input of Channel B to output of Channel A
0xff	00	7:6	00	R/W	Controls LOCK pin output 00: Logical AND of Lock Status from CH A and CH B 01: Lock Status from Channel A 10: Lock Status from Channel B 11: Logical OR of Lock Status from CH A and CH B
		5	0	R/W	Loss of Signal / Interrupt (LOS/INT) pin output 0: LOS 1: Interrupt
		3	0	R/W	Selects Both Channels for Register Write. Register read from one channel based on the selected channel in register 0xff bits 1:0. See Table 5
		2	0	R/W	0 = reads/writes directed to shared registers 1 = reads/writes directed to channel registers based on target channel defined by register 0xff bits 1:0. See Table 5
		1:0	0	R/W	Selects Target Channel for Register Reads and Writes. See Table 5

SMBus Strap Observation

Register 0x00, bits 7:4

In order to communicate with the DS110DF111 over the SMBus, it is necessary for the SMBus controller to know the address of the DS110DF111. The address strap observation bits in control/shared register 0x00 are primarily useful as a test of SMBus operation. In order to use the address strap observation bits of control/shared register 0x00, it is necessary first to set the diagnostic test control bits of control/shared register 0x06. This four bit field should be written with a value of 0xa. When this value is written to bits 3:0 of control/shared register 0x06, then the value of the SMBus address straps can be read in register 0x00, bits 7:4. The value read will be the same as the value present on the ADDR line when the DS110DF111 powers up. For example, if a value of 0x0 is read from control/shared register 0x00, bits 7:4, then at power-up the ADDR line was set to 0. The DS110DF111 is set to a SMBus Write address of 0x30.

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Interrupt Channel Flag Bits

Register 0x05, bits 3:2

The operation of these bits is described in the section on interrupt handling later in this data sheet.

Control/Shared Register Reset

Register 0x04, bit 6

Register 0x04, bit 6, clears all the control/shared registers back to their factory defaults. This bit is self clearing, so it is cleared after it is written and the control/shared registers are reset to their factory default values.

Device Revision and Device ID

Register 0x01

Control/shared register 0x01 contains the device revision and device ID. The device ID will be different for the different devices in the retimer family. This register is useful because it can be interrogated by software to determine the device variant and revision installed in a particular system. The software might then configure the device with appropriate settings depending upon the device variant and revision.

Table 5. Channel Select Register Values Mapped to Register Set Target

REGISTER 0xFF VALUE (HEX)	SHARED/CHANNEL REGISTER SELECTION	BROADCAST CHANNEL REGISTER SELECTION	TARGETED CHANNEL REGISTER SELECTION	COMMENTS
0x00	Shared	N/A	N/A	All reads and writes target shared register set
0x01	Shared	N/A	N/A	All reads and writes target shared register set
0x02	Shared	N/A	N/A	All reads and writes target shared register set
0x03	Shared	N/A	N/A	All reads and writes target shared register set
0x04	Channel	No	A	All reads and writes target channel register set
0x05	Channel	No	B	All reads and writes target channel register set
0x08	Shared	N/A	N/A	All reads and writes target channel register set
0x09	Shared	N/A	N/A	All reads and writes target shared register set
0x0a	Shared	N/A	N/A	All reads and writes target shared register set
0x0b	Shared	N/A	N/A	All reads and writes target shared register set
0x0c	Channel	Yes	A	All writes target all channel register sets, all reads target Channel A register set
0x0d	Channel	Yes	B	All writes target all channel register sets, all reads target Channel B register set

Channel Select Register

Register 0xff, bits 3:0

Register 0xff, as described above, selects the channel or channels for channel register reads and writes. It is worth describing the operation of this register again for clarity. If bit 3 of register 0xff is set, then any channel register write applies to all channels. Channel register read operations always target only the channel specified in bits 1:0 of register 0xff regardless of the state of bit 3 of register 0xff. Read and write operations target the channel register sets only when bit 2 of register 0xff is set.

Bit 2 of register 0xff is the universal channel register enable. This bit must be set in order for any channel register reads and writes to occur. If this bit is set, then read operations from or write operations to register 0x00, for example, target channel register 0x00 for the selected channel rather than the control/shared register 0x00. In order to access the control/shared registers again, bit 2 of register 0xff should be cleared. Then the control/shared registers can again be accessed using the SMBus. Write operations to register 0xff always target the register with address 0xff in the control/shared register set. There is no other register, and specifically, no channel register, with address 0xff.

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The contents of the channel select register, register 0xff, cannot be read back over the SMBus. Read operations on this register will always yield an invalid result. All eight bits of this register should always be set to the desired values whenever this register is written. Always write 0x0 to the four most significant bits of register 0xff. The register set target selected by each valid value written to the channel select register is shown in Table 5.

Reading to and Writing From the Channel Registers

Each channel has a complete set of channel registers associated with it. The channel registers or the control/ shared registers are selected by channel select register 0xff. The settings in this register control the target for subsequent register reads and writes until the contents of register 0xff are explicitly changed by a register write to register 0xff. As noted, there is only one register with an address of 0xff, the channel select register.

Table 6. Channel Register Definition

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x00	00	2	0	R/W/SC	Reset Channel Registers to Defaults (Self-clearing)
0x01	00	4	0	R	CDR Lock Loss Interrupt
		0	0	R	Signal Detect Loss Interrupt
0x02	00	7:0	00'h	R	CDR Status [7:0] Bit[7] = PPM Count met Bit[6] = Auto Adapt Complete Bit[5] = Fail Lock Check Bit[4] = Lock Bit[3] = CDR Lock Bit[2] = Single Bit Limit Reached Bit[1] = Comp LPF High Bit[0] = Comp LPF Low
0x03	00	7:6	00	R/W	Used for setting CTLE value when Channel Register 0x2D[3] is high. Read-back value going to analog in Channel Register 0x52. CTLE Boost Stage [0] <1:0> Bits [7:6] CTLE Boost Stage [1] <1:0> Bits [5:4] CTLE Boost Stage [2] <1:0> Bits [3:2] CTLE Boost Stage [3] <1:0> Bits [1:0]
		5:4	00	R/W	
		3:2	00	R/W	
		1:0	00	R/W	
0x09	00	5	0	R/W	Enable Override Output Mux (Register 0x1E[7:5])
		2	0	R/W	Enable Override Divider Select (Register 0x18[6:4])
0x0A	10	3	0	R/W	Enable CDR Reset Override (Register 0x0A[2])
		2	0	R/W	CDR Reset Override Bit
0x0C	08	7:4	0000	R/W	Status Control[3:0]
		3	1	R/W	Single Bit Transition Detector – Lock Qualification 1: Enables SBT 0: Disables SBT
0x0D	00	5	0	R/W	PRBS pattern shift Enable. Use in conjunction with 0x1E[4] and 0x30[3] to start PRBS. Note: This bit must be set high last.

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Table 6. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x11	20	7:6	00	R/W	Eye Opening Monitor Voltage Range <1:0> 00: 3.125 mV 01: 6.250 mV 10: 9.375 mV 11: 12.500 mV
		5	1	R/W	Eye Opening Monitor Power Down
		3	0	R/W	DFE Tap 2 Polarity (Use w/manual DFE override, 0x15[7])
		2	0	R/W	DFE Tap 3 Polarity (Use w/manual DFE override, 0x15[7])
		1	0	R/W	DFE Tap 4 Polarity (Use w/manual DFE override, 0x15[7])
		0	0	R/W	DFE Tap 5 Polarity (Use w/manual DFE override, 0x15[7])
0x12	A0	7	1	R/W	DFE Tap 1 Polarity (Use w/manual DFE override, 0x15[7])
		5	1	R/W	DFE Select negative gm
		4:0	0000	R/W	DFE Tap 1 Weight <4:0>
0x13	90	4	1	R/W	Enable DC offset control
		2	0	R/W	CTLE Boost Stage 3, Bit 2 (Limiting Bit)
		1	0	R/W	Enable DWDM Mode
0x14	00	7	0	R/W	Force Signal Detect On
		6	0	R/W	Force Signal Detect Off
		5:4	00	R/W	Signal Detect – Assert Reference Levels
		3:2	00	R/W	Signal Detect – De-assert Reference Levels
0x15	10	7	0	R/W	Enables manual DFE tap settings Use with 0x11[3:0], 0x12[7], 0x12[4:0], 0x20[7:0], 0x21[7:0]
		6	0	R/W	Compress the range of de-emphasis to 0-6 dB
		3	0	R/W	Driver Power-Down
		2:0	000	R/W	Driver De-emphasis Setting<2:0>; 0dB - 12dB; See Table 16
0x18	40	6:4	000	R/W	VCO Divider Ratio <2:0> (Enable from Register 0x09, Bit 2) 000: Full-Rate 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Default value at power up
		2	0	R/W	Enable slow rise/fall time edge rate
0x1E	E1	7:5	111	R/W	Selects PFD MUX for Loopback 000: Raw Data 001: Re-timed Data 100: PRBS Generator 111: Mute
		4	0	R/W	Enable the PRBS serializer, used with 0x1E[7:5], 0x30[3:0], 0x0D[5]
		3	0	R/W	Disable the DFE function (Disable = 1)
0x1F	55	7	0	R/W	Invert the polarity of the driver
0x20	00	7:4	0000	R/W	DFE Tap 5 Weight <3:0> (Use w/manual DFE override, 0x15[7])
		3:0	0000	R/W	DFE Tap 4 Weight <3:0> (Use w/manual DFE override, 0x15[7])

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Table 6. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x21	00	7:4	0000	R/W	DFE Tap 3 Weight <3:0> (Use w/manual DFE override, 0x15[7])
		3:0	0000	R/W	DFE Tap 2 Weight <3:0> (Use w/manual DFE override, 0x15[7])
0x23	40	6	1	R/W	DFE Override
0x24	00	7	0	R/W	Enable Fast Eye Opening Monitor Mode
		2	0	R/W/SC	Start DFE Adaptation (Self- Clearing)
		0	0	R/W/SC	Start Eye Opening Monitor Counter (Self-Clearing)
0x25	00	7:0	00'h	R	Eye Opening Monitor Count <15:8>
0x26	00	7:0	00'h	R	Eye Opening Monitor Count <7:0>
0x27	00	7:0	00'h	R	HEO Value <7:0> (Measured in 0-63 phase settings)
0x28	00	7:0	00'h	R	VEO Value <7:0>
0x29	00	6:5	00	R	Eye Opening Monitor Voltage Range Setting <1:0> See 0x11[7:6]
0x2A	30	7:0	30'h	R/W	Eye Opening Monitor Timer Threshold <7:0>
0x2C	72	5:4	11	R/W	DFE Adaptation Figure of Merit Type <1:0> 00: Not Valid 01: State Machine uses only HEO 10: State Machine uses only VEO 11: State Machine uses both HEO and VEO
		3:0	0010	R/W	Determines number of DFE settings to look-beyond current best Figure of Merit (FOM)
0x2D	80	7	1	R/W	Enable Driver Short Circuit protection
		6	0	R/W	Enable FAST signal detect
		5	0	R/W	Increase the Assert and De-assert reference thresholds
		4	0	R/W	Set high (1) to decrease the signal detect gain
		3	0	R/W	Set high (1) to override the EQ setting going to the analog from 0x03[7:0]
		2:0	000	R/W	Output Driver VOD [2:0] 000: 600 mV 001: 700 mV 010: 800 mV 011: 900 mV 100: 1000 mV 101: 1100 mV 110: 1200 mV 111: 1300 mV
0x2F	06	7:6	0	R/W	Rate <1:0>
		5:4	0	R/W	Subrate <1:0>
		3	0	R/W	CTLE Adaptation Index Override 0: CTLE adaption will start at Reg_0x40 + Reg_0x39[3:0]. So this may be used to preclude lower CTLE settings. 1: CTLE will not adapt and will use the CTLE setting of Reg_0x40 + Reg_0x39[3:0] for scalar divide ratios of 1 or 2. Divide ratios of 4 & 8 will take CTLE settings from 0x3A unless 0x55[0] is high, which will revert to the setting in Reg_0x40 + Reg_0x39[3:0].
		0	0	R	Start CTLE Adaptation

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Table 6. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x30	00	4	0	R	Goes High if Interrupt from CDR Goes High
		3	0	R/W	Enable PRBS digital CLK
0x31	40	6:5	10	R/W	Adaptation Mode <1:0> 00: No adaption 01: Adapt only CTLE till optimal 10: Adapt CTLE till optimal, then DFE, then CTLE again 11: Adapt CTLE till LOCK, then DFE, then CTLE till optimal
		4:3	00	R/W	CTLE Adaptation Figure of Merit Type <1:0> 00: SM uses both HEO and VEO 01: SM uses only HEO 10: SM uses only VEO 11: SM uses both HEO and VEO
0x32	11	7:4	0001	R/W	HEO Interrupt Threshold <3:0> Compares HEO value, Reg_0x27[7:0] vs. threshold of Reg_0x32[7:4]*4
		3:0	0001	R/W	VEO Interrupt Threshold <3:0> Compares VEO value, Reg_0x28[7:0] vs. threshold of Reg_0x32[3:0]*4
0x33	88	7:4	1000	R/W	HEO Threshold for CTLE Adaptation Handoff to DFE Adaptation Compares HEO value, Reg_0x27[7:0] vs. threshold of Reg_0x33[7:4]*2
		3:0	1000	R/W	VEO Threshold for CTLE Adaptation Handoff to DFE Adaptation Compares HEO value, Reg_0x27[7:0] vs. threshold of Reg_0x33[3:0]*2
0x34	3F	3:0	1111	R/W	Maximum DFE Tap Absolute Value for Taps 2–5 <3:0>
0x35	1F	4:0	1 1111	R/W	Maximum DFE Tap Absolute Value for Tap 1 <4:0>
0x36	33	6	0	R/W	Enable HEO/VEO Interrupt
		5:4	11	R/W	Reserved
		2	0	R/W	Reserved
		1:0	11	R/W	Reserved
0x39	00	4:0	0 0000	R/W	Start Index for CTLE Adaptation <4:0> (Enable from Register 0x2f, Bit 3)
0x3A	A5	7:6	10	R/W	Fixed CTLE Stage 0 Boost Setting for Divide Ratios 4 and 8 <1:0>
		5:4	10	R/W	Fixed CTLE Stage 1 Boost Setting for Divide Ratios 4 and 8 <1:0>
		3:2	01	R/W	Fixed CTLE Stage 2 Boost Setting for Divide Ratios 4 and 8 <1:0>
		1:0	01	R/W	Fixed CTLE Stage 3 Boost Setting for Divide Ratios 4 and 8 <1:0>
0x3E	80	7	1	R/W	Enable HEO/VEO lock monitoring once SBT/FLD declare lock. Once the lock and adaptation processes are complete, HEO/VEO monitoring is performed once per the interval determined by Reg_0x69[3:0].
0x40 - 0x4F		CTLE Settings for Adaptation			
0x50	00	4	0	R/W	Slicer Sign Bit
		3:0	0000	R/W	Slicer adjustment in 5mV steps. Maximum adjustment value is 50mV or 0x50[3:0] = A'h
0x52	00	7:0	00'h	R	CTLE Boost setting readback register.

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Table 6. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x54	00	7	0	R	Signal Detect observation bit.
		6	0	R	EQ Limiting (CTLE Stage 3[2]) observation bit.
		1	0	R	CDR Lock Interrupt
		0	0	R	Signal Detect Interrupt
0x55	00	4	0	R	Allows observation of the alternate HEO/VEO Figure of Merit In Reg_0x27 and Reg_0X28
		0	0	R	Enables Adaption in the lower divide ratios
0x56	00	1	0	R/W	CDR loss of lock. Sticky Bit. Clears when read
		0	0	R/W	Loss of Signal. Sticky Bit. Clears when read
0x60	00	7:0	00'h	R/W	Group 0 (Rate/Subrate defined) PPM counter <7:0> LSBs
0x61	00	7	0	R/W	Override standard Group 0 tie cells for PPM count and tolerance with Channel Registers 0x60, 0x61, and 0x64
		6:0	000 0000	R/W	Group 0 (Rate/Subrate defined) PPM counter <14:8> MSBs
0x62	00	7:0	00'h	R/W	Group 1 (Rate/Subrate defined) PPM counter <7:0> LSBs
0x63	00	7	0	R/W	Override standard Group 1 tie cells for PPM count and tolerance with Channel Registers 0x62, 0x63, and 0x64
		6:0	000 0000	R/W	Group 1 (Rate/Subrate defined) PPM counter <14:8> MSBs
0x64	00	7:4	0000	R/W	Group 0 PPM Delta
		3:0	0000	R/W	Group 1 PPM Delta
0x69	0A	3:0	1010	R/W	HEO/VEO interval while monitoring lock. Monitoring will take place 1 out of the indicated count intervals (default h'A). Interval time is determined 0x2B[5:4], which is 6.5ms by default.
0x6A	44	7:4	0100	R/W	Vertical Eye Opening Lock Threshold <3:0>
		3:0	0100	R/W	Horizontal Eye Opening Lock Threshold <3:0>
0x6B	40	7:0	40'h	R/W	Adaptation Figure of Merit Term A<7:0> FoM = Min [(HEO - B)*A, (VEO - C)*(1-A)] FoM = Min [(HEO - 0x6C) * (0x6B)/127, (VEO - 0x6D) * (128 - 0x6B)/127]
0x6C	00	7:0	0x0	R/W	Adaptation Figure of Merit Term B<7:0> FoM = Min [(HEO - B)*A, (VEO - C)*(1-A)] FoM = Min [(HEO - 0x6C) * (0x6B)/127, (VEO - 0x6D) * (128 - 0x6B)/127]
0x6D	00	7:0	0x0	R/W	Adaptation Figure of Merit Term C<7:0> FoM = Min [(HEO - B)*A, (VEO - C)*(1-A)] FoM = Min [(HEO - 0x6C) * (0x6B)/127, (VEO - 0x6D) * (128 - 0x6B)/127]
0x6E	00	7	0x0	R/W	Enable Alternate Figure of Merit for CTLE Adaptation
		6	0x0	R/W	Enable Alternate Figure of Merit for DFE Adaptation
0x70	03	2:0	011	R/W	CTLE Adaptation Look-Beyond Count <2:0>
0x71	00	5	0	R	DFE Tap 1 Polarity (Read Only)
		4:0	0 0000	R	DFE Tap 1 Weight (Read Only) <4:0>
0x72	00	4	0	R	DFE Tap 2 Polarity (Read Only)
		3:0	0000	R	DFE Tap 2 Weight (Read Only) <3:0>

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Table 6. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x73	00	4	0	R	DFE Tap 3 Polarity (Read Only)
		3:0	0000	R	DFE Tap 3 Weight (Read Only) <3:0>
0x74	00	4	0	R	DFE Tap 4 Polarity (Read Only)
		3:0	0000	R	DFE Tap 4 Weight (Read Only) <3:0>
0x75	00	4	0	R	DFE Tap 5 Polarity (Read Only)
		3:0	0000	R	DFE Tap 5 Weight (Read Only) <3:0>

Resetting Individual Channels of the Retimer

Register 0x00, bit 2, and register 0x0a, bits 3:2

Bit 2 of channel register 0x00 is used to reset all the registers for the corresponding channel to their factory default settings. This bit is self-clearing. Writing this bit will clear any register changes you have made in the DS110DF111 since it was powered-up.

To reset just the CDR state machine without resetting the register values, which will re-initiate the lock and adaptation sequence for a particular channel, use channel register 0x0a. Set bit 3 of this register to enable the reset override, then set bit 2 to force the CDR state machine into reset. These bits can be set in the same operation. When bit 2 is subsequently cleared, the CDR state machine will resume normal operation. If a signal is present at the input to the selected channel, the DS110DF111 will attempt to lock to it and will adapt its CTLE and its DFE according to the currently configured adapt mode for the selected channel. The adapt mode is configured by channel register 0x31, bits 6:5.

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Rate and Subrate Setting

Each channel of the DS110DF111 will, by default operate at 10.3125 Gbps and 1.25 Gbps. The device can be configured to operate at other VCO frequencies between 8.5 GHz and 11.3 GHz using the RATE (Reg: 0x2F bits [7:6]) and SUBRATE (Reg: 0x2F bits [5:4]) registers.

The DS110DF111 is designed to lock to signals conforming to several different data transmission standards. These standards may define a single data rate or multiple data rates. The rate and subrate settings of the DS110DF111 may be used to select a data transmission standard to which the input signal is expected to conform. The DS110DF111 searches each data rate applicable to the selected standard to find a valid signal to which it then phase locks.

Table 7. Rate/Subrate VCO and Data-rate Information

RATE	SUBRATE	INPUT DATA RATES	GROUP 0 DIVIDE RATIOS	GROUP 1 DIVIDE RATIOS	GROUP 0 VCO	GROUP 1 VCO	DS110DF111	DS125DF111
00	00	1.25G, 10.3125G	8	1	10G	10.3125G	X	X
00	01	2.125G, 4.25G, 8.5G, 10.51875G	1, 2, 4	1	8.5G	10.51875G	X	X
00	10	2.5G, 5G, 10G	1, 2, 4	1, 2, 4	10G	10G	X	X
00	11	2.4576G, 4.9152G, 9.8304G	1, 2, 4	1, 2, 4	9.8304G	9.8304G	X	X
01	00	3.072G, 6.144G	2, 4	2, 4	12.288G	12.288G		X
01	01	2.48832G, 9.95328G	1, 4	1, 4	9.95328G	9.95328G	X	X
01	10	1.5G, 3G, 6G, 12G	1, 2, 4, 8	1, 2, 4, 8	12.0G	12.0G		X
01	11	8.25G	1	1	8.25G	8.25G		
10	00	8.5G	1	1	8.5G	8.5G	X	
10	01	11.5G	1	1	11.5G	11.5G		X
10	10	6.25G, 12.5G	2	2	12.5G	12.5G		X
10	11	3.125G, 6.25G	2, 4	2, 4	12.5G	12.5G		X
11	00	10.3125G	1	1	10.3125G	10.3125G	X	X
11	01	9.95328G	1	1	9.95328G	9.95328G	X	X
11	10	7.5G	1	1	7.5G	7.5G		
11	11	1.25G, 10.3125G	8	1	10G	10.3125G	X	X

Overriding the CTLE Boost Setting

Register 0x03, Register 0x2D, bit 3, and Register 0x3a

To override the adaptive CTLE boost settings, channel register 0x03 is used in conjuction with override register bit for the CTLE (0x2D[3]).

The current CTLE setting applied to the high-speed analog input can always be readback from register 0x52. This readback register value is valid for adaptive CTLE settings or when the override mechanism is enabled and the CTLE value from register 0x03 is being used.

When in divide by 4 or 8 VCO settings, CTLE channel register 0x3A comes into play. Divide by 4 and divide by 8 data-rates do not automatically adapt the CTLE setting, they use the value in register 0x3A as a settable CTLE level.

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Table 8. Default Output Status Description

INPUT SIGNAL STATUS	CHANNEL STATUS	OUTPUT STATUS
Not Present	No Signal Detected	Mute
Present	Not Locked	Mute
Present	Locked	Raw or Retimed, Set by 0x1e[7], 0x09[5]

Table 9. Output Multiplexer Override Settings, Retimed or Raw, Register 0x1E Bit 7

BIT FIELD VALUE	OUTPUT MULTIPLEXER	COMMENTS
0x1	Retimed Data	Default when the retimer is locked
0x0	Raw Data	Output of the CTLE + DFE, before retiming

Overriding the Output Multiplexer

Register 0x09, bit 5, Register 0x14, bits 7:6, and Register 0x1e, bits 7:5

By default, the DS110DF111 output for each channel will be as shown in Table 8 and Table 9.

This default behavior can be modified by register writes. Register 0x1e, bits 7:5, contain the output multiplexer override value. The values of this three-bit field and the corresponding meanings of each are shown in Table 9.

When no signal is present at the input to the selected channel of the DS110DF111 the signal detect circuitry will power down the channel. This includes the output driver which is therefore muted when no signal is present at the input.

Table 10. Divider Ratio Map

Bit Field Value Reg 18 [6:4]	Divider Ratio
0	1
1	2
2	4
3	8

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Overriding the VCO Divider Selection

Register 0x09, bit 2, and Register 0x18, bits 6:4

In normal operation, the DS110DF111 sets its VCO divider to the correct divide ratio, either 1, 2, 4, or 8 depending upon the bit rate of the signal at the channel input. It is possible to override the divider selection. This might be desired if the VCO is set to free run, for example, to output a signal at a sub-harmonic of the actual VCO frequency.

In order to override the VCO divider settings, first set bit 2 of register 0x09. This is the VCO divider override enable. Once this bit is set, the VCO divider setting is controlled by the value in register 0x18, bits 6:4. The valid values for this three-bit field are 0x0 to 0x3. The mapping of the bit field values to the divider ratio is shown in Table 10.

In normal operation, the DS110DF111 will determine the required VCO divider ratio automatically. In order for the DS110DF111 to acquire LOCK, the override divider selection must be included in the Group 0 VCO list for the current Rate/Subrate setting.

Using the Internal Eye Opening Monitor

Register 0x11, bits 7:6 and bit 5, Register 0x22, bit 7, Register 0x24, bit 7 and bit 0, Register 0x25, Register 0x26, Register 0x27, Register 0x28, Register 0x2a and Register 0x3e, bit 7

The DS110DF111 includes an internal eye opening monitor. The eye opening monitor is used by the retime to compute a figure of merit for automatic adaptation of the CTLE and the DFE. It can also be controlled and queried through the SMBus by a system controller.

The eye opening monitor produces error hit counts for settable phase and voltage offsets of the comparator in the retimer. This is similar to the way many Bit Error Rate Test Sets measure eye opening. At each phase and amplitude offset setting, the eye opening monitor determines the nominal bit value (“0” or “1”) using its primary comparator. This is the bit value that is resynchronized to the recovered clock and presented at the output of the DS110DF111. The eye opening monitor also determines the bit value detected by the offset comparator. This information yields an eye contour. Here's how this works.

If the offset comparator is offset in voltage by an amount larger than the vertical eye opening, for example, then the offset comparator will always decide that the current bit has a bit value of “0”. When the bit is really a “1”, as determined by the primary comparator, this is considered a bit error. The number of bit errors is counted for a settable interval at each setting of the offset phase and voltage of the offset comparator. These error counts can be read from registers 0x25 and 0x26 for sequential phase and voltage offsets. These error counts for all phase and voltage offsets form a 64 X 64 point array. A surface or contour plot of the error hit count versus phase and voltage offset produces an eye diagram, which can be plotted by external software.

The eye opening monitor works in two modes. In the first, only the horizontal and vertical eye openings are measured. The eye opening monitor first sweeps its variable-phase clock through one unit interval with the comparison voltage set to the mid-point of the signal. This determines the mid-point of the horizontal eye opening. The eye opening monitor then sets its variable phase clock to the mid-point of the horizontal eye opening and sweeps its comparison voltage. These two measurements determine the horizontal and vertical eye openings. The horizontal eye opening value is read from register 0x27 and the vertical eye opening from register 0x28. Both values are single byte values.

The measurement of horizontal and vertical eye opening is very fast. The speed of this measurement makes it useful for determining the adaptation figure of merit. In normal operation, the HEO and VEO are automatically measured periodically to determine whether the DS110DF111 is still in lock. Reading registers 0x27 and 0x28 will yield the most-recently measured HEO and VEO values.

In normal operation, the eye monitor circuitry is powered down most of the time to save power. When the eye is to be measured under external control, it must first be enabled by writing a 0 to bit 5 of register 0x11. The default value of this bit is 1, which powers down the eye monitor except when it is powered-up periodically by the CDR state machine and used to test CDR lock. The eye monitor must be powered up to measure the eye under external SMBus control.

Bits 7:6 of register 0x11 are also used during eye monitor operation to set the EOM voltage range. This is described below. A single write to register 0x11 can set both bit 5 and bits 7:6 in one operation.

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Register 0x3e, bit 7, enables horizontal and vertical eye opening measurements as part of the lock validation sequence. When this bit is set, the CDR state machine periodically uses the eye monitor circuitry to measure the horizontal and vertical eye opening. If the eye openings are too small, according to the pre-determined thresholds in register 0x6a, then the CDR state machine declares lock loss and begins the lock acquisition process again. For SMBus acquisition of the internal eye, this lock monitoring function must be disabled. Prior to overriding the EOM by writing a 1 to bit 0 of register 0x24, disable the lock monitoring function by writing a 0 to bit 7 of register 0x3e.

Once the eye has been acquired, you can reinstate HEO and VEO lock monitoring by once again writing a 1 to bit 7 of register 0x3e. Under external SMBus control, the eye opening monitor can be programmed to sweep through all its 64 states of phase and voltage offset autonomously. This mode is initiated by setting register 0x24, bit 7, the fast_eom mode bit.

Register 0x11, bits 7:6 and bit 5, Register 0x22, bit 7, Register 0x24, bit 7 and bit 0, Register 0x25, Register 0x26, Register 0x27, Register 0x28, Register 0x2a and Register 0x3e, bit 7

Register 0x22, bit 7, the eom_ov bit, should be cleared in this mode. When the fast_eom bit is set, the eye opening monitor operation is initiated by setting bit 0 of register 0x24, which is self-clearing. As soon as this bit is set, the eye opening monitor begins to acquire eye data. The results of the eye opening monitor error counter are stored in register 0x25 and 0x26. In this mode the eye opening monitor results can be obtained by repeated multi-byte reads from register 0x25. It is not necessary to read from register 0x26 for a multi-byte read. As soon as the eight most significant bits are read from register 0x25, the eight least significant bits for the current setting are loaded into register 0x25 and they can be read immediately. As soon as the read of the eight most significant bits has been initiated, the DS110DF111 sets its phase and voltage offsets to the next setting and starts its error counter again. The result of this is that the data from the eye opening monitor is available as quickly as it can be read over the SMBus with no further register writes required. The external controller just reads the data from the DS110DF111 over the SMBus as fast as it can. When all the data has been read, the DS110DF111 clears the eom_start bit.

If multi-byte reads are not used, meaning that the device is addressed each time a byte is read from it, then it is necessary to read register 0x25 to get the MSB (the eight most significant bits) and register 0x26 to get the LSB (the eight least significant bits) of the current eye monitor measurement. Again, as soon as the read of the MSB has been initiated, the DS110DF111 sets its phase and voltage offsets to the next setting and starts its error counter again. In this mode both registers 0x25 and 0x26 must be read in order to get the eye monitor data. The eye monitor data for the next set of phase and voltage offsets will not be loaded into registers 0x25 and 0x26 until both registers have been read for the current set of phase and voltage offsets. In all eye opening monitor modes, the amount of time during which the eye opening monitor accumulates eye opening data can be set by the value of register 0x2a. In general, the greater this value the longer the accumulation time. When this value is set to its maximum possible value of 0xff, the maximum number of samples acquired at each phase and amplitude offset is approximately 218. Even with this setting, the eye opening monitor values can be read from the SMBus with no delay. The eye opening monitor operation is sufficiently fast that the SMBus read operation cannot outrun it.

The eye opening is measured at the input to the data comparator. At this point in the data path, a significant amount of gain has been applied to the signal by the CTLE. In many cases, the vertical eye opening as measured by the EOM will be on the order of 400 to 500 mV peak-to-peak. The secondary comparator, which is used to measure the eye opening, has an adjustable voltage range from ±100 mV to ±400 mV. The EOM voltage range is normally set by the CDR state machine during lock and adaptation, but the range can be overridden by writing a two-bit code to bits 7:6 of register 0x11. The values of this code and the corresponding EOM voltage ranges are shown in Table 11.

Table 11. EOM Voltage Range vs Reg 0x11 [7:6]

VALUE IN BITS 7:6 OF REGISTER 0x11	EOM VOLTAGE RANGE (± mV)
0x0	±100
0x1	±200
0x2	±300
0x3	±400

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Note that the voltage ranges shown in Table 11 are the voltage ranges of the signal at the input to the data path comparator. These values are not directly equivalent to any observable voltage measurements at the input to the DS110DF111. Note also that if the EOM voltage range is set too small the voltage sweep of the secondary comparator may not be sufficient to capture the vertical eye opening. When this happens the eye boundaries will be outside the vertical voltage range of the eye measurement.

To summarize, the procedure for reading the eye monitor data from the DS110DF111is shown below.

1. Select the DS110DF111 channel to be used for the eye monitor measurement by writing the channel select register, register 0xff, with the appropriate value as shown in Table 5 if the correct channel register set is already selected, this step may be skipped.
2. Select the eye monitor voltage range by setting bits 7:6 of register 0x11 according to the values in Table 11. The CDR state machine will have set this range during lock acquisition, but it may be necessary to change it to capture the entire vertical eye extent.
3. Power up the eye monitor circuitry by clearing bit 5 of register 0x11. Normally the eye monitor circuitry is powered up periodically by the CDR state machine. Clearing bit 5 of register 0x11 enables the eye monitor circuitry unconditionally. This bit should be set again once the eye acquisition is complete. Clearing bit 5 and setting bits 7:6 of register 0x11 as desired can be combined into a single register write if desired.
4. Clear bit 7 of register 0x22. This is the eye monitor override bit. It is cleared by default, so you may not need to change it.
5. Set bit 7 of register 0x24. This is the fast eye monitor enable bit.
6. Set bit 1 of register 0x24. This initiates the automatic fast eye monitor measurement. This bit can be set at the same time a bit 7 of register 0x24 if desired.
7. Read the data array from the DS110DF111. This can be accomplished in two ways.
   – If you are using multi-byte reads, address the DS110DF111 to read from register 0x25. Continue to read from this register without addressing the device again until you have read all the data desired. The read operation can be interrupted by addressing the device again and then resumed by reading once again from register 0x25.
   – If you are not using multi-byte reads, then read the MSB for each phase and amplitude offset setting from register 0x25 and the LSB for each setting from register 0x26. In this mode, you address the device each time you want to read a new byte.
8. In either mode, the first four bytes do not contain valid data. These should be discarded.
9. Continue reading eye monitor data until you have read the entire 64X64 array.
10. Clear bit 7 of register 0x24. This disables fast eye monitor mode.
11. Set bit 5 of register 0x11. This will return control of the eye monitor circuitry to the CDR state machine.
12. Set bit 7 of register 0x3e. This re-enables the HEO and VEO lock monitoring.

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Overriding the DFE Tap Weights and Polarities

Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x24, bit 2, Register 0x2f, bit 0, and Registers 0x71–0x75

For the DS110DF111 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired.

Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, which powers down the DFE, should be cleared. This bit is cleared by default. It is not necessary to change the default settings of these registers, but verify that they are set as described.

It is necessary to set bit 7 of register 0x15 to manually set the DFE tap weights. This bit is cleared by default.

Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting.

The polarity of the tap weight for tap 1 is set using bit 7 of the same register, register 0x12. The polarity is set to 0 by default, which corresponds to a negative algebraic sign for the tap.

The other four taps are set using four-bit fields in registers 0x20 and 0x21. The polarities of these taps are set by bits 3:0 in register 0x11. These tap polarities are all set to 0 by default.

As is the case for the CTLE settings, if changing the DFE tap weights or polarities causes the DS110DF111 to lose lock, it may readapt its CTLE in order to reacquire lock. If this occurs, the CTLE settings may appear to change spontaneously when the DFE tap weights are changed. The mechanism is the same as that described above for the CTLE boost settings.

When the DS110DF111 is set to adapt mode 2 or 3 using bits 6:5 of register 0x31, it will automatically adapt its DFE whenever its CDR state machine is reset. This occurs when the user manually resets the CDR state machine using bits 3:2 of register 0x0a, or when a signal is first presented at the input to the channel when the channel is in an unlocked state.

Regardless of the adapt mode, DFE adaptation can be initiated under SMBus control. Because the DFE tap weight registers are used by the DFE state machine during adaptation, they may be reset prior to adaptation, which can cause the adaptation to fail. The DFE tap observation registers can be used to prevent this.

Prior to initiating DFE adaptation under SMBus control, write the starting values of the DFE tap settings into the DFE tap weight registers, registers 0x11, 0x12, 0x20, and 0x21. The values can be read from the observation registers, registers 0x71 through 0x75. For each DFE tap, read the current value in the observation register. Both the polarities and the tap weights are contained in the observation registers. For each DFE tap, write the current tap polarity and tap weight into the DFE tap register. Once all these values have been written, DFE adaptation can be initiated and it will proceed normally. If the DS110DF111 fails to find a set of DFE tap weights producing a better adaptation figure of merit than the starting tap weights, the starting tap weights will be retained and used.

CTLE adaptation can also be initiated manually. Setting and then clearing bit 0 of register 0x2f will initiate adaptation of the CTLE. As with the DFE, if the DS110DF111 fails to find a set of CTLE settings that produce a better adaptation figure of merit than the starting CTLE values, the starting CTLE values will be retained and used.

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Enabling Slow Rise/Fall Time on the Output Driver

Register 0x18, bit 2

Normally the rise and fall times of the output driver of the DS110DF111 are set by the slew rate of the output transistors. By default, the output transistors are biased to provide the maximum possible slew rate, and hence the minimum possible rise and fall times. In some applications, slower rise and fall times may be desired. For example, slower rise and fall times may reduce the amplitude of electromagnetic interference (EMI) produced by a system.

Setting bit 2 of register 0x18 will adjust the output driver circuitry to increase the rise and fall times of the signal. Setting this bit will approximately double the nominal rise and fall times of the DS110DF111 output driver. This bit is cleared by default.

Inverting the Output Polarity

Register 0x1f, bit 7

In some systems, the polarity of the data does not matter. In systems where it does matter, it is sometimes necessary, for the purposes of trace routing, for example, to invert the normal polarities of the data signals.

The DS110DF111 can invert the polarity of the data signals by means of a register write. Writing a 1 to bit 7 of register 0x1f inverts the polarity of the output signal for the selected channel. This can provide additional flexibility in system design and board layout.

Overriding the Figure of Merit Adaption

Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6

The default figure of merit for both the CTLE and DFE adaptation is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both large and approximately equal in magnitude. This usually provides optimum bit error rate performance for most transmission channels.

Table 12. DS110DF111 Adaption Algorithm Settings, Register 0x31 Bits 6:5

REGISTER 0X31, BIT 6 adapt_mode [1]	REGISTER 0x31, BIT 5 adapt_mode [0]	ADAPT MODE SETTING <1:0>	ADAPTION ALGORITHM
0	0	00	No Adaption
0	1	01	Adapt CTLE Until Optimum
1	0	10	Adapt CTLE Until Optimum the DFE, then CTLE Again (Default)
1	1	11	Adapt CTLE Until Lock, the DFE, the CTLE Again

In the DS110DF111 the CTLE figure of merit type is selected using the two-bit field in register 0x31, bits 6:5.

Table 13. Figure of Merit Type Settings

VALUE IN BITS 5:4 OF REGISTER 0x2C	FIGURE OF MERIT TYPE
0x0	Both HEO and VEO used
0x1	Only HEO used
0x2	Only VEO used
0x3 (Default)	Both HEO and VEO used

For some transmission media the adaptation can reach a better setting if a different figure of merit is used. The DS110DF111 includes the capability of adapting based on a configurable figure of merit. The configurable figure of merit is structured as shown in the equation below.

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FOM = Minimum [(HEO - b) x a, (VEO - c) x (1 - a)]

where

- HEO is horizontal eye opening
- VEO is vertical eye opening
- FOM is the figure of merit
- the factors a, b, and c are set using registers 0x6b, 0x6c, and 0x6d respectively (1)

In order to use the configurable figure of merit, the enable bits must be set. To use the configurable figure of merit for the CTLE adaptation, set bit 7 of register 0x6e. To use the configurable figure of merit for the DFE adaptation, set bit 6 of register 0x6e. The same scaling factors are used for both CTLE and DFE adaptation when the configurable figure of merit is enabled.

Setting the Rate and Subrate for Lock Acquisition

Register 0x2f, bits 7:6

The rate and subrate settings, which constrain the data rate search can be set using channel register 0x2f. Bits 7:6 are RATE<1:0>, and bits 5:4 are SUBRATE<1:0>.

Setting the Adaption/Lock Mode

Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a

There are four adaptation modes available in the DS110DF111.

- Mode 0: The user is responsible for setting the CTLE and DFE (for the DS110DF111) values. This mode is used if the transmission channel response is fixed.
- Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled , but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces.
- Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0.
- Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels.

Bits 6:5 of register 0x31 determine the adaptation mode to be used. The mapping of these register bits to the adaptation algorithm is shown in.

By default the DS110DF111 requires that the equalized internal eye exhibit horizontal and vertical eye openings greater than a pre-set minimum in order to declare a successful lock. The minimum values are set in register 0x6a.

The DS110DF111 continuously monitors the horizontal and vertical eye openings while it is in lock. If the eye opening falls below the threshold set in register 0x6a, the DS110DF111 will declare a loss of lock.

The continuous monitoring of the horizontal and vertical eye openings may be disabled by clearing bit 7 of register 0x3e.

Initiating Adaption

Register 0x24, bit 2, and Register 0x2f, bit 0

When the DS110DF111 becomes unlocked, it will automatically try to acquire lock. If an adaptation mode is selected using bits 6:5 in register 0x31, the DS110DF111 will also try to adapt its CTLE and DFE.

Adaptation can also be initiated by the user. CTLE adaptation can be initiated by setting and then clearing register 0x2f, bit 0. In the DS110DF111, DFE adaptation can be initiated by setting and then clearing bit 2 of register 0x24.

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Overriding the CTLE Settings used for CTLE Adaption

Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x40-0x4f

The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS110DF111 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS110DF111 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS110DF111 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS110DF111 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS110DF111 still continues to try additional CTLE settings for a pre-determined trial count called the “look-beyond” count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The “look-beyond” count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default.

The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x4F. The default values for these settings are shown in Table 14. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS110DF111.

Table 14. CTLE Settings for Adaption, Register 0x40-0x4F

REGISTER (HEX)	BITS 7:6 (CTLE STAGE 0)	BITS 5:4 (CTLE STAGE 1)	BITS 3:2 (CTLE STAGE 2)	BITS 1:0 (CTLE STAGE 3)	CTLE BOOST STRING	CTLE ADAPTATION INDEX
40	0	0	0	0	0000	0
41	1	0	0	0	1000	1
42	2	0	0	0	2000	2
43	1	1	0	0	1100	3
44	3	0	0	0	3000	4
45	2	1	0	0	2100	5
46	1	1	1	0	1110	6
47	2	2	0	0	2200	7
48	2	3	0	0	2300	8
49	2	1	1	1	2111	9
4A	1	2	2	1	1221	10
4B	3	1	1	1	3111	11
4C	2	1	2	1	2121	12
4D	2	2	1	1	2211	13
4E	3	2	1	2	3212	14
4F	3	3	2	1	3321	15

As an alternative to, or in conjunction with, writing the CTLE boost setting registers 0x40 through 0x4f, it is possible to set the starting CTLE boost setting index. To override the default setting, which is 0, set bit 3 of register 0x2f. When this bit is set, the starting index for adaptation comes from register 0x39, bits 4:0. This is the index into the CTLE settings table in registers 0x40 through 0x4f. When this starting index is 0, which is the default, CTLE adaptation starts at the first setting in the table, the one in register 0x40, and continues until the optimum FOM is reached.

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Table 15. VOD Settings

VODA/B	BIT 2, sel_vod[2]	BIT 1, sel_vod[1]	BIT 0, sel_vod[0]	OUTPUT VOD (mVppd)
0	0	0	0	600
R	0	0	1	700
	0	1	0	800
	0	1	1	900
F	1	0	0	1000
1	1	0	1	1100
	1	1	0	1200
	1	1	1	1300

Setting the Output Differential Voltage

Register 0x2d, bits 2:0

There are eight levels of output differential voltage available in the DS110DF111, from 0.6 V to 1.3 V in 0.1 V increments. The values in bits 2:0 of register 0x2d set the output VOD. The available VOD settings and the corresponding values of this bit field are shown in Table 15. Not all VOD levels are available using the VODA/B control pins.

Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 16.

Table 16. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

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Table 17. Revision History

Revision	Date	Update	Comments
0.1	4-25-2012	Lee Sledjeski	Initial Revision
0.2	7-23-2012	Nate Unger	1. Added LBK pin and function2.
0.3	7-24-2012	Nate Unger	1.Added pin mode functions; VOD, De-emphasis, loopback, RATE/SUBRATE, 2.Changed Loopback feature to control wire-side loopback when pulled down
0.4	7-27-2012	Nate Unger	1. Moved LBK pin to 6 2. Removed RATE and SUBRATE 3. Added DEMA and DEMB 4. Added VODA and VODB5
0.41	7-29-2012	Nate Unger	Revised look and feel to fit TI template Added RATE and SUBRATE table for register operation Added loopback diagrams Fixed table and figure numbering Fixed many formatting issues Inserted register commands for loopback
0.42	8-1-2012	Nate Unger	Updated table reference numbers Added register descriptions for 0x18, 0x1f, 0x20 Reduced reference modes from table 21 Fixed figure 1 reference on page Fixed reference to VODB pin 10 in table 7
0.45	8-24-2012	Lee Sledjeski	Updated pin type to reflect definitions Added Shared reg0x07[1:0] for Loopback Added Channel reg0x04[3:2] for DWDM/ZR
0.5	9-27-2012	Lee Sledjeski	Updated Address input to a 2-level pin Updated Table 9 (SMBus address) Added FANOUT modes to the Loopback function Reduced CTLE table to 16 values
0.5	9-27-2012	Lee Sledjeski	Copied version from DS110RT/DF111
0.51	9-28-2012	Lee Sledjeski	Updated Rate/Subrate information in Table 13
0.52	9-28-2012	Lee Sledjeski	Updated graphics to DS125DF111 part #
0.53	9-28-2012	Lee Sledjeski	Removed register description and tables Added Alpha vs Production section
0.55	10-15-2012	Lee Sledjeski	Changed temperature range: -40 – 85C
0.6	10-26-2012	Lee Sledjeski	Updated Electrical Table Removed non-DF information Added ADDR1 input on Pin 9
0.65	10-30-2012	Lee Sledjeski	Added LOS/INT# pin 13 information Updated graphics and tables to have a common pin naming convention; Strap/Slave/Pin/Master
	11-7-2012	Lee Sledjeski	Converted to DS110 datasheet
0.70	12-12-12	Lee Sledjeski	Adjusted Package Thermal and power dissipation Removed VRX-IN Increased Dj to 5ps Removed Jtrans
0.71	12-18-12	Lee Sledjeski	Used DS110DF111 Version 0.70 as a starting point to create new DS125DF111 datasheet Updated default to be Rate/Subrate = 06 which enables all divider options 1,2,4, and 8.
0.8	1-31-2013	Lee Sledjeski	Removed references to Alpha Silicon Made DS110 primary version Default data – rates 1.25 / 10.3125 Gbps Adjusted Trise,TPD,Tlock range Added TPD – raw data
0.81	2-04-2013	Lee Sledjeski	Updated 1st page graphic to remove TIA interface
0.82	3-26-2013	Lee Sledjeski	Updated SMBus table to match pinout
0.85	4-03-2013	Lee Sledjeski	Updated DEM table to match PRS features doc
0.9	4-10-2013	Lee Sledjeski	Updated Version and Device ID (expected RTM)

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Table 17. Revision History (continued)

0.91	4-10-2013	Lee Sledjeski	Fixed description on Channel Reg 0x31
0.92	4-16-2013	Lee Sledjeski	Updated VOD Table 17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS110DF111SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	1D111B3	Samples
DS110DF111SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	1D111B3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

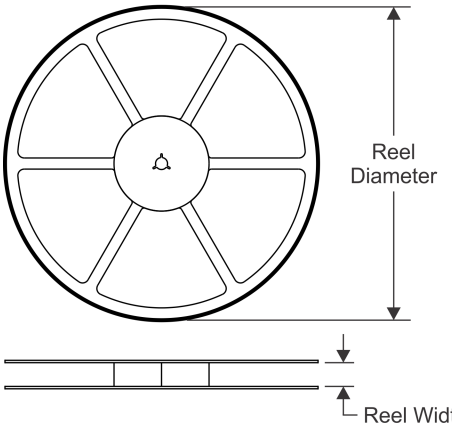
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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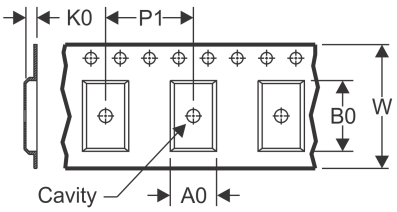
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TAPE AND REEL INFORMATION

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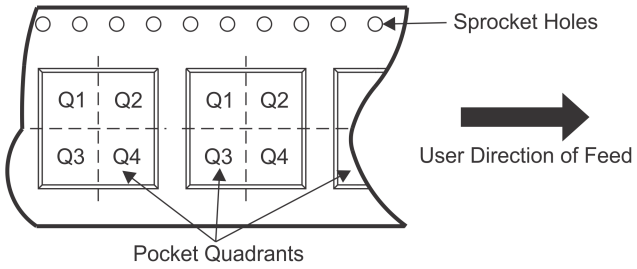


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

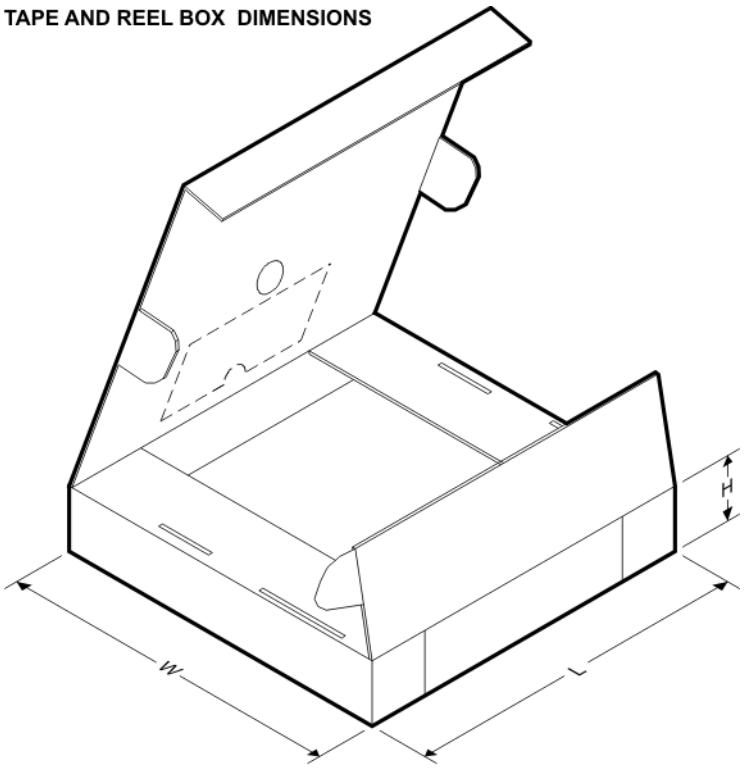
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS110DF111SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS110DF111SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

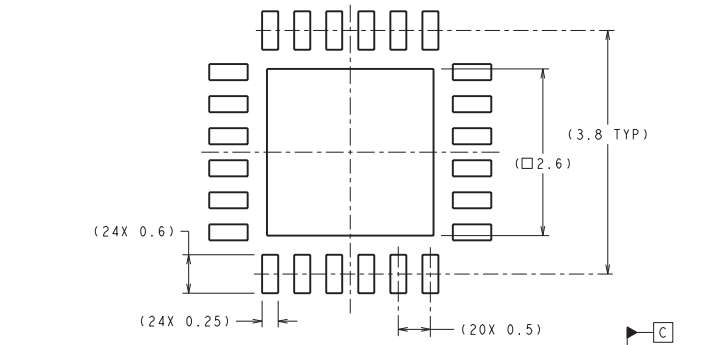
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

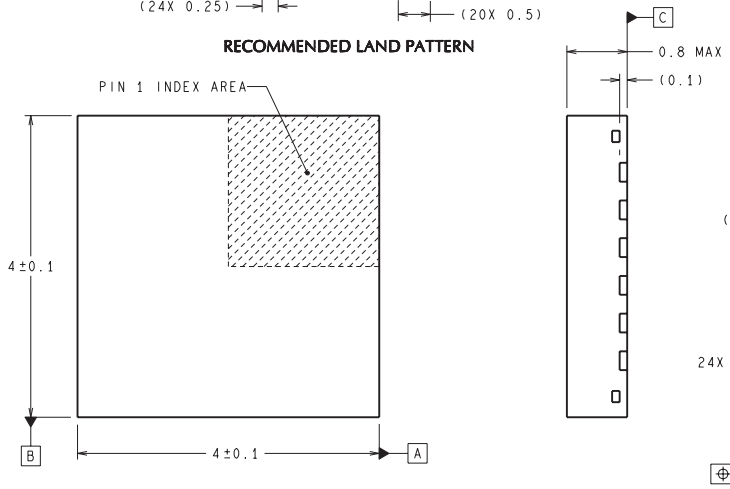
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS110DF111SQ/NOPB	WQFN	RTW	24	1000	213.0	191.0	55.0
DS110DF111SQE/NOPB	WQFN	RTW	24	250	213.0	191.0	55.0

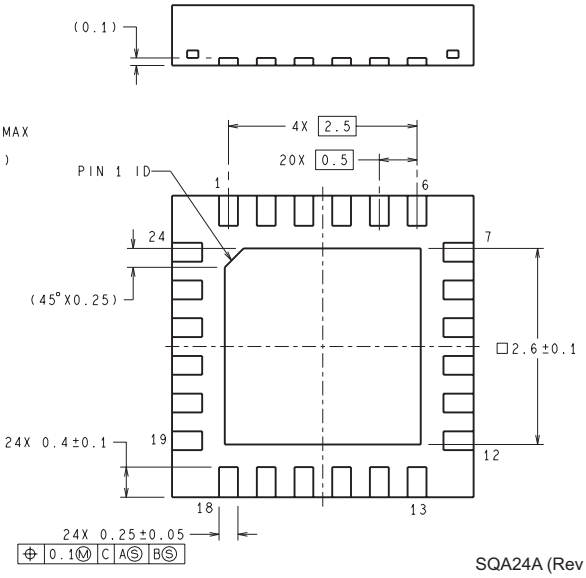
RTW0024A



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SQA24A (Rev B)

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