TDA8026

Multiple smart card slot interface IC

Rev. 1.1 — 30 June 2016 Product data sheet

1. General description

The TDA8026 is a cost-effective, analog interface for addressing multiple smart card slots in a Point Of Sales (POS) terminal. It can address up to two main cards (synchronous or asynchronous smart cards supported) and up to four Security Access Modules (SAMs). Its packaging supports the latest payment terminal security requirements.

2. Features and benefits

- I^2C-bus controlled IC card interface in a TFBGA64 package
- Supply voltage between 2.7 V and 5.5 V
- Dedicated microcontroller interface supply voltage ($V_{DD(INTF)}$)
- Shutdown mode ensures very low power consumption when the TDA8026 is inactive
- Programmable power reduction modes triggered when the card slots are inactive
- $V_{CC(n)}$ generation via DC-to-DC converter: two card slots can be fully loaded, the three others in reduced consumption mode
- Two clock input pins: CLKIN1 for card slot 1 and CLKIN2 for card slots 2 to 5
- Two transparent I/O lines on microcontroller side, one for card slot 1 and the other for card slots 2 to 5
- Five protected, half-duplex, bidirectional, buffered I/O lines with current limitation at ± 15 mA and a maximum frequency 1 MHz
- Two I^2C-bus controlled auxiliary I/O lines
- $V_{CC(n)}$ regulation on all card slots at $I_{CC} \leq 55$ mA:
  - 5 V, 3 V or 1.8 V ± 5 %
  - Current spikes of 40 nAs up to 20 MHz for 5 V cards with controlled rise and fall times
  - Current limitation of approximately 100 mA
- Thermal protection and short-circuit protection on all card contacts
- Automatic activation and deactivation sequences initiated by the software or hardware in the event of a short-circuit, card take-off or voltage drop-out for $V_{DD(INTF)}$, V_{DD} or V_{UP}
- Enhanced ElectroStatic Discharge (ESD) protection on the card-side up to 6 kV
- 20 MHz clock input
- Card clock generation up to 20 MHz and dividable by 1, 2, 4 or 5 with synchronous frequency changes:
  - Stop, HIGH or LOW
  - Clock frequency between 1 MHz and 2.2 MHz in card low-power mode
  - Current limitation on pin $CLK_{(n)}$

- $RST_{(n)}$ signal lines with current limitation at 20 mA, controlled by an embedded programmable clock pulse counter on asynchronous cards or by a register on synchronous cards
- ISO 7816-3 and EMV 4.3[1] payment systems compatibility
- $V_{DD(INTF)}$ supply voltage supervisor ensures correct communication between microcontroller and circuit; threshold internally fixed or set using an external resistor bridge
- V_{DD} supply voltage supervisor for spike suppression during power-on and emergency deactivation at power-off; threshold internally fixed
- Card presence input with a 17.8 ms (typical) built-in debouncing system on card slots 1 and 2
- One interrupt signal (IRQN)

3. Applications

- Point Of Sale terminals
- Multiple SAM contact readers

4. Quick reference data

Table 1. Quick reference data

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage	on pin V_{DD}; DC-to-DC converter on	[1]	2.7	-	5.5	V
		on pin V_{DD}; DC-to-DC converter off and $V_{CC(n)}$ pin = 5 V	[1]	5.25	-	5.5	V
I_{DD}	supply current	shutdown mode		-	25	40	µA
		Standby mode		-	300	450	µA
		clock-stop mode; all card slots in this mode; $f_{clk(ext)}$ stopped on pins $CLK_{(n)}$; pins CLKIN1 and CLKIN2 either stopped, HIGH-level or LOW-level		-	3.7	-	mA
		active mode; all $V_{CC(n)}$ pins = 5 V; $f_{clk(ext)}$ on pins $CLK_{(n)}$ = 5 MHz; $I_{CC(1)}$ = $I_{CC(2)}$ = 55 mA; $I_{CC(3)}$ = $I_{CC(4)}$ = $I_{CC(5)}$ = 2 mA	[2] [3]	-	210	260	mA
$V_{DD(INTF)}$	interface supply voltage	on pin $V_{DD(INTF)}$		1.6	-	3.6	V
$I_{DD(INTF)}$	interface supply current	shutdown mode		-	10	15	µA
		active mode; all $V_{CC(n)}$ pins = 5 V; $f_{clk(ext)}$ on pins $CLK_{(n)}$ = 5 MHz		-	35	-	µA

1. for C3 version

Table 1. Quick reference data *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Card supply voltage pins: $V_{CC(1)}$ to $V_{CC(5)}$ [4]							
V_{CC}	supply voltage	active mode; 2.7 V < V_{DD} < 5.5 V	[5]				
		5 V card; DC $I_{CC(n)} \leq$ 55 mA		4.75	5	5.25	V
		3 V card; DC $I_{CC(n)} \leq$ 55 mA		2.85	3	3.15	V
		1.8 V card; DC $I_{CC(n)} \leq$ 35 mA		1.71	1.8	1.89	V
		active mode; AC current pulses with I < 200 mA, t < 400 ns and f < 20 MHz	[5]				
		5 V card; current spikes of 40 nAs		4.65	-	5.35	V
		3 V card; current spikes of 17.5 nAs		2.76	-	3.24	V
		1.8 V card; current spikes of 11.1 nAs		1.62	-	1.98	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	20 kHz to 200 MHz with default Register6 (Slew Rate register) settings		-	-	350	mV
I_{CC}	supply current	$V_{CC(n)}$ = 5 V		-	-	55	mA
		V_{CC}(n) = 3 V		-	-	55	mA
		V_{CC}(n) = 1.8 V		-	-	35	mA
		sum of all card supply currents on pins $V_{CC(n)}$; active mode; All V_{CC} pins = 5 V; $f_{clk(ext)}$ on pins $CLK_{(n)}$ = 5 MHz; $I_{CC(1)}$ = $I_{CC(2)}$ = 55 mA; $I_{CC(3)}$ = $I_{CC(4)}$ = $I_{CC(5)}$ = 2 mA	[3]	-	116	125	mA
General							
t_{deact}	deactivation time	total sequence	[6]	60	80	100	µs
t_{deb}	debounce time			-	17.8	23.8	ms
P_{tot}	total power dissipation	T_{amb} = −25 °C to +85 °C		-	455	665	mW
T_{amb}	ambient temperature			−25	+25	+85	°C

[1] Refer to Section 8.6 for further information about the DC-to-DC converter operation.

[2] Typical value measurement based on a 85 % DC-to-DC converter and inductance efficiency; depends on PCB layout and external component quality (inductor, capacitor).

[3] Maximum value measurement based on a 125 mA (sum of all card supply currents on pins $V_{CC(n)}$) current load and a 75 % DC-to-DC converter and inductance efficiency; depends on PCB layout and external component quality (inductor, capacitor).

[4] Two ceramic multilayer 100 nF (minimum) capacitors with a low Equivalent Series Resistance (ESR) should be used to meet these specifications.

[5] Output voltage to the card including ripple.

[6] Refer to Section 8.8.3 for further information.

5. Ordering information

The TDA8026 is available in 2 versions. All version have the same functionality. The C3 version is compliant with EMVC0 4.3

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8026ET/C2	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls	SOT1073-1
TDA8026ET/C3	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls	SOT1073-1

6. Block diagram

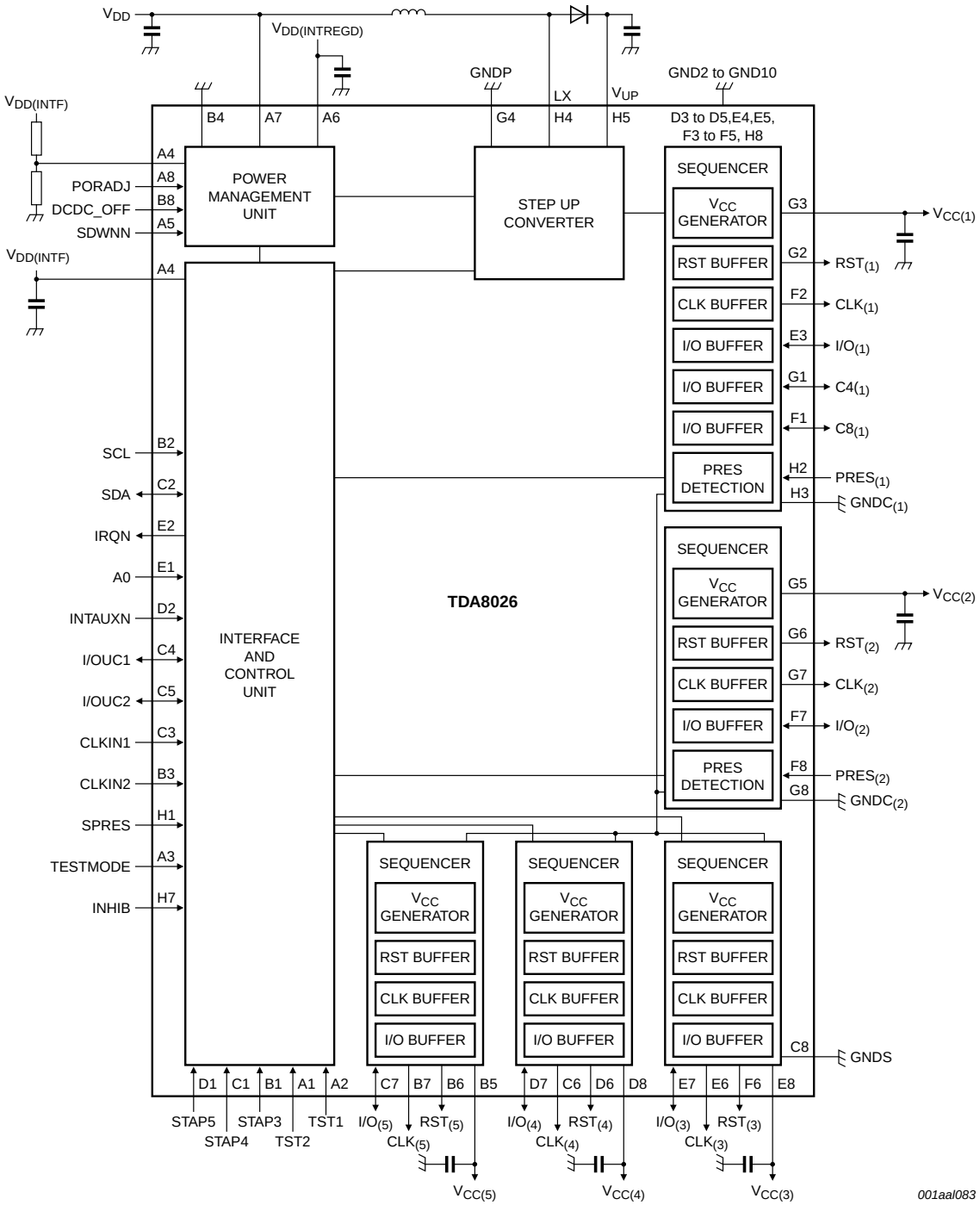


Fig 1. TDA8026 Block diagram

7. Pinning information

7.1 Pinning

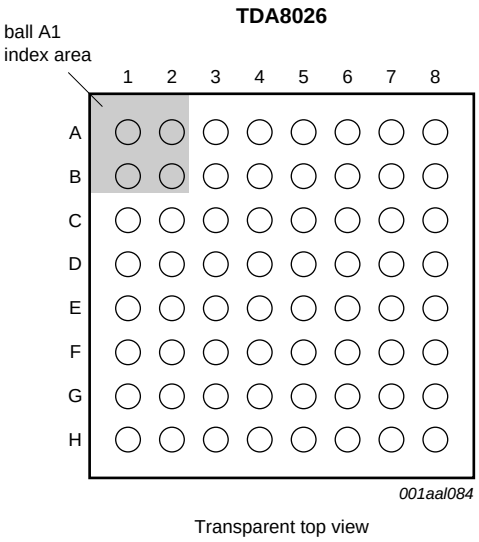


Fig 2. TDA8026 pin configuration for the TFBGA64 package

Table 3. TDA8026 ball map

Ball position[1][2]								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
A	TST2	TST1	TESTMODE	$V_{DD(INTF)}$	SDWNN	$V_{DD(INTREGD)}$	V_{DD}	PORADJ
B	STAP3	SCL	CLKIN2	GND1	$V_{CC(5)}$	$RST_{(5)}$	$CLK_{(5)}$	DCDC_OFF
C	STAP4	SDA	CLKIN1	I/OUC1	I/OUC2	$CLK_{(4)}$	$I/O_{(5)}$	GNDS
D	STAP5	INTAUXN	GND2	GND3	GND4	$RST_{(4)}$	$I/O_{(4)}$	$V_{CC(4)}$
E	A0	IRQN	$I/O_{(1)}$	GND5	GND6	$CLK_{(3)}$	$I/O_{(3)}$	$V_{CC(3)}$
F	$C8_{(1)}$	$CLK_{(1)}$	GND7	GND8	GND9	$RST_{(3)}$	$I/O_{(2)}$	$PRES_{(2)}$
G	$C4_{(1)}$	$RST_{(1)}$	$V_{CC(1)}$	GNDP	$V_{CC(2)}$	$RST_{(2)}$	$CLK_{(2)}$	$GNDC_{(2)}$
H	SPRES	$PRES_{(1)}$	$GNDC_{(1)}$	LX	V_{UP}	n.c.	INHIB	GND10

[1] The numbers in subscript and between brackets "$_{(n)}$" indicate the relevant card slot.

[2] The ball positions are those when the TDA8026 is viewed from the top.

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Supply power	Description
IRQN	E2	O	$V_{DD(INTF)}$	microcontroller interrupt; active LOW; open-drain
INTAUXN	D2	I	$V_{DD(INTF)}$	auxiliary interrupt line input: auxiliary contact reader front end not connected: connect INTAUXN pad to supply voltage $V_{DD(INTF)}$ auxiliary contact reader front end connected: connect INTAUXN pad to an external 10 kΩ pull-up resistor; active LOW
SDWNN	A5	I[3]	$V_{DD(INTF)}$	shutdown and reset input; active LOW
$V_{DD(INTF)}$	A4	P	$V_{DD(INTF)}$	microcontroller interface supply voltage
SDA	C2	I/O	$V_{DD(INTF)}$	serial data line to and from the I^2C-bus master; open-drain
SCL	B2	I	$V_{DD(INTF)}$	serial clock line from the I^2C-bus master
A0	E1	C	$V_{DD(INTF)}$	I^2C-bus address configuration and selection
SPRES	H1	C	$V_{DD(INTF)}$	PRES mode[2] configuration and selection
CLKIN1	C3	I	$V_{DD(INTF)}$	card slot 1 external clock input; connect external clock ($f_{clk(ext)}$) to generate the $CLK_{(1)}$ frequency
CLKIN2	B3	I	$V_{DD(INTF)}$	card slots 2 to 5 external clock input; connect external clock ($f_{clk(ext)}$) to generate the $CLK_{(2)}$ to $CLK_{(5)}$ frequency
GND1	B4	G	-	ground connection
I/OUC1	C4	I/O[3]	$V_{DD(INTF)}$	card slot 1 microcontroller data input and output
I/OUC2	C5	I/O[3]	$V_{DD(INTF)}$	card slots 2 to 5 microcontroller data input and output
$V_{CC(1)}$	G3	P	$V_{CC(1)}$	card slot 1 card supply; position C1
$RST_{(1)}$	G2	O	$V_{CC(1)}$	card slot 1 card reset output; position C2
$CLK_{(1)}$	F2	O	$V_{CC(1)}$	card slot 1 card clock output; provides f_{CLK}; position C3
$C4_{(1)}$	G1	I/O[4]	$V_{CC(1)}$	card slot 1 auxiliary input and output; position C4
$C8_{(1)}$	F1	I/O[4]	$V_{CC(1)}$	card slot 1 auxiliary input and output; position C8
$I/O_{(1)}$	E3	I/O[4]	$V_{CC(1)}$	card slot 1 card input and output; position C7
$GNDC_{(1)}$	H3	G	-	card slot 1 card ground signal; position C5
$PRES_{(1)}$	H2	I	$V_{DD(INTF)}$	card slot 1 card presence input
$V_{CC(2)}$	G5	P	$V_{CC(2)}$	card slot 2 card supply; position C1
$RST_{(2)}$	G6	O	$V_{CC(2)}$	card slot 2 card reset; position C2
$CLK_{(2)}$	G7	O	$V_{CC(2)}$	card slot 2 card clock output; provides f_{CLK}; position C3
$I/O_{(2)}$	F7	I/O[4]	$V_{CC(2)}$	card slot 2 card input and output; position C7
$GNDC_{(2)}$	G8	G	-	card slot 2 card signal ground; position C5
$PRES_{(2)}$	F8	I	$V_{DD(INTF)}$	card slot 2 card presence input
GNDS	C8	G	-	card slots 3 to 5 card signal ground; position C5
$V_{CC(3)}$	E8	P	$V_{CC(3)}$	card slot 3 card supply; position C1
$RST_{(3)}$	F6	O	$V_{CC(3)}$	card slot 3 card reset output; position C2
$CLK_{(3)}$	E6	O	$V_{CC(3)}$	card slot 3 card clock output; provides f_{CLK}; position C3
$I/O_{(3)}$	E7	I/O[4]	$V_{CC(3)}$	card slot 3 card input and output; position C7

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Supply power	Description
$V_{CC(4)}$	D8	P	$V_{CC(4)}$	card slot 4 card supply; position C1
$RST_{(4)}$	D6	O	$V_{CC(4)}$	card slot 4 card reset output; position C2
$CLK_{(4)}$	C6	O	$V_{CC(4)}$	card slot 4 card clock output; provides f_{CLK}; position C3
$I/O_{(4)}$	D7	I/O[4]	$V_{CC(4)}$	card slot 4 card input and output; position C7
$V_{CC(5)}$	B5	P	$V_{CC(5)}$	card slot 5 card supply; position C1
$RST_{(5)}$	B6	O	$V_{CC(5)}$	card slot 5 card reset output; position C2
$CLK_{(5)}$	B7	O	$V_{CC(5)}$	card slot 5 card clock output; provides f_{CLK}; position C3
$I/O_{(5)}$	C7	I/O[4]	$V_{CC(5)}$	card slot 5 card input and output; position C7
TST1	A2	C	$V_{DD(INTF)}$	test pin; connect to ground
TST2	A1	C	$V_{DD(INTF)}$	test pin; connect to ground
STAP3	B1	I	$V_{DD(INTF)}$	card slot 3 presence status input[5]
STAP4	C1	I	$V_{DD(INTF)}$	card slot 4 presence status input[5]
STAP5	D1	I	$V_{DD(INTF)}$	card slot 5 status presence input[5]
n.c.	H6	-	-	not connected
PORADJ	A8	I	$V_{DD(INTF)}$	power-on reset threshold input for $V_{DD(INTF)}$: threshold used: connect pin PORADJ using an external resistor bridge threshold not used: connect to $V_{DD(INTF)}$
V_{DD}	A7	P	V_{DD}	main supply voltage
V_{UP}	H5	O	V_{UP}	DC-to-DC converter output
LX	H4	I	LX	DC-to-DC converter power supply input
GNDP	G4	G	-	DC-to-DC converter ground
$V_{DD(INTREGD)}$	A6	O	V_{DD}	internal voltage regulator output
DCDC_OFF	B8	C	$V_{DD(INTF)}$	DC-to-DC converter on/off control; active HIGH
INHIB	H7	C	$V_{DD(INTF)}$	connect to ground
TESTMODE	A3	C	$V_{DD(INTF)}$	connect to ground
GND2	D3	G	-	ground
GND3	D4	G	-	ground
GND4	D5	G	-	ground
GND5	E4	G	-	ground
GND6	E5	G	-	ground
GND7	F3	G	-	ground
GND8	F4	G	-	ground
GND9	F5	G	-	ground
GND10	H8	G	-	ground

[1] I = Input, O = Output, P = Power, G = Ground, C = Configuration.

[2] Refer to the *Application note AN10724* for further information.

[3] Integrated pull-up to $V_{DD(INTF)}$ value.

[4] Integrated pull-up to the related $V_{CC(n)}$ value.

[5] In Shutdown mode, set to LOW.

8. Functional description

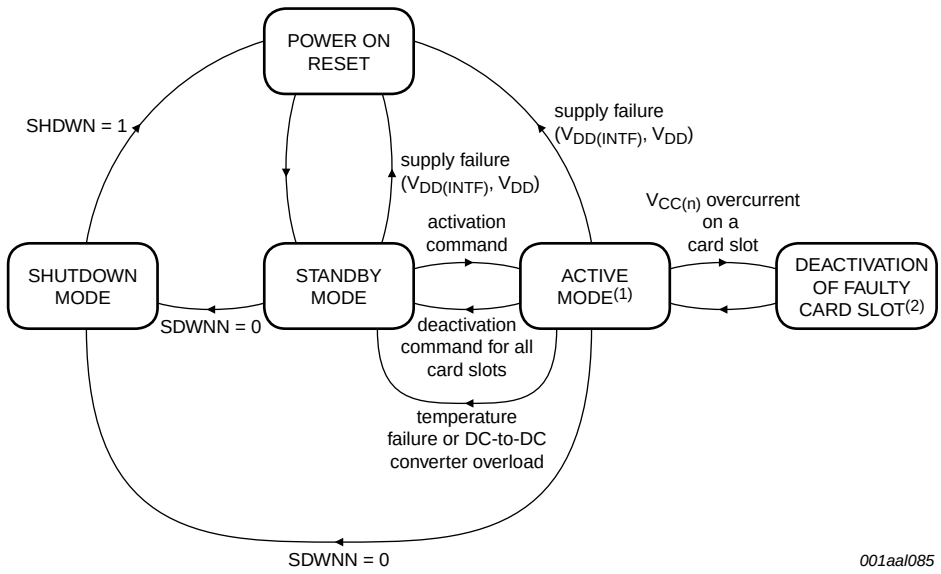
Remark: Throughout this document ISO 7816-3 and EMV standard terminology conventions have been adhered to and it is assumed that the reader is familiar with these.

8.1 Power supplies

The TDA8026 supply pins are V_{DD}, $V_{DD(INTF)}$ and GND1 to GND10.

- V_{DD} must be between 2.7 V and 5.5 V
- $V_{DD(INTF)}$ must be between 1.6 V and 3.6 V

The V_{DD}, $V_{DD(INTF)}$ supply voltages can be applied to the device at any time, in any sequence. All interface signals to the system controller are referenced to the $V_{DD(INTF)}$ supply voltage which can be lower or higher than V_{DD}. The integrated DC-to-DC converter generates the card supply voltage ($V_{CC(n)}$) of either 5 V , 3 V or 1.8 V (± 5 %). In addition, the internal voltage regulator delivers $V_{DD(INTREGD)}$ 3.3 V supply voltage.



(1) Active mode; DC-to-DC converter is ON.

(2) $V_{CC(n)}$ overcurrent on a card slot causes deactivation of a faulty card slot. All others remain active.

Fig 3. TDA8026 Power diagram

8.2 Power modes

Three power modes are available for the TDA8026. These are:

- Standby mode
- Active mode with a clock-stop sub-mode
- Shutdown mode

8.2.1 Standby mode

In Standby mode, both the supply voltages V_{DD} and $V_{DD(INTF)}$ are applied within the specification limits as described in Table 40 on page 40. In addition, the DC-to-DC converter is not running and the card slots are not activated.

8.2.2 Active mode

In active mode, both the V_{DD} and $V_{DD(INTF)}$ supply voltages are applied to the device within the specification limits as described in Table 40 on page 40. A minimum of one card slot is activated. All card slots can be activated at once and communication performed with up to two cards slots.

The DC-to-DC converter has been developed to handle a 116 mA (typical) DC load. This allows two active card slots to communicate with a load of 55 mA while the three remaining card slots are in clock-stop mode (see Section 8.2.3 for information about this mode) with a 2 mA load.

The DC-to-DC converter overload protection is triggered when a higher current load than specified in Table 40 on page 40 is supplied to the DC-to-DC converter (see Section 8.11 for further information).

8.2.3 Clock-stop mode

Clock-stop mode is a low-power mode which is triggered when a card is activated without any communication. In this mode, a supply voltage with a low frequency clock is applied to cards that do not support the clock-stop feature.

8.2.4 Shutdown mode

Shutdown mode is the very low power consumption mode, typically 25 μA. The TDA8026 enters this mode when the SDWNN pin is driven LOW. Only presence monitoring on card slot 1 remains enabled. When card insertion or removal is detected on card slot 1, an interrupt signal (IRQN) is sent to the microcontroller.

In shutdown mode, it is assumed that the $V_{DD(INTF)}$ and V_{DD} supply voltages are stable and the SDWNN pin is active LOW.

8.2.4.1 Entering shutdown mode

Shutdown mode is activated when the SDWNN pin is driven LOW. On entering this mode:

1. All card slots are automatically deactivated
2. The power consumption is reduced on completion of the deactivation sequence.

This causes the following:

- Digital module moves in to reset mode. However, card presence monitoring on slot 1 continues to operate normally
- All card slots are disabled and all card pins are forced to 0 V. Again, card presence monitoring on slot 1 continues to operate normally
- Thermal protection is disabled
- The DC-to-DC converter is bypassed
- All interface signal pull-up resistors are disconnected from their supply rail (except the pull-up resistor on the SDWNN pin)

- I/OUC1 and I/OUC2 are set to high-impedance.

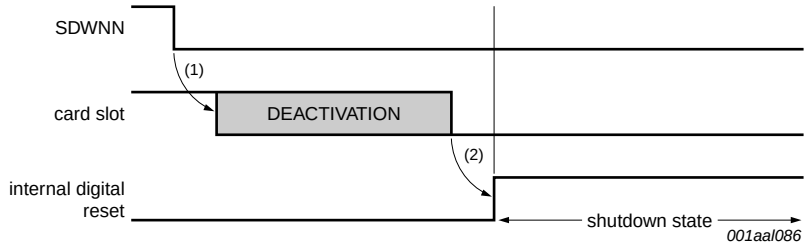


Fig 4. The enter shutdown sequence

8.2.4.2 Exiting shutdown mode

The TDA8026 performs the following steps when exiting shutdown mode:

1. Card insertion on card slot 1 is signalled by the IRQN pin signal being driven LOW.
2. Using the IRQN pin signal, the microcontroller detects the card insertion and drives the SDWNN pin HIGH to wake-up the TDA8026
3. When the SDWNN pin is HIGH, the IRQN pin is set to HIGH and the analog module is powered-up. A full power-up sequence is executed by the TDA8026
4. When the TDA8026 is ready, the IRQN pin is set to LOW
5. The microcontroller detects the device interrupt using the IRQN pin and services it which resets pin IRQN to HIGH

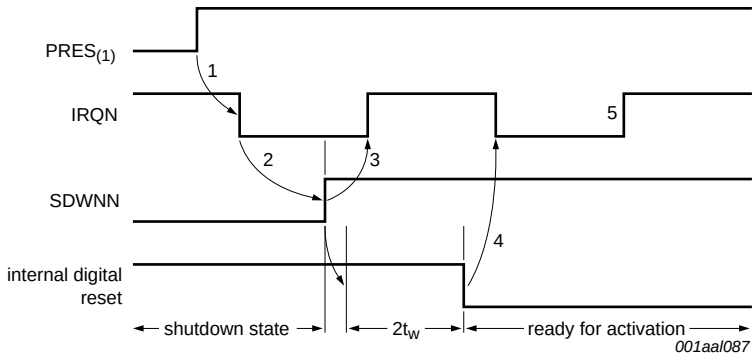


Fig 5. The exit shutdown sequence

8.3 Voltage supervisors

8.3.1 Block diagram

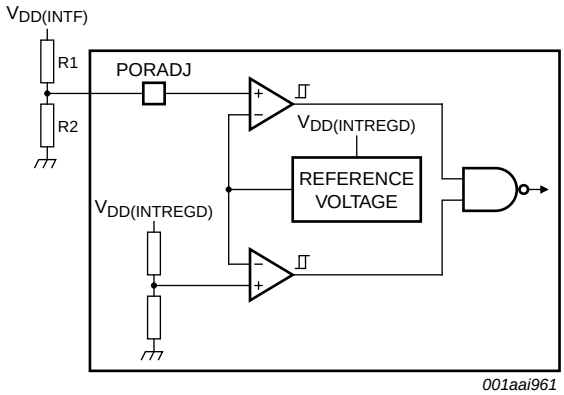


Fig 6. The voltage supervisor circuit

8.3.2 Description

The voltage supervisor can be used to perform Power-On Resets (POR) and supply drop detection during a card session. The supervisors control the internal regulated supply voltage ($V_{DD(INTREGD)}$) and the microcontroller interface supply voltage ($V_{DD(INTF)}$) to ensure problem-free operation of the TDA8026. This block controls:

- V_{DD} using the internal voltage regulator's output ($V_{DD(INTREGD)}$)
- the microcontroller interface supply voltage ($V_{DD(INTF)}$) using the voltage on the PORADJ pin (V_{PORADJ})

When an alarm occurs, the internal digital controller resets the TDA8026.

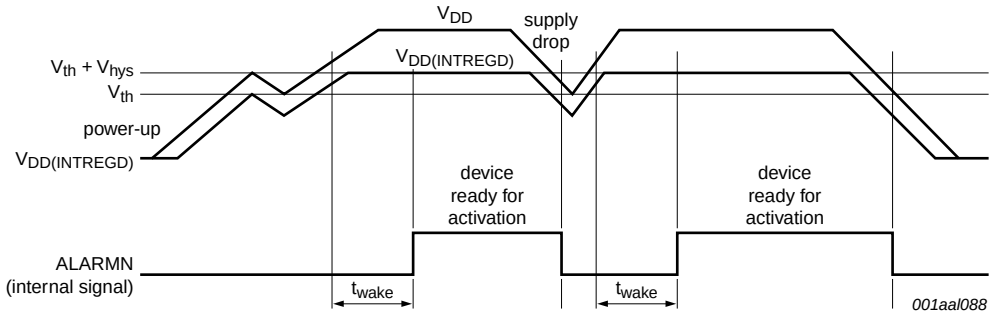


Fig 7. V_{DD} voltage supervisor

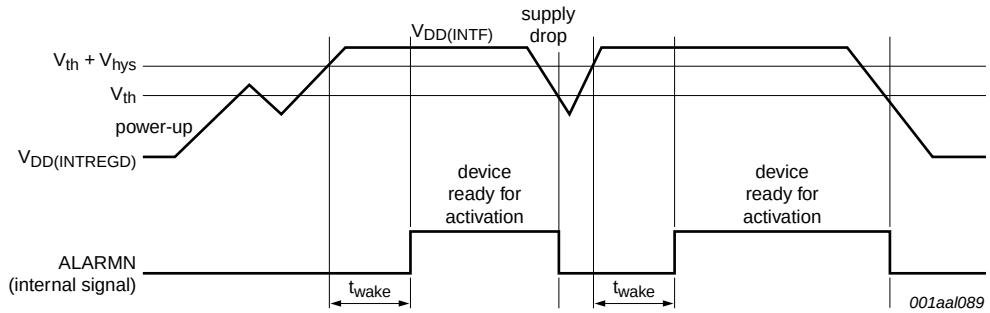


Fig 8. $V_{DD(INTF)}$ voltage supervisor

Remark: Refer to the *Application note AN10724* for further information.

8.3.3 $V_{DD(INTREGD)}$ voltage supervisor without external divider on PORADJ pin

An alarm signal is triggered and the analog controller resets the TDA8026 when:

- $V_{DD(INTREGD)}$ is less than V_{th} on pin $V_{DD(INTREGD)}$
- Pin PORADJ monitoring $V_{DD(INTF)}$ is less than V_{th}

The alarm is reset and the TDA8026 leaves reset mode 8 ms after V_{DD} and V_{PORADJ} are above their respective $V_{th} + V_{hys}$.

V_{th} on $V_{DD(INTF)}$ is set as shown in Equation 1:

$$V_{th} = V_{bg}\left(1 + \frac{R2}{R1}\right) \quad (1)$$

Thus V_{bg} = 1.21 V (see Figure 6).

In reset mode, the TDA8026 is inactive and does not respond to any external command lines.

8.4 I²C-bus description

Remark: Refer to the *I²C-bus specification* for more information.

The I²C-bus interface in the TDA8026 is an I²C-bus slave operating either Standard mode (100 kHz) or Fast mode (400 kHz). In addition, it integrates shift register functions, shift timing generation and slave address recognition.

8.4.1 I²C-bus protocol

The I²C-bus protocol is based on bidirectional, 2-line communication between ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to the $V_{DD(INTF)}$ supply voltage using a pull-up resistor (refer to the *I²C-bus specification* for more details).

The I²C-bus protocol is defined as follows:

- Data transfer can only be initialized when the I²C-bus is not busy.
- During data transfer, the data line must remain stable when the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

8.4.2 Bus conditions

The following bus conditions are defined.

Bus not busy — Both data and clock lines remain HIGH.

Start data transfer — The START condition is generated when the state of the data line changes from HIGH to LOW while the clock line is HIGH.

Stop data transfer — The STOP condition is generated when the state of the data line changes from LOW to HIGH while the clock line is HIGH.

Data valid — The data line state represents valid data, after a START condition with the data line stable for the duration of the clock signal HIGH period. There is one clock pulse per bit of data.

8.4.3 Data transfer

Each data transfer is triggered by a START condition and finished by a STOP condition (see Figure 13 for timing information).

Data transfers can be performed in Standard mode at 100 kHz or Fast mode at 400 kHz. Data transfer is performed on a byte for byte basis in both read or write modes. The information is transmitted in bytes and each receiver acknowledges with a 9th bit (acknowledge).

Each byte is followed by an acknowledge bit and the transmitter must release the SDA line during the acknowledge bit. The master generates an extra acknowledge related clock pulse. The addressed slave receiver must generate an acknowledge bit after receiving each byte. The master-receiver must generate an acknowledge bit after receiving each byte clocked out of the slave transmitter.

The acknowledging device must pull-down the SDA line during the acknowledge clock pulse to ensure the SDA line is stable LOW during the acknowledge related clock pulse HIGH period.

In addition, the set-up and hold times must be taken into account. The master-receiver must signal the end of the last data byte to the slave transmitter by not sending an acknowledge bit on the last byte that has been clocked out of the slave. The transmitter must ensure the data line is HIGH to enable the master to generate the STOP condition.

8.4.4 Device addressing

Three device addresses are needed to control the TDA8026.

- One high address: The high address enables selection of a bank page (Bank 0 or Bank 1) based on a configuration byte. A bank page relates to a card slot or general registers. See Table 7 for detailed information.
- Two low addresses: The microcontroller uses two low addresses to read and write into the selected bank page (see Table 6 on page 15 to Table 39 on page 38 for detailed information).

The addresses for the device are shown in Table 5 and Table 6.

Table 5. Base addressing

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	1	A0	0	R/W

Bit 1 is the address bit which selects Register0 or Register1. Bit 0 defines either Read or Write mode.

- When bit 0 is set to logic 1, read mode is selected
- When bit 0 is set to logic 0, write mode is selected

Table 6. Write mode addresses

A0 Pin	Bank 0 base register address (Hex)	Bank 1 Register0 address (Hex)	Bank 1 Register1 address (Hex)
0	48h	40h	42h
1	4Ch	44h	46h

Bank 1 page selection is performed when the configuration byte (CSb[7:0]) is written to the high address representing bank 0 based on the A0 pin value.

Using pin A0, two TDA8026s can be used in parallel based on the selection made to the address selection pin A0. Pin A0 is externally hardwired to the pins $V_{DD(INTF)}$ or GND. The voltage on the A0 pin sets the bit 2 address bit

8.5 Banks and registers

The device registers enable the microcontroller to control the TDA8026. These registers are defined as banks:

- Bank 0 register is a read/write register which enables selection of the required card slot number and access to the corresponding registers Bank 1 registers. In addition, Bank 0 is used to write information about the interrupt status and the product version. The registers in bank 0 (CSb[7:0] = 1h to 5h) are similar to the registers of the TDA8023.
- Bank 1 provides access to the corresponding card slot registers. Bank 1 is composed of several pages which in turn contain registers related to each individual card slot or general registers. Typically, pages can contain two general registers or five card slot related registers.

Remark: The registers are organized in bank pages in order to keep compatibility with the TDA8023.

Bank 1 page selection is performed when the configuration byte (CSb[7:0]) is written to the high I^2C-bus address representing bank 0 based on the A0 pin.

8.5.1 Register overview

Table 7. Register overview

Page number/ register Subaddress (Hex)[1]	Register name	R/W	Bit definition								Reset value (Binary)
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Bank 0: Card slot selection, product version and interrupt registers (see Table 8 and Table 9)											
-/48h	CSb	R/W	CSb[7:0]								0000 0001
Bank 1: Card slot registers (see Table 11 through Table 33)											
Slot 1											
01h/40h	Register0	R	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	PRESL	PRES	0000 1000
01h/40h	Register0	W	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START	0000 0000
01h/42h	Register1[3]	R/W	-[2]	RSTIN	C81	C41	CLKPD[1:0]		CLKDIV[1:0]		0111 1111
01h/42h	Register1[4]	R/W	D[7:0]								1010 1010
01h/42h	Register1[5]	R/W	C[15:8]								1010 0100
01h/42h	Register1[6]	R/W	C[7:0]								0111 0100
Slot 2											
02h/40h	Register0	R	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	PRESL	PRES	0000 1000
02h/40h	Register0	W	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START	0000 0000
02h/42h	Register1[3]	R/W	CFGP2	RSTIN	-[2]		CLKPD[1:0]		CLKDIV[1:0]		0100 1111
02h/42h	Register1[4]	R/W	D[7:0]								1010 1010
02h/42h	Register1[5]	R/W	C[15:8]								1010 0100
02h/42h	Register1[6]	R/W	C[7:0]								0111 0100
Slot 3											
03h/40h	Register0	R	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	-[2]	STAP3	0000 1000
03h/40h	Register0	W	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START	0000 0000
03h/42h	Register1[3]	R/W	-[2]	RSTIN	-[2]		CLKPD[1:0]		CLKDIV[1:0]		0100 1111
03h/42h	Register1[4]	R/W	D[7:0]								1010 1010
03h/42h	Register1[5]	R/W	C[15:8]								1010 0100
03h/42h	Register1[6]	R/W	C[7:0]								0111 0100

Table 7. Register overview *…continued*

Page number/ register Subaddress (Hex)[1]	Register name	R/W	Bit definition								Reset value (Binary)
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Slot 4											
04h/40h	Register0	R	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	-[2]	STAP4	0000 1000
04h/40h	Register0	W	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START	0000 0000
04h/42h	Register1[3]	R/W	-[2]	RSTIN	-[2]		CLKPD[1:0]		CLKDIV[1:0]		0100 1111
04h/42h	Register1[4]	R/W	D[7:0]								1010 1010
04h/42h	Register1[5]	R/W	C[15:8]								1010 0100
04h/42h	Register1[6]	R/W	C[7:0]								0111 0100
Slot 5											
05h/40h	Register0	R	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	-[2]	STAP5	0000 1000
05h/40h	Register0	W	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START	0000 0000
05h/42h	Register1[3]	R/W	-[2]	RSTIN	-[2]		CLKPD[1:0]		CLKDIV[1:0]		0100 1111
05h/42h	Register1[4]	R/W	D[7:0]								1010 1010
05h/42h	Register1[5]	R/W	C[15:8]								1010 0100
05h/42h	Register1[6]	R/W	C[7:0]								0111 0100
Bank 1: General registers (see Table 34 through Table 39)											
00h/42h	Product version	R	PV[7:0]								1100 0010
00h/42h	Interrupt status	R	-[2]		INTAUX	INT[4:0]					0001 1111
06h/40h	Slew rate	R/W	CLK_SR[3:2]		IO_SR[3:2]		CLK_SR[1:0]		IO_SR[1:0]		0100 0100

[1] See Table 8, Table 9 and Table 11 through Table 39 for detailed information.

[2] Reserved bit position.

[3] REG[1:0] = 00 depending on the setting for Bank1 CSb[7:0].

[4] REG[1:0] = 01 depending on the setting for Bank1 CSb[7:0].

[5] REG[1:0] = 10 depending on the setting for Bank1 CSb[7:0].

[6] REG[1:0] = 11 depending on the setting for Bank1 CSb[7:0].

8.5.2 Bank 0 register description

The device registers enable the microcontroller to control the TDA8026. The registers are organized in bank pages to ensure compatibility with the TDA8023.

Bank 0 write register enables selection of the card slot number and access to the corresponding registers in bank 1. The card slot registers in bank 1 are accessed using the configuration byte (CSb[7:0]). The range 01h to 05h is used to select the specific card slot starting at card slot 1 (01h) and ending with card slot 5 (05h) in a similar way to the TDA8023 registers.

8.5.2.1 Bank 0 register (address: 48h) bit allocation

Table 8. Bank 0 register (address: 48h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CSb[7:0]							
Access	R/W							

8.5.2.2 Bank 0 bit description

Table 9. Bank 0 bit description

Bit	Symbol	Value	Description
7 to 0	CSb[7:0]		Bank 1 page selection:
		00h	selects product version and interrupts status register page
		01h	selects card slot 1 page
		02h	selects card slot 2 page
		03h	selects card slot 3 page
		04h	selects card slot 4 page
		05h	selects card slot 5 page
		06h	selects the clock frequency and I/O lines slew rate settings page

8.5.3 Bank 1 card slots 1 and 2 register descriptions

8.5.3.1 Bank 1 CSb[7:0] Register0 (address 40h) card slot 1 and card slot 2 bit allocation

Table 10. Bank 1 CSb[7:0] Register0 (address 40h) card slot 1 and card slot 2 bit allocation

Bit	7	6	5	4	3	2	1	0
Card slot 1 (address 01h) and Card slot 2 (address 02h)								
Symbol	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	PRESL	PRES
Access	[1]R	R	R	R	R	R	R	R
Symbol	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START
Access	[1]W	W	W	W	W	W	W	W

[1] See Table 11 for the read mode bits and Table 12 for the write mode bits.

When at least one of the PRESL, SUPL, PROT, MUTE and EARLY bits is set to logic 1, IRQN pin is driven LOW until the status byte has been read. After power-on, the SUPL bit is set to logic 1 until the status byte has been read and the IRQN pin is LOW until the voltage supervisor is deactivated.

8.5.3.2 Bank 1 Register0 card slot 1 (address 01h) and card slot 2 (address 02h) read mode bit descriptions

Table 11. Bank 1 Register0 card slot 1 (address 01h) and card slot 2 (address 02h) read mode bit descriptions

Bit	Symbol	Value	Description
7	ACTIVE	1	set to logic 1: the card is active
		0	set to logic 0: the card is inactive
6	EARLY	1	set to logic 1: during ATR, when the card answers too early
		0	set to logic 0: after reading the byte
5	MUTE	1	set to logic 1: during ATR, when the card does not answer according to the ISO 7816 time period
		0	set to logic 0: after reading the byte
4	PROT	1	set to logic 1: during a card session when an overload or overheating occurs
		0	set to logic 0: after reading the byte
3	SUPL	1	set to logic 1: when the supervisor signals a fault
		0	set to logic 0: after reading the byte
2	CLKSW	1	set to logic 1: when the card slot is in Power-down mode and the clock has switched to $f_{osc(int)}/2$ **Remark:** ($f_{osc(int)}$ is the internal oscillator frequency)
		0	set to logic 0: when exiting Power-down mode and when the clock is switched back to the $f_{clk(ext)}$ frequency[1]
1	PRESL	1	set to logic 1: the card has been inserted or extracted
		0	set to logic 0: after reading the byte
0	PRES	1	set to logic 1: the card is present
		0	set to logic 0: the card is not present or has been removed

[1] $f_{clk(ext)}$ is the external clock frequency applied to pins CLKIN1 and CLKIN2.

8.5.3.3 Bank 1 Register0 card slot 1 (address 01h) and card slot 2 (address 02h) write mode bit descriptions

Table 12. Bank 1 Register0 card slot 1 (address 01h) and card slot 2 (address 02h) write mode bit descriptions

Bit	Symbol	Value	Description
7	VCC1V8[1]		used together with the 5V/3VN bit
		1	set to logic 1: $V_{CC(n)}$ = 1.8 V; ignores the 5V/3VN bit logic state
		0	set to logic 0: $V_{CC(n)}$ is set using the 5V/3VN bit
6	I/OEN[2]	1	set to logic 1: pins I/OUCn are switched to pins $I/O_{(n)}$
		0	set to logic 0: pins I/OUCn and $I/O_{(n)}$ are high-impedance with internal pull-up resistor
5 to 4	REG[1:0]	-	See Table 13 “Bank 1 CSb[7:0] Register0 (address 42h) card slots 1 and card slots 2 bit allocation” on page 22 for detailed information
3	PWDN[3]	1	set to logic 1 to apply the CLKPD[1:0] bit clock settings to pin $CLK_{(n)}$ for the selected card slot
		0	set to logic 0 to apply the CLKDIV[1:0] bits clock options to pin $CLK_{(n)}$ for the selected card slot
2	5V/3VN[1]	1	used together with VCC1V8 bit. set to logic 1 and the VCC1V8 bit is logic 0: $V_{CC(n)}$ = 5 V
		0	set to logic 0 and the VCC1V8 bit is logic 0: $V_{CC(n)}$ = 3 V
1	WARM	1	set to logic 1: a warm reset procedure is started
		0	set to logic 0: by hardware when a START bit is detected or when MUTE bit is set to logic 1
0	START	1	set to logic 1: starts the activation sequence and cold reset procedure (only if the SUPL and PROT bits are logic 0 and the PRES bit is logic 1)
		0	set to logic 0: starts the deactivation sequence

[1] This bit cannot be written when the START bit is logic 1.

[2] It is a mandatory condition for card slots 2 to 5 that only one card slot I/O line is enabled at a time. When switching from one slot to another, the enabled I/O must be disabled before the I/O line for the required card slot is enabled.

Remark: If both pins I/OUC1 and I/OUC2 are connected at the same time, this mandatory condition also applies to card slot 1.

[3] In synchronous mode, this bit cannot be written when START bit is logic 1.

8.5.3.4 Bank 1 CSb[7:0] Register0 (address 42h) card slots 1 and card slot 2 bit allocation

Table 13. Bank 1 CSb[7:0] Register0 (address 42h) card slots 1 and card slots 2 bit allocation

Bit	7	6	5	4	3	2	1	0
Card slot 1 (address 01h) and Card slot 2 (address 02h)								
Card Slot 1 Reg[1:0] = 00; see Table 14 on page 22								
Symbol	-[1]	RSTIN	C8(1)	C4(1)	CLKPD[1:0][2]		CLKDIV[1:0][3]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Card Slot 2 Reg[1:0] = 00; see Table 14 on page 22								
Symbol	CFGP2	RSTIN	-[1]		CLKPD[1:0][2]		CLKDIV[1:0[3]]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Card Slot 1 and card slot 2 Reg[1:0] = 01; see Table 16 on page 24								
Symbol	D[7:0]							
Access	R/W							
Card Slot 1 and card slot 2 Reg[1:0] = 10; see Table 18 on page 24								
Symbol	C[15:8]							
Access	R/W							
Card Slot 1 and card slot 2 Reg[1:0] = 11; see Table 20 on page 24								
Symbol	C[7:0]							
Access	R/W							

[1] Reserved bit position.

[2] CLKPD[2] = bit 3 and CLKPD[1] = bit 2.

[3] CLKDIV[2] = bit 2 and CLKDIV[1] = bit 1.

8.5.3.5 Bank 1 Register1 (REG[1:0] = 00) card slot 1 (address 01h) and card slot 2 (address 02h) read/write mode bit descriptions

Table 14. Bank 1 Register1 (REG[1:0] = 00) card slot 1 (address 01h) and card slot 2 (address 02h) Read/Write mode bit descriptions

Bit	Symbol	Value	Description
7	CFGP2[1]		enables another type of card detection switch to be used on card socket 1 and card socket 2
		1	if CFGP2 is logic 1, an interrupt is generated during each power-up because the reset value of CFGP2 is logic level 0. Refer to the *Application note AN10724* for further information
		0	the reset value of CFGP2 is logic 0. Refer to the *Application note AN10724* for further information
6	RSTIN	1	synchronous mode: when set to logic 1, pin $RST_{(n)}$ is set to HIGH
			asynchronous mode: RSTIN is controlled by hardware (ATR management)
		0	set to logic 0: pin $RST_{(n)}$ is LOW
5	C8(1)[2]	-	writing C8(1) bit writes the corresponding value on $C8_{(1)}$ pin
		-	reading C8(1) bit reads the state of $C8_{(1)}$ pin
4	C4(1)[2]	-	writing C41 bit writes the corresponding value on $C4_{(1)}$ pin
		-	reading C41 bit reads the state of $C4_{(1)}$ pin

Table 14. Bank 1 Register1 (REG[1:0] = 00) card slot 1 (address 01h) and card slot 2 (address 02h) Read/Write mode bit descriptions *…continued*

Bit	Symbol	Value	Description
3 to 2	CLKPD[1:0]	-	asynchronous mode: when PWDN bit is set to logic 1, the CLKPD[1] and CLKPD[2] bits define the card clock
		-	synchronous mode: when the PWDN bit and the START bit are set to logic 1, the CLKPD[2] bit remains logic 0 and the clock frequency is controlled by the CLKPD[1] bit
		00	asynchronous mode: the card clock is stopped and set to logic 0
		-	synchronous mode: the card clock is set to logic 0
		01	asynchronous mode: the card clock is stopped and set to logic 1
		-	synchronous mode: the card clock is set to logic 1
		10	asynchronous mode: the card clock = $f_{osc(int)}/2$ **Remark:** ($f_{osc(int)}$ is the internal oscillator frequency)
		11	asynchronous mode: the card clock frequency ($f_{(clk)}$) is set using the CLKDIV[1:0] bits.
1 to 0	CLKDIV[1:0]		asynchronous mode: when the PWDN bit is set to logic 0 the CLKDIV[1:0] bits define the card clock frequency.
			synchronous mode: the CLKDIV[1:0] bits are logic 0
		00	[3]card slot 1 card clock frequency = $f_{clk(ext)}$ on pin $CLK_{(1)}$
			card slot 2 card clock frequency = $f_{clk(ext)}$ on pin $CLK_{(2)}$
		01	card slot 1 card clock frequency = $f_{clk(ext)}$ / 2 on pin $CLK_{(1)}$
			card slots 2 card clock frequency = $f_{clk(ext)}$ / 2 on pin $CLK_{(2)}$
		10	card slot 1 card clock frequency = $f_{clk(ext)}$ / 4 on pin $CLK_{(1)}$
			card slot 2 card clock frequency = $f_{clk(ext)}$ / 4 on pin $CLK_{(2)}$
		11	card slot 1 card clock frequency = $f_{clk(ext)}$ / 5 on pin $CLK_{(1)}$
			card slot 2 card clock frequency = $f_{clk(ext)}$ / 5 on pin $CLK_{(2)}$

[1] Only for card slot 2 register.

[2] Only for card slot 1 register.

[3] $f_{clk(ext)}$ is the external clock frequency applied to pins CLKIN1 and CLKIN2.

8.5.3.6 Bank 1 Register1 (REG[1:0] = 01) card slot 1 (address 01h) and card slot 2 (address 02h) bit allocation

Table 15. Bank 1 Register1 (REG[1:0] = 01) card slot 1 (address 01h) and card slot 2 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	D[7:0]							
Access	R/W							

8.5.3.7 Bank 1 Register1 (REG[1:0] = 01) card slot 1 (address 01h) and card slot 2 (address 02h) read/write mode bit descriptions

Table 16. Bank 1 Register1 (REG[1:0] = 01) card slot 1 (address 01h) and card slot 2 (address 02h) Read/Write mode bit descriptions

Bit	Symbol	Description
7 to 0	D[7:0]	programmable 8-bit clock counter. This value is applied to all slots. The reset value is AAh. See Section 8.9 “Answer to reset counters” on page 36

8.5.3.8 Bank 1 Register1 (REG[1:0] = 10) card slot 1 (address 01h) and card slot 2 (address 02h) bit allocation

Table 17. Bank 1 Register1 (REG[1:0] = 10) card slot 1 (address 01h) and card slot 2 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C[15:8]							
Access	R/W							

8.5.3.9 Bank 1 Register1 (REG[1:0] = 10) card slot 1 (address 01h) and card slot 2 (address 02h) read/write mode bit descriptions

Table 18. Bank 1 Register1 (REG[1:0] = 10) card slot 1 (address 01h) and card slot 2 (address 02h) Read/Write mode bit descriptions

Bit	Symbol	Description
7 to 0	C[15:8]	most significant byte of a programmable 16-bit clock counter. This value is applied to all slots. The reset value is A4h. See Section 8.9 “Answer to reset counters” on page 36

8.5.3.10 Bank 1 Register1 (REG[1:0] = 11) card slot 1 (address 01h) and card slot 2 (address 02h) bit allocation

Table 19. Bank 1 Register1 (REG[1:0] = 11) card slot 1 (address 01h) and card slot 2 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C[7:0]							
Access	R/W							

8.5.3.11 Bank 1 Register1 (REG[1:0] = 11) card slot 1 (address 01h) and card slot 2 (address 02h) read/write mode bit descriptions

Table 20. Bank 1 Register1 (REG[1:0] = 11) card slot 1 (address 01h) and card slot 2 (address 02h) read/write mode bit descriptions

Bit	Symbol	Description
7 to 0	C[7:0]	least significant byte of a programmable 16-bit clock counter. This value is applied to all slots. The reset value is 74h. See Section 8.9 “Answer to reset counters” on page 36.

8.5.4 Card slots 3 to 5 register descriptions

8.5.4.1 Bank 1 CSb[7:0] Register0 (address 40h) card slots 3 to 5 bit allocation

Table 21. Bank 1 CSb[7:0] Register0 (address 40h) card slots 3 to 5 bit allocation

Bit	7	6	5	4	3	2	1	0
Card slot 3 (address 03h), Card slot 4 (address 04h) and Card slot 5 (address 05h)								
Symbol	ACTIVE	EARLY	MUTE	PROT	SUPL	CLKSW	-[1]	STAP
Access	R[2]	R	R	R	R	R	R	R
Symbol	VCC1V8	I/OEN	REG[1:0]		PDWN	5V/3VN	WARM	START
Access	W[2]	W	W	W	W	W	W	W

[1] Reserved bit position.

[2] See table Table 22 for more detailed information on read mode bits and Table 23 for more detailed information on write mode bits.

8.5.4.2 Bank 1 Register0 card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read mode bit descriptions

Table 22. Bank 1 Register0 card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read mode bit descriptions

Bit	Symbol	Value	Description
7	ACTIVE	1	set to logic 1: the card is active
		0	set to logic 0: the card is inactive
6	EARLY	1	set to logic 1: during ATR, when the card answers too early
		0	set to logic 0: after reading the byte
5	MUTE	1	set to logic 1: during ATR, when the card does not answer according to the ISO 7816 time period
		0	set to logic 0: after reading the byte
4	PROT	1	set to logic 1: during a card session when an overload or overheating occurs
		0	set to logic 0: after reading the byte
3	SUPL	1	set to logic 1: the supervisor signaled a fault
		0	set to logic 0: after reading the byte
2	CLKSW	1	set to logic 1: when the card slot is in Power-down mode and the clock has switched to $f_{osc(int)}/2$ **Remark:** ($f_{osc(int)}$ is the internal oscillator frequency)
		0	set to logic 0: when exiting Power-down mode and when the clock is switched back to $f_{clk(ext)}$
1	-	-	reserved
0	STAP	-	gives the value of the corresponding STAPn pin when read

When at least one of the SUPL, PROT, MUTE and EARLY bits are set to logic 1, the IRQN pin is driven LOW until the status byte has been read. After power-on, the SUPL bit is set to logic 1 until the status byte has been read and the IRQN pin is LOW until the voltage supervisor is deactivated.

8.5.4.3 Bank 1 Register0 card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) write mode bit descriptions

Table 23. Bank 1 Register0 card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) write mode bit descriptions

Bit	Symbol	Value	Description
7	VCC1V8[1]		used together with the 5V/3VN bit
		1	set to logic 1: $V_{CC(n)}$ = 1.8 V; ignores the 5V/3VN bit logic state
		0	if set to logic 0 $V_{CC(n)}$ is set using the 5V/3VN bit
6	I/OEN[2]	1	set to logic 1: pins I/OUCn are switched to pins $I/O_{(n)}$
		0	set to logic 0: pins I/OUCn and $I/O_{(n)}$ are high-impedance with internal pull-up resistor
5 to 4	REG[1:0]	-	see Table 24 “Bank 1 CSb[7:0] Register1 (address 42h) card slots 3 and 5 bit allocation” on page 27 for detailed information
3	PWDN[3]	1	set to logic 1: to apply the CLKPD[1:0] bit clock settings to pin $CLK_{(n)}$ for the selected card slot
		0	set to logic 0: to apply the CLKDIV[1:0] bits clock options to pin $CLK_{(n)}$ for the selected card slot
2	5V/3VN[1]		used together with VCC1V8 bit
		1	set to logic 1: and the VCC1V8 bit is logic 0: $V_{CC(n)}$ = 5 V
		0	set to logic 0: and the VCC1V8 bit is logic 0: $V_{CC(n)}$ = 3 V
1	WARM	1	set to logic 1: a warm reset procedure is started
		0	set to logic 0: by the hardware: a START bit is detected or the MUTE bit is set to logic 1
0	START	1	set to logic 1: when the SUPL and PROT bits are logic 0 and the PRES bit is logic 1, the activation sequence and cold reset procedure are started
		0	set to logic 0: deactivation sequence starts

[1] This bit cannot be written when START bit is logic 1.

[2] It is a mandatory condition for card slots 2 to 5 that only one card slot I/O line is enabled at a time. When switching from one slot to another, the enabled I/O must be disabled before the I/O line for the required card slot is enabled.

Remark: If both pins I/OUC1 and I/OUC2 are connected at the same time, this mandatory condition also applies to card slot 1.

[3] In synchronous mode, this bit cannot be written when START bit is logic 1.

8.5.4.4 Bank 1 CSb[7:0] Register1 (address 42h) card slots 3 and 5 bit allocation

Table 24. Bank 1 CSb[7:0] Register1 (address 42h) card slots 3 and 5 bit allocation

Bit	7	6	5	4	3	2	1	0
Card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h)								
Reg[1:0] = 00								
Symbol	-[1]	RSTIN	-[1]		CLKPD[1:0][2]		CLKDIV[1:0][3]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reg[1:0] = 01								
Symbol	D[7:0]							
Access	R/W							
Reg[1:0] = 10								
Symbol	C[15:8]							
Access	R/W							
Reg[1:0] = 11								
Symbol	C[7:0]							
Access	R/W							

[1] Reserved bit position.

[2] CLKPD[2] = bit 3 and CLKPD[1] = bit 2.

[3] CLKDIV[2] = bit 2 and CLKDIV[1] = bit 1.

8.5.4.5 Bank 1 Register1 (REG[1:0] = 00) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode

Table 25. Bank 1 Register1 (REG[1:0] = 00) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode

Bit	Symbol	Value	Description
7	-	-	reserved
6	RSTIN	1	synchronous mode: when set to logic 1, pin $RST_{(n)}$ is set to HIGH asynchronous mode: RSTIN is controlled by the hardware (ATR management)
		0	set to logic 0: $RST_{(n)}$ is set LOW
5 to 4	-	-	reserved

Table 25. Bank 1 Register1 (REG[1:0] = 00) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode *…continued*

Bit	Symbol	Value	Description
3 to 2	CLKPD[1:0]	-	asynchronous mode: when PWDN bit is set to logic 1, the CLKPD[1] and CLKPD[2] bits define the card clock
		-	synchronous mode: when the PWDN bit and the START bit are set to logic 1, the CLKPD[2] bit remains logic 0 and the clock frequency is controlled by the CLKPD[1] bit
		00	asynchronous mode: the card clock is stopped and set to logic 0
		-	synchronous mode: the card clock is set to logic 0
		01	asynchronous mode: the card clock is stopped and set to logic 1
		-	synchronous mode: the card clock is set to logic 1
		10	asynchronous mode: the card clock = $f_{osc(int)}/2$ **Remark:** ($f_{osc(int)}$ is the internal oscillator frequency)
		11	asynchronous mode: the card clock frequency ($f_{(clk)}$) is set using the CLKDIV[1:0] bits.
1 to 0	CLKDIV[1:0]		synchronous mode: the CLKDIV[1] and CLKDIV[2] bits are set to logic 0 by the hardware asynchronous mode: PWDN bit is logic 0, the CLKDIV[1] and CLKDIV[2] bits define the card clock as follows:
		00	$f_{clk(ext)}$ on pin CLKIN2 for card slots 2 to 5
		01	$f_{clk(ext)}$ / 2 on pin CLKIN2 for card slots 2 to 5
		10	$f_{clk(ext)}$ / 4 on pin CLKIN2 for card slots 2 to 5
		11	$f_{clk(ext)}$ / 5 on pin CLKIN2 for card slots 2 to 5

8.5.4.6 Bank 1 Register1 (REG[1:0] = 01) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) bit allocation

Table 26. Bank 1 Register1 (REG[1:0] = 01) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	D[7:0]							
Access	R/W							

8.5.4.7 Bank 1 Register1 (REG[1:0] = 01) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode bit descriptions

Table 27. Bank 1 Register1 (REG[1:0] = 01) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode bit descriptions

Bit	Symbol	Description
7 to 0	D[7:0]	programmable 8-bit clock counter. This value applies to all slots. The reset value is AAh. See Section 8.9 “Answer to reset counters” on page 36

8.5.4.8 Bank 1 Register1 (REG[1:0] = 10) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) bit allocation

Table 28. Bank 1 Register1 (REG[1:0] = 10) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C[15:8]							
Access	R/W							

8.5.4.9 Bank 1 Register1 (REG[1:0] = 10) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode bit descriptions

Table 29. Bank 1 Register1 (REG[1:0] = 10) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode bit descriptions

Bit	Symbol	Description
7 to 0	C[15:8]	most significant byte of a programmable 16-bit clock counter. This value applies to all slots. The reset value is A4h. See ATR Section 8.9 “Answer to reset counters” on page 36

8.5.4.10 Bank 1 Register1 (REG[1:0] = 11) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) bit allocation

Table 30. Bank 1 Register1 (REG[1:0] = 11) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C[7:0]							
Access	R/W							

8.5.4.11 Bank 1: Bank 1 Register1 (REG[1:0] = 11) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode bit descriptions

Table 31. Bank 1: Bank 1 Register1 (REG[1:0] = 11) card slot 3 (address 03h), card slot 4 (address 04h) and card slot 5 (address 05h) read/write mode bit descriptions

Bit	Symbol	Description
7 to 0	C[7:0]	least significant byte of a programmable 16-bit clock counter. This value applies to all slots. The reset value is 74h. See Section 8.9 on page 36

8.5.5 Selection of asynchronous or synchronous mode

When the activation sequence starts, the selected card slot on the TDA8026 uses the RSTIN bit value to configure itself for use with asynchronous or synchronous cards. If the RSTIN bit is set to logic 1 at the activation sequence start (the START bit changes from LOW to HIGH), the TDA8026 will manage asynchronous cards.

In asynchronous mode, the card slot $RST_{(n)}$ pin is controlled by the corresponding ATR counter (see Section 8.9 on page 36).

In synchronous mode, the card slot $RST_{(n)}$ pin is controlled by the corresponding RSTIN bit. The card clock configuration is set by the PWDN bit value at the activation sequence start of the selected card slot (the START bit changed from LOW to HIGH).

- If the PDWN bit is set to logic 0 at the start of the activation, the card clock value is the CLKIN1 pin frequency for card slot 1 and the CLKIN2 pin frequency for card slots 2 to 5. If CLKDIV[1:0] = 00, the first four clock cycles are not transferred to $CLK_{(n)}$. When CLKDIV[1:0] = 01, 10 or 11, the first five clock cycles are not transferred to $CLK_{(n)}$.
- If the PDWN bit is set to logic 1 at the start of the activation, the clock uses the CLKPD1 bit.

The card clock frequency and the stop state are configured using the CLKDIV[1:0] and CLKPD[1:0] bits. Refer to Table 32 for the configuration in asynchronous mode and Table 33 for synchronous mode.

Table 32. Asynchronous mode card clock settings

PWDN bit	CLKDIV[1:0] bit	CLKPD[1:0] bit	Card clock (CLK)
0	00	-	$f_{clk(ext)}$
0	01	-	$f_{clk(ext)}$ / 2
0	10	-	$f_{clk(ext)}$ / 4
0	11	-	$f_{clk(ext)}$ / 5
1	-	00	logic 0
1	-	01	logic 1
1	-	10	$f_{osc(int)}/2$
1	-	11	$f_{clk(ext)}$ / x (no change)

Table 33. Synchronous mode card clock settings

PWDN bit	CLKDIV[1:0] bit	CLKPD[1:0] bit	Card clock (CLK)
logic 1 at activation sequence start	-	x0	logic 0
logic 1 at activation sequence start	-	x1	logic 1
logic 0 at activation sequence start[1]	-	xx	$f_{clk(ext)}$

[1] If CLKDIV[1:0] = 00, the first four clock cycles are not transferred to $CLK_{(n)}$. When CLKDIV[1:0] is not 00, the first five clock cycles are not transferred to $CLK_{(n)}$.

$f_{clk(ext)}$ is the clock input frequency on either pin CLKIN1 or pin CLKIN2 depending on the card slot number.

During transitions, no pulse is shorter than 45 % of the smallest period and both the first/last clock pulse around the change have the correct width; making the frequency change synchronous.

When changing the card clock frequency from one $f_{clk(ext)}$ frequency division to another, the modification is only active after the next rising clock edge.

Any change after switching the card clock frequency from an external $f_{clk(ext)}$ frequency division to the internal oscillator frequency ($f_{osc(int)}$) is not immediate. The change is indicated by the state of the CLKSW bit (see the register descriptions in Table 11 and Table 22). In addition, it is assumed that the $f_{clk(ext)}$ / x frequency division is less than or equal to 6.25 MHz.

8.5.6 General registers

8.5.6.1 Bank 1 General registers (address: 40h, 42h; CSb[7:0] = 00h, 06h) bit allocation

Table 34. Bank 1 General registers (addresses: 40h, 42h; CSb[7:0] = 00h, 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Address 40h; CSb[7:0] = 00h, see Table 35								
Symbol	PV[7:0]							
Access	R							
Address 40h; CSb[7:0] = 06h								
Symbol	CLK_SR[3:2]		IO_SR[3:2]		CLK_SR[1:0]		IO_SR[1:0]	
Access	R/W		R/W		R/W		R/W	
Address 42h; CSb[7:0] = 00h								
Symbol	-[1]		INTAUX	INT[4:0][2]				
Access	R		R	R				

[1] Reserved bit position.

[2] The INT numbers do not match the bit positions and are as follows:
bit 4 = INT5, bit 3 = INT4, bit 2 = INT3, bit 1 = INT2 and bit 0 = INT1

8.5.6.2 Bank 1 Product version register (address 40h; CSb[7:0] = 00h) read mode bit descriptions

Table 35. Bank 1 Product version register (address 40h; CSb[7:0] = 00h) read mode bit descriptions

Bit	Symbol	Description
7 to 0	PV[7:0]	reading this register returns the product version. The MSB nibble is C (commercial product) and the LSB nibble is 2 (release number)

8.5.6.3 Bank 1 Interrupt register (address 42h; CSb[7:0] = 00h) read mode bit descriptions

Table 36. Bank 1 Interrupt register (address 42h; CSb[7:0] = 00h) read mode bit descriptions

Bit	Symbol	Value	Description
7 to 6	-	-	reserved
5	INTAUX	-	auxiliary interrupt line
4 to 0	INT[4:0][1]		These interrupt bits remain at logic 1 until the interrupt SUPL, PROT, MUTE and EARLY bits have been read
			INT5: card slot 5 interrupt:
		1	set to logic 1: when any of the bits SUPL, PROT, MUTE and EARLY are set to logic 1
		0	set to logic 0: when any of the bits SUPL, PROT, MUTE and EARLY are set to logic 0 when read
			INT4: card slot 4 interrupt:
		1	set to logic 1: when any of the bits SUPL, PROT, MUTE and EARLY are set to logic 1
		0	set to logic 0: when any of the bits SUPL, PROT, MUTE and EARLY are set to logic 0 when read
			INT3: card slot 3 interrupt:
		1	set to logic 1: when any of the bits SUPL, PROT, MUTE and EARLY are set to logic 1
		0	set to logic 0: when any of the bits SUPL, PROT, MUTE and EARLY are set to logic 0 when read
			INT2: card slot 2 interrupt:
		1	set to logic 1: when any of the bits PRESL, SUPL, PROT, MUTE and EARLY are set to logic 1
		0	set to logic 0: when any of the bits PRESL, SUPL, PROT, MUTE and EARLY are set to logic 0 when read
			INT1: card slot 1 interrupt:
		1	set to logic 1: when any of the bits PRESL, SUPL, PROT, MUTE and EARLY are set to logic 1
		0	set to logic 0: when any of the bits PRESL, SUPL, PROT, MUTE and EARLY are set to logic 0 when read

[1] The INTx numbers do not match the bit positions and are as follows:
bit 4 = INT5, bit 3 = INT4, bit 2 = INT3, bit 1 = INT2 and bit 0 = INT1

8.5.6.4 Bank 1 Slew rate register (address 40h; CSb[7:0] = 06h) read/write mode bit descriptions

Table 37. Bank 1 Slew rate register (address 40h; CSb[7:0] = 06h) read/write mode bit descriptions

Bit	Symbol	Description
7 to 6	CLK_SR[3:2]	card slot 2 to 5 clock slew rate selection
5 to 4	IO_SR[3:2]	card slot 2 to 5 I/O slew rate selection
3 to 2	CLK_SR[1:0]	card slot 1 clock slew rate selection
1 to 0	IO_SR[1:0]	card slot 1 I/O slew rate selection

Refer Section 8.10 on page 38 for more detailed information.

8.6 DC-to-DC converter

The DC-to-DC converter has been designed to provide an average of 5.4 V to the programmable voltage regulators (5 V, 3 V and 1.8 V) for the card slots. It is capable of delivering a total DC current of 116 mA to the card slots.

If the total current from all card slots exceeds 170 mA, the overcurrent/overload protection deactivates the DC-to-DC converter. The addition of a 10 μH external coil and Schottky diode ensures the DC-to-DC converter operates at an input voltage range between 2.7 V and 5.5 V.

When the DC-to-DC converter cannot act as a step-up converter, an overload alarm is sent to the digital module and all card slot interfaces are deactivated. This causes the IRQN line to be driven LOW and the Bank 1 Register 0 PROT bit is set to logic 1.

The DC-to-DC converter is deactivated when the TDA8026 is in shutdown mode.

The card slots can be directly supplied by the V_{DD} supply voltage, if it is always above 5.25 V, thus removing the need to use the DC-to-DC converter. In this situation, the supply voltage can be directly applied to the V_{UP} and LX pins as shown in Figure 9.

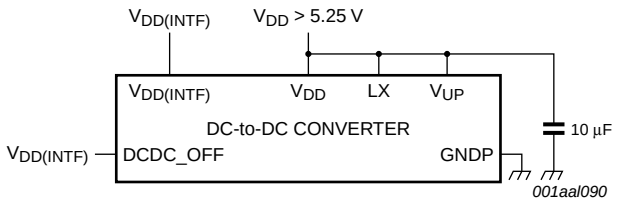


Fig 9. The DC-to-DC converter

When DCDC_OFF is set to $V_{DD(INTF)}$, the DC-to-DC converter is shutdown:

- the output power transistors are switched OFF
- the DC-to-DC converter current consumption is 0 A.

8.7 V_{CC} buffer

The current on the V_{CC} buffer is internally limited to approximately 100 mA. When this limit is reached, the automatic deactivation sequence is performed. Each card slot has its own limitation and deactivation of one card slot does not affect the other card slots.

The $V_{CC(n)}$ voltage should be decoupled with two low ESR 100 nF (minimum) capacitors. One capacitor should be placed close to the V_{CC} pin of the device and the other close to the C1 pin of the card connector. See Figure 14 for detailed information.

8.8 Sequencer and clock counter

Each card slot has a dedicated sequencer and clock counter.

The sequencer ensures that the activation and deactivation sequences meet the ISO 7816 and EMV 4.3 standards, even during an emergency deactivation caused by card removal during transaction, supply drop out or a hardware problem. The sequencer is clocked with an internal oscillator ($f_{osc(int)}$).

Card slot 1 or card slot 2 can only be activated if a card is detected as present in the slot and if an alarm is not triggered by the voltage supervisor. When both of these parameters are met, the card slots can be activated by setting the Command register START bit. The activation sequence is described in Section 8.8.2.

Card slots 3 to 5 do not have presence monitoring. The corresponding STAP pin is used for card presence detection on these slots.

The deactivation is initiated by the system controller or automatically in the case of a hardware problem or a supply drop out. The deactivation sequence is described in Section 8.8.3.

Outside a session, the card contacts are forced to low-impedance with respect to the GNDC pin.

8.8.1 Standby mode

Standby mode is the default state after a power-on reset. This mode ensures the power consumption remains low until a card is inserted or the microcontroller starts a card session. When there is not an ongoing card session, the internal oscillator runs at its low frequency (t_{15}).

A debouncing time of 17.8 ms is applied to card slot 1 and card slot 2 to allow for card insertion (presence) detection.

8.8.2 Activation sequence

When the card is inactive, pins $V_{CC(n)}$, $CLK_{(n)}$, $RST_{(n)}$ and $I/O_{(n)}$ are LOW which is low-impedance with respect to pin $GNDC_{(n)}$ or pin GNDS depending of the card slot.

The sequencer is clocked by an internal oscillator. When everything is satisfactory (voltage supply, card presence, no hardware problem), the system controller can trigger the card present activation sequence by setting card slot's START bit to logic 1:

- The internal oscillator switches to its high frequency (t_0, see Figure 10).
- The DC-to-DC converter starts (t_1).
- $V_{CC(n)}$ starts to rise from 0 V to 1.8 V, 3 V or 5 V during the controlled rise time (t_2).
- The voltage on the $I/O_{(n)}$ pin rises to $V_{CC(n)}$, due to integrated 10 kΩ pull-ups for $V_{CC(n)}$ (t_3).
- $CLK_{(n)}$ clock signal is sent to the card ($t_4 = t_{act}$) and the $RST_{(n)}$ pin is enabled. The $RST_{(n)}$ pin is managed by the ATR counter or the Register1 RSTIN bit depending on the card slot mode (asynchronous or synchronous).

The sequencer is clocked by $\frac{f_{osc(int)}}{64}$ which leads to a time interval T = 25 µs (typical).

Thus, $t_1 = 0$, $t_2 = t_1 + \frac{3T}{2}$, $t_3 = t_1 + \frac{7T}{2}$ and $t_4 = t_1 + 4T$.

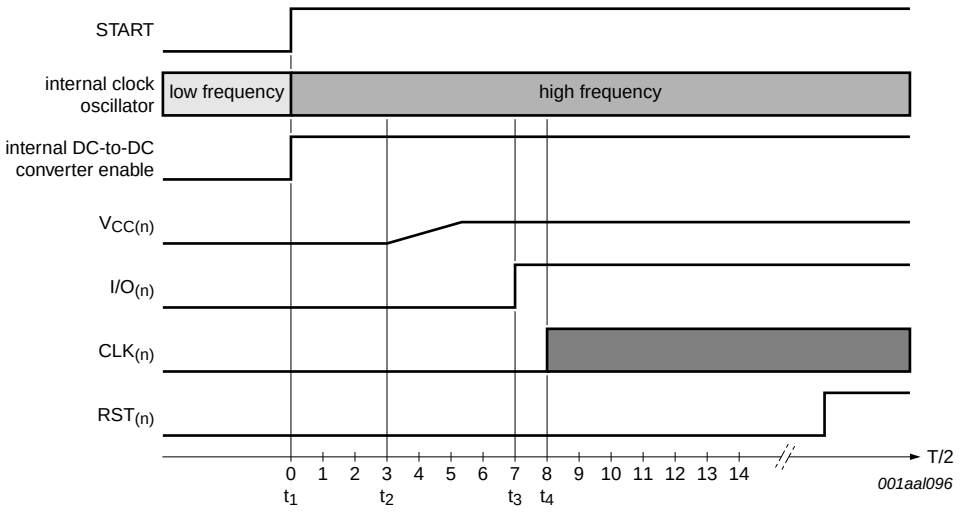


Fig 10. The card slot activation sequence

In Figure 10 only one card slot is activated. If another card slot is active, the DC-to-DC converter remains active.

8.8.3 Deactivation sequence

When the session finishes, the microcontroller resets the START bit to logic 0 (Figure 11) and the following deactivation sequence is performed:

- Card reset: $RST_{(n)}$ pin falls to 0 V (t_{11}).
- Pin $CLK_{(n)}$ is stopped (t_{12}).
- Pin $I/O_{(n)}$ falls to 0 V (t_{13}).
- Pin $V_{CC(n)}$ falls to 0 V with a controlled slew rate (t_{14}).
- The DC-to-DC converter is stopped.
- Pins $CLK_{(n)}$, $RST_{(n)}$, $V_{CC(n)}$ and $I/O_{(n)}$ are driven to 0 V with a low-impedance switch attached to pin GNDS (t_{15}).
- The internal oscillator switches to its low frequency (t_{15})

Thus, $t_{11} = 0$, $t_{12} = t_{11} + \frac{T}{2}$, $t_{13} = t_{11} + T$, $t_{14} = t_{11} + \frac{3T}{2}$ and $t_{15} = t_{11} + \frac{7T}{2}$.

The deactivation time t_{deact} is the time that $V_{CC(n)}$ needs to be driven below 0.4 V, counting from the moment START bit is reset.

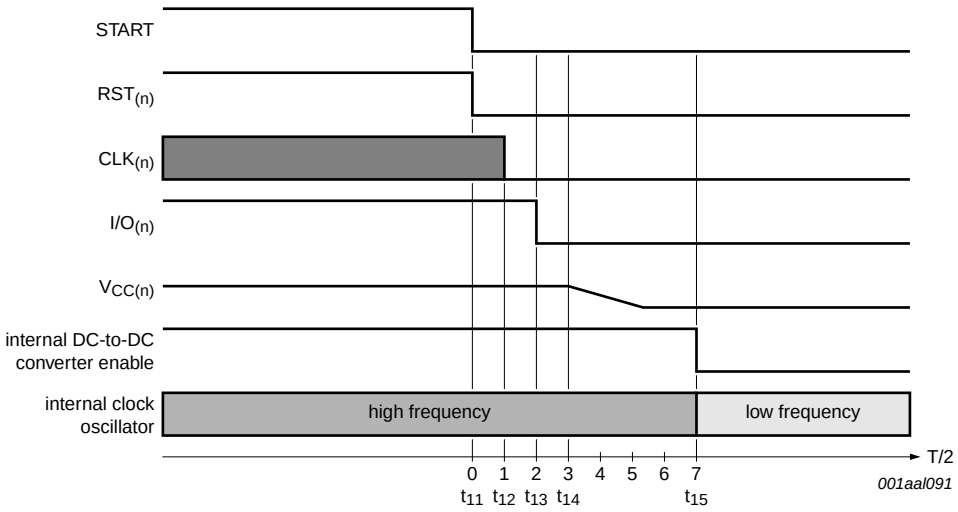


Fig 11. Deactivation sequence

In Figure 11 only one card slot is active. If another card slot is active, the DC-to-DC converter is still active.

8.9 Answer to reset counters

Each TDA8026 card slot has its own sequencer. The sequencer controls the activation and deactivation sequences. In addition to these sequencers, there are two Answer To Reset (ATR) counters:

- ATR dedicated to card slot 1
- ATR dedicated to the other slots

The operating mode (asynchronous or synchronous) has to be selected by the microcontroller. The ATR counters are used in asynchronous mode to manage the $RST_{(n)}$ pin and to check the card's ATR. In synchronous mode, the RST pin is controlled by the microcontroller using the RSTIN bit (see the bit description in Table 11 on page 20 and Table 22 on page 25) and the card's ATR is not checked.

The ATR counter module comprises two counters:

- EARLY answer counter: The early answer counter consists of a fixed part which counts up to 200 clock cycles. The secondary part counts up to the D[7:0] bits value of clock cycles (see the register descriptions in Table 16 on page 24 and Table 27 on page 28). The default D[7:0] bits value is 170 which gives a total default count of 370 clock cycles
- MUTE counter: The mute counter counts up to C[15:8] and C[7:0] bits value for the clock cycles (see the register descriptions in Table 22 on page 25 and Table 30 on page 29). The default value of the C[15:0] bits is 42100 which gives a default count of 42100 clock cycles.

  Both counters can be easily quickly reprogrammed, if for example, a card does not fully meet the EMVCo/ISO7816 standards or to enable the implementation of new and enhanced standards.

When operating, the microcontroller starts to configure the selected card slot (card supply voltage) and then triggers the activation sequence using the START bit. The sequencer then performs the activation sequence. The DC-to-DC converter is started, pin $V_{CC(n)}$ is set to the previously configured card supply voltage, pin $I/O_{(n)}$ is enabled and $CLK_{(n)}$ starts (see Section 8.8.2 on page 34 and Section 8.8.3 on page 35). Pin $RST_{(n)}$ is set to LOW.

The ATR counter dedicated to the card slot makes the following checks and takes the steps required:

- START bits from a card detected on pin $I/O_{(n)}$ during the first 200 clock cycles are ignored and the count continues.
- START bits from a card detected while pin $RST_{(n)}$ is set to LOW, with the number of clock cycles between 200 and the C[15:0] bits value (default 42100), cause the EARLY and MUTE bits to be set to logic 1. Pin $RST_{(n)}$ remains LOW and the microcontroller decides if it will accept the card.
- START bits detected after the number of clock cycles is equal to the C[15:0] bits value cause pin $RST_{(n)}$ to be set to HIGH.
- START bits received from the card when the first number of clock cycles is equal to the D[7:0] bits value (default 370) and pin $RST_{(n)}$ set to HIGH cause the EARLY bit to be set to logic 1.
- Cards not answering before 42100 clock cycles (or the C[15:0] bits value) with $RST_{(n)}$ set to HIGH cause the MUTE bit to be set to logic 1.
- Cards answering within the correct time frame, stops the clock cycles count and the microcontroller can send commands to the card.

Figure 12 shows the timings checked by the ATR counters.

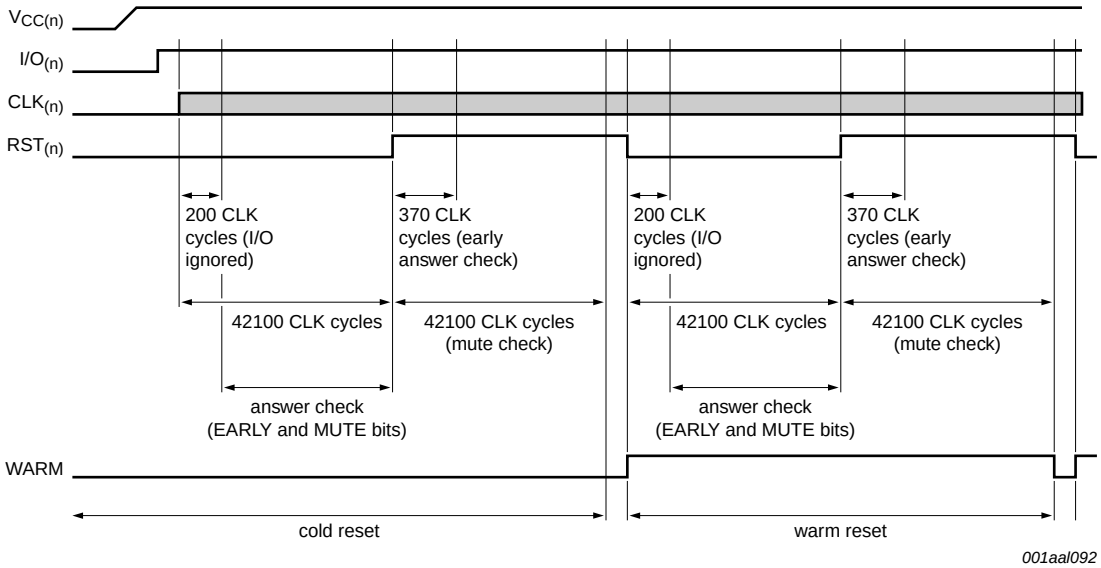


Fig 12. ATR counter timing check

When the EARLY and MUTE bits are set to logic 1, they signal an interrupt (see the bit descriptions in Table 12 on page 21, Table 22 on page 25 and Table 36 on page 32).

The sequence described in Section 8.9 relates to a cold reset. If the card is mute (has not answered), the microcontroller can start a warm reset by setting WARM bit to logic 1 (see the bit descriptions in Table 11 on page 20 and Table 22 on page 25). Then, the ATR counter set pin $RST_{(n)}$ to LOW and performs the same timing checks (see Figure 12).

Remark: It is assumed that two card activations will not take place simultaneously on card slots 2 to 5 because only one $I/O_{(n)}$ line is available for these four slots. There is no protection on the second ATR counter against starting an activation while a count is ongoing. The first ATR counter is dedicated to the slot 1. Consequently, it is mandatory to enable only one slot $I/O_{(n)}$ line at the same time for card slots 2 to 5. When switching from one slot to another one, it is mandatory to first disable the slot $I/O_{(n)}$ line in use before enabling the slot $I/O_{(n)}$ line required. During this transition, no $I/O_{(n)}$ lines are enabled for card slots 2 to 5. This allows the ATR counter to be reset between card slot switching actions. If both pins I/OUC1 and I/OUC2 are connected at the same time, this mandatory condition also applies to card slot 1.

8.10 Slew rate control

Slew rate control is embedded for the clock buffer and the $I/O_{(n)}$ line of each card slot. The rising and falling edge of the card clock signal can be configured using 2 bits in Register6 of bank 1. The settings based on a 30 pF load capacitance and a $V_{CC(n)}$ = 5 V are shown in Table 38.

Table 38. Clock Slew rate

CLK_SR[1] (high)	CLK_SR[2] (low)	Rise and fall time (ns)
L	L	10
L	H	7
H	L	6
H	H	5

[1] The high slots are define by [1] (slot 1) and [3] (all other slots).

[2] The low slots are define by [0] (slot 1) and [2] (all other slots).

The rise and fall time is calculated from 10 % to 90 % and 90 % to 10 % (respectively) of the signal amplitude. The default setting for CLK_SR[1]/CLK_SR[3] (high) is LOW and CLK_SR[0]/CLK_SR[2] (low) is HIGH.

Only the falling edge of the card $I/O_{(n)}$ signal can be configured with the two programmable bits in Register6 of bank 1. The settings based on a 30 pF load capacitance and a $V_{CC(n)}$ = 5 V are shown in Table 39 on page 38:

Table 39. I/O slew rate

IO_SR[1] (high)	IO_SR[2] (low)	Fall time (ns)
L	L	67
L	H	54
H	L	35
H	H	17

[1] The high slots are define by [1] (slot 1) and [3] (all other slots).

[2] The low slots are define by [0] (slot 1) and [2] (all other slots).

The fall time is calculated from 90 % to 10 % of the signal amplitude. The default setting for IO_SR[0]/IO_SR[2] (low) and IO_SR[1]/IO_SR[3] (high) is LOW (see table Table 39 on page 38).

8.11 Fault detection

The following fault conditions are monitored by the TDA8026.

- **Overheating:** All the card slots are automatically deactivated and the device is forced in to Standby mode when the detected temperature range is between 125 °C to 209 °C. The card slot PROT bit is set to logic 1. Above 209 °C the device is shutdown.
- **Card removal during transaction:** A deactivation sequence is performed in accordance with the EMV 4.2 standard.
- **DC-to-DC converter overload:** All card slots are automatically deactivated and the device is placed in Standby mode when the current supplied by the DC-to-DC converter exceeds 170 mA (I_{CC} parameter for $V_{CC(n)}$). The card slot PROT bit is set to logic 1
- **Card slot current limitation and deactivation:** A current level drawn by a card which exceeds 120 mA (I_{sd} parameter for $V_{CC(n)}$) triggers the deactivation sequence on the faulty card slot. During the deactivation, the current is limited to approximately 110 mA. The card slot PROT bit is set to logic 1
- **V_{DD} or $V_{DD(INTF)}$ dropping:** A voltage drop occurring on V_{DD} or $V_{DD(iNTF)}$ generates card slot deactivation followed by a device reset. The completion of this phase is validated when the SUPL bits are set to logic 1.

9. Limiting values

Table 40. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	on pin V_{DD}		–0.5	+6	V
$V_{DD(INTF)}$	interface supply voltage	on pin $V_{DD(INTF)}$		–0.5	+4.6	V
V_{IH}	HIGH-level input voltage	on all card pins		–0.5	+6	V
		on all other pins		–0.5	+4.6	V
V_o	output voltage	on pin LX	[1]	–0.5	+7.2	V
		DC-to-DC converter output on pin V_{UP}	[1]	–0.5	+7.2	V
P_{tot}	total power dissipation	T_{amb} = –25 °C to +85 °C		-	665	mW
T_{stg}	storage temperature			–55	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[2]			
		on $I/O_{(n)}$, $V_{CC(n)}$, $CLK_{(n)}$, $GNDC_{(n)}$, PRES, $RST_{(n)}$, $C4_{(1)}$, $C8_{(1)}$ card pins	[3]	–7	+7	kV
		on all other pins		–2	+2	kV
		MM				
		on all pins		–200	+200	V
		CDM				
		on all pins		–500	+500	V

[1] The limiting values depend on the external inductor and V_{UP} decoupling capacitor used.

[2] Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM; 1500 Ω; 100 pF) defines three pulses positive and three pulses negative on each pin referenced to ground.

[3] The 7 kV ESD test is performed in the typical application configuration as depicted in the *Application note AN10724* with two external capacitors connected to each $V_{CC(n)}$ line.

10. Thermal characteristics

Table 41. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	47.1	K/W

[1] With a 4-layer board

11. Characteristics

Table 42. Supply

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$[1] = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage	on pin V_{DD}; DC-to-DC converter on	[2]	2.7	-	5.5	V
		on pin V_{DD}; DC-to-DC converter off; $V_{CC(n)}$ pins = 5 V	[2]	5.25	-	5.5	V
V_{hys}	hysteresis voltage	on pin V_{DD}	[3]	50	100	150	mV
$V_{DD(INTF)}$	interface supply voltage	on pin $V_{DD(INTF)}$		1.6	-	3.6	V
V_{th}	threshold voltage	decreasing voltage on pin V_{DD}	[3]	2.35	2.45	2.55	V
		on pin $V_{DD(INTF)}$	[4]	1.19	1.26	1.32	V
I_{DD}	supply current	shutdown mode		-	25	40	µA
		Standby mode		-	300	450	µA
		clock-stop mode; All card slots in this mode; $f_{clk(ext)}$ = stopped on pins CLKIN1 and CLKIN2		-	3.7	-	mA
		active mode; All $V_{CC(n)}$ pins = 5 V; $f_{clk(ext)}$ = 5 MHz; $I_{CC(1)}$ = $I_{CC(2)}$ = 55 mA; $I_{CC(3)}$ = $I_{CC(4)}$ = $I_{CC(5)}$ = 2 mA	[5] [6]	-	210	260	mA
$I_{DD(INTF)}$	interface supply current	shutdown mode		-	10	15	µA
		active mode; All $V_{CC(n)}$ pins = 5 V; $f_{clk(ext)}$ = 5 MHz;		-	35	-	µA
		increasing voltage on pin V_{DD}	[3]	2.35	2.55	2.65	V
t_{wake}	wake-up time			5.8	-	11	ms

[1] $f_{clk(ext)}$ is the external clock frequency applied to pins CLKIN1 and CLKIN2.

[2] Refer to Section 8.6 for further information about DC-to-DC converter operation.

[3] See Figure 6 “The voltage supervisor circuit” on page 12.

[4] See Section 8.3.2 “Description” for a description of the voltage supervisor.

[5] Typical value measurement based on a 85 % DC-to-DC converter and inductance efficiency; depends on PCB layout and external component quality (inductor, capacitor).

[6] Maximum measurement value based on a 125 mA I_{CC} current load and a 75 % DC-to-DC converter and inductance efficiency; depends on PCB layout and external component quality (inductor, capacitor).

Table 43. Supply supervisor

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PORADJ Pin							
I_L	leakage current			–1	-	+1	µA
I_{IL}	LOW-level input current			–1	-	+1	µA
I_{IH}	HIGH-level input current			–1	-	+1	µA

Table 44. DC-to-DC converter

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 μH; decoupling capacitors on pins V and V_{UP} = 10 μF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{osc(int)}$	internal oscillator frequency			2.1	2.8	3.5	MHz
V_o	output voltage	from DC-to-DC converter; DC-to-DC converter on; not bypassed		5.25	5.5	-	V
V_i	input voltage	pin LX input voltage; DC-to-DC converter on; not bypassed		-	-	7.2	V
$t_{on(DCDC)}$	DC-to-DC converter turn-on time	V_{DD} < 4.2 V		-	1.4	-	μs
		V_{DD} > 4.2 V		-	0.35	-	μμs

Table 45. Card drivers

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 μH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 μF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Card supply voltage: $V_{CC(1)}$ to $V_{CC(5)}$ [1]							
V_{CC}	supply voltage	Standby mode					
		no load		–0.1	-	+0.1	V
		I_o = 1 mA		–0.1	-	+0.3	V
		active mode; 2.7 V < V_{DD} < 5.5 V	[2]				
		5 V card; DC $I_{CC(n)}$ ≤ 55 mA		4.75	5	5.25	V
		3 V card; DC $I_{CC(n)}$ ≤ 55 mA		2.85	3	3.15	V
		1.8 V card; DC $I_{CC(n)}$ ≤ 35 mA		1.71	1.8	1.89	V
		active mode; AC current pulses with I < 200 mA, t < 400 ns and f < 20 MHz	[2]				
		5 V card; 40 nAs current spikes		4.65	-	5.35	V
		3 V card; 17.5 nAs current spikes		2.76	-	3.24	V
		1.8 V card; 11.1 nAs current spikes		1.62	-	1.98	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	on pins $V_{CC(n)}$; 20 kHz < card clock frequency < 200 MHz		-	-	350	mV

Table 45. Card drivers *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	Standby mode and pin $V_{CC(n)}$ grounded		-	-	−1	mA
		active mode; 2.7 V < V_{DD} < 5.5 V					
		5 V card		-	-	55	mA
		3 V card		-	-	55	mA
		1.8 V card		-	-	35	mA
		sum of all card supply currents on pins $V_{CC(n)}$; active mode; All V_{CC} pins = 5 V; $f_{clk(ext)}$ on pins $CLK_{(n)}$ = 5 MHz; $I_{CC(1)}$ = $I_{CC(2)}$ = 55 mA; $I_{CC(3)}$ = $I_{CC(4)}$ = $I_{CC(5)}$ = 2 mA	[5]	-	116	125	mA
SR	slew rate	rising; maximum C_L = 200 nF; 5 V, 3 V and 1.8 V cards		0.06	0.16	0.27	V/µs
C_{dec}	decoupling capacitance	connected to $V_{CC(n)}$; 100 nF and 100 nF at 20 %		160	200	240	nF
Card reset output pins: $RST_{(1)}$ to $RST_{(5)}$							
V_o	output voltage	Standby mode					
		no load		0	-	0.1	V
		I_o = 1 mA		0	-	0.3	V
I_o	output current	Standby mode and pin $RST_{(n)}$ grounded		0	-	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} ≤ 200 µA - C2 version		0	-	0.3	V
		I_{OL} ≤ 200 µA - C3 version		0	-	0.15 VCC(n)	V
		I_{OL} ≤ 20 mA		$V_{CC(n)}$ − 0.4	-	$V_{CC(n)}$	V
V_{OH}	HIGH-level output voltage	−200 µA ≤ I_{OH} ≤ 0		$V_{CC(n)}$ − 0.5	-	$V_{CC(n)}$	V
		−20 mA ≤ I_{OH} ≤ 0		0	-	0.4	V
t_r	rise time	C_L = 100 pF; 10 % to 90 %		-	-	0.1	µs
t_f	fall time	C_L = 100 pF; 90 % to 10 %		-	-	0.1	µs
Clock to card output pins: $CLK_{(1)}$ to $CLK_{(5)}$; default register values							
V_o	output voltage	Standby mode					
		no load		0	-	0.1	V
		I_o = 1 mA		0	-	0.3	V
I_o	output current	Standby mode and $CLK_{(n)}$ pin grounded		0	-	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} ≤ 200 µA - C2 version		0	-	0.3	V
		I_{OL} ≤ 200 µA - C3 version		0	-	0.15 VCC(n)	V
		I_{OL} ≤ 70 mA		$V_{CC(n)}$ − 0.4	-	$V_{CC(n)}$	V
V_{OH}	HIGH-level output voltage	−200 µA ≤ I_{OH} ≤ 0		$V_{CC(n)}$ − 0.5	-	$V_{CC(n)}$	V
		−70 mA ≤ I_{OH} ≤ 0		0	-	0.4	V
t_r	rise time	C_L = 30 pF; 10 % to 90 %		-	-	7	ns

Table 45. Card drivers *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_f	fall time	C_L = 30 pF; 90 % to 10 %		-	-	7	ns
f_{CLK}	frequency on pin CLK	all $CLK_{(n)}$ pins; operating		0	-	20	MHz
δ_{clk}	clock duty cycle	C_L = 30 pF		45	-	55	%
SR	slew rate	rise and fall; C_L = 30 pF; 90 % to 10 %		0.2	-		V/ns
Data line pins: $I/O_{(1)}$ to $I/O_{(5)}$, $C4_{(1)}$ and $C8_{(1)}$							
V_o	output voltage	Standby mode					
		no load		0	-	0.1	V
		I_o = 1 mA		-	-	0.3	V
I_o	output current	Standby mode and $I/O_{(n)}$, $C4_{(1)}$ or $C8_{(1)}$ pins grounded.		0	-	−1	mA
V_{OL}	LOW-level output voltage	$I_{OL} \leq$ 1 mA - C2 version		0	-	0.3	V
		$I_{OL} \leq$ 1 mA - C3 version		0	-	0.15 VCC(n)	V
		$I_{OL} \leq$ 15 mA		$V_{CC(n)}$ − 0.4	-	$V_{CC(n)}$	V
V_{OH}	HIGH-level output voltage	no DC load		$0.9V_{CC(n)}$	-	$V_{CC(n)}$ + 0.1	V
		−20 µA $\leq I_{OH} \leq$ 0		$0.8V_{CC(n)}$	-	$V_{CC(n)}$ + 0.1	V
		−40 µA $\leq I_{OH} \leq$ 0		$0.7V_{CC(n)}$	-	$V_{CC(n)}$ + 0.1	V
		−15 mA $\leq I_{OH} \leq$ 0		0	-	0.4	V
V_{IL}	LOW-level input voltage	All $V_{CC(n)}$ - C2 version		−0.3	-	+0.8	V
		All $V_{CC(n)}$ - C3 version		−0.3	-	0.2 VCC	V
V_{IH}	HIGH-level input voltage	$V_{CC(n)}$ = 5 V and 3 V		$0.6V_{CC(n)}$	-	$V_{CC(n)}$	V
		$V_{CC(n)}$ = 1.8 V - C2 version		$0.7V_{CC(n)}$	-	$V_{CC(n)}$	V
		$V_{CC(n)}$ = 1.8 V - C3 version		1.55	-	$V_{CC(n)}$	V
V_{hys}	hysteresis voltage	on $I/O_{(n)}$		-	50	-	mV
I_{IL}	LOW-level input current	0 V applied to pin	[3]	-	-	650	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{CC(n)}$	[3]	-	-	10	µA
I_{pu}	pull-up current	$V_{OH} = 0.9V_{CC(n)}$; C_L = 30 pF	[3]	1	-	-	mA
t_d	delay time	falling edge on pins I/O and $I/O\mu_{(n)}$ or vice versa	[3][4]		-	400	ns
$t_{r(i)}$	input rise time	V_{IL} minimum to V_{IH} maximum; 10 % to 90 %		-	-	1.2	µs
$t_{f(i)}$	input fall time	V_{IL} maximum to V_{IH} minimum; 90 % to 10 %		-	-	1.2	µs
$t_{r(o)}$	output rise time	V_{IL} minimum to V_{IH} maximum; 10 % to 90 %		-	-	0.1	µs
$t_{f(o)}$	output fall time	V_{IL} maximum to V_{IH} minimum; 90 % to 10 %		-	-	0.1	µs
C_i	input capacitance		[3]	-	-	10	pF
R_{pu}	pull-up resistance	between pins $I/O_{(n)}$ or $C4_{(1)}$ or $C8_{(1)}$ and $V_{CC(n)}$	[3]	8	10	12	kΩ
f_{max}	maximum frequency	input clock	[3]	-	-	500	kHz

Table 45. Card drivers *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 μH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 μF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Card presence input: pin PRES; active HIGH when SPRES pin = LOW or active LOW when SPRES pin = HIGH							
V_{IL}	LOW-level input voltage			–0.3	-	+0.2 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.8 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{LIL}	LOW-level input leakage current	V_i = 0.2$V_{DD(INTF)}$		-	-	70	μA
I_{LIH}	HIGH-level input leakage current	V_i = 0.8$V_{DD(INTF)}$		-	-	5	μA
t_{deb}	debounce time			-	17.8	23.8	ms

[1] Two ceramic multilayer capacitors of minimum 100 nF with low Equivalent Series Resistance (ESR) should be used in order to meet these specifications.

[2] Output voltage towards the card, including ripple.

[3] $I/O_{(n)}$ pin has an internal 10 kΩ pull-up resistor to $V_{CC(n)}$.

[4] I/OUCn pin has an internal 11 kΩ pull-up resistor to $V_{DD(INTF)}$.

[5] Maximum value measurement based on a 125 mA (sum of all card supply currents on pins $V_{CC(n)}$) current load and a 75 % DC-to-DC converter and inductance efficiency; depends on PCB layout and external component quality (inductor, capacitor).

Table 46. Sequencer and clock counter

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 μH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 μF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{act}	activation time	total sequence	[1]	-	-	135	μs
t_{deact}	deactivation time	total sequence	[1]	60	80	100	μs
T_{clk}	clock period	sequencer		-	25	-	μs

[1] Refer to Section 8.8.3 for further information.

Table 47. Interface signals to microcontroller

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 μH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 μF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Data line pins: I/OUC1 and I/OUC2[1]							
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA		0	-	0.3	V
V_{OH}	HIGH-level output voltage	no DC load		0.9 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.2	V
		–10 μA ≤ I_{OH} ≤ 0		0.75 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.2	V
V_{IL}	LOW-level input voltage			–0.3	-	+0.25 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{IL}	LOW-level input current	V_{IL} = 0 V		-	-	600	μA
V_{hys}	hysteresis voltage	on $I/OUC_{(n)}$		-	0.19$V_{DD(INTF)}$	-	V
I_{LIH}	HIGH-level input leakage current	V_{IH} = $V_{DD(INTF)}$		-	-	10	μA

Table 47. Interface signals to microcontroller *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{r(o)}$	output rise time	V_{IL} minimum to V_{IH} maximum; 10 % to 90 %		-	-	0.1	µs
$t_{r(i)}$	input rise time	V_{IL} minimum to V_{IH} maximum; 10 % to 90 %		-	-	1.2	µs
$t_{f(o)}$	output fall time	V_{IL} maximum to V_{IH} minimum; 90 % to 10 %		-	-	0.1	µs
$t_{f(i)}$	input fall time	V_{IL} maximum to V_{IH} minimum; 90 % to 10 %		-	-	1.2	µs
C_i	input capacitance		[1]	-	-	10	pF
$R_{pu(int)}$	internal pull-up resistance	between pins I/OUC$_{(n)}$ and $V_{DD(INTF)}$	[1]	9	11	13	kΩ
I_{pu}	pull-up current	V_{OH} = 0.9 V_{DD}, C_i = 30 pF		–1	-	-	mA
Clock input pins: CLKIN1 and CLKIN2							
$f_{clk(ext)}$	external clock frequency	on pins CLKIN1 and CLKIN2		0	-	20	MHz
V_{IL}	LOW-level input voltage	$V_{DD(INTF)}$ > 2 V		0	-	0.3 $V_{DD(INTF)}$	V
		1.6 V ≤ $V_{DD(INTF)}$ ≤ 2 V		0	-	0.15$V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage	$V_{DD(INTF)}$ > 2 V		0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
		1.6 V ≤ $V_{DD(INTF)}$ ≤ 2 V		0.85 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
t_r	rise time	10 % to 90 %		-	-	0.1 / $f_{clk(ext)}$	ns
t_f	fall time	90 % to 10 %		-	-	0.1 / $f_{clk(ext)}$	ns
Logic input pins: A0, SPRES, INHIB, DCDC_OFF and TESTMODE							
V_{IL}	LOW-level input voltage			–0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{LIL}	LOW-level input leakage current			–1	-	+1	µA
V_{hys}	hysteresis voltage	on pin SPRES		-	0.14$V_{DD(INTF)}$	-	V
I_{LIH}	HIGH-level input leakage current			–1	-	+1	µA
C_i	input capacitance			-	-	10	pF
Logic input pin: SDWNN							
V_{IL}	LOW-level input voltage			–0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{LIH}	HIGH-level input leakage current			–1	-	+1	µA
C_i	input capacitance			-	-	10	pF
$R_{pu(int)}$	internal pull-up resistance	between pins SDWNN and $V_{DD(INTF)}$		2	2.5	3	MΩ

Table 47. Interface signals to microcontroller *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Logic input pin: INTAUXN							
V_{IL}	LOW-level input voltage			–0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{LIL}	LOW-level input leakage current			–425	–330	–260	µA
C_i	input capacitance			-	-	10	pF
$R_{pu(int)}$	internal pull-up resistance	between pins INTAUXN and $V_{DD(INTF)}$; SDWNN pin equal to pin $V_{DD(INTF)}$		8	10	12	kΩ
Interrupt line: IRQN pin; open-drain, active LOW output							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	-	0.3	V
I_{LH}	HIGH-level leakage current			-	-	10	µA
Logic input/output pins: TST1, TST2, STAP3, STAP4, STAP5							
V_{IL}	LOW-level input voltage			–0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
V_{OL}	LOW-level output voltage	$V_{DD(INTF)}$ = 3.3 V; I_{OL} = 4 mA		0	-	0.4	V
		$V_{DD(INTF)}$ = 1.8 V; I_{OL} = 4 mA		0	-	0.4	V
V_{OH}	HIGH-level output voltage	$V_{DD(INTF)}$ = 3.3 V; I_{OH} = –4 mA		$V_{DD(INTF)}$ – 0.4	-	$V_{DD(INTF)}$	V
		$V_{DD(INTF)}$ = 1.8 V; I_{OH} = –4 mA		$V_{DD(INTF)}$ – 0.4	-	$V_{DD(INTF)}$	V
I_{OL}	LOW-level output current	$V_{DD(INTF)}$ = 3.3 V; V_{OL} = 0.3 $V_{DD(INTF)}$		4	-	-	mA
		$V_{DD(INTF)}$ = 1.8 V; V_{OL} = 0.3 $V_{DD(INTF)}$		2	-	-	mA
I_{OH}	HIGH-level output current	$V_{DD(INTF)}$ = 3.3 V; V_{OH} = 0.7 $V_{DD(INTF)}$		–4	-	-	mA
		$V_{DD(INTF)}$ = 1.8 V; V_{OH} = 0.7 $V_{DD(INTF)}$		–2	-	-	mA
I_{LIL}	LOW-level input leakage current			–1	-	+1	µA
I_{LIH}	HIGH-level input leakage current			–1	-	+1	µA
C_i	input capacitance			-	-	10	pF
C_o	output capacitance			-	30	-	pF

Table 47. Interface signals to microcontroller *...continued*

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 µH; decoupling capacitors on pins V_{DD} and V_{UP} = 10 µF; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Serial data input/output pin: SDA; open-drain							
V_{IL}	LOW-level input voltage			−0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA		-	-	0.3	V
I_{LH}	HIGH-level leakage current	I/O		-	-	1	µA
I_{LL}	LOW-level leakage current	depending on the pull-up resistance; input or output		-	-	1	µA
Serial clock input pin: SCL							
V_{IL}	LOW-level input voltage			−0.3	-	+0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{LIH}	HIGH-level input leakage current			-	-	1	µA
I_{IL}	LOW-level input current	depends on the pull-up resistance		-	-	1	µA
I^2C-bus timing; see Figure 13							
f_{SCL}	SCL clock frequency			0	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	hold time after which first clock pulse is generated		0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{HD;DAT}$	data hold time		[2]	0	-	-	ns
$t_{SU;DAT}$	data set-up time			100	-	-	ns
t_r	rise time	both SDA and SCL signals; 10 % to 90 %		-	-	300	ns
t_f	fall time	both SDA and SCL signals; 90 % to 10 %		-	-	300	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs

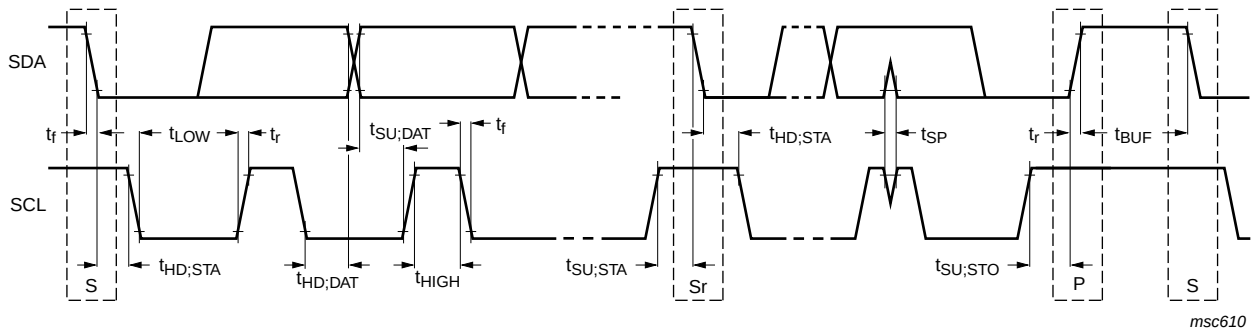
[1] I/OUCn pin has an internal 11 kΩ pull-up resistor to $V_{DD(INTF)}$.

[2] The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

Table 48. Protections

V_{DD} = $V_{DD(INTF)}$ = 3.3 V; $f_{clk(ext)}$ = 10 MHz; GND = 0 V; inductor = 10 μH; decoupling capacitors on pin V_{DD} and V_{UP} = 10 μF; T_{amb} = 25 °C unless otherwise specified.

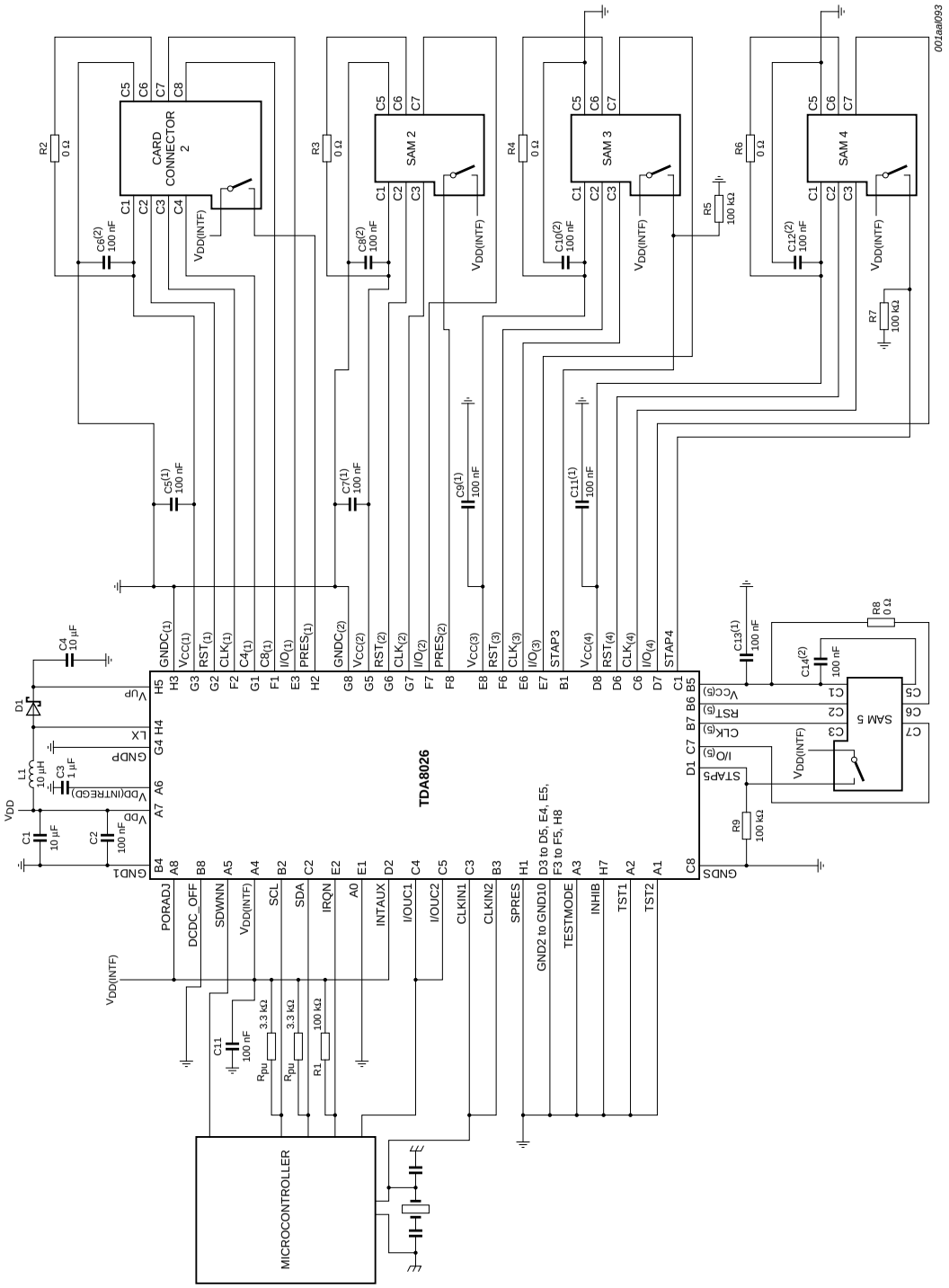
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{sd}	shutdown temperature			125	167	209	°C
I_{sd}	shutdown current	all $V_{CC(n)}$ pins		80	120	150	mA
I_{Olim}	output current limit	pins $I/O_{(n)}$		−15	-	+15	mA
		pins $CLK_{(n)}$		−70	-	+70	mA
		pins $RST_{(n)}$		−20	-	+20	mA
		pins $V_{CC(n)}$		80	-	150	mA
T_{amb}	ambient temperature			−25	+25	+85	°C
T_j	junction temperature			-	-	+125	°C
I_{CC}	supply current	sum of all $V_{CC(n)}$ signals on all card slots; active mode; DC-to-DC converter on		-	170	-	mA



P = STOP condition; S = START condition.

Fig 13. Timing requirements for the I²C-bus

12. Application information



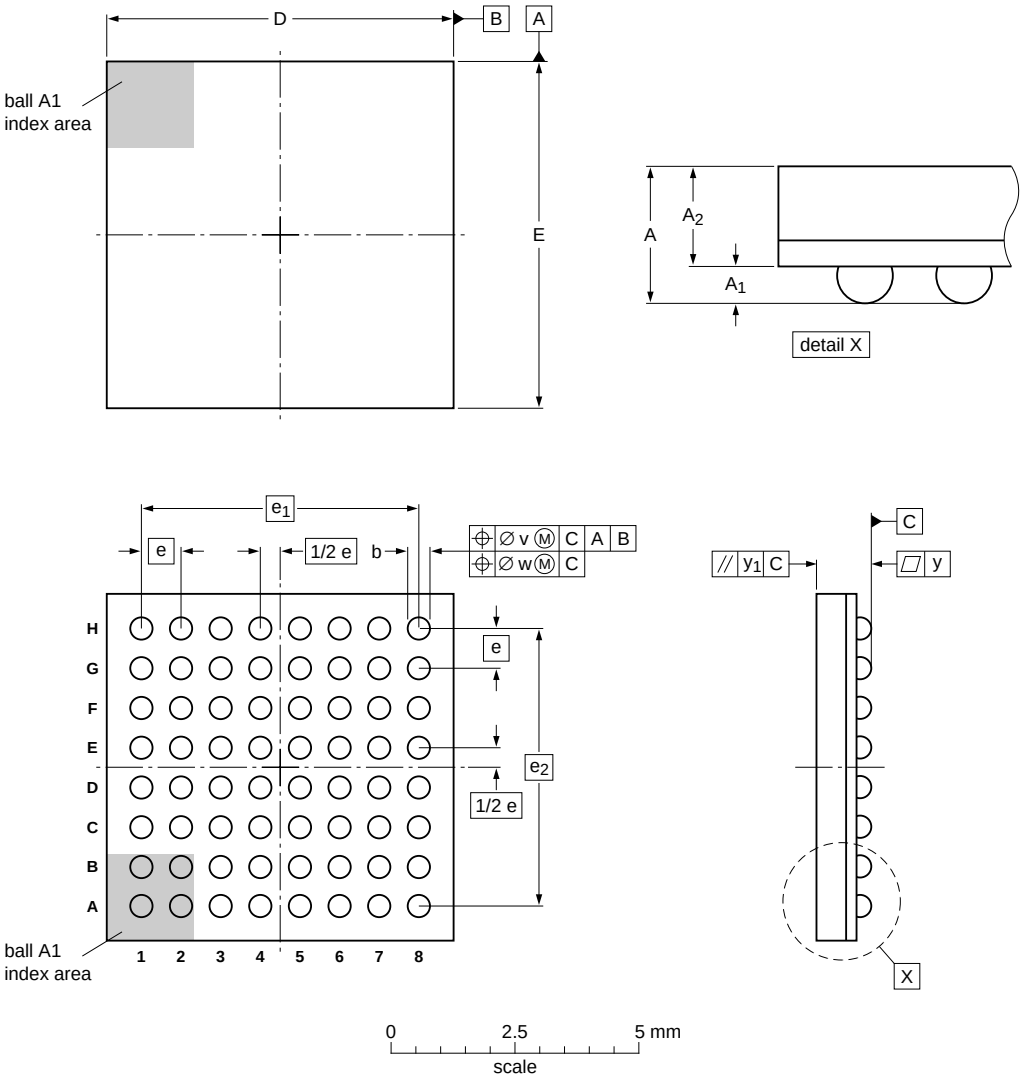
(1) Low ESR capacitor, placed near the IC.

(2) Low ESR capacitor, placed near the C1 connector contact.

Fig 14. Application diagram: TDA8026 with one card and four SAMs

13. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls **SOT1073-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.2	0.35	0.85	0.45	7.1	7.1	0.8	5.6	5.6	0.15	0.08	0.12	0.1
	nom	1.1	0.30	0.80	0.40	7.0	7.0							
	min	1.0	0.25	0.75	0.35	6.9	6.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1073-1	- - -	- - -	- - -			~~08-03-06~~ 08-03-14

Fig 15. Package outline SOT1073-1 (TFBGA64)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 49 and 50

Table 49. SnPb eutectic process (from J-STD-020C)

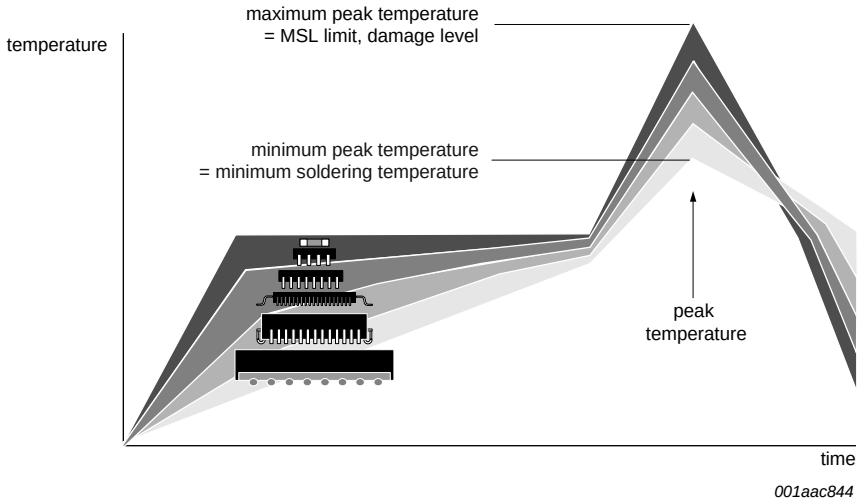
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 50. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 51. Abbreviations and acronyms

Acronym	Description
ATR	Answer To Request
CDM	Charged Device Model
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
POS	Point Of Sales
SAM	Security Access Module

16. Revision history

Table 52. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8026 v. 1.1	20160630	Product data sheet	[1]	TDA8026 v.1
Modifications	• C3 version EMVC0 4.3 compliant added • Table 45 “Card drivers”: updated			
TDA8026 v.1	20100309	Product data sheet	-	

[1] Versions 1.0 to 1.2 have all been superseded by this version which includes changes to symbols, pin names and drawings.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 30 June 2016
Document identifier: TDA8026_1

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