

MC74LVX245

Octal Bus Transceiver

With 5 V-Tolerant Inputs

The MC74LVX245 is an advanced high speed CMOS octal bus transceiver.

It is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by the level of the T/R input. The output enable pin (\overline{OE}) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

Features

- High Speed: $t_{PD} = 4.7$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V;
Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

Application Notes

- Do not force a signal on an I/O pin when it is an active output, damage may occur
- All floating (high impedance) input or I/O pins must be fixed by means of pullup or pulldown resistors or bus terminator ICs
- A parasitic diode is formed between the bus and V_{CC} terminals. Therefore, the LVX245 cannot be used to interface 5.0 V to 3.0 V systems directly

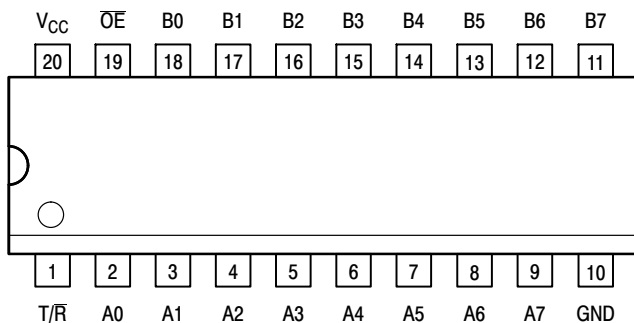


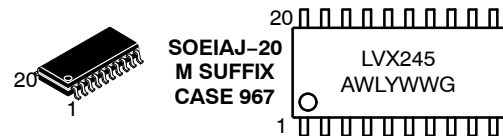
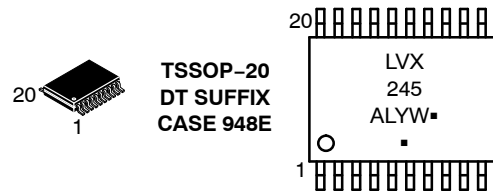
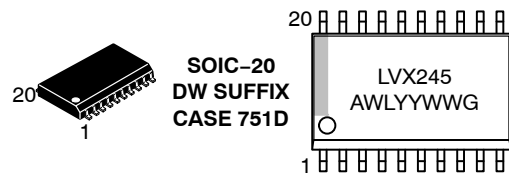
Figure 1. 20-Lead Pinout (Top View)



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MARKING DIAGRAMS



LVX245 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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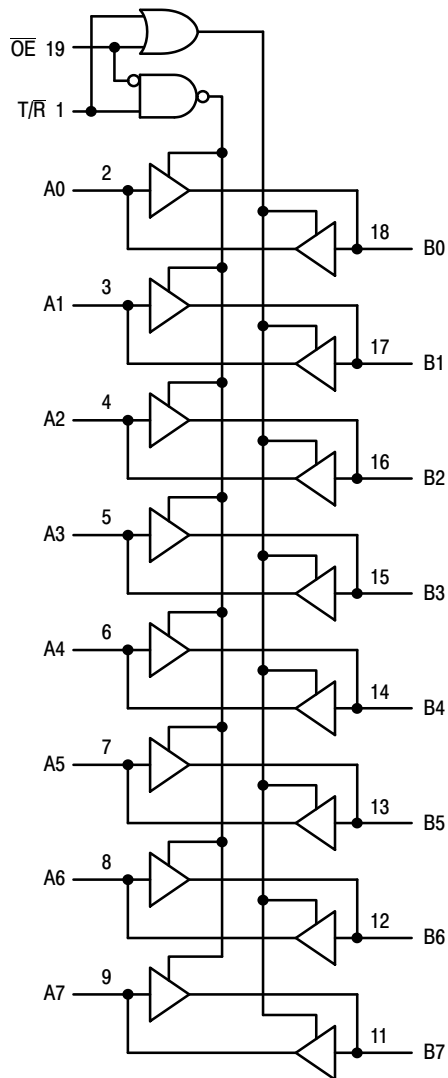


Figure 2. Logic Diagram

Table 1. PIN NAMES

| Pins | Function |
|-----------------|--|
| \overline{OE} | Output Enable Input |
| T/R | Transmit/Receive Input |
| A0-A7 | Side A 3-State Inputs or 3-State Outputs |
| B0-B7 | Side B 3-State Inputs or 3-State Outputs |

| INPUTS | | OPERATING MODE Non-Inverting |
|--------|-----|---------------------------------|
| OE | T/R | |
| L | L | B Data to A Bus |
| L | H | A Data to B Bus |
| H | X | Z |

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|------------------------|-----------------------|
| MC74LVX245DWR2G | SOIC-20 (Pb-Free) | 1000 / Tape & Reel |
| MC74LVX245DTR2G | TSSOP-20* | 2500 / Tape & Reel |
| MC74LVX245MG | SOEIAJ-20 (Pb-Free) | 50 Units / Rail |
| MC74LVX245MELG | SOEIAJ-20 (Pb-Free) | 2000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|---|------------------------------|------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _{in} | DC Input Voltage (T/R, OE) | -0.5 to +7.0 | V |
| V _{I/O} | DC Output Voltage | -0.5 to V _{CC} +0.5 | V |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current | ±20 | mA |
| I _{out} | DC Output Current, per Pin | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±75 | mA |
| P _D | Power Dissipation | 180 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 3.6 | V |
| V _{in} | DC Input Voltage (T/R, OE) | 0 | 5.5 | V |
| V _{I/O} | DC Output Voltage | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -40 | +85 | °C |
| Δt/ΔV | Input Rise and Fall Time | 0 | 100 | ns/V |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -40 to 85°C | | Unit | |
|-----------------|--|---|----------------------|-----------------------|------------|--------------------|------------------------------|--------------------|------|----|
| | | | | Min | Typ | Max | Min | Max | | |
| V _{IH} | High-Level Input Voltage | | 2.0 3.0 3.6 | 1.5 2.0 2.4 | | | 1.5 2.0 2.4 | | V | |
| V _{IL} | Low-Level Input Voltage | | 2.0 3.0 3.6 | | | 0.5 0.8 0.8 | | 0.5 0.8 0.8 | | V |
| V _{OH} | High-Level Output Voltage (V _{in} = V _{IH} or V _{IL}) | I _{OH} = -50 μA I _{OH} = -50 μA I _{OH} = -4 mA | 2.0 3.0 3.0 | 1.9 2.9 2.58 | 2.0 3.0 | | 1.9 2.9 2.48 | | | V |
| V _{OL} | Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL}) | I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA | 2.0 3.0 3.0 | | 0.0 0.0 | 0.1 0.1 0.36 | | 0.1 0.1 0.44 | | V |
| I _{in} | Input Leakage Current | V _{in} = 5.5 V or GND (T/R, OE) | 3.6 | | | ±0.1 | | ±1.0 | | μA |
| I _{oZ} | Maximum 3-State Leakage Current | V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 3.6 | | | ±0.2 5 | | ±2.5 | | μA |
| I _{CC} | Quiescent Supply Current | V _{in} = V _{CC} or GND | 3.6 | | | 4.0 | | 40.0 | | μA |

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A = - 40 to 85°C | | Unit |
|--|--|---|-----------------------|------|------|-------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay Input to Output | V _{CC} = 2.7 V C _L = 15 pF | | 6.1 | 10.7 | 1.0 | 13.5 | ns |
| | | C _L = 50 pF | | 8.6 | 14.2 | 1.0 | 17.0 | |
| | | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF | | 4.7 | 6.6 | 1.0 | 8.0 | |
| | | C _L = 50 pF | | 7.2 | 10.1 | 1.0 | 11.5 | |
| t _{PZL} , t _{PZH} | Output Enable Time to High and Low Level | V _{CC} = 2.7 V C _L = 15 pF | | 9.0 | 16.9 | 1.0 | 20.5 | ns |
| | | R _L = 1 kΩ C _L = 50 pF | | 11.5 | 20.4 | 1.0 | 24.0 | |
| | | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF | | 7.1 | 11.0 | 1.0 | 13.0 | |
| | | R _L = 1 kΩ C _L = 50 pF | | 9.6 | 14.5 | 1.0 | 16.5 | |
| t _{PLZ} , t _{PHZ} | Output Disable Time From High and Low Level | V _{CC} = 2.7 V C _L = 50 pF | | 11.5 | 18.0 | 1.0 | 21.0 | ns |
| | | R _L = 1 kΩ | | | | | | |
| | | V _{CC} = 3.3 ± 0.3 V C _L = 50 pF | | 9.6 | 12.8 | 1.0 | 14.5 | |
| | | R _L = 1 kΩ | | | | | | |
| t _{OSSL} , t _{OSLH} | Output-to-Output Skew (Note 1) | V _{CC} = 2.7 V C _L = 50 pF | | | 1.5 | | 1.5 | ns |
| | | V _{CC} = 3.3 ± 0.3 V C _L = 50 pF | | | 1.5 | | 1.5 | |

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | T _A = 25°C | | | T _A = - 40 to 85°C | | Unit |
|------------------|--|-----------------------|-----|-----|-------------------------------|-----|------|
| | | Min | Typ | Max | Min | Max | |
| C _{in} | Input Capacitance (T/ \bar{R} , $\bar{O}\bar{E}$) | | 4 | 10 | | 10 | pF |
| C _{I/O} | Maximum 3-State I/O Capacitance | | 8 | | | | pF |
| C _{PD} | Power Dissipation Capacitance (Note 2) | | 21 | | | | pF |

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per bit). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, C_L = 50pF, V_{CC} = 3.3V, Measured in SOIC Package)

| Symbol | Characteristic | T _A = 25°C | | Unit |
|------------------|--|-----------------------|------|------|
| | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 0.5 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | -0.5 | -0.8 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

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SWITCHING WAVEFORMS

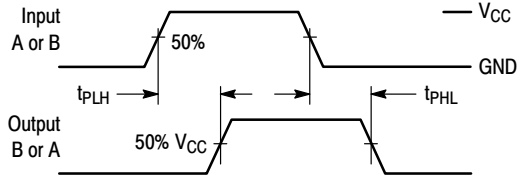


Figure 3.

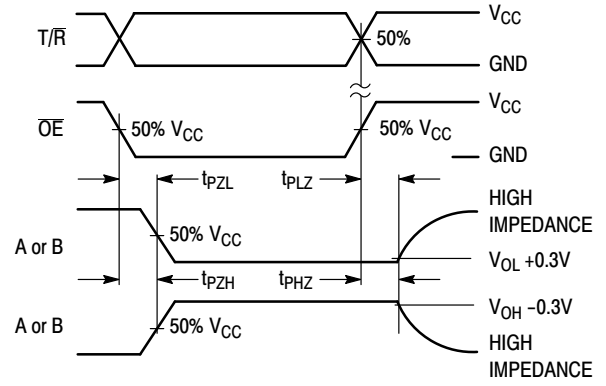
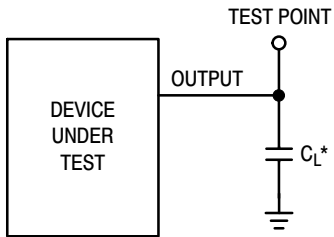


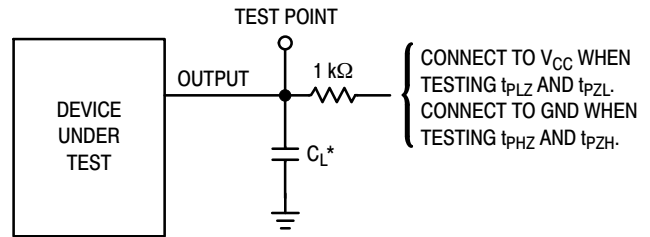
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



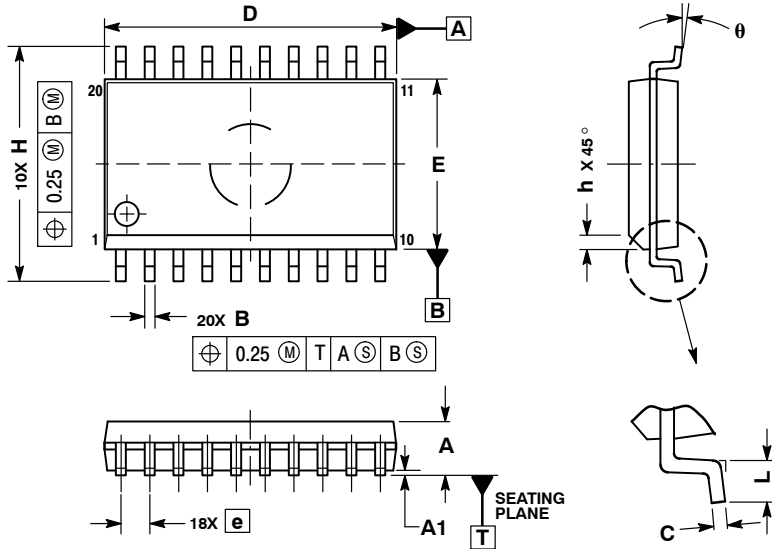
*Includes all probe and jig capacitance

Figure 6. 3-State Test Circuit

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PACKAGE DIMENSIONS

SOIC-20
CASE 751D-05
ISSUE G

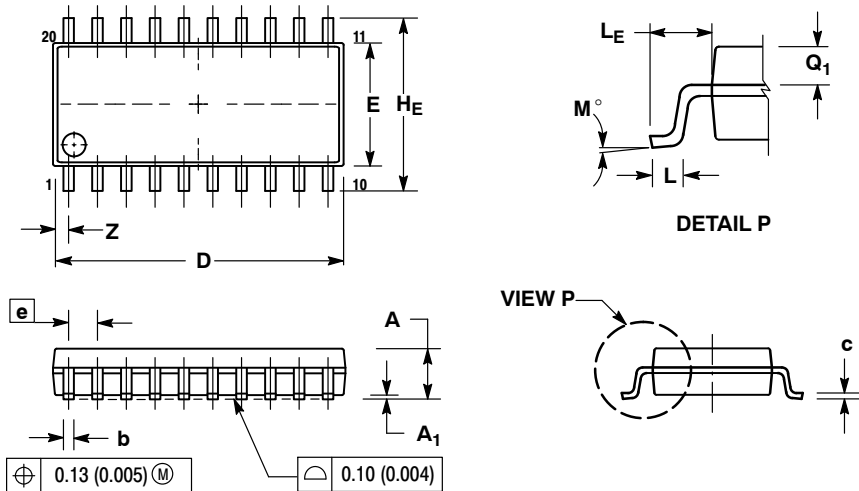


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| theta | 0° | 7° |

SOEIAJ-20
CASE 967-01
ISSUE A



NOTES:

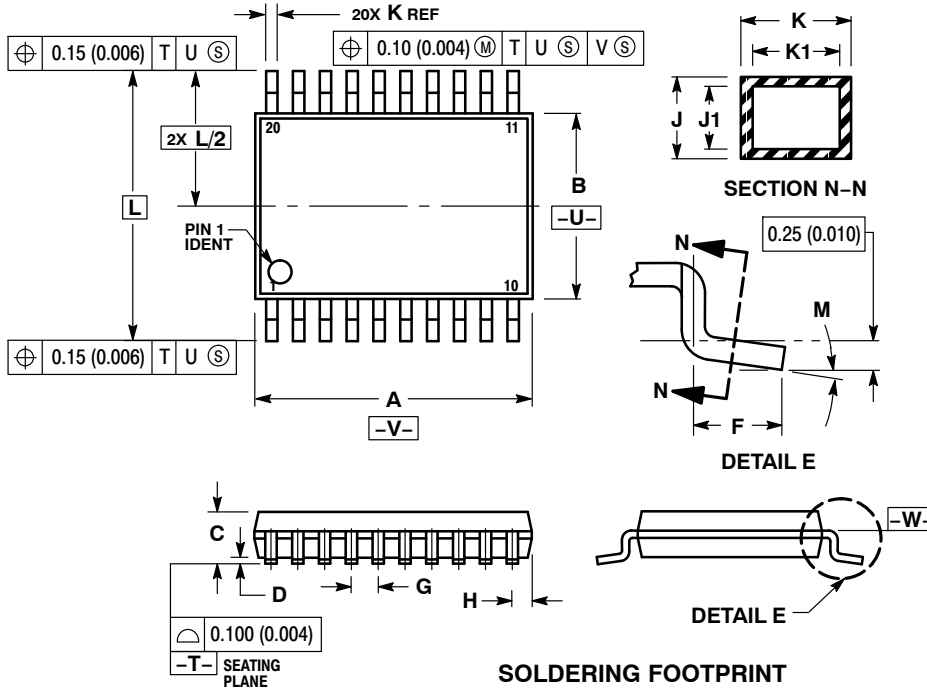
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A1 | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H_E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L_E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q1 | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

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PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

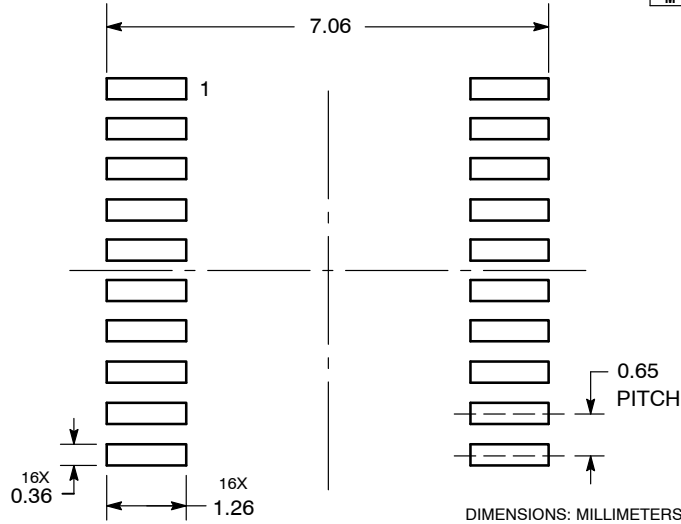


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT



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