



### **General Description**

The MAX7314 I<sup>2</sup>C-compatible serial interfaced peripheral provides microprocessors with 16 I/O ports plus one output-only port and one input-only port. Each I/O port can be individually configured as either an open-drain current-sinking output rated at 50mA and 5.5V, or a logic input with transition detection. The output-only port can be assigned as an interrupt output for transition detection. The outputs are capable of driving LEDs, or providing logic outputs with external resistive pullup up to 5.5V.

Eight-bit PWM current control is built in for all 17 output ports. A 4-bit global control applies to all LED outputs and provides coarse adjustment of current from fully off to fully on with 14 intensity steps in between. Each output has an individual 4-bit control, which further divides the globally set current into 16 more steps. Alternatively, the current control can be configured as a single 8-bit control that sets all outputs at once.

Each output has independent blink timing with two blink phases. All LEDs can be individually set to be on or off during either blink phase, or to ignore the blink control. The blink period is controlled by a clock input (up to 1kHz) on BLINK or by a register. The BLINK input can also be used as a logic control to turn the LEDs on and off, or as a general-purpose input.

The MAX7314 supports hot insertion. All port pins, the  $\overline{\text{INT}}$  output, SDA, SCL,  $\overline{\text{RST}}$ , BLINK, and the slave address input ADO remain high impedance in powerdown (V+ = 0V) with up to 6V asserted upon them.

The MAX7314 is controlled through a 2-wire serial interface, and uses four-level logic to allow four  $I^2C$ addresses from only one select pin.

**Applications** 

LCD Backlights LED Status Indication Relay Drivers Keypad Backlights RGB LED Drivers System I/O Ports

Pin Configurations continued at end of data sheet.

#### \_\_Features

- ♦ 400kbps, 2-Wire Serial Interface, 5.5V Tolerant
- ♦ 2V to 3.6V Operation
- Overall 8-Bit PWM LED Intensity Control Global 16-Step Intensity Control Individual 16-Step Intensity Controls
- ♦ 2-Phase LED Blinking
- ♦ 50mA Maximum Port Output Current
- Supports Hot Insertion
- Outputs are 5.5V-Rated Open Drain
- ♦ Inputs are Overvoltage Protected to 5.5V
- Transition Detection with Interrupt Output
- ♦ 1.2µA (typ), 3.6µA (max) Operating Current
- Small 4mm x 4mm, Thin QFN Package
- ◆ -40°C to +125°C Temperature Range

## **Ordering Information**

PART	TEMP RANGE	PIN- PACKAGE	PKG CODE
MAX7314ATG	-40°C to +125°C	24 Thin QFN 4mm x 4mm x 0.8mm	T2444-4
MAX7314AEG	-40°C to +125°C	24 QSOP	_

## **Typical Application Circuit**



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Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

### **ABSOLUTE MAXIMUM RATINGS**

Voltage (with respect to GND)

V+	0.3V to +4V
SCL, SDA, ADO, BLINK, RST, PO-P15	0.3V to +6V
INT/016	0.3V to +8V
DC Current on P0-P15, INT/O16	55mA
DC Current on SDA	10mA
Maximum GND Current	350mA

Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
24-Pin QSOP (derate 9.5mW/°C over +70°	C)761mW
24-Pin QFN (derate 20.8mW/°C over +70°	C)1666mW
Operating Temperature Range	
(TMIN to TMAX)	40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

(Typical Operating Circuit, V+ = 2V to 3.6V,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at V+ = 3.3V,  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			ТҮР	МАХ	UNITS
Operating Supply Voltage	V+			2		3.6	V
Output Load External Supply Voltage	V <sub>EXT</sub>			0		5.5	V
Chandless Ourread		SCL and SDA at V+; other	$T_A = +25^{\circ}C$		1.2	2.3	
(Interface Idle, PWM Disabled)	I+	digital inputs at V+ or GND;	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			2.8	μΑ
		PWM intensity control disabled	$T_A = T_{MIN}$ to $T_{MAX}$			3.6	
Quere la Querra et		SCL and SDA at V+; other	$T_A = +25^{\circ}C$		8.5	15.1	
Supply Current (Interface Idle, PWM Enabled)	Ι_+	digital inputs at V+ or GND;	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			16.5	μΑ
(Interface fole, 1 Will Enabled)		PWM intensity control disabled	$T_A = T_{MIN}$ to $T_{MAX}$			17.2	
Supply Current		$f_{SCL} = 400 \text{kHz}$ ; other digital	$T_A = +25^{\circ}C$		50	95.3	
(Interface Running, PWM	Ι+	inputs at V+ or GND; PWM	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			99.2	μA
Disabled)		intensity control enabled	$T_A = T_{MIN}$ to $T_{MAX}$			102.4	
Supply Current		f <sub>SCL</sub> = 400kHz; other digital	$T_A = +25^{\circ}C$		57	110.2	
(Interface Running, PWM	۱+	inputs at V+ or GND; PWM	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			117.4	μA
Enabled)		intensity control enabled	$T_A = T_{MIN}$ to $T_{MAX}$			122.1	
Input High Voltage SDA, SCL, AD0, BLINK, P0–P15	VIH			0.7 x V+			V
Input Low Voltage SDA, SCL, AD0, BLINK, P0–P15	VIL					0.3 × V+	V
Input Leakage Current SDA, SCL, AD0, BLINK, P0-P15	I <sub>IH</sub> , I <sub>IL</sub>	$0 \le input voltage \le 5.5V$		-0.2		+0.2	μA
Input Capacitance SDA, SCL, AD0, BLINK, P0–P15					8		pF

## **ELECTRICAL CHARACTERISTICS (continued)**

(Typical Operating Circuit, V+ = 2V to 3.6V,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at V+ = 3.3V,  $T_A$ = + 25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIO	NS	MIN	ТҮР	MAX	UNITS
Output Low Voltage			$T_A = +25^{\circ}C$		0.15	0.26	
		$V + = 2V$ , $I_{SINK} = 20mA$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			0.3	V
			$T_A = T_{MIN}$ to $T_{MAX}$			0.32	
			$T_A = +25^{\circ}C$		0.13	0.23	
	Vol	$V + = 2.5V, I_{SINK} = 20mA$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			0.26	V
			$T_A = T_{MIN}$ to $T_{MAX}$			0.28	
			$T_A = +25^{\circ}C$		0.12	0.23	
		$V + = 3.3V$ , $I_{SINK} = 20mA$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			0.24	V
			$T_A = T_{MIN}$ to $T_{MAX}$			0.26	
Output Low-Voltage SDA	Volsda	$I_{SINK} = 6 m A$				0.4	V
PWM Clock Frequency	fpwm				32		kHz

### TIMING CHARACTERISTICS

(Typical Operating Circuit, V+ = 2V to 3.6V,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at V+ = 3.3V,  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
Serial Clock Frequency	fscl				400	kHz
Bus Free Time Between a STOP and a START Condition	tBUF		1.3			μs
Hold Time, Repeated START Condition	<sup>t</sup> HD, STA		0.6			μs
Repeated START Condition Setup Time	tsu, sta		0.6			μs
STOP Condition Setup Time	tsu, sto		0.6			μs
Data Hold Time	<sup>t</sup> hd, dat	(Note 2)			0.9	μs
Data Setup Time	<sup>t</sup> SU, DAT		180			ns
SCL Clock Low Period	tLOW		1.3			μs
SCL Clock High Period	thigh		0.7			μs
Rise Time of Both SDA and SCL Signals, Receiving	t <sub>R</sub>	(Notes 3, 4)		20 + 0.1C <sub>b</sub>	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	tF	(Notes 3, 4)		20 + 0.1C <sub>b</sub>	300	ns
Fall Time of SDA Transmitting	tf.tx	(Notes 3, 5)		20 + 0.1C <sub>b</sub>	250	ns
Pulse Width of Spike Suppressed	tsp	(Note 6)		50		ns
Capacitive Load for Each Bus Line	Cb	(Note 3)			400	pF
RST Pulse Width	tw		1			μs

## TIMING CHARACTERISTICS (continued)

(Typical Operating Circuit, V+ = 2V to 3.6V,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at V+ = 3.3V,  $T_A = +25^{\circ}$ C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
Interrupt Valid	tıv	Figure 10			6.5	μs
Interrupt Reset	tıR	Figure 10			1	μs
Output Data Valid	t <sub>DV</sub>	Figure 10			5	μs
Input Data Set-Up Time	tDS	Figure 10	100			ns
Input Data Hold Time	tDН	Figure 10	1			μs

Note 1: All parameters tested at  $T_A = +25^{\circ}C$ . Specifications over temperature are guaranteed by design.

Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V<sub>IL</sub> of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 3: Guaranteed by design.

Note 4: C<sub>b</sub> = total capacitance of one bus line in pF. t<sub>R</sub> and t<sub>F</sub> measured between 0.3 x V<sub>DD</sub> and 0.7 x V<sub>DD</sub>.

**Note 5:**  $I_{SINK} \le 6mA$ .  $C_b$  = total capacitance of one bus line in pF.  $t_R$  and  $t_F$  measured between 0.3 x V<sub>DD</sub> and 0.7 x V<sub>DD</sub>.

**Note 6:** Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

## **Typical Operating Characteristics**

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$ 





## **Typical Operating Characteristics (continued)**

 $(T_A = +25^{\circ}C, unless otherwise noted.)$ 





OUTPUT 2 2V/div **OUTPUT 2 INDIVIDUAL INTENSITY** SET TO 14/15 2ms/div



**MAX7314** 

## **Pin Description**

PI	N		FUNCTION
QSOP	QFN	NAME	FUNCTION
1	22	ĪNT/O16	Output Port. Open-drain output rated at 7V, 50mA. Configurable as interrupt output or general-purpose output.
2	23	RST	Reset Input. Active low clears the 2-wire interface and puts the device in the same condition as power-up reset.
3	24	AD0	Address Input. Sets device slave address. Connect to either GND, V+, SCL, or SDA to give four logic combinations. See Table 1.
4–11, 13–20	1–8, 10–17	P0-P15	Input/Output Ports. P0–P15 are open-drain I/Os rated at 5.5V, 50mA.
12	9	GND	Ground. Do not sink more than 350mA into the GND pin.
21	18	BLINK	Input Port Configurable as Blink Control or General-Purpose Input
22	19	SCL	I <sup>2</sup> C-Compatible Serial Clock Input
23	20	SDA	I <sup>2</sup> C-Compatible Serial Data I/O
24	21	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047µF ceramic capacitor.
—	PAD	Exposed Pad	Exposed Pad on Package Underside. Connect to GND.



Figure 1. Simplified Schematic of I/O Ports

## **Functional Overview**

The MAX7314 is a general-purpose input/output (GPIO) peripheral that provides 16 I/O ports, P0–P15, controlled through an I<sup>2</sup>C-compatible serial interface. A 17th output-only port, INT/O16, can be configured as an interrupt output or as a general-purpose output port.

All output ports sink loads up to 50mA connected to external supplies up to 5.5V, independent of the MAX7314's supply voltage. The MAX7314 is rated for a ground current of 350mA, allowing all 17 outputs to sink 20mA at the same time. Figure 1 shows the output structure of the MAX7314. The ports default to inputs on power-up.



#### **Port Inputs and Transition Detection**

Input ports registers reflect the incoming logic levels of the port pins, regardless of whether the pin is defined as an input or an output. Reading an input ports register latches the current-input logic level of the affected eight ports. Transition detection allows all ports configured as inputs to be monitored for changes in their logic status. The action of reading an input ports register samples the corresponding 8 port bits' input condition. This sample is continuously compared with the actual input conditions. A detected change in input condition causes the INT/O16 interrupt output to go low, if configured as an interrupt output. The interrupt is cleared either automatically if the changed input returns to its original state, or when the appropriate input ports register is read.

The INT/O16 pin can be configured as either an interrupt output or as a 17th output port with the same static or blink controls as the other 16 ports (Table 4).

#### **Port Output Control and LED Blinking**

The two blink phase 0 registers set the output logic levels of the 16 ports PO–P15 (Table 8). These registers control the port outputs if the blink function is disabled. A duplicate pair of registers, the blink phase 1 registers, are also used if the blink function is enabled (Table 9). In blink mode, the port outputs can be flipped between using the blink phase 0 registers and the blink phase 1 registers using hardware control (the BLINK input) and/or software control (the blink flip flag in the configuration register) (Table 4). The logic level of the BLINK input can be read back through the blink status bit in the configuration register (Table 4). The BLINK input, therefore, can be used as a general-purpose logic input (GPI port) if the blink function is not required.

#### **PWM Intensity Control**

The MAX7314 includes an internal oscillator, nominally 32kHz, to generate PWM timing for LED intensity control. PWM intensity control can be enabled on an output-by-output basis, allowing the MAX7314 to provide any mix of PWM LED drives and glitch-free logic outputs (Table 10). PWM can be disabled entirely, in which case all output ports are static and the MAX7314 operating current is lowest because the internal oscillator is turned off.

PWM intensity control uses a 4-bit master control and 4 bits of individual control per output (Tables 13, 14). The 4-bit master control provides 16 levels of overall intensity control, which applies to all PWM-enabled output ports. The master control sets the maximum pulse width from 1/15 to 15/15 of the PWM time period. The individual settings comprise a 4-bit number, further reducing the duty cycle to be from 1/16 to 15/16 of the time window set by the master control.

For applications requiring the same PWM setting for all output ports, a single global PWM control can be used instead of all the individual controls to simplify the control software and provide 240 steps of intensity control (Tables 10 and 13).

#### Standby Mode

When the serial interface is idle and the PWM intensity control is unused, the MAX7314 automatically enters standby mode. If the PWM intensity control is used, the operating current is slightly higher because the internal PWM oscillator is running. When the serial interface is active, the operating current also increases because the MAX7314, like all I<sup>2</sup>C slaves, has to monitor every transmission.



### Serial Interface Serial Addressing

The MAX7314 operates as a slave that sends and receives data through an I<sup>2</sup>C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX7314 and generates the SCL clock that synchronizes the data transfer (Figure 2).



Figure 3. Start and Stop Conditions



Figure 4. Bit Transfer



Figure 5. Acknowledge

The MAX7314 SDA line operates as both an input and an open-drain output. A pullup resistor, typically  $4.7 k\Omega$ , is required on the SDA. The MAX7314 SCL line operates only as an input. A pullup resistor, typically  $4.7 k\Omega$ , is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX7314 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 3).

#### Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

#### Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

#### Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7314, the device generates the acknowledge bit because the MAX7314 is the recipient. When the master, the master generates the acknowledge bit because the master is the recipient.

#### Slave Address

/N/IXI/N

The MAX7314 has a 7-bit long slave address (Figure 6). The eighth bit following the 7-bit slave address is the R/W bit. The R/W bit is low for a write command, high for a read command.



Figure 6. Slave Address

The second (A5), third (A4), fourth (A3), sixth (A1), and last (A0) bits of the MAX7314 slave address are always 1, 0, 0, 0, and 0. Slave address bits A6 and A2 are selected by the address input AD0. AD0 can be connected to GND, V+, SDA, or SCL. The MAX7314 has four possible slave addresses (Table 1), and therefore a maximum of four MAX7314 devices can be controlled independently from the same interface.

### Table 1. MAX7314 Address Map

		DEVICE ADDRESS										
	A6	A6 A5 A4 A3 A		A2	A1	A0						
SCL	1	1	0	0	0	0	0					
SDA	1	1	0	0	1	0	0					
GND	0	1	0	0	0	0	0					
V+	0	1	0	0	1	0	0					

#### Message Format for Writing the MAX7314

**MAX7314** 

A write to the MAX7314 comprises the transmission of the MAX7314's slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX7314 is to be written to by the next byte, if received (Table 2). If a STOP condition is detected after the command byte is received, then the MAX7314 takes no further action beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX7314 selected by the command byte (Figure 8). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX7314 internal registers because the command byte address autoincrements (Table 2). A diagram of a write to the output ports registers (blink phase 0 registers or blink phase 1 registers) is given in Figure 10.



Figure 7. Command Byte Received



Figure 8. Command and Single Data Byte Received



Figure 9. n Data Bytes Received



Figure 10. Read, Write, and Interrupt Timing Diagrams

#### Message Format for Reading

The MAX7314 is read using the MAX7314's internally stored command byte as an address pointer the same way the stored command byte is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write (Table 2). Thus, a read is initiated by first configuring the MAX7314's command byte by performing a write (Figure 7). The master can now read n consecutive bytes from the MAX7314 with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address has been autoincremented after the write (Table 2). A diagram of a read from the input ports registers is shown in Figure 10 reflecting the states of the ports.

#### **Operation with Multiple Masters**

If the MAX7314 is operated on a 2-wire interface with multiple masters, a master reading the MAX7314 should use a repeated start between the write, which sets the MAX7314's address pointer, and the read(s) that takes the data from the location(s) (Table 2). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX7314's address pointer but before master 1 has read the data. If master 2 subsequently changes the MAX7314's address pointer, then master 1's delayed read can be from an unexpected location.

#### **Command Address Autoincrementing**

The command address stored in the MAX7314 circulates around grouped register functions after each data byte is written or read (Table 2).



### Table 2. Register Address Map

REGISTER	ADDRESS CODE (hex)	AUTOINCREMENT ADDRESS
Read input ports P7–P0	0x00	0x01
Read input ports P15–P8	0x01	0x00
Blink phase 0 outputs P7–P0	0x02	0x03
Blink phase 0 outputs P15–P8	0x03	0x02
Ports configuration P7–P0	0x06	0x07
Ports configuration P15–P8	0x07	0x06
Blink phase 1 outputs P7-P0	0x0A	0x0B
Blink phase 1 outputs P15–P8	0x0B	0x0A
Master, O16 intensity	0x0E	0x0E (no change)
Configuration	0x0F	0x0F (no change)
Outputs intensity P1, P0	0x10	0x11
Outputs intensity P3, P2	0x11	0x12
Outputs intensity P5, P4	0x12	0x13
Outputs intensity P7, P6	0x13	0x14
Outputs intensity P9, P8	0x14	0x15
Outputs intensity P11, P10	0x15	0x16
Outputs intensity P13, P12	0x16	0x17
Outputs intensity P15, P14	0x17	0x10

#### **Device Reset**

The reset input  $\overline{\text{RST}}$  is an active-low input. When taken low,  $\overline{\text{RST}}$  clears any transaction to or from the MAX7314 on the serial interface and configures the internal registers to the same state as a power-up reset (Table 3), which resets all ports as inputs. The MAX7314 then waits for a START condition on the serial interface.

## **Detailed Description**

#### **Initial Power-Up**

On power-up, and whenever the RST input is pulled low, all control registers are reset and the MAX7314 enters standby mode (Table 3). Power-up status makes all ports into inputs and disables both the PWM oscillator and blink functionality. RST can be used as a hardware shutdown input, which effectively turns off any LED (or other) loads and puts the device into its lowest power condition.

#### **Configuration Register**

The configuration register is used to configure the PWM intensity mode, interrupt, and blink behavior, operate the INT/O16 output, and read back the interrupt status (Table 4).

#### **Ports Configuration**

The 16 I/O ports P0 through P15 can be configured to any combination of inputs and outputs using the ports configuration registers (Table 5). The INT/O16 output can also be configured as an extra general-purpose output, and the BLINK input can be configured as an extra general-purpose input using the configuration register (Table 4).

#### Input Ports

The input ports registers are read only (Table 6). They reflect the incoming logic levels of the ports, regardless of whether the port is defined as an input or an output by the ports configuration registers. Reading an input ports register latches the current-input logic level of the affected eight ports. A write to an input ports register is ignored.

## Table 3. Power-Up Configuration

REGISTER FUNCTION	POWER-UP CONDITION	ADDRESS CODE	REGISTER DATA									
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0		
Blink phase 0 outputs P7–P0	High-impedance outputs	0x02	1	1	1	1	1	1	1	1		
Blink phase 0 outputs P15–P8	High-impedance outputs	0x03	1	1	1	1	1	1	1	1		
Ports configuration P7–P0	Ports P7–P0 are inputs	0x06	1	1	1	1	1	1	1	1		
Ports configuration P15–P8	Ports P15–P8 are inputs	0x07	1	1	1	1	1	1	1	1		
Blink phase 1 outputs P7-P0	High-impedance outputs	0x0A	1	1	1	1	1	1	1	1		
Blink phase 1 outputs P15–P8	High-impedance outputs	0x0B	1	1	1	1	1	1	1	1		
Master, O16 intensity	PWM oscillator is disabled; O16 is static logic output	0x0E	0	0	0	0	1	1	1	1		
Configuration	INT/O16 is interrupt output; blink is disabled; global intensity is enabled		0	0	0	0	1	1	0	0		
Outputs intensity P1, P0	P1, P0 are static logic outputs	0x10	1	1	1	1	1	1	1	1		
Outputs Intensity P3, P2	P3, P2 are static logic outputs	0x11	1	1	1	1	1	1	1	1		
Outputs intensity P5, P4	P5, P4 are static logic outputs	0x12	1	1	1	1	1	1	1	1		
Outputs intensity P7, P6	P7, P6 are static logic outputs	0x13	1	1	1	1	1	1	1	1		
Outputs intensity P9, P8	P9, P8 are static logic outputs	0x14	1	1	1	1	1	1	1	1		
Outputs intensity P11, P10	P11, P10 are static logic outputs	0x15	1	1	1	1	1	1	1	1		
Outputs intensity P13, P12	P13, P12 are static logic outputs	0x16	1	1	1	1	1	1	1	1		
Outputs intensity P15, P14	P15, P14 are static logic outputs	0x17	1	1	1	1	1	1	1	1		

#### Transition Detection

All ports configured as inputs are always monitored for changes in their logic status. The action of reading an input ports register or writing to the configuration register samples the corresponding 8 port bits' input condition (Tables 4, 6). This sample is continuously compared with the actual input conditions. A detected change in input condition causes an interrupt condition. The interrupt is cleared either automatically if the changed input returns to its original state, or when the appropriate input ports register is read, updating the compared data (Figure 10). Randomly changing a port from an output to an input may cause a false interrupt to occur if the state of the input does not match the content of the appropriate input ports register. The interrupt status is available as the interrupt flag INT in the configuration register (Table 4).

The input status of all ports is sampled immediately after power-up as part of the MAX7314's internal initialization, so if all the ports are pulled to valid logic levels at that time, an interrupt does not occur at power-up.

#### **INT/O16** Output

M/IXI/M

The  $\overline{INT}/O16$  output pin can be configured as either the  $\overline{INT}$  output that reflects the interrupt flag logic state or as a general-purpose output O16. When used as a general-purpose output, the  $\overline{INT}/O16$  pin has the same blink and PWM intensity control capabilities as the other ports.

Set the interrupt enable I bit in the configuration register to configure INT/O16 as the INT output (Table 4). Clear interrupt enable to configure INT/O16 as the O16. The O16 logic state is set by the 2 bits O1 and O0 in the configuration register. O16 follows the rules for blinking selected by the blink enable flag E in the configuration register. If blinking is disabled, then interrupt output control O0 alone sets the logic state of the INT/O16 pin. If blinking is enabled, then both interrupt output controls O0 and O1 set the logic state of the INT/O16 pin according to the blink phase. PWM intensity control for O16 is set by the 4 global intensity bits in the master and O16 intensity register (Table 13).

### Table 4. Configuration Register

REGISTER		ADDRESS CODE				REGISTI	ER DATA	۱.		
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0
CONFIGURATION	R/W	0x0F	INTERRUPT STATUS	BLINK STATUS	INTERRUPT OUTPUT	CONTROL AS GPO	INTERRUPT ENABLE	GLOBAL INTENSITY	BLINK FLIP	enable Blink
Write device configuration	0		INT		01	0		6	Б	E
Read back device configuration	1			DLINK	01	00	1	G	В	E
Disable blink	—	-	Х	Х	Х	Х	Х	Х	Х	0
Enable blink	—		Х	Х	Х	Х	Х	Х	Х	1
Flip blink register (see text)	—	-	Х	Х	Х	Х	Х	Х	0	1
	—		Х	Х	Х	Х	Х	Х	1	1
Disable global intensity control—intensity is set by registers 0x10–0x17 for ports P0 through P15 when configured as outputs, and by D3–D0 of register 0x0E for INT/O16 when INT/O16 pin is configured as an output port	_		х	х	х	х	х	0	х	x
Enable global intensity control—intensity for all ports configured as outputs is set by D3–D0 of register 0x0E			Х	х	Х	х	Х	1	х	х
Disable data change interrupt—INT/O16 output is controlled by the O0 and O1 bits	_		Х	х	Х	х	0	Х	Х	х
Enable data change interrupt—INT/O16 output is controlled by port input data change	_		х	х	х	х	1	х	х	х
INT/O16 output is low (blink is disabled)	—		Х	Х	Х	0	0	Х	Х	0
INT/O16 output is high impedance (blink is disabled)	_		Х	Х	Х	1	0	Х	Х	0
INT/016 output is low during blink phase 0	_		Х	Х	Х	0	0	Х	Х	1
INT/O16 output is high impedance during blink phase 0	_		Х	Х	Х	1	0	Х	Х	1
INT/016 output is low during blink phase 1	—		Х	Х	0	Х	0	Х	Х	1
INT/O16 output is high impedance during blink phase 1	_		Х	Х	1	Х	0	Х	Х	1

X = Don't care.

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## Table 4. Configuration Register (continued)

REGISTER		ADDRESS CODE				REGISTI	ER DATA	۱.		
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0
CONFIGURATION	R/W		INTERRUPT STATUS	BLINK STATUS	INTERRUPT OUTPUT	CONTROL AS GPO	INTERRUPT ENABLE	GLOBAL INTENSITY	BLINK FLIP	BLINK ENABLE
Write device configuration	0		INT		01	00		G	в	F
Read back device configuration	1			DEINK	01	00	•	ŭ	D	-
Read back BLINK input pin status— input is low	1	0.05	Х	0	Х	Х	Х	Х	Х	х
Read back BLINK input pin status— input is high	1	UXUF	Х	1	Х	Х	Х	х	Х	х
Read back data change interrupt status —data change is not detected, and INT/O16 output is high when interrupt enable (I bit) is set	1		0	х	Х	х	х	х	Х	х
Read back data change interrupt status —data change is detected, and INT/O16 output is low when interrupt enable (I bit) is set	1		1	Х	Х	Х	Х	Х	Х	х

X = Don't care.

#### **Blink Mode**

In blink mode, the output ports can be flipped between using either the blink phase 0 registers or the blink phase 1 registers. Flip control is both hardware (the BLINK input) and software control (the blink flip flag B in the configuration register) (Table 4).

The blink function can be used for LED effects by programming different display patterns in the two sets of output port registers, and using the software or hardware controls to flip between the patterns.

If the blink phase 1 registers are written with 0xFF, then the BLINK input can be used as a hardware disable to, for example, instantly turn off an LED pattern programmed into the blink phase 0 registers. This technique can be further extended by driving the BLINK input with a PWM signal to modulate the LED current to provide fading effects.

The blink mode is enabled by setting the blink enable flag E in the configuration register (Table 4). When blink mode is enabled, the states of the blink flip flag and the BLINK input are EXOR'ed to set the phase, and the output ports are set by either the blink phase 0 registers or the blink phase 1 registers (Figure 11) (Table 7).

The blink mode is disabled by clearing the blink enable flag E in the configuration register (Table 4). When blink mode is disabled, the state of the blink flip flag is ignored, and the blink phase 0 registers alone control the output ports.

#### **Blink Phase Registers**

When the blink function is disabled, the two blink phase 0 registers set the logic levels of the 16 ports (P0 through P15) when configured as outputs (Table 8). A duplicate pair of registers called the blink phase 1 registers are also used if the blink function is enabled (Table 9). A logic high sets the appropriate output port high impedance, while a logic low makes the port go low.



Figure 11. Blink Logic

### **Table 5. Ports Configuration Registers**

REGISTER	R/W	ADDRESS CODE				REGISTE	ER DATA			
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0
Ports configuration P7–P0 (1 = input, 0 = output)	0	0x06	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read back ports configuration P7–P0	1									
Ports configuration P15–P8 (1 = input, 0 = output)	0	0x07	OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8
Read back ports configuration P15–P8	1									

### **Table 6. Input Ports Registers**

REGISTER	R/W	ADDRESS CODE				REGISTE	ER DATA	١		
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0
Read input ports P7–P0	1	0x00	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Read input ports P15–P8	1	0x01	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IP8

### Table 7. Blink Logic

BLINK ENABLE FLAG E	BLINK FLIP FLAG B	BLINK INPUT PIN	BLINK FLIP FLAG Exor Blink input pin	BLINK FUNCTION	OUTPUT REGISTERS USED
0	Х	Х	Х	Disabled	Blink phase 0 registers
	0	0	0		Blink phase 0 registers
4	0	1	1	Fachlad	Blink phase 1 registers
	1	0	1	Enabled	Blink phase 1 registers
	1	1	0		Blink phase 0 registers

Reading a blink phase register reads the value stored in the register, not the actual port condition. The port output itself may or may not be at a valid logic level, depending on the external load connected.

The 17th output, O16, is controlled through 2 bits in the configuration register, which provide the same static or blink control as the other 16 output ports.

#### **PWM Intensity Control**

The MAX7314 includes an internal oscillator, nominally 32kHz, to generate PWM timing for LED intensity control or other applications such as PWM trim DACs. PWM can be disabled entirely for all the outputs. In this case, all outputs are static and the MAX7314 operating current is lowest because the internal PWM oscillator is turned off.

The MAX7314 can be configured to provide any combination of PWM outputs and glitch-free logic outputs. Each PWM output has an individual 4-bit intensity control (Table 14). When all outputs are to be used with the same PWM setting, the outputs can be controlled together instead using the global intensity control (Table 13). Table 10 shows how to set up the MAX7314 to suit a particular application.

#### **PWM Timing**

The PWM control uses a 240-step PWM period, divided into 15 master intensity timeslots. Each master intensity timeslot is divided further into 16 PWM cycles (Figure 12).

The master intensity operates as a gate, allowing the individual output settings to be enabled from 1 to 15 timeslots per PWM period (Figures 13, 14, 15) (Table 13).

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### Table 8. Blink Phase 0 Registers

REGISTER	R/W	ADDRESS CODE				REGISTE	ER DATA			
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0
Write outputs P7–P0 phase 0	0	0,000		OPe				OP2		
Read back outputs P7–P0 phase 0	1	0X02	UF7	OFU	0F5	OF4	UF3	UF2	OFI	OFU
Write outputs P15–P8 phase 0	0	0,02				0012				
Read back outputs P15–P8 phase 0	1	0x03	UF 15	OF 14	UF 13	UF 12	OFTI	UF IU	0F9	UFO

Table 9. Blink Phase 1 Registers

REGISTER	R/W	ADDRESS CODE				REGISTE	ER DATA	<b>N</b>		
		(hex)	D7	D6	D5	D4	D3	D2	D1	D0
Write outputs P7–P0 phase 1	0	0,000		OPE	OPE		002	OP2		
Read back outputs P7-P0 phase 1	1	UXUA	UP7	OP6	UP5	UP4	UP3	UP2	UPI	OPU
Write outputs P15–P8 phase 1	0				0012			0010		
Read back outputs P15-P8 phase 1	1	UXUB	UP 15	UP 14	UP 13	UP12	UPTI	UPIU	UP9	UPO

Each output's individual 4-bit intensity control only operates during the number of timeslots gated by the master intensity. The individual controls provide 16 intensity settings from 1/16 through 16/16 (Table 14).

Figures 16, 17, and 18 show examples of individual intensity control settings. The highest value an individual or global setting can be set to is 16/16. This setting forces the output to ignore the master control, and follow the logic level set by the appropriate blink phase register bit. The output becomes a glitch-free static output with no PWM.

**Using PWM Intensity Controls with Blink Disabled** When blink is disabled (Table 7), the blink phase 0 registers specify each output's logic level during the PWM on-time (Table 8). The effect of setting an output's blink phase 0 register bit to zero or 1 is shown in Table 11. With its output bit set to zero, an LED can be controlled with 16 intensity settings from 1/16th duty through fully on, but cannot be turned fully off using the PWM intensity control. With its output bit set to 1, an LED can be controlled with 16 intensity settings from fully off through 15/16th duty.

#### Using PWM Intensity Controls with Blink Enabled

When blink is enabled (Table 7), the blink phase 0 registers and blink phase 1 registers specify each output's logic level during the PWM on-time during the respective blink phases (Tables 8 and 9). The effect of setting an output's blink phase x register bit to zero or 1 is shown in Table 12. LEDs can be flipped between either directly on and off, or between a variety of high/low PWM intensities.

#### Global/O16 Intensity Control

The 4 bits used for output O16's PWM individual intensity setting also double as the global intensity control (Table 13). Global intensity simplifies the PWM settings when the application requires them all to be the same, such as for backlight applications, by replacing the 17 individual settings with 1 setting. Global intensity is enabled with the global intensity flag G in the configuration register (Table 4). When global PWM control is used, the 4 bits of master intensity and 4 bits of global intensity effectively combine to provide an 8-bit, 240step intensity control applying to all outputs.

It is not possible to apply global PWM control to a subset of the ports, and use the others as logic outputs. To mix static logic outputs and PWM outputs, individual PWM control must be selected (Table 10).



## **Table 10. PWM Application Scenarios**

APPLICATION	RECOMMENDED CONFIGURATION
All outputs static without PWM	Set the master, O16 intensity register 0x0E to any value 0x00 to 0xOF. The global intensity G bit in the configuration register is don't care. The output intensity registers 0x10 through 0x17 are don't care.
A mix of static and PWM outputs, with PWM outputs using different PWM settings	Set the master and global intensity register 0x0E to any value from 0x10 to 0xFF. Clear global intensity G bit to zero in the configuration register to disable global intensity control. For the static outputs, set the output intensity value to 0xF. For the PWM outputs, set the output intensity value in the 0x0 to 0xE range.
A mix of static and PWM outputs, with PWM outputs all using the same PWM setting	As above. Global intensity control cannot be used with a mix of static and PWM outputs, so write the individual intensity registers with the same PWM value.
All outputs PWM using the same PWM setting	Set the master, O16 intensity register 0x0E to any value from 0x10 to 0xFF. Set global intensity G bit to 1 in the configuration register to enable global intensity control. The master, O16 intensity register 0x0E is the only intensity register used. The output intensity registers 0x10 through 0x17 are don't care.



Figure 12. PWM Timing



Figure 13. Master Set to 1/15

Figure 14. Master Set to 14/15

14	15	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	1	2

Figure 15. Master Set to 15/15

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MASTER INTENSITY TIMESLOT

NEXT MASTER INTENSITY TIMESLOT

Figure 16. Individual (or Global) Set to 1/16

1

				MAS	TER	INTE	VSIT	7 TIN	<b>NESL</b>	.0T										Ν	EXT	MAS	TER	INTE	NSIT	Y TI	MESI	_0T			
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

Figure 17. Individual (or Global) Set to 15/16

										M	ASTE	R IN	TENS	SITY 1	IMES	SLOT	CON	TRO	LISI	GNO	RED										
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Figure 18. Individual (or Global) Set to 16/16

### Table 11. PWM Intensity Settings (Blink Disabled)

OUTPUT (OR GLOBAL) INTENSITY	PWM DUT OUTPUT BLI REGISTE	TY CYCLE NK PHASE 0 R BIT = 0	LED BEHAVIOR WHEN OUTPUT BLINK PHASE 0 REGISTER BIT = 0 (LED IS ON WHEN	PWM DUT OUTPUT BLI REGIST	TY CYCLE NK PHASE 0 FER = 1	LED BEHAVIOR WHEN OUTPUT BLINK PHASE 0 REGISTER BIT = 1 (LED IS ON WHEN
SETTING	LOW TIME	HIGH TIME	OUTPUT IS LOW)	LOW TIME	HIGH TIME	OUTPUT IS LOW)
0x0	1/16	15/16	Lowest PWM intensity	15/16	1/16	Highest PWM intensity
0x1	2/16	14/16		14/16	2/16	
0x2	3/16	13/16		13/16	3/16	
0x3	4/16	12/16	>	12/16	4/16	^
0x4	5/16	11/16	nsit	11/16	5/16	
0x5	6/16	10/16	inte	10/16	6/16	ens
0x6	7/16	9/16	MN	9/16	7/16	1 int
0x7	8/16	8/16	D D	8/16	8/16	$\sim$
0x8	9/16	7/16	tsing	7/16	9/16	р Д
0x9	10/16	6/16	crea	6/16	10/16	asir
0xA	11/16	5/16	- Inc	5/16	11/16	icre
0xB	12/16	4/16	$\checkmark$	4/16	12/16	<u> </u>
0xC	13/16	3/16		3/16	13/16	
0xD	14/16	2/16		2/16	14/16	
0xE	15/16	1/16	Highest PWM intensity	1/16	15/16	Lowest PWM intensity
0xF	Static low	Static low	Full intensity, no PWM (LED on continuously)	Static high impedance	Static high impedance	LED off continuously



### Table 12. PWM Intensity Settings (Blink Enabled)

OUTPUT					EXAMPLES OF LEI (LED IS ON WHEN	D BLINK BEHAVIOR I OUTPUT IS LOW)
(OR GLOBAL) INTENSITY	PHA REGISTE	SE X R BIT = 0	PHA REGIS	SE X TER = 1	BLINK PHASE 0 REGISTER BIT = 0	BLINK PHASE 0 REGISTER BIT = 1
SETTING	LOW TIME	HIGH TIME	LOW TIME	HIGH TIME	BLINK PHASE 1 REGISTER BIT = 1	BLINK PHASE 1 REGISTER BIT = 0
0x0	1/16	15/16	15/16	1/16		
0x1	2/16	14/16	14/16	2/16		
0x2	3/16	13/16	13/16	3/16		
0x3	4/16	12/16	12/16	4/16	Phase 0: LED on at low intensity	Phase 0: LED on at high intensity
0x4	5/16	11/16	11/16	5/16	Thase I. LED OF at high intensity	Thase T. LED of allow intensity
0x5	6/16	10/16	10/16	6/16		
0x6	7/16	9/16	9/16	7/16		
0x7	8/16	8/16	8/16	8/16	Output is half intensity of	during both blink phases
0x8	9/16	7/16	7/16	9/16		
0x9	10/16	6/16	6/16	10/16		
0xA	11/16	5/16	5/16	11/16		
0xB	12/16	4/16	4/16	12/16	Phase 0: LED on at high intensity	Phase 0: LED on at low intensity
0xC	13/16	3/16	3/16	13/16	Thase T. LED OF at low intensity	Thase T. LED OF at high intensity
0xD	14/16	2/16	2/16	14/16		
0xE	15/16	1/16	1/16	15/16		
0xF	Static low	Static low	Static high impedance	Static high impedance	Phase 0: LED on continuously Phase 1: LED off continuously	Phase 0: LED off continuously Phase 1: LED on continuously

## **Applications Information**

#### **Hot Insertion**

I/O ports P0–P15, interrupt output  $\overline{INT}$ /O16,  $\overline{RST}$  input, BLINK input, and serial interface SDA, SCL, AD0 remain high impedance with up to 6V asserted on them when the MAX7314 is powered down (V+ = 0V). The MAX7314 can therefore be used in hot-swap applications.

#### **Output Level Translation**

The open-drain output architecture allows the ports to level translate the outputs to higher or lower voltages than the MAX7314 supply. An external pullup resistor can be used on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to 5.5V. For interfacing CMOS inputs, a pullup resistor value of 220k $\Omega$  is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

#### **Driving LED Loads**

When driving LEDs, a resistor in series with the LED must be used to limit the LED current to no more than 50mA. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

 $\mathsf{R}_{\mathsf{LED}}$  is the resistance of the resistor in series with the LED  $(\Omega).$ 

 $V_{SUPPLY}$  is the supply voltage used to drive the LED (V).  $V_{LED}$  is the forward voltage of the LED (V).

 $V_{OL}$  is the output low voltage of the MAX7314 when sinking  $I_{LED}$  (V).

ILED is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 14mA from a 5V supply,  $R_{LED} = (5 - 2.2 - 0.25) / 0.014 = 182\Omega$ .



## Table 13. Master, O16 Intensity Register

REGISTER		ADDRESS CODE	REGISTER DATA							
	R/W	(hex)	D7	D6	D5	D4	D3	D2	D1	D0
MASTER AND GLOBAL INTENSITY			MSB			LSB	MSB			LSB
			MASTER INTENSITY				O16 INTENSITY			
Write master and global intensity	0		MO	MO	MI	MO	62	Ga	G1	60
Read back master and global intensity	1		1013	IVIZ		IVIO	03	62	GI	GU
Master intensity duty cycle is 0/15 (off); internal oscillator is disabled; all outputs will be static with no PWM	_	OXOE	0	0	0	0	_	_	_	
Master intensity duty cycle is 1/15			0	0	0	1	—	—	—	
Master intensity duty cycle is 2/15	—		0	0	1	0				
Master intensity duty cycle is 3/15			0	0	1	1				
Master intensity duty cycle is 13/15			1	1	0	1				
Master intensity duty cycle is 14/15			1	1	1	0				
Master intensity duty cycle is 15/15 (full)			1	1	1	1				
O16 intensity duty cycle is 1/16	—						0	0	0	0
O16 intensity duty cycle is 2/16							0	0	0	1
O16 intensity duty cycle is 3/16	—						0	0	1	0
					_					
O16 intensity duty cycle is 14/16			_	_			1	1	0	1
O16 intensity duty cycle is 15/16					_		1	1	1	0
O16 intensity duty cycle is 16/16 (static output, no PWM)	_		_	_	_	_	1	1	1	1

### Table 14. Output Intensity Registers

REGISTER		ADDRESS CODE	S REGISTER DATA							
	R/W	(hex)	D7	D6	D5	D4	D3	D2	D1	D0
			MSB			LSB	MSB			LSB
			OUTPUT P1 INTENSITY OUTPUT P0 INTENSITY							
Write output P1, P0 intensity	0		D112	D112	D111	P110	POIS	POI2	POI1	POIO
Read back output P1, P0 intensity	1		1 110	1 112	1 111	1 110	1 010	1 012	1.011	1 010
Output P1 intensity duty cycle is 1/16	—	-	0	0	0	0	—	—	—	—
Output P1 intensity duty cycle is 2/16	—	-	0	0	0	1	—	—	—	—
Output P1 intensity duty cycle is 3/16	—	-	0	0	1	0	—		—	—
	—				—	—				
Output P1 intensity duty cycle is 14/16	—	0X10	1	1	0	1	—	—	—	—
Output P1 intensity duty cycle is 15/16	—		1	1	1	0				
Output P1 intensity duty cycle is 16/16 (static logic level, no PWM)	_		1	1	1	1	_	_	_	_
Output PO intensity duty cycle is 1/16	1						0	0	0	0
Output P0 intensity duty cycle is 2/16							0	0	0	1
Output P0 intensity duty cycle is 3/16							0	0	1	0
							0	0	· ·	0
Output PO intensity duty cycle is 14/16							1	1	0	1
Output P0 intensity duty cycle is 15/16							1	1	1	0
Output P0 intensity duty cycle is 16/16							•	•	•	Ŭ
(static logic level, no PWM)	—			—	—	—	1	1	1	1
			MSB			LSB	MSB			LSB
001F013 F3, F2 INTENSIT		0v11	<b>OUTPUT P3 INTENSITY</b>			<b>OUTPUT P2 INTENSITY</b>				
Write output P3, P2 intensity	0	UX11	210			0210				DOIO
Read back output P3, P2 intensity	1		P313	P 312	P311	P310	P213	P212	F211	P210
OUTPUTS P5, P4 INTENSITY		0x12								
Write output P5_P4 intensity	0									
Read back output P5_P4 intensity	1		P5I3	P512	P5I1	P510	P4I3	P4I2	P4I1	P410
			<u> </u>							
	İ		MSB			LSB	MSB			LSB
OUTPUTS P7, P6 INTENSITY		010	OU	OUTPUT P7 INTENSITY			OUTPUT P6 INTENSITY			
Write output P7, P6 intensity	0	0x13	0710		ניקס		DOIO	DOIO	Dold	DOIO
Read back output P7, P6 intensity	1		P/13	P/12	P/I1	P/10	P613	P612	P611	P610

## Table 14. Output Intensity Registers (continued)

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REGISTER		ADDRESS CODE		REGISTER DATA						
	R/W	(hex)	D7	D6	D5	D4	D3	D2	D1	D0
	1		MSB			LSB	MSB			LSB
OUTPUTS P9, P8 INTENSITY		014	OUTPUT P9 INTENSITY				OUTPUT P8 INTENSITY			
Write output P9, P8 intensity	0	0x14	Dolo	Dolo	Dold	Dolo	Dolo	Dolo	Dold	Dolo
Read back output P9, P8 intensity	1		P913	P912	P911	P910	P813	P812	P811	P810
			MSB			LSB	MSB			LSB
OUTPUTS PTT, PTU INTENSITY		0v15	OUTPUT P11 INTENSITY				OUTPUT P10 INTENSITY			
Write output P11, P10 intensity	0	- Ux15 -		D1110		DIIIO	Diolo	DIOIO		
Read back output P11, P10 intensity	1		PIII3	PTHZ	PIIII	PTHU	P1013	P 1012	PIUII	P 1010
			MSB			LSB	MSB			LSB
001F013F13,F12INTEN3111		0v16	OUTPUT P13 INTENSITY			OUTPUT P12 INTENSITY			SITY	
Write output P13, P12 intensity	0	UX 16	D1212	D1212	D1211	D1210	D1012	D1010	DIOII	D1210
Read back output P13, P12 intensity	1		F 1313	F 1312	FISH	F 1310	F 1213	F IZIZ	F IZII	F 1210
		0x17 -	MSB			LSB	MSB			LSB
001P013 P13, P14 INTENSIT			OUTPUT P15 INTENSITY			OUTPUT P14 INTENSITY				
Write output P15, P14 intensity	0		D1512	D1512	D1511	P1510	D1/13	D1/10	D1/11	D1/10
Read back output P15, P14 intensity	1		1 1010	1 1312	1 1311	1 1310	1 1413	1 1412	1 1411	1 1410
OUTPUT O16 INTENSITY				See	master, C	016 inten	sity regis	ter (Table	ə 13).	

#### **Driving Load Currents Higher than 50mA**

The MAX7314 can be used to drive loads drawing more than 50mA, like relays and high-current white LEDs, by paralleling outputs. Use at least one output per 50mA of load current; for example, a 5V 330mW relay draws 66mA and needs two paralleled outputs to drive it. Ensure that the paralleled outputs chosen are controlled by the same blink phase register, i.e., select outputs from the P0 through P7 range, or the P8 through P15 range. This way, the paralleled outputs are turned on and off together. Do not use output O16 as part of a load-sharing design. O16 cannot be switched at the same time as any of the other outputs because it is controlled by a different register. The MAX7314 must be protected from the negative voltage transient generated when switching off inductive loads, such as relays, by connecting a reversebiased diode across the inductive load (Figure 19). The peak current through the diode is the inductive load's operating current.

#### **Power-Supply Considerations**

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The MAX7314 operates with a power-supply voltage of 2V to 3.6V. Bypass the power supply to GND with at least  $0.047\mu$ F as close to the device as possible. For the QFN version, connect the underside exposed pad to GND.

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## Pin Configurations

MAX7314





TRANSISTOR COUNT: 25,991 PROCESS: BICMOS



Figure 19. Diode-Protected Switching Inductive Load

### **Package Information**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



### Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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#### ООО "ЛайфЭлектроникс"

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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