# 74LV04

#### Hex inverter

Rev. 4 — 8 December 2015

Product data sheet

### 1. General description

The 74LV04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC04 and 74HCT04.

The 74LV04 provides six inverting buffers.

### 2. Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V<sub>CC</sub> = 2.7 V and V<sub>CC</sub> = 3.6 V
- Typical output ground bounce < 0.8 V at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot: > 2 V at  $V_{CC}$  = 3.3 V and  $T_{amb}$  = 25 °C
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

### 3. Ordering information

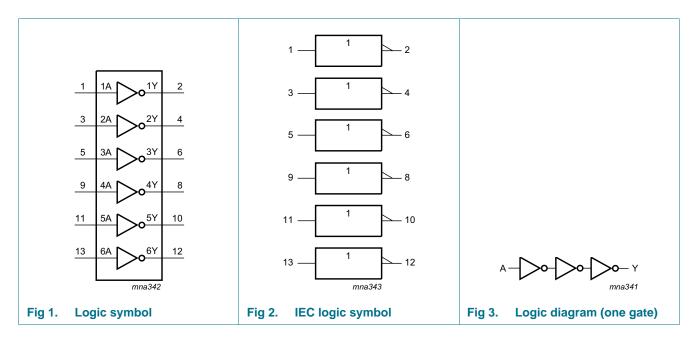
Table 1. Ordering information

Type number	Package										
	Temperature range	Name	Description	Version							
74LV04D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1							
74LV04DB	4DB -40 °C to +125 °C SSOP14 plastic shrink small outline package; 14 leads; body width 5.3 mm										
74LV04PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1							
74LV04BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1							



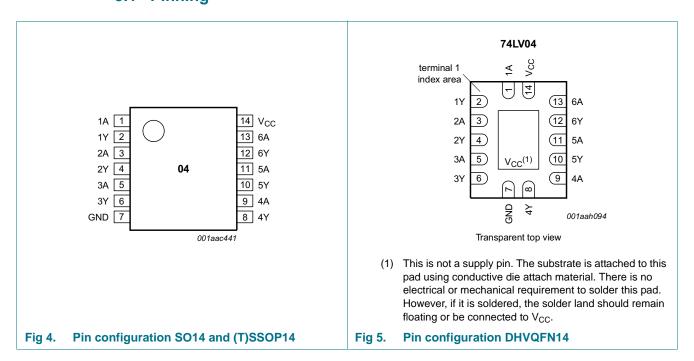
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### 4. Functional diagram



### 5. Pinning information

### 5.1 Pinning



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### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nA	Output nY
L	Н
Н	L

# 7. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±50	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I <sub>CC</sub>	supply current			-	50	mA
$I_{GND}$	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C

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 Table 4.
 Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$				
	SO14 package		[2]	-	500	mW
	(T)SSOP14 package		[3]	-	500	mW
	DHVQFN14 package		[4]	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.
- [3] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.
- [4] P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

### 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage	[1]	1.0	3.3	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.0 V to 2.0 V	-	-	500	ns/V
		V <sub>CC</sub> = 2.0 V to 2.7 V	-	-	200	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	100	ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V	-	-	50	ns/V

<sup>[1]</sup> The static characteristics are guaranteed from  $V_{CC}$  = 1.2 V to  $V_{CC}$  = 5.5 V, but LV devices are guaranteed to function down to  $V_{CC}$  = 1.0 V (with input levels GND or  $V_{CC}$ ).

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## 9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	35 °C	-40 °C to	Unit	
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = -100 \mu A; V_{CC} = 1.2 V$	-	1.2	-	-	-	V
		$I_O = -100 \mu A; V_{CC} = 2.0 V$	1.8	2.0	-	1.8	-	V
		$I_O = -100 \mu A; V_{CC} = 2.7 V$	2.5	2.7	-	2.5	-	V
		$I_O = -100 \mu A; V_{CC} = 3.0 \text{ V}$	2.8	3.0	-	2.8	-	V
		$I_O = -100 \mu A; V_{CC} = 4.5 V$	4.3	4.5	-	4.3	-	V
		$I_{O} = -6 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	2.82	-	2.2	-	٧
		$I_{O} = -12 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.6	4.2	-	3.5	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = 100 \mu A; V_{CC} = 1.2 V$	-	0	-	-	-	V
		$I_O = 100 \mu A; V_{CC} = 2.0 V$	-	0	0.2	-	0.2	V
		$I_O = 100 \mu A; V_{CC} = 2.7 V$	-	0	0.2	-	0.2	V
		$I_O = 100 \mu A; V_{CC} = 3.0 V$	-	0	0.2	-	0.2	V
		$I_O = 100 \mu A; V_{CC} = 4.5 V$	-	0	0.2	-	0.2	V
		$I_{O} = 6 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	0.25	0.40	-	0.50	V
		$I_O = 12 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.35	0.55	-	0.65	V
I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	1.0	μА
CC	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	20.0	-	40	μА
7l <sup>CC</sup>	additional supply current	per input; $V_I = V_{CC} - 0.6 \text{ V}$ ; $V_{CC} = 2.7 \text{ V}$ to 3.6 V	-	-	500	-	850	μА
Cı	input capacitance		-	3.5	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C.

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### 10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions	-40	°C to +85	S°C	–40 °C t	Unit		
					Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see Figure 6	[2]						
		V <sub>CC</sub> = 1.2 V		-	40	-	-	-	ns
		V <sub>CC</sub> = 2.0 V		-	14	20	-	25	ns
		V <sub>CC</sub> = 2.7 V		-	10	15	-	19	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V; } C_L = 15 \text{ pF}$	[3]	-	6	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	8	12	-	15	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V		-	-	9	-	11	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L = 50 \text{ pF}; f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[4]	-	21	-	-	-	pF

- [1] All typical values are measured at  $T_{amb}$  = 25 °C.
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$ ).
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 $f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

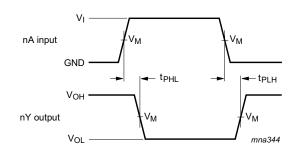
 $C_L$  = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$  = sum of the outputs.

### 11. Waveforms



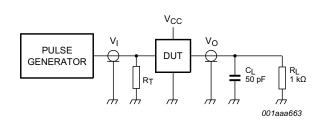
Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
Vcc	V <sub>M</sub>	V <sub>M</sub>
	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input				
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>			
< 2.7 V	V <sub>CC</sub>	≤ 2.5 ns			
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns			
≥ 4.5 V	V <sub>CC</sub>	≤ 2.5 ns			

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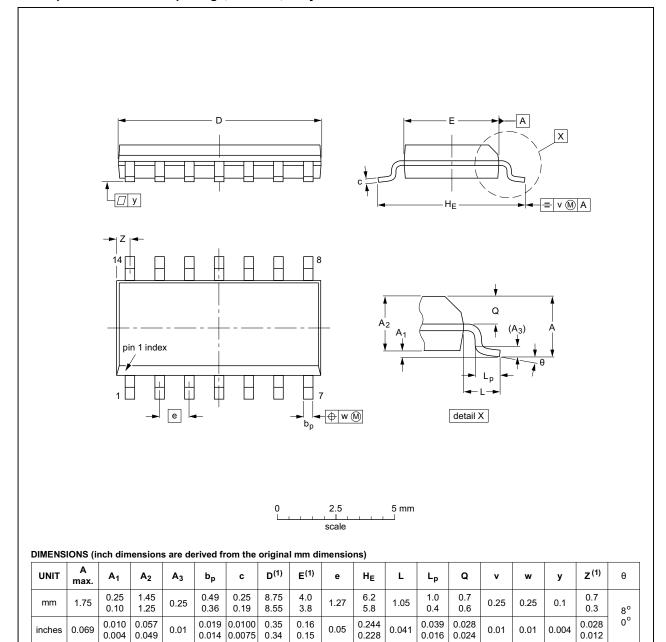
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### 12. Package outline

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	135UE DATE	
SOT108-1	076E06	MS-012			<del>99-12-27</del> 03-02-19	

Fig 8. Package outline SOT108-1 (SO14)

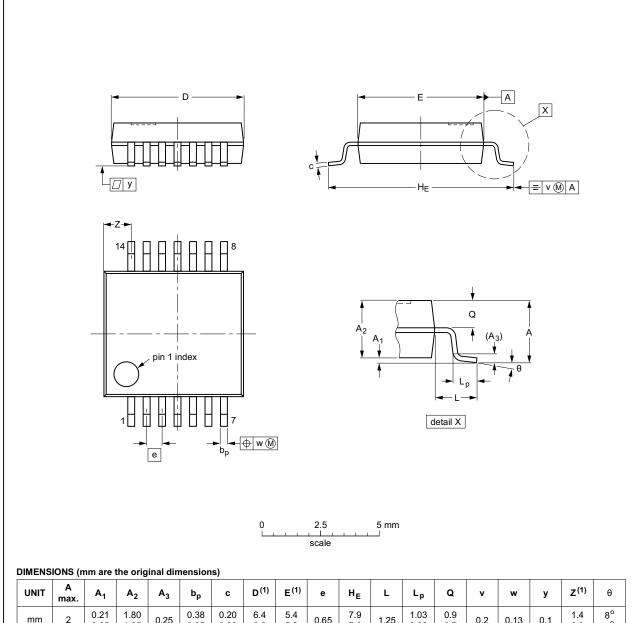
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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	b <sub>p</sub>	C	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

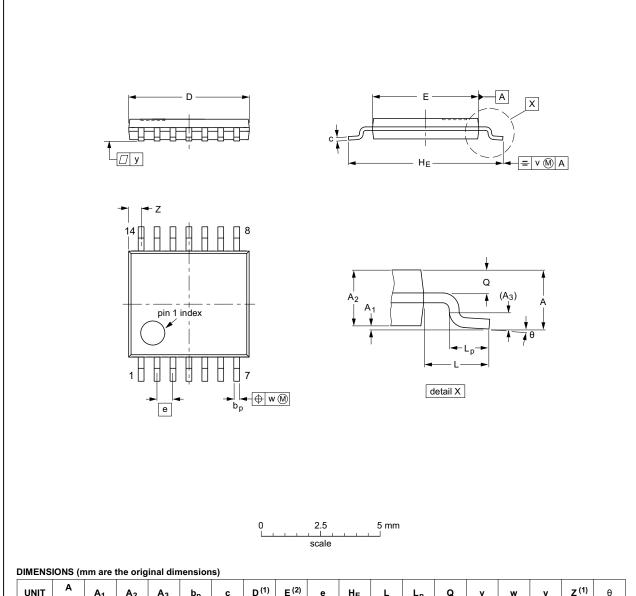
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT337-1		MO-150				<del>99-12-27</del> 03-02-19	

Package outline SOT337-1 (SSOP14) Fig 9.

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	٧	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

JEI <sup>-</sup>	PROJECTIO	ON ISSUE DATE
		<del>99-12-27</del> 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body  $2.5 \times 3 \times 0.85$  mm

SOT762-1

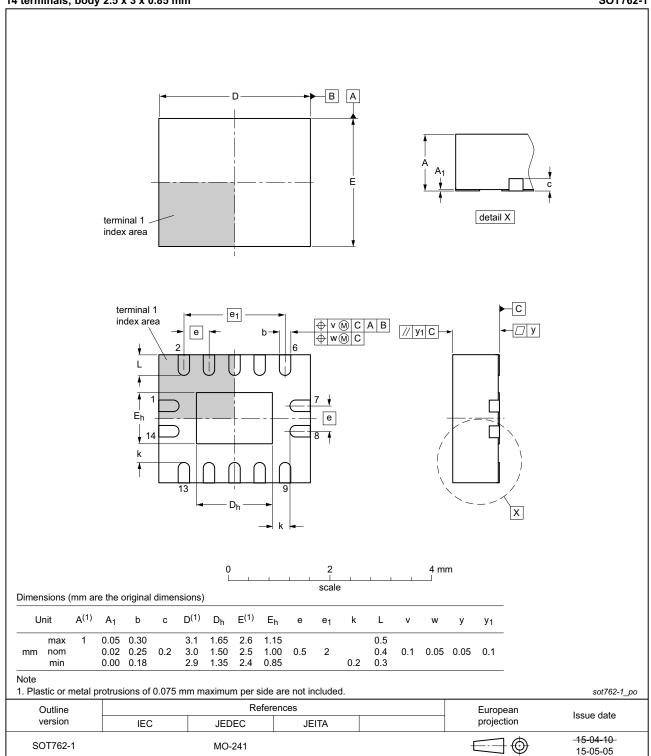


Fig 11. Package outline SOT762-1 (DHVQFN14)

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### 13. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes						
74LV04 v.4	20151208	Product data sheet	-	74LV04 v.3						
Modifications:	Type number	Type number 74LV04N (SOT27-1) removed.								
74LV04 v.3	20071204	20071204 Product data sheet - 74LV04 v.2								
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>									
	Section 3: DHVQFN14 package added.									
	<ul> <li><u>Section 8</u>: derating values added for DHVQFN14 package.</li> </ul>									
	<ul> <li><u>Section 12</u>: outline drawing added for DHVQFN14 package.</li> </ul>									
74LV04 v.2	19980420	Product specification	-	74LV04 v.1						
74LV04 v.1	19970203	Product specification	-	-						

#### 15.1 Data sheet status

15. Legal information

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

#### Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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