maxim integrated™

MAX3110E/MAX3111E

SPI/MICROWIRE-Compatible UART and ±15kV ESD-Protected RS-232 Transceivers with Internal Capacitors

General Description

The MAX3110E/MAX3111E combine a full-featured universal asynchronous receiver/transmitter (UART) with ±15kV ESD-protected RS-232 transceivers and integrated charge-pump capacitors into a single 28-pin package for use in space-, cost-, and power-constrained applications. The MAX3110E/MAX3111E also feature an SPI™/QSPI™/MICROWIRE™-compatible serial interface to save additional board space and microcontroller (µC) I/O pins.

A proprietary low-dropout output stage enables the 2-driver/2-receiver interface to deliver true RS-232 performance down to V_{CC} = +3V (+4.5V for MAX3110E) while consuming only 600µA. The receivers remain active in a hardware/software-invoked shutdown, allowing external devices to be monitored while consuming only 10µA. Each device is guaranteed to operate at up to 230kbps while maintaining true EIA/TIA-232 output voltage levels.

The MAX3110E/MAX3111E's UART includes a crystal oscillator and baud-rate generator with software-programmable divider ratios for all common baud rates from 300baud to 230kbaud. The UART features an 8-word-deep receive FIFO that minimizes processor overhead and provides a flexible interrupt with four maskable sources. Two control lines (one input and one output) are included for hardware handshaking.

The UART and RS-232 functions can be used together or independently since the two functions share only supply and ground connections (the MAX3110E/MAX3111E are hardware- and software-compatible with the MAX3100 and MAX3222E).

Applications

Point-of-Sale (POS) Devices

Handy-Terminals

Telecom/Networking Diagnostic Ports

Industrial Front-Panel Interfaces

Hand-Held/Battery-Powered Equipment

Pin Configuration appears at end of data sheet.

†Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

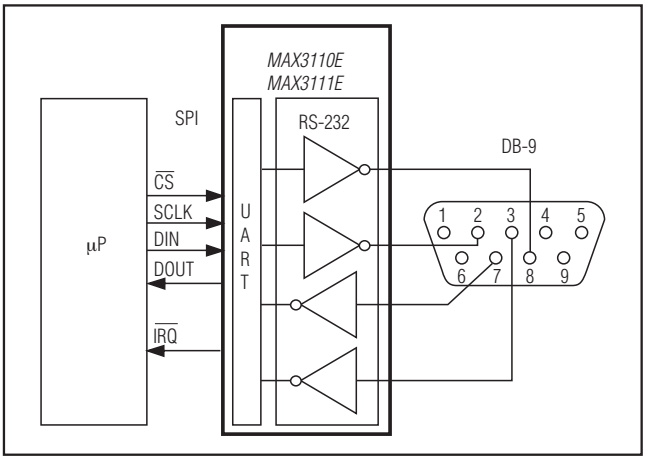
- **Integrated RS-232 Transceiver and UART in a Single 28-Pin Package**
- **SPI/QSPI/MICROWIRE-Compatible µC Interface**
- **Internal Charge-Pump Capacitors—No External Components Required!**
- **True RS-232 Operation Down to V_{CC} = +3V (MAX3111E)**
- **ESD Protection for RS-232 I/O Pins**
  - **±15kV—Human Body Model**
  - **±8kV—IEC 1000-4-2, Contact Discharge**
  - **±15kV—IEC 1000-4-2, Air-Gap Discharge**
- **Single-Supply Operation**
  - **+5V (MAX3110E)**
  - **+3.3V (MAX3111E)**
- **Low Power**
  - **600µA Supply Current**
  - **10µA Shutdown Supply Current with Receiver Interrupt Active**
- **Guaranteed 230kbps Data Rate**
- **Hardware/Software-Compatible with MAX3100 and MAX3222E**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	V_{CC} (V)
MAX3110ECWI	0°C to +70°C	28 Wide SO	5
MAX3110ECNI	0°C to +70°C	28 Plastic DIP	5

Ordering Information continued at end of data sheet.

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-1494; Rev 1; 12/05

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND (MAX3110E) .....-0.3V to +6V
V_{CC} to GND (MAX3111E).....-0.3V to +4V
V+ to GND (Note 1).....-0.3V to +7V
V- to GND (Note 1).....+0.3V to -7V
V+ to V- (Note 1).....+13V
Input Voltages to GND
  $\overline{CS}$, X1, $\overline{CTS}$, RX, DIN, SCLK..... -0.3V to (V_{CC} + 0.3V)
  T_IN, $\overline{SHDN}$ .....-0.3V to +6V
  R_IN .....±25V
Output Voltage to GND
  DOUT, $\overline{RTS}$, TX, X2 .....-0.3V to (V_{CC} + 0.3V)
  $\overline{IRQ}$ .....-0.3V to +6V
  T_OUT .....±13.2V
  R_OUT.....-0.3V to (V_{CC} + 0.3V)
TX, $\overline{RTS}$ Output Current 100mA
Short-Circuit Duration
  X2, DOUT, $\overline{IRQ}$ (to V_{CC} or GND).....Continuous
  T_OUT (to GND) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
  28-pin Wide SO (derate 12.5mW/°C above +70°C) 1W
  28-pin Plastic DIP (derate 14.3mW/°C above +70°C) 1.14W
Operating Temperature Ranges
  MAX311_EC_ _ ..... 0°C to +70°C
  MAX311_EE_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
  PDIP lead(Pb)-free.....+225°C
  PDIP containing lead(Pb).....+240°C
  Wide SO lead(Pb)-free.....+225°C
  Wide SO containing lead(Pb) .....+240°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference should not exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX3110E

(V_{CC} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured for baud rate set to 9600baud at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{CC} = +5V, T_A = +25°C)							
Supply Current	I_{CC}	$\overline{SHDN}$ = V_{CC}, no load			0.6	2	mA
Supply Current with Hardware Shutdown	$I_{CCSHDN(H)}$	$\overline{SHDN}$ = GND (Note 3)			0.48	1	mA
Supply Current with Hardware and Software Shutdown	$I_{CCSHDN(H+S)}$	$\overline{SHDN}$ = GND, SHDNi bit = 1 (Note 4)			3	20	µA
UART OSCILLATOR INPUT (X1)							
Input High Voltage	V_{IH1}			0.7V_{CC}			V
Input Low Voltage	V_{IL1}					0.2V_{CC}	V
Input Current	I_{IN1}	V_{X1} = 0 or 5.5V	SHDNi bit = 0			25	µA
			SHDNi bit = 1			2	
Input Capacitance	C_{IN1}				5		pF
UART LOGIC INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{CTS}$, RX)							
Input High Voltage	V_{IH2}			0.7V_{CC}			V
Input Low Voltage	V_{IL2}					0.3V_{CC}	V
Input Hysteresis	V_{HYST2}				250		mV
Input Leakage Current	I_{LKG1}					±1	µA
Input Capacitance	C_{IN2}				5		pF
RS-232 LOGIC INPUTS (T_IN, $\overline{SHDN}$)							
Input High Voltage	V_{IH3}	V_{CC} = 5V		2.4			
Input Low Voltage	V_{IL3}					0.8	V
Transmitter Input Hysteresis	V_{HYST3}				500		mV
Input Leakage Current	I_{IN3}				±0.01	±1	µA

ELECTRICAL CHARACTERISTICS—MAX3110E (continued)

(V_{CC} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured for baud rate set to 9600baud at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RS-232 RECEIVER INPUTS (R_IN)						
Input Voltage Range			-25		+25	V
Input High Voltage	V_{IH4}	T_A = +25°C, V_{CC} = 5V	2.4			V
Input Low Voltage	V_{IL4}	T_A = +25°C, V_{CC} = 5V			0.8	V
Input Hysteresis	V_{HYST4}			500		mV
Input Resistance	R_{IN}	T_A = +25°C	3	5	7	kΩ
RS-232 ESD PROTECTION (R_IN, T_OUT)						
ESD Protection		Human Body Model		±15		kV
		IEC 1000-4-2 Air Discharge		±15		
		IEC 1000-4-2 Contact Discharge		±8		
RS-232 RECEIVER OUTPUTS (R_OUT)						
Output High Voltage				±0.05	±10	µA
Output Low Voltage	V_{OL1}	I_{SINK} = 1.6mA			0.4	V
RS-232 TRANSMITTER OUTPUTS (T_OUT)						
Output Voltage Swing		3kΩ load on all transmitter outputs	5	±5.4		V
Output Resistance	R_O	V_{CC} = V+ = V- = 0, V_{OUT} = ±2V	300	10M		Ω
Output Short-Circuit Current					±60	mA
Output Leakage Current	I_{LKG2}	V_{CC} = 0 or 5.5V, V_{OUT} = ±12V, transmitters disabled			±25	µA
UART OUTPUTS (DOUT, TX, $\overline{RTS}$)						
Output Leakage Current	I_{LKG3}	DOUT only, $\overline{CS}$ = V_{CC}			±1	µA
Output High Voltage	V_{OH2}	I_{SOURCE} = 5mA; DOUT, $\overline{RTS}$	V_{CC} - 0.5			V
		I_{SOURCE} = 10mA; TX only	V_{CC} - 0.5			
Output Low Voltage	V_{OL2}	I_{SINK} = 4mA; DOUT, $\overline{RTS}$			0.4	V
		I_{SINK} = 25mA; TX only			0.9	
Output Capacitance	C_{OUT1}			5		pF
UART $\overline{IRQ}$ OUTPUTS ($\overline{IRQ}$ = open drain)						
Output Leakage Current	I_{LKG4}	$V_{\overline{IRQ}}$ = 5.5V			±1	µA
Output Low Voltage	V_{OL3}	I_{SINK} = 4mA			0.4	V
Output Capacitance	C_{OUT2}			5		pF
UART AC TIMING						
$\overline{CS}$ Low to DOUT Valid	t_{DV}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ High to DOUT Tri-State	t_{TR}	C_{LOAD} = 100pF, $R_{\overline{CS}}$ = 10kΩ			100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Hold Time	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 100pF			100	ns

ELECTRICAL CHARACTERISTICS—MAX3110E (continued)

(V_{CC} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured for baud rate set to 9600baud at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIN to SCLK Setup Time	t_{DS}			100			ns
DIN to SCLK Hold Time	t_{DH}			0			ns
SCLK Period	t_{CP}			238			ns
SCLK High Time	t_{CH}			100			ns
SCLK Low Time	t_{CL}			100			ns
SCLK Rising Edge to $\overline{CS}$ Falling	t_{CS0}			100			ns
$\overline{CS}$ Rising Edge to SCLK Rising Edge	t_{CS1}			200			ns
CS High Pulse Width	t_{CSW}			200			ns
Output Rise Time	t_r	TX, $\overline{RTS}$, DOUT; C_L = 100pF			10		ns
Output Fall Time	t_f	TX, $\overline{RTS}$, DOUT, $\overline{IRQ}$; C_L = 100pF			10		ns
RS-232 AC TIMING							
Maximum Data Rate		R_L = 3kΩ, C_L = 1000pF, one transmitter switching		250			kbps
Receiver Propagation Delay	t_{PHL}	Receiver input to receiver output			150		ns
	t_{PLH}	C_L = 150pF			150		
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	(Note 5)			100		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$				50		ns
Transition-Region Slew Rate		V_{CC} = 5V, R_L = 3kΩ to 7kΩ, T_A = +25°C, measured from +3V to -3V or -3V to +3V	C_L = 150pF to 1000pF	6		30	V/µs
			C_L = 150pF to 2500pF	4		30	

ELECTRICAL CHARACTERISTICS—MAX3111E

(V_{CC} = +3.0V to +3.6V, V_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured for baud rate set to 9600baud at V_{CC} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{CC} = 3.3V, T_A = +25°C)							
Supply Current	I_{CC}	$\overline{SHDN}$ = V_{CC}, no load			0.45	1.4	mA
Supply Current with Hardware Shutdown	$I_{CCSHDN(H)}$	$\overline{SHDN}$ = GND (Note 3)			0.18	0.4	mA
Supply Current with Hardware and Software Shutdown	$I_{CCSHDN(H+S)}$	$\overline{SHDN}$ = GND SHDNi bit = 1 (Note 4)			1	20	µA
UART OSCILLATOR INPUT (X1)							
Input High Voltage	V_{IH1}			0.7V_{CC}			V
Input Low Voltage	V_{IL1}					0.2V_{CC}	V
Input Current	I_{IN1}	V_{X1} = 0 or 3.6V	SHDNi bit = 0			25	µA
			SHDNi bit = 1			2	
Input Capacitance	C_{IN1}				5		pF
UART LOGIC INPUTS (DIN, SCLK, $\overline{CS}$, RX)							
Input High Voltage	V_{IH2}			0.7V_{CC}			V
Input Low Voltage	V_{IL2}					0.3V_{CC}	V
Input Hysteresis	V_{HYST2}				165		mV
Input Leakage Current	I_{LKG1}					±1	µA
Input Capacitance	C_{IN2}				5		pF
RS-232 LOGIC INPUTS (T_IN, $\overline{SHDN}$)							
Input High Voltage	V_{IH3}	V_{CC} = 3.3V		2.0			V
Input Low Voltage	V_{IL3}					0.8	V
Transmitter Input Hysteresis	V_{HYST3}				500		mV
Input Leakage Current	I_{IN3}				±0.01	±1	µA
RS-232 RECEIVER INPUTS (R_IN)							
Input Voltage Range				-25		+25	V
Input High Voltage	V_{IH4}	T_A = +25°C, V_{CC} = 3.3V		2.4			V
Input Low Voltage	V_{IL4}	T_A = +25°C, V_{CC} = 3.3V				0.6	V
Input Hysteresis	V_{HYST4}				500		mV
Input Resistance	R_{IN}	T_A = +25°C		3	5	7	kΩ
RS-232 ESD PROTECTION (R_IN, T_OUT)							
ESD Protection		Human Body Model			±15		kV
		IEC 1000-4-2 Air Discharge			±15		
		IEC 1000-4-2 Contact Discharge			±8		

ELECTRICAL CHARACTERISTICS—MAX3111E (continued)

(V_{CC} = +3.0V to +3.6V, V_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured for baud rate set to 9600baud at V_{CC} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
RS-232 RECEIVER OUTPUTS (R_OUT)						
Output High Voltage	V_{OH1}	I_{SOURCE} = 1mA	V_{CC} - 0.6			V
Output Low Voltage	V_{OL1}	I_{SINK} = 1.6mA			0.4	V
RS-232 TRANSMITTER OUTPUTS (T_OUT)						
Output Voltage Swing		3kΩ load on all transmitter outputs	±5	±5.4		V
Output Resistance	R_O	V_{CC} = V+ = V- = 0, V_{OUT} = ±2V	300	10M		Ω
Output Short-Circuit Current					±60	mA
Output Leakage Current	I_{LKG2}	V_{CC} = 0 or 3.6V, V_{OUT} = ±12V, transmitters disabled			±25	µA
UART OUTPUTS (DOUT, TX, $\overline{RTS}$)						
Output Leakage Current	I_{LKG3}	DOUT only; $\overline{CS}$ = V_{CC}			±1	µA
Output High Voltage	V_{OH2}	I_{SOURCE} = 5mA; DOUT, $\overline{RTS}$	V_{CC} - 0.5			V
		I_{SOURCE} = 10mA, TX only	V_{CC} - 0.5			
Output Low Voltage	V_{OL2}	I_{SINK} = 4mA; DOUT, $\overline{RTS}$			0.4	V
		I_{SINK} = 25mA, TX only			0.9	
Output Capacitance	C_{OUT1}			5		pF
UART $\overline{IRQ}$ OUTPUT ($\overline{IRQ}$ = open drain)						
Output Leakage Current	I_{LKG4}	$V_{\overline{IRQ}}$ = 3.6V			±1	µA
Output Low Voltage	V_{OL3}	I_{SINK} = 4mA			0.4	V
Output Capacitance	C_{OUT2}			5		pF
UART AC TIMING						
$\overline{CS}$ Low to DOUT Valid	t_{DV}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ High to DOUT Tri-State	t_{TR}	C_{LOAD} = 100pF, $R_{\overline{CS}}$ = 10kΩ			100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Hold Time	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 100pF			100	ns
DIN to SCLK Setup Time	t_{DS}		100			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Period	t_{CP}		238			ns
SCLK High Time	t_{CH}		100			ns
SCLK Low Time	t_{CL}		100			ns
SCLK Rising Edge to $\overline{CS}$ Falling	t_{CS0}		100			ns
$\overline{CS}$ Rising Edge to SCLK Rising Edge	t_{CS1}		200			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
Output Rise Time	t_r	TX, $\overline{RTS}$, DOUT; C_{LOAD} = 100pF		10		ns
Output Fall Time	t_f	TX, $\overline{RTS}$, DOUT, $\overline{IRQ}$; C_{LOAD} = 100pF		10		ns

ELECTRICAL CHARACTERISTICS—MAX3111E (continued)

(V_{CC} = +3.0V to +3.6V, V_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured for baud rate set to 9600baud at V_{CC} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 AC TIMING							
Maximum Data Rate		R_L = 3kΩ, C_L = 1000pF, one-transmitter switching		250			kbps
Receiver Propagation Delay	t_{PHL}	Receiver input to receiver output			150		ns
	t_{PLH}	C_L = 150pF			150		
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	(Note 5)			200		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$				100		ns
Transition-Region Slew Rate		V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, T_A = +25°C, measured from +3V to -3V or -3V to +3V	C_L = 150pF to 1000pF	6		30	V/µs
			C_L = 150pF to 2500pF	4		30	

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

Note 3: $I_{CCSHDN(H)}$ represents a hardware-only shutdown. In hardware shutdown, the UART is in normal operation and the charge pumps for the RS-232 transmitters are shut down.

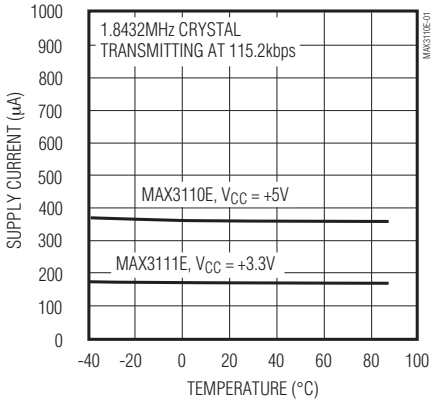
Note 4: $I_{CCSHDN(H+S)}$ represents a simultaneous software and hardware shutdown in which the UART and charge pumps are shut down.

Note 5: Transmitter skew is measured at the transmitter zero cross points.

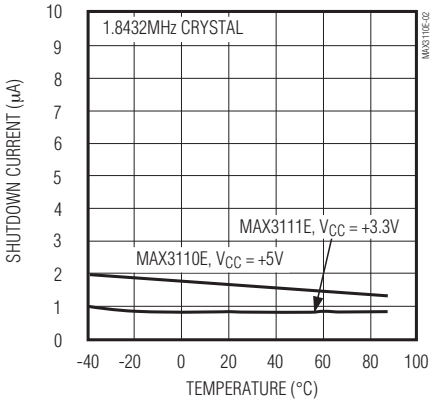
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

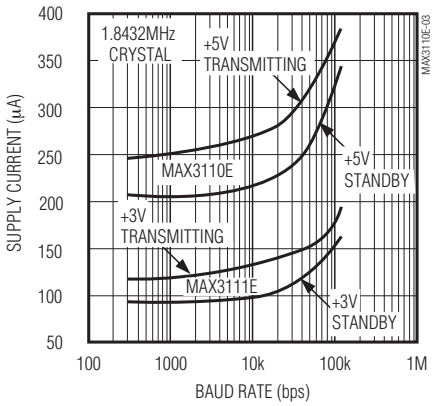
UART SUPPLY CURRENT vs. TEMPERATURE



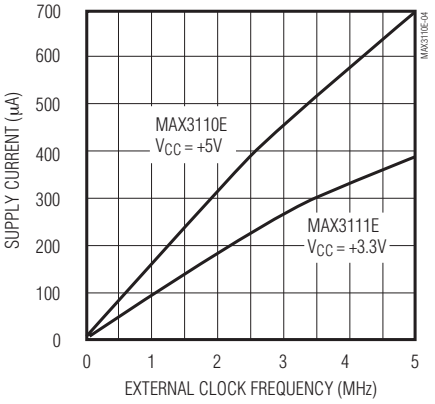
UART SHUTDOWN CURRENT vs. TEMPERATURE



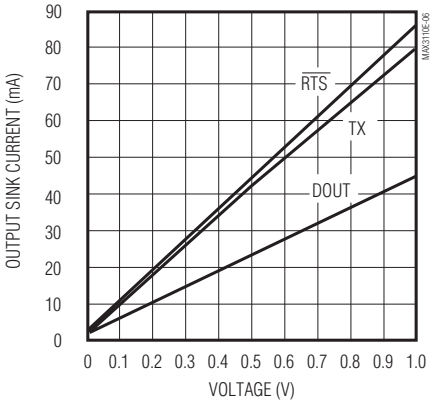
UART SUPPLY CURRENT vs. BAUD RATE



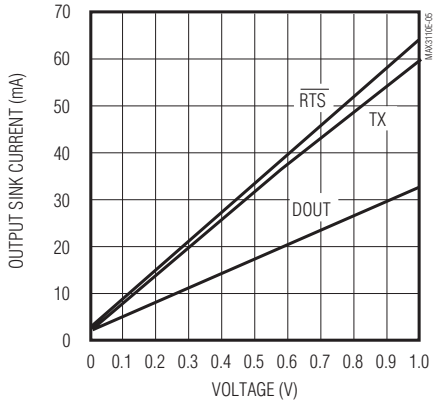
UART SUPPLY CURRENT vs. EXTERNAL CLOCK FREQUENCY



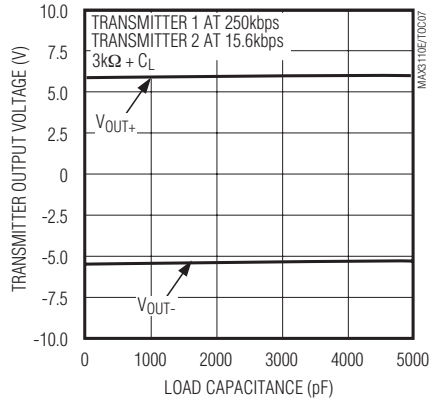
MAX3110E TX, $\overline{RTS}$, DOUT OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE (V_{CC} = +5V)



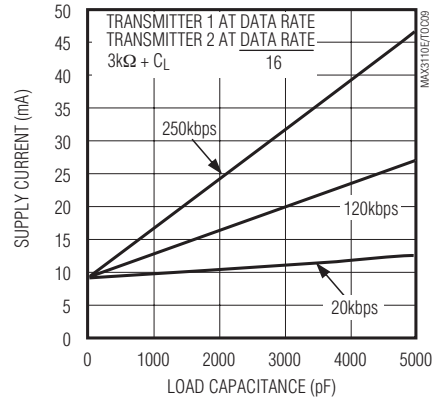
MAX3111E TX, $\overline{RTS}$, DOUT OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE (V_{CC} = +3.3V)



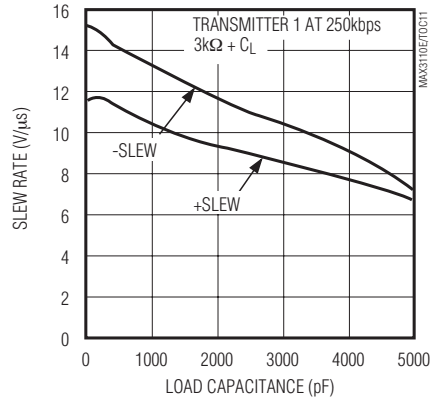
RS-232 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



RS-232 TRANSCEIVER SUPPLY CURRENT vs. LOAD CAPACITANCE



RS-232 TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	R2IN	RS-232 Receiver Input 2
2	R2OUT	RS-232 Receiver Output 2, TTL/CMOS
3	T2IN	RS-232 Transmitter Input 2, TTL/CMOS
4	T1IN	RS-232 Transmitter Input 1, TTL/CMOS
5	R1OUT	RS-232 Receiver Output 1, TTL/CMOS
6	R1IN	RS-232 Receiver Input 1
7	T1OUT	RS-232 Transmitter Output 1
8	V_{CC}	Positive Supply Voltage
9	X2	UART Crystal Connection. Leave X2 unconnected when using an external CMOS clock. See the *Crystals, Oscillators, and Ceramic Resonators* section.
10	X1	UART Crystal Connection. X1 also serves as an external CMOS clock input. See the *Crystals, Oscillators, and Ceramic Resonators* section.
11	$\overline{CTS}$	UART Clear-to-Send Active-Low Input. Read via the CTS bit.
12	$\overline{RTS}$	UART Request-to-Send Active-Low Output. Controlled by the RTS bit. Also used to control the driver enable in RS-485 networks.
13	RX	UART Asynchronous Serial-Data (receiver) Input. The serial information received from the RS-232 receiver. A transition on RX while in shutdown generates an interrupt (Table 1).
14	TX	UART Asynchronous Serial-Data (transmitter) Output
15	DIN	SPI/MICROWIRE Serial-Data Input. Schmitt-trigger Input.
16	DOUT	SPI/MICROWIRE Serial-Data Output. High impedance when $\overline{CS}$ is high.
17	SCLK	SPI/MICROWIRE Serial-Clock Input. Schmitt-trigger input.
18	$\overline{CS}$	UART Active-Low Chip-Select Input. DOUT goes high impedance when $\overline{CS}$ is high. $\overline{IRQ}$, TX, and $\overline{RTS}$ are always active. Schmitt-trigger input.
19	$\overline{IRQ}$	UART Active-Low Interrupt Output. Open-drain interrupt output to microprocessor.
20	$\overline{SHDN}$	Hardware Shutdown Input. Drive $\overline{SHDN}$ low to shut down the RS-232 transmitters and charge pump. Drive high for normal operation.
21	V+	+5.5V generated by the internal charge pump. **Do not make any connection to this terminal.**
22	C1+	Positive terminal of the internal voltage-doubler charge-pump capacitor. **Do not make any connection to this terminal.**
23	C1-	Negative terminal of the internal voltage-doubler charge-pump capacitor. **Do not make any connection to this terminal.**
24	C2+	Positive terminal of internal inverting charge-pump capacitor. **Do not make any connection to this terminal.**
25	C2-	Negative terminal of internal inverting charge-pump capacitor. **Do not make any connection to this terminal.**
26	V-	-5.5V generated by the internal charge pump. **Do not make any connection to this terminal.**
27	GND	Ground
28	T2OUT	RS-232 Transmitter Output 2

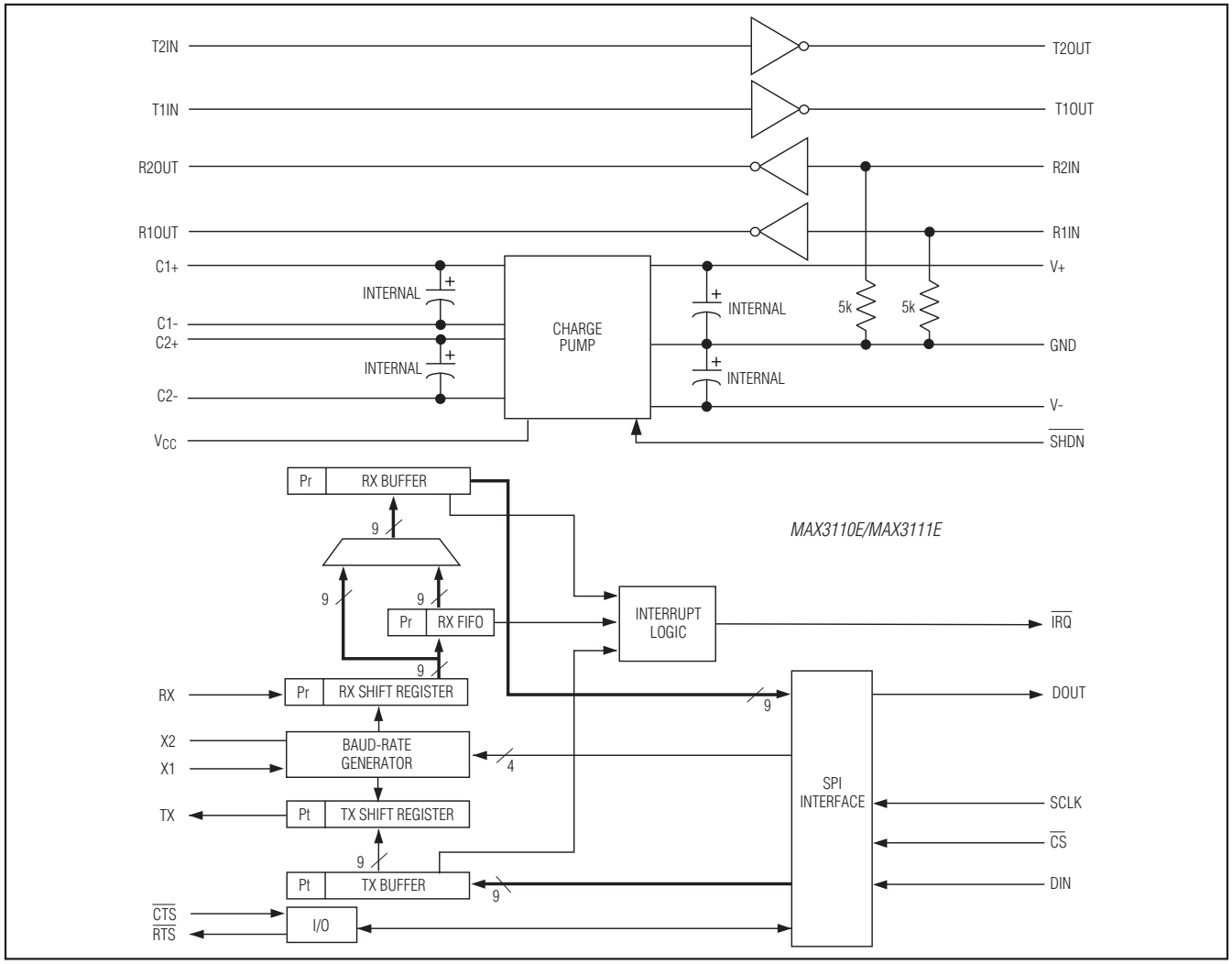


Figure 1. MAX3110E/MAX3111E Functional Diagram

Detailed Description

The MAX3110E/MAX3111E contain an SPI/QSPI/MICROWIRE-compatible UART and an RS-232 transceiver with two drivers and two receivers. The UART is compatible with SPI and QSPI for CPOL = 0 and CPHA = 0. The UART supports data rates up to 230kbaud for standard UART bit streams as well as IrDA and includes an 8-word receive FIFO. Also included is a 9-bit-address recognition interrupt.

The RS-232 transceiver has electrostatic discharge (ESD) protection on the transmitter outputs and the receiver inputs. The internal charge-pump capacitors minimize the number of external components required. The RS-232 transceivers meet EIA/TIA-232 specifications for V_{CC} down to the minimum supply voltage and are guaranteed to operate for data rates up to 250kbps.

The UART and RS-232 functions operate as one device or independently since the two functions share only supply and ground connections.

UART

The universal asynchronous receiver transmitter (UART) interfaces the SPI/QSPI/MICROWIRE-compatible synchronous serial data from a microprocessor (µP) to asynchronous, serial-data communication ports (RS-232, IrDA). Figure 1 shows the MAX3110E/MAX3111E functional diagram. Included in the UART function is an SPI/QSPI/MICROWIRE interface, a baud-rate generator, and an interrupt generator.

SPI Interface

The MAX3110E/MAX3111E are compatible with SPI, QSPI (CPOL = 0, CPHA = 0), and MICROWIRE serial-interface standards (Figure 2). The MAX3110E/MAX3111E have a unique full-duplex-only architecture that expects a 16-bit word for DIN and simultaneously produces a 16-bit word for DOUT regardless of which read/write register is used. The DIN stream is monitored for its first two bits to tell the UART the type of data transfer being executed (see the *Write Configuration Register*, *Read Configuration Register*, *Write Data Register*, and *Read Data Register* sections). DIN (MOSI) is latched on SCLK's rising edge. DOUT (MISO) should be read into the µP on SCLK's rising edge. The first bit (bit 15) of DOUT transitions on $\overline{CS}$'s falling edge, and bits 14–0 transition on SCLK's falling edge. Figure 3 shows the detailed serial timing specifications for the synchronous SPI port.

Only 16-bit words are expected. If $\overline{CS}$ goes high in the middle of a transmission (any time before the 16th bit), the sequence is aborted (i.e., data does not get written to individual registers). Most operations, such as the clearing of internal registers, are executed only on $\overline{CS}$'s rising edge. Every time $\overline{CS}$ goes low, a new 16-bit stream is expected. An example of using the Write Configuration Register is shown in Figure 4.

Table 1 describes the bits located in the Write Configuration, Read Configuration, Write Data, and Read Data Registers. This table also describes whether the bit is a read or a write bit and the power-on reset state (POR) of the bits. Figure 5 shows an example of parity and word-length control.

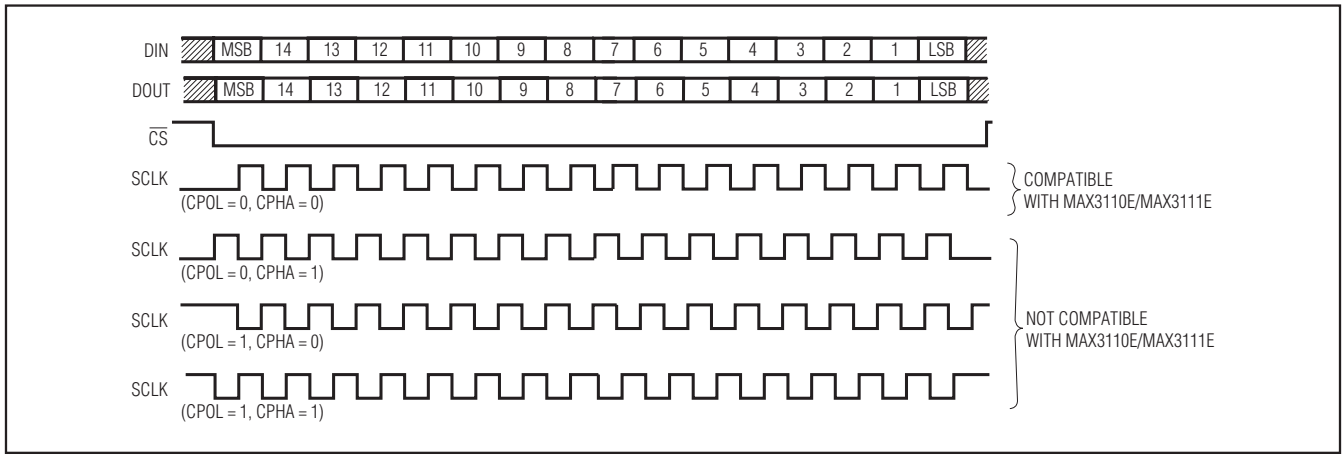


Figure 2. Compatible CPOL and CPHA Timing Modes

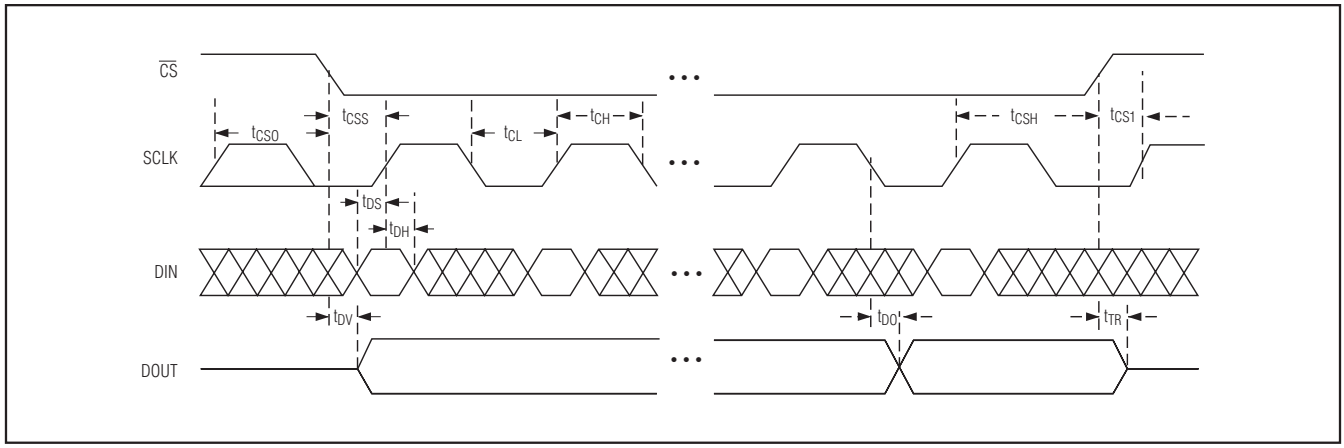


Figure 3. Detailed Serial Timing Specifications for the Synchronous SPI Port

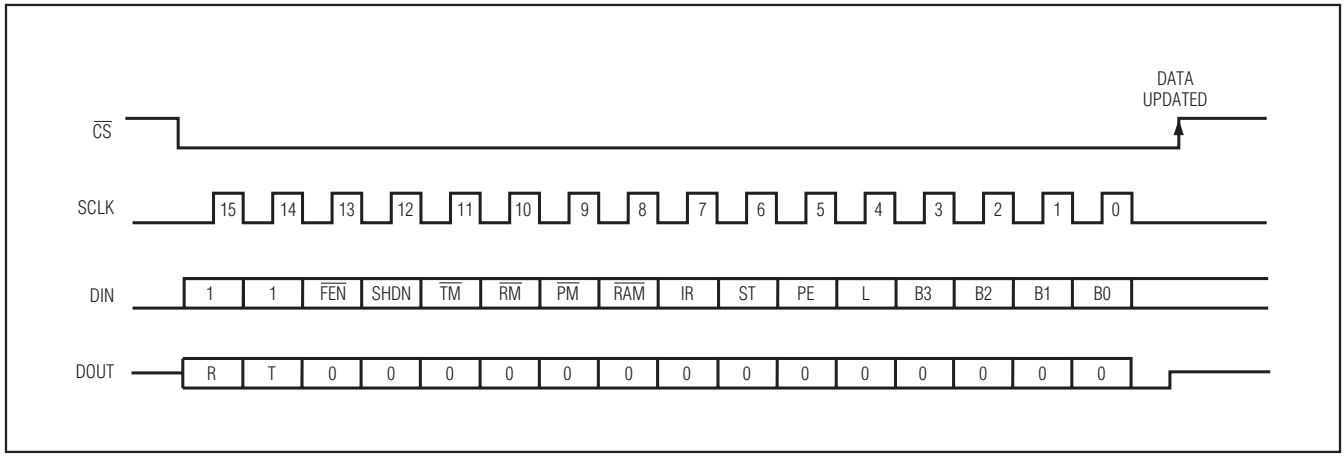


Figure 4. Write Configuration Register Example

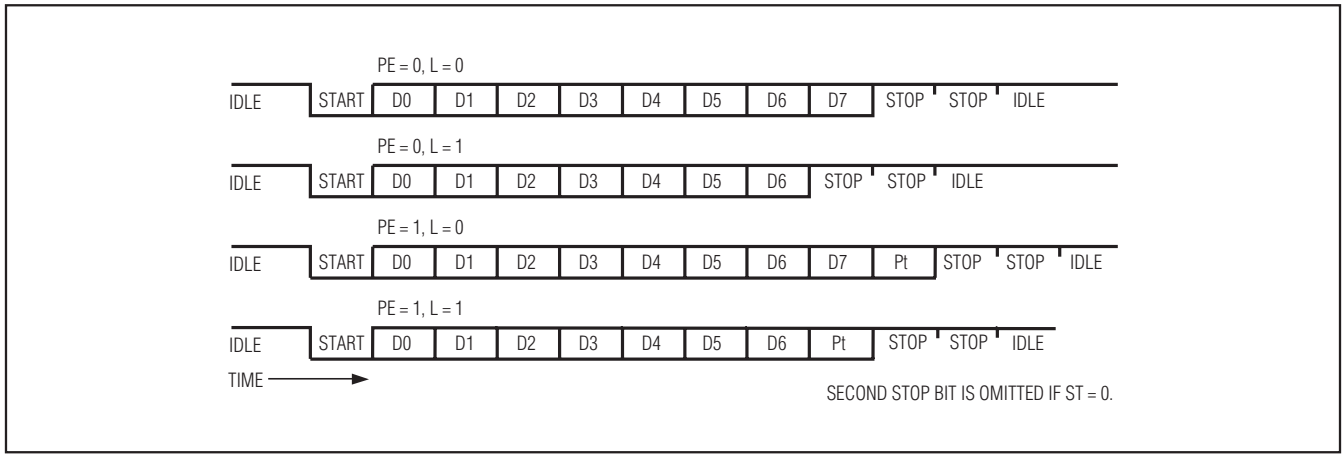


Figure 5. Parity and Word-Length Control

Table 1. Bit Descriptions

BIT NAME	BIT TYPE	POR STATE	DESCRIPTION
B0–B3	write	0000	Baud-Rate Divisor Select Bits. Sets the baud clock's value (Table 6).
B0–B3	read	0000	Baud-Rate Divisor Select Bits. Reads the 4-bit baud clock value assigned to these registers.
CTS	read	No change	Clear-to-Send-Input. Records the state of the $\overline{CTS}$ pin (CTS bit = 0 implies $\overline{CTS}$ pin = logic high).
D0t–D7t	write	XXXXXXXX	Transmit-Buffer Register. Eight data bits written into the transmit-buffer register. D7t is ignored when L = 1.
D0r–D7r	read	00000000	Eight data bits read from the receive FIFO or the receive-buffer register. When L = 1, D7r is always 0.
$\overline{FEN}$	write	0	FIFO Enable. Enables the receive FIFO when $\overline{FEN}$ = 0. When $\overline{FEN}$ = 1, FIFO is disabled.
$\overline{FEN}$	read	0	FIFO-Enable Readback. $\overline{FEN}$'s state is read.
IR	write	0	Enables the IrDA timing mode when IR = 1.
IR	read	0	Reads the value of the IR bit.
L	write	0	Bit to set the word length of the transmitted or received data. L = 0 results in 8-bit words (9-bit words if PE = 1) (see Figure 5). L = 1 results in 7-bit words (8-bit words if PE = 1).
L	read	0	Reads the value of the L bit.
Pt	write	X	Transmit-Parity Bit. This bit is treated as an extra bit that is transmitted if PE = 1. In 9-bit networks, the MAX3110E/MAX3111E do not calculate parity. If PE = 0, then this bit (Pt) is ignored in transmit mode (see the *9-Bit Networks* section).
Pr	read	X	Receive-Parity Bit. This bit is the extra bit received if PE = 1. Therefore, PE = 1 results in 9-bit transmissions (L = 0). If PE = 0, then Pr is set to 0. Pr is stored in the FIFO with the receive data (see the *9-Bit Networks* section).
PE	write	0	Parity-Enable Bit. Appends the Pt bit to the transmitted data when PE = 1, and sends the Pt bit as written. No parity bit is transmitted when PE = 0. With PE = 1, an extra bit is expected to be received. This data is put into the Pr register. Pr = 0 when PE = 0. The MAX3110E/MAX3111E do not calculate parity.
PE	read	0	Reads the value of the Parity-Enable bit.
$\overline{PM}$	write	0	Mask for Pr bit. $\overline{IRQ}$ is asserted if $\overline{PM}$ = 1 and Pr = 1 (Table 7).
$\overline{PM}$	read	0	Reads the value of the $\overline{PM}$ bit (Table 7).
R	read	0	Receive Bit or FIFO Not Empty Flag. R = 1 means new data is available to be read or is being read from the receive register or FIFO. If performing a Read Data or Write Data operation, the R bit will clear on the falling edge of SCLK's 16th pulse if no new data is available.
$\overline{RM}$	write	0	Mask for R bit. $\overline{IRQ}$ is asserted if $\overline{RM}$ = 1 and R = 1 (Table 7).
$\overline{RM}$	read	0	Reads the value of the $\overline{RM}$ bit (Table 7).
$\overline{RAM}$	write	0	Mask for RA/FE bit. $\overline{IRQ}$ is asserted if $\overline{RAM}$ = 1 and RA/FE = 1 (Table 7).
$\overline{RAM}$	read	0	Reads the value of the $\overline{RAM}$ bit (Table 7).
RTS	write	0	Request-to-Send Bit. Controls the state of the $\overline{RTS}$ output. This bit is reset on power-up (RTS bit = 0 sets the $\overline{RTS}$ pin = logic high).

Table 1. Bit Descriptions (continued)

BIT NAME	BIT TYPE	POR STATE	DESCRIPTION
RA/FE	read	0	Receiver-Activity/Framing-Error Bit. In shutdown mode, this is the RA bit. In normal operation, this is the FE bit. In shutdown mode, a transition on RX sets RA = 1. In normal mode, a framing error sets FE = 1. A framing error occurs if a zero is received when the first stop bit is expected. FE is set when a framing error occurs, and cleared upon receipt of the next properly framed character independent of the FIFO being enabled. When the device wakes up, it is likely that a framing error will occur. This error is cleared with a Write Configuration. The FE bit is not cleared on a Read Data operation. When an FE is encountered, the UART resets itself to the state where it is looking for a start bit.
SHDNi	write	0	Software-Shutdown Bit. Enter software shutdown with a Write Configuration where SHDNi = 1. Software shutdown takes effect after $\overline{CS}$ goes high, and causes the oscillator to stop as soon as the transmitter becomes idle. Software shutdown also clears R, T, RA/FE, D0r–D7r, D0t–D7t, Pr, Pt, and all data in the receive FIFO. RTS and CTS can be read and updated while in shutdown. Exit software shutdown with a Write Configuration where SHDNi = 0. The oscillator restarts typically within 50ms of $\overline{CS}$ going high. RTS and CTS are unaffected. Refer to the *Pin Description* for hardware shutdown ($\overline{SHDN}$ input).
SHDNo	read	0	Shutdown Read-Back Bit. The Read Configuration register outputs SHDNo = 1 when the UART is in shutdown. Note that this bit is not sent until the current byte in the transmitter is sent (T = 1). This tells the processor when it may shut down the RS-485/RS-422 driver. This bit is also set immediately when the device is shut down through the $\overline{SHDN}$ pin.
ST	write	0	Transmit-Stop Bit. One stop bit will be transmitted when ST = 0. Two stop bits will be transmitted when ST = 1. The receiver only requires one stop bit.
ST	read	0	Reads the value of the ST bit.
T	read	1	Transmit-Buffer-Empty Flag. T = 1 means that the transmit buffer is empty and ready to accept another data word.
$\overline{TE}$	write	0	Transmit-Enable Bit. If $\overline{TE}$ = 1, then only the $\overline{RTS}$ pin is updated on $\overline{CS}$'s rising edge. The contents of $\overline{RTS}$, Pt, and D0t–D7t transmit on $\overline{CS}$'s rising edge when $\overline{TE}$ = 0.
$\overline{TM}$	write	0	Mask for T Bit. $\overline{IRQ}$ is asserted if $\overline{TM}$ = 1 and T = 1 (Table 7).
$\overline{TM}$	read	0	Reads the value of the $\overline{TM}$ bit (Table 7).

Notice to High-Level Programmers: The UART follows the SPI convention of providing a bidirectional data path for writes and reads. Whenever the data is written, data is also read back. This speeds operation over the SPI bus, and the UART needs this speed advantage when operating at high baud rates. In most high-level languages, such as C, there are commands for writing and reading stream I/O devices such as the console or serial port. In C specifically, there is a "PUTCHAR" command that transmits a character and a "GETCHAR" command that receives a character. If programmers were to write direct write and read commands in C with no underlying driver code, they would notice that a PUTCHAR command is really a PUTGETCHAR command. These C commands assume some form of BIOS-level support for these commands. The proper way to implement these commands is to write driver code, usually in the form of an assembly-language interrupt-service routine and a callable routine used by high-level routines. This driver handles the interrupts and manages the receive and transmit buffers for the MAX3110E/MAX3111E. When a PUTCHAR executes, this driver is called and it safely buffers any characters received when the current character is transmitted. When a GETCHAR executes, it checks its own receive buffer before getting data from the UART. See the C-language *Outline for a MAX3110E/MAX3111E Software Driver* in Listing 1, which appears at the end of this data sheet.

Listing 1 is a C-language outline of an interrupt-driven software driver that interfaces to a MAX3110E/MAX3111E, providing an intermediate layer between the bit-manipulation subroutine and the familiar PUTCHAR/GETCHAR subroutines.

The user must supply code for managing the transmit and receive queues as well as the low-level hardware interface itself. The interrupt control hardware must be initialized before this driver is called.

Write Configuration Register (D15, D14 = 1, 1)

Configure the UART by writing a 16-bit word to the write configuration register, which programs the baud rate, data word length, parity enable, and enable of the 8-word receive FIFO. In this mode, bits 15 and 14 of the DIN configuration word are both required to be 1 in order to enable the write configuration mode. Bits 13–0 of the DIN configuration word set the configuration of the UART. Table 2 shows the bit assignment for the write configuration register. The write configuration register allows selection between normal UART timing and IrDA timing, provides shutdown control, and contains four interrupt mask bits.

Using the write configuration register clears the receive FIFO and the R, T, RA/FE, D0r–D7r, D0t–D7t, Pr, and Pt registers. RTS and CTS remain unchanged. The new configuration is valid on $\overline{CS}$'s rising edge if the transmit buffer is empty (T = 1) and transmission is over. If the latest transmission has not been completed (T = 0), the registers are updated when the transmission is over.

The write configuration register bits ($\overline{FEN}$, SHDNi, IR, ST, PE, L, B3–B0) take effect after the current transmission is over. The mask bits ($\overline{TM}$, $\overline{RM}$, $\overline{PM}$, $\overline{RAM}$) take effect immediately after SCLK's 16th rising edge.

Bits 15 and 14 of the DOUT write configuration (R and T) are sent out of the MAX3110E/MAX3111E along with 14 trailing zeros. The use of the R and T bits is optional, but ignore the 14 trailing zeros.

Warning! The UART requires stable crystal oscillator operation before configuration (typically ~25ms after power-up). Upon power-up, compare the write configuration bits with the read configuration bits in a software loop until both match. This ensures that the oscillator is stable and that the UART is configured correctly.

Read Configuration Register (D15, D14 = 0, 1)

The read configuration register is used to read back the last configuration written to the UART. In this register, bits 15 and 14 of the DIN configuration word are required to be 0 and 1, respectively, to enable the read configuration mode. Bits 13–1 of the DIN word should be zeros, and bit 0 is the test bit to put the UART in test mode (see the *Test Mode* section). Table 3 shows the bit assignment for the read configuration register.

Test Mode

The device enters a test mode if bit 0 of the DIN configuration word equals one when doing a read configuration. In this mode, if $\overline{CS}$ = 0, the $\overline{RTS}$ pin transmits a clock that is 16-times the baud rate. The TX pin is low as long as $\overline{CS}$ remains low while in test mode. Table 3 shows the bit assignment for the read configuration register.

Write Data Register (D15, D14 = 1, 0)

Use the write data register for transmitting to the TX-buffer and receiving from the RX buffer (and RX FIFO when enabled). When using this register, the DIN and DOUT write data words are used simultaneously, and bits 13–11 for both the DIN and DOUT write data words are meaningless zeros. The DIN write data word contains the data that is being transmitted, and the DOUT write data word contains the data that is being received from the RX FIFO. Table 4 shows the bit assignment for the write data mode. To change the $\overline{RTS}$ pin's output state without transmitting data, set the $\overline{TE}$ bit high. If performing a write data operation, the R bit will clear on the falling edge of SCLK's 16th clock pulse if no new data is available.

Read Data Register (D15, D14 = 0, 0)

Use the read data register for receiving data from the RX FIFO. When using this register, bits 15 and 14 of DIN are both required to be 0. Bits 13–0 of the DIN read-data word should be zeros. Table 5 shows the bit assignments for the read data mode. Reading data clears the R bit and interrupt $\overline{IRQ}$. If performing a read data operation, the R bit will clear on the falling edge of SCLKs 16th clock pulse if no new data is available.

Table 2. Write Configuration (D15, D14 = 1, 1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	1	1	$\overline{FEN}$	SHDNi	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR	ST	PE	L	B3	B2	B1	B0
DOUT	R	T	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D15 is present at DOUT on $\overline{CS}$'s falling edge. Consecutive bits are clocked out on SCLK's falling edge.

Notes:

bit 15: DOUT

R = 1, Data is available to be read or is being read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bits 13–0: DOUT

Zeros

bits 15, 14: DIN

1,1 = Write Configuration

bit 13: DIN

$\overline{FEN}$ = 0, FIFO is enabled.

$\overline{FEN}$ = 1, FIFO is disabled.

bit 12: DIN

SHDNi = 1, Enter software shutdown.

SHDNi = 0, Exit software shutdown.

bit 11: DIN

$\overline{TM}$ = 1, Transmit buffer empty interrupt is enabled.

$\overline{TM}$ = 0, Transmit buffer empty interrupt is disabled.

bit 10: DIN

$\overline{RM}$ = 1, Data available in the receive register or FIFO interrupt is enabled.

$\overline{RM}$ = 0, Data available in the receive register or FIFO interrupt is disabled.

bit 9: DIN

$\overline{PM}$ = 1, Parity bit high received interrupt is enabled.

$\overline{PM}$ = 0, Parity bit received interrupt is disabled.

bit 8: DIN

$\overline{RAM}$ = 1, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is enabled.

$\overline{RAM}$ = 0, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is disabled.

bit 7: DIN

IR = 1, IrDA mode is enabled.

IR = 0, IrDA mode is disabled.

bit 6: DIN

ST = 1, Transmit two stop-bits.

ST = 0, Transmit one stop-bit.

bit 5: DIN

PE = 1, Parity is enabled for both transmit (state of Pt) and receive.

PE = 0, Parity is disabled for both transmit and receive.

bit 4: DIN

L = 1, 7-bit words (8-bit words if PE = 1)

L = 0, 8-bit words (9-bit words if PE = 1)

bits 3–0: DIN

B3–B0 = XXXX, Baud-Rate Divisor Select Bits (see Table 6)

Table 3. Read Configuration (D15, D14 = 0, 1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST
DOUT	R	T	$\overline{FEN}$	SHDNo	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR	ST	PE	L	B3	B2	B1	B0

D15 is present at DOUT on $\overline{CS}$'s falling edge. Consecutive bits are clocked out on SCLK's falling edge.

Notes:

bit 15: DOUT

R = 1, Data is available to be read or is being read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bit 13: DOUT

$\overline{FEN}$ = 0, FIFO is enabled.

$\overline{FEN}$ = 1, FIFO is disabled.

bit 12: DOUT

SHDNo = 1, Software shutdown is enabled.

SHDNo = 0, Software shutdown is disabled.

bit 11: DOUT

$\overline{TM}$ = 1, Transmit buffer empty interrupt is enabled.

$\overline{TM}$ = 0, Transmit buffer empty interrupt is disabled.

bit 10: DOUT

$\overline{RM}$ = 1, Data available in the receive register or FIFO interrupt is enabled.

$\overline{RM}$ = 0, Data available in the receive register or FIFO interrupt is disabled.

bit 9: DOUT

$\overline{PM}$ = 1, Parity bit high received interrupt is enabled.

$\overline{PM}$ = 0, Parity bit received interrupt is disabled.

bit 8: DOUT

$\overline{RAM}$ = 1, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is enabled.

$\overline{RAM}$ = 0, Receiver-activity (shutdown mode)/Framing-error (normal operation) interrupt is disabled.

bit 7: DOUT

IR = 1, IrDA mode is enabled.

IR = 0, IrDA mode is disabled.

bit 6: DOUT

ST = 1, Transmit two stop-bits.

ST = 0, Transmit one stop-bit.

bit 5: DOUT

PE = 1, Parity is enabled for both transmit (state of Pt) and receive.

PE = 0, Parity is disabled for both transmit and receive.

bit 4: DOUT

L = 1, 7-bit words (8-bit words if PE = 1)

L = 0, 8-bit words (9-bit words if PE = 1)

bits 3–0: DOUT

B3–B0 = XXXX Baud-Rate Divisor Select Bits (see Table 6)

bit 15, 14: DIN

0,1 = Read Configuration

bits 13–1: DIN

Zeros

bit 0: DIN

If TEST = 1 and $\overline{CS}$ = 0, then $\overline{RTS}$ =16xBaudCLK

TEST = 0, Disables test mode

Table 4. Write Data (D15, D14 = 1, 0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	1	0	0	0	0	$\overline{TE}$	RTS	Pt	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
DOUT	R	T	0	0	0	RA/FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

D15 is present at DOUT on $\overline{CS}$'s falling edge. Consecutive bits are clocked out on SCLK's falling edge.

Notes:

bit 15: DOUT

R = 1, Data is available to be read or is being read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bits 13–11: DOUT

Zeros

bit 10: DOUT

RA/FE = Receive-Activity (UART shutdown)/Framing-Error (Normal Operation) bit

bit 9: DOUT

CTS = $\overline{CTS}$ input state. If CTS = 0, then $\overline{CTS}$ = 1 and vice versa.

bit 8: DOUT

Pr = Received Parity Bit. This is only valid if PE = 1.

bits 7–0: DOUT

D7r–D0r = Received Data Bits. D7r = 0 for L = 1.

bits 15, 14: DIN

1, 0 = Write Data

bits 13–11: DIN

Zeros

bit 10: DIN

$\overline{TE}$ = 1, Disables transmit and only $\overline{RTS}$ will be updated.

$\overline{TE}$ = 0, Enables transmit.

bit 9: DIN

RTS = 1, Configures $\overline{RTS}$ = 0 (logic low).

RTS = 0, Configures $\overline{RTS}$ = 1 (logic high).

bit 8: DIN

Pt = 1, Transmit parity bit is high. If PE = 1, a high parity bit will be transmitted. If PE = 0, then no parity bit will be transmitted.

Pt = 0, Transmit parity bit is low. If PE = 1, a low parity bit will be transmitted. If PE = 0, then no parity bit will be transmitted.

bits 7–0: DIN

D7t–D0t = Transmitting Data Bits. D7t is ignored when L = 1.

Table 5. Read Data (D15, D14 = 0, 0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DOUT	R	T	0	0	0	RA/FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

D15 is present at DOUT on $\overline{CS}$'s falling edge. Consecutive bits are clocked out on SCLK's falling edge.

Notes:

bits 15: DOUT

R = 1, Data is available to be read or is being read from the receive register or FIFO.

R = 0, Receive register and FIFO are empty.

bit 14: DOUT

T = 1, Transmit buffer is empty.

T = 0, Transmit buffer is full.

bits 13–11: DOUT

Zeros

bit 10: DOUT

RA/FE = Receive-Activity (UART shutdown)/Framing-Error (Normal Operation) Bit

bit 9: DOUT

CTS = $\overline{CTS}$ input state. If CTS = 0, then $\overline{CTS}$ = 1 and vice versa.

bit 8: DOUT

Pr = Received parity bit. This is only valid if PE = 1.

bits 7–0: DOUT

D7r–D0r = Received Data Bits. D7r = 0 for L = 1.

bits 15, 14: DIN

0, 0 = Read Data

bits 13–0: DIN

Zeros

Baud-Rate Generator

The baud-rate generator determines the rate at which the transmitter and receiver operate. Bits B3–B0 in the write configuration register determine the baud-rate divisor (BRD), which divides the X1 oscillator frequency. The on-board oscillator operates with either a 1.8432MHz or a 3.6864MHz crystal or is driven at X1 with a 45% to 55% duty-cycle square wave. Table 6 shows baud-rate divisors for given input codes as well as the baud rate for 1.8432MHz and 3.684MHz crystals. The generator's clock is 16-times the baud rate.

Interrupt Sources and Masks

Using the Read Data or Write Data register clears the interrupt $\overline{IRQ}$, assuming the conditions that initiated the interrupt no longer exist. Table 7 gives the details for each interrupt source. Figure 6 shows the functional diagram for the interrupt sources and mask blocks.

Following are two examples of setting up an IRQ for the MAX3110E/MAX3111E:

Example 1. Set up only the transmit buffer-empty interrupt. Send the 16-bit word below into DIN of the MAX3110E/MAX3111E using the Write Configuration register. This 16-bit word configures the MAX3110E/MAX3111E for 9600bps, 8-bit words, no parity, and one stop bit with a 1.8432MHz crystal.

binary 1100100000001010

HEX C80A

Example 2. Set up only the data-available (or data-being-read) interrupt.

Send the 16-bit word below into DIN of the MAX3110E/MAX3111E using the Write Configuration register. This 16-bit word configures the MAX3110E/MAX3111E for 9600bps, 8-bit words, no parity, and one stop bit with a 1.8432MHz crystal.

binary 1100010000001010

HEX C40A

Receive FIFO

The MAX3110E/MAX3111E contain an 8-word receive FIFO for data received by the UART to minimize processor overhead. Using the UART-software shutdown clears the receive FIFO. Upon power-up, the receive FIFO is enabled. To disable the receive FIFO, set the $\overline{FEN}$ bit high when writing to the Write Configuration register. To check whether the FIFO is enabled or disabled, read back the $\overline{FEN}$ bit using the Read Configuration.

Table 6. Baud-Rate Selection*

BAUD B3	B2	B1	B0	DIVISION RATIO	BAUD RATE (f_{OSC} = 1.8432MHz)	BAUD RATE (f_{OSC} = 3.6864MHz)
0	0	0	0**	1	**115.2k****	**230.4k****
0	0	0	1	2	**57.6k**	**115.2k**
0	0	1	0	4	28.8k	**57.6k**
0	0	1	1	8	14.4k	28.8k
0	1	0	0	16	7200	14.4k
0	1	0	1	32	3600	7200
0	1	1	0	64	1800	3600
0	1	1	1	128	900	1800
1	0	0	0	3	**38.4k**	76.8k
1	0	0	1	6	**19.2k**	**38.4k**
1	0	1	0	12	**9600**	**19.2k**
1	0	1	1	24	**4800**	**9600**
1	1	0	0	48	**2400**	**4800**
1	1	0	1	96	**1200**	**2400**
1	1	1	0	192	**600**	**1200**
1	1	1	1	384	**300**	**600**

**Standard baud rates shown in bold*
***Default baud rate*

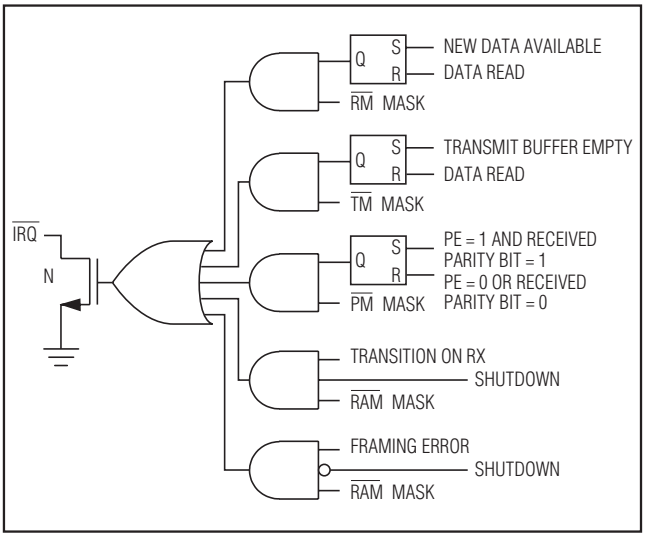


Figure 6. Functional Diagram for Interrupt Sources and Mask Blocks

Table 7. Interrupt Sources and Masks—Bit Descriptions

BIT NAME	MASK BIT	MEANING WHEN SET	DESCRIPTION
Pr	$\overline{PM}$	Received parity bit = 1	The Pr bit reflects the value in the word currently in the receive-buffer register (oldest data available). The Pr bit is set when parity is enabled (PE = 1) and the received parity bit is 1. The Pr bit is cleared either when parity is not enabled (PE = 0) or when parity is enabled and the received bit is 0. An interrupt is issued based on the oldest Pr value in the receiver FIFO. The oldest Pr value is the next value read by a Read Data operation.
R	$\overline{RM}$	Data available	The R bit is set when new data is available to be read or when data is being read from the receive register/FIFO. FIFO is cleared when all data has been read. An interrupt is asserted as long as R = 1 and $\overline{RM}$ = 1.
RA/FE	$\overline{RAM}$	Transition on RX when in shutdown; framing error when not in shutdown	This is the RA (RX-transition) bit in shutdown, and the framing-error (FE) bit in operating mode. RA is set if there has been a transition on RX since entering shutdown. RA is cleared when the MAX3110E/MAX3111E exits shutdown. $\overline{IRQ}$ is asserted when RA is set and $\overline{RAM}$ = 1. FE is determined solely by the currently received data and is not stored in FIFO. The FE bit is set if a zero is received when the first stop bit is expected. FE is cleared upon receipt of the next properly framed character. $\overline{IRQ}$ is asserted when FE is set and $\overline{RAM}$ = 1.
T	$\overline{TM}$	Transmit buffer is empty	The T bit is set when the transmit buffer is ready to accept data. $\overline{IRQ}$ is asserted low if $\overline{TM}$ = 1 and the transmit buffer becomes empty. This source is cleared on the rising edge of SCLK's 16th clock pulse when using a Read Data or Write Data operation. $\overline{CS}$'s rising edge during a Read Data operation. Although the interrupt is cleared, poll T to determine transmit-buffer status.

UART Software Shutdown

When in software shutdown, the UART's oscillator turns off to reduce power dissipation. The UART enters shutdown by a software command (SHDNi bit = 1). The software shutdown is entered upon completing the transmission of the data in both the Transmit register and the Transmit-Buffer register. The SHDNo bit is set when the UART enters shutdown. The microcontroller (µC) monitors the SHDNo bit to determine when the UART is shut down and then shuts down the RS-232 transceivers.

Software shutdown clears the receive FIFO, R, RA/FE, D0r–D7r, Pr, and Pt registers and sets the T bit high. Configuration bits ($\overline{RM}$, $\overline{TM}$, $\overline{PM}$, $\overline{RAM}$, IR, ST, PE, L, B0–B3, and RTS) are programmable when SHDNo = 1 and CTS is also readable. Although RA is reset upon entering shutdown, it goes high when any transitions are detected on the RX pin. This allows the UART to monitor activity on the receiver when in shutdown.

When taking the part out of software shutdown (SHDNi = 0), the oscillator turns on when $\overline{CS}$ goes high. After $\overline{CS}$ goes high, the oscillator typically takes about 25ms to stabilize. Configure the UART after the oscillator has stabilized by using a write configuration that clears all registers but RTS and CTS. If a framing error occurs, you may have not waited long enough for the oscillator to stabilize.

The hardware shutdown affects only the RS-232 transceiver, and the software shutdown affects only the UART. See the *RS-232 Transceiver Hardware Shutdown* section.

Dual Charge-Pump Voltage Converter

The internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump), using a +3.3V supply (MAX3111E) or a +5V supply (MAX3110E). The charge pump operates in discontinuous mode; if the output voltages are less than 5.5V, the charge pump is enabled, and if the output voltages exceed 5.5V, the charge pump is disabled. Each charge pump includes internal flying capacitors and reservoir capacitors to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting-level translators that convert CMOS-logic levels to ±5.0V EIA/TIA-232 levels. The transmitters guarantee a 230kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Transmitters can be paralleled because the outputs are forced into a high-impedance state when the device is in hardware shutdown ($\overline{SHDN}$ = GND). The MAX3110E/MAX3111E permit the outputs to be driven up to ±12V while in shutdown. The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. The MAX3110E/MAX3111E receivers have inverting outputs and are always active, even when the part is in hardware (or software) shutdown.

RS-232 Transceiver Hardware Shutdown

Supply current falls to $I_{CCSHDN(H)}$ when in hardware shutdown mode ($\overline{SHDN}$ = low). When shut down, the device's charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100µs, as shown in Figure 7. Connect $\overline{SHDN}$ to V_{CC} if the shutdown mode is not used. The UART software shutdown does not affect the RS-232 transceiver.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX3110E/MAX3111E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX3110E/MAX3111E keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection is tested in various ways; the transmitter outputs and receiver inputs devices are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact-Discharge Method specified in IEC 1000-4-2
- ±15kV using the Air-Gap Method specified in IEC 1000-4-2

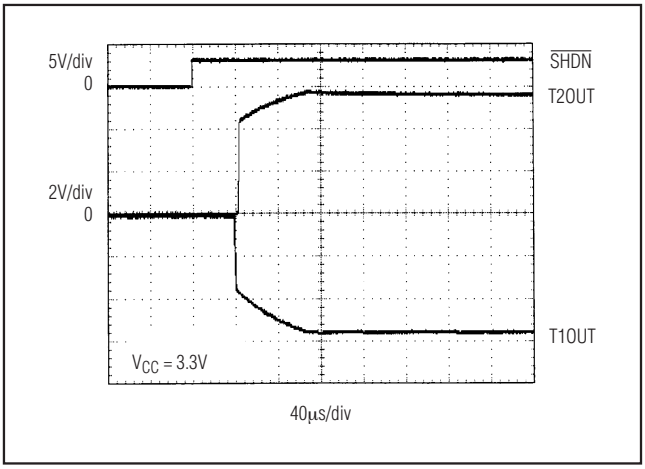


Figure 7. MAX3111E Transmitter Outputs Exiting Shutdown or Powering Up

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim's Quality Assurance (QA) group for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 8a shows the Human Body Model, and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3110E/MAX3111E help you design equipment that meets Level 4 (the highest level) of IEC 1000-4-2 without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD that withstands voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 9a shows the IEC 1000-4-2 model, and Figure 9b shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD contact-discharge test.

LapLink is a trademark of Traveling Software.

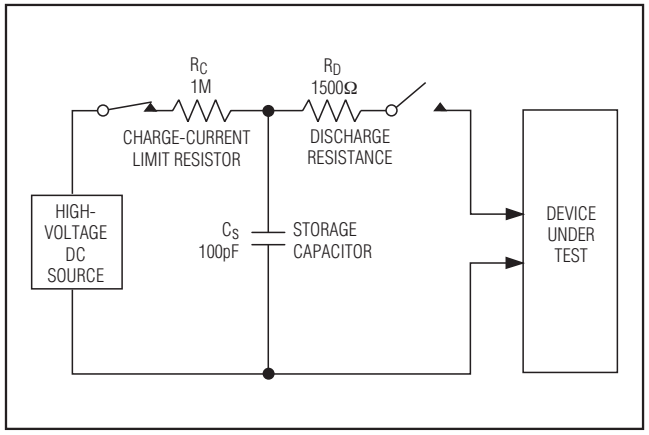


Figure 8a. Human Body ESD Test Model

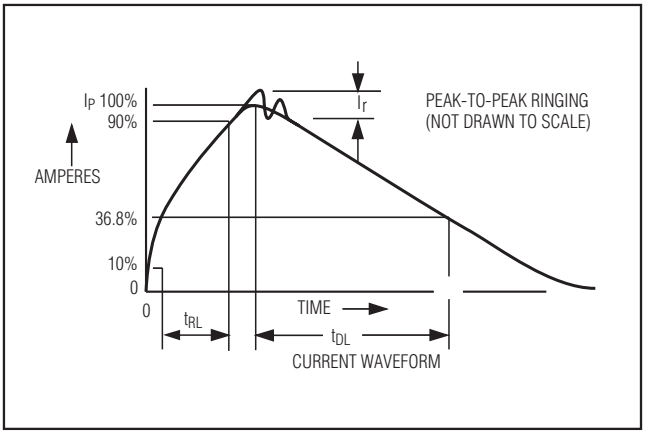


Figure 8b. Human Body Model Current Waveform

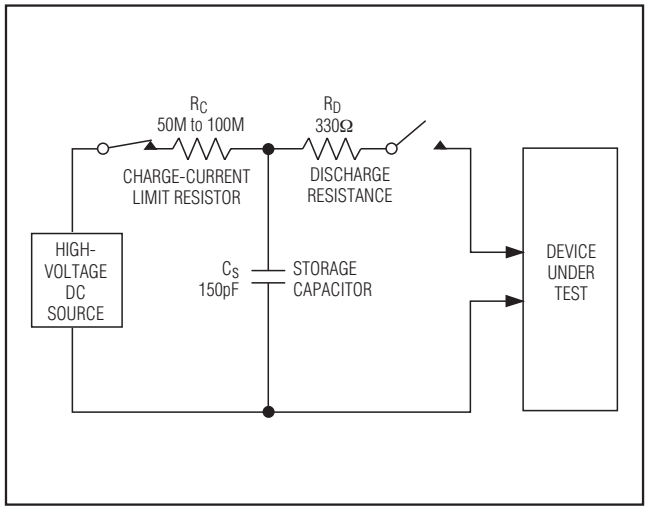


Figure 9a. IEC 1000-4-2 ESD Test Model

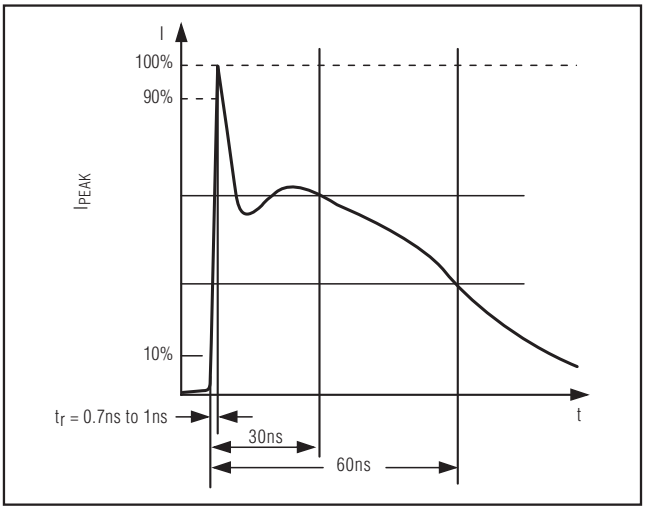


Figure 9b. IEC 1000-4-2 ESD Generator Current Waveform

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Crystals, Oscillators, and Ceramic Resonators

The MAX3110E/MAX3111E include an oscillator circuit derived from an external crystal oscillator for baud-rate generation. For standard baud rates, use a 1.8432MHz or 3.6864MHz crystal. The 1.8432MHz crystal results in lower operating current; however, the 3.6864MHz crystal may be more readily available in surface mount.

Ceramic resonators are low-cost alternatives to crystals and operate similarly, although the Q and accuracy are lower. Some ceramic resonators are available with integral load capacitors, which can further reduce cost. The tradeoff between crystals and ceramic resonators is in initial-frequency accuracy and temperature drift. Keep the total error in the baud-rate generator below 1% for reliable operation with other systems. This is accomplished easily with a crystal and, in most cases, is achieved with ceramic resonators. Table 8 lists different types of crystals and resonators and their suppliers.

The MAX3110E/MAX3111E's oscillator supports parallel-resonant mode crystals and ceramic resonators or can be driven from an external clock source. Internally, the oscillator consists of an inverting amplifier with its input, X1, tied to its output, X2, by a bias network that self-biases the inverter at approximately $V_{CC}/2$. The external feedback circuit, usually a crystal from X2 to X1, provides 180° of phase shift, causing the circuit to oscillate. As shown in the *Standard Application Circuit,* the crystal or resonator is connected between X1 and X2, with the load capacitance for the crystal being the series combination of C1 and C2. For example, for a 1.8432MHz crystal with a specified load capacitance of 11pF, use capacitors of 22pF on either side of the crystal to ground. Series-resonant mode crystals have a slight frequency error, typically oscillating 0.03% higher than specified series-resonant frequency when operated in parallel mode.

Note: It is very important to keep crystal, resonator, and load-capacitor leads and traces as short and direct as possible. Make the X1 and X2 trace lengths and ground tracks short, with no intervening traces. This helps minimize parasitic capacitance and noise pickup in the oscillator, and reduces EMI. Minimize capacitive loading on X2 to minimize supply current. The MAX3110E/MAX3111E's X1 input can be driven directly by an external CMOS clock source. The trip level is approximately equal to $V_{CC}/2$. Make no connection to X2 in this mode. If a TTL or non-CMOS clock source is used, AC-couple it with a 10nF capacitor to X1. A 2V peak-to-peak swing on the input is required for reliable operation.

RS-232 Transmitter Outputs Exiting Shutdown

Figure 7 shows two RS-232 transmitter outputs exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high; the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V.

Table 8. Component and Supplier List

DESCRIPTION	FREQUENCY (MHz)	TYPICAL C1, C2 (pF)	SUPPLIER	PART NUMBER	PHONE NUMBER
Through-Hole Crystal (HC-49/U)	1.8432	25	ECS International, Inc.	ECS-18-13-1	913-782-7787
Through-Hole Ceramic Resonator	1.8432	47	Murata North America	CSA1.84MG	800-831-9172
Through-Hole Crystal (HC-49/US)	3.6864	33	ECS International, Inc.	ECS-36-18-4	913-782-7787
SMT Crystal	3.6864	39	ECS International, Inc.	ECS-36-20-5P	913-782-7787
SMT Ceramic Resonator	3.6864	None (integral)	AVX/Kyocera	PBRC-3.68B	803-448-9411

High Data Rates

The MAX3110E/MAX3111E maintain the RS-232 ±5.0V minimum transmitter output-voltage specification even at the highest guaranteed data rate. Figure 10 shows a transmitter loopback test circuit. Figure 11 shows a loopback test result at 120kbps, and Figure 12 shows the same test at 250kbps. For Figure 11, both transmitters are driven simultaneously at 120kbps into an RS-232 receiver in parallel with 1000pF. For Figure 12, a single transmitter is driven at 250kbps, and both transmitters are loaded with an RS-232 receiver in parallel with 1000pF.

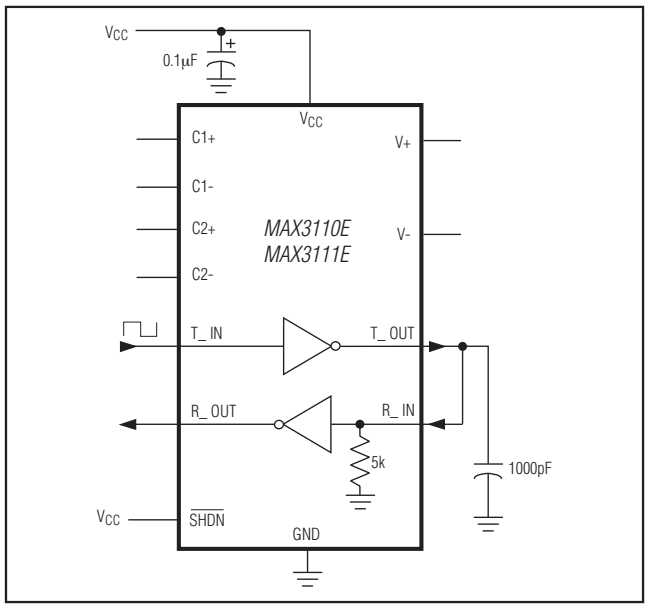


Figure 10. Loopback Test Circuit

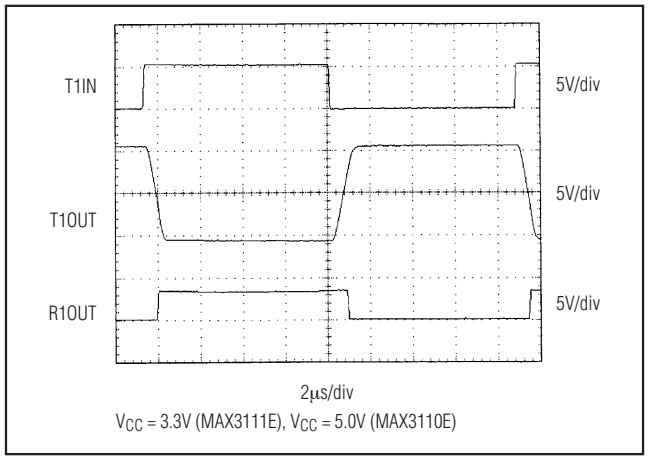


Figure 11. Loopback Test Result at 120kbps

Interconnection with 3.3V and 5V Logic

The MAX3110E/MAX3111E can directly interface with various 3.3V and 5V logic families, including ACT and HCT CMOS. See Table 9 for more information on possible combinations of interconnections.

Typical Applications

The MAX3110E/MAX3111E each contain a UART, two RS-232 drivers, and two RS-232 receivers in one package. The standard RS-232 typical operating circuit is shown in Figure 13.

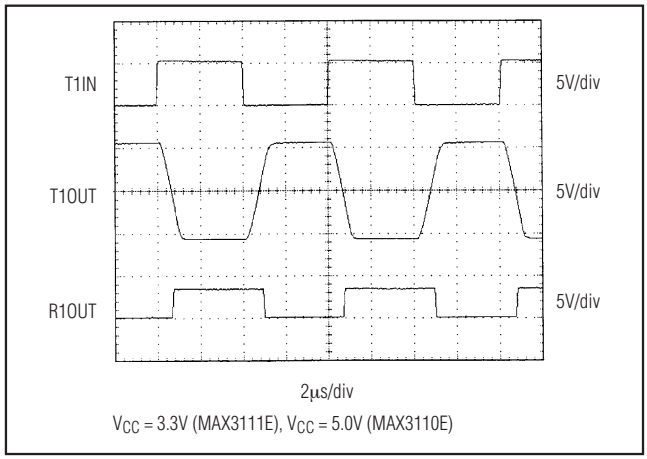


Figure 12. Loopback Test Result at 250kbps

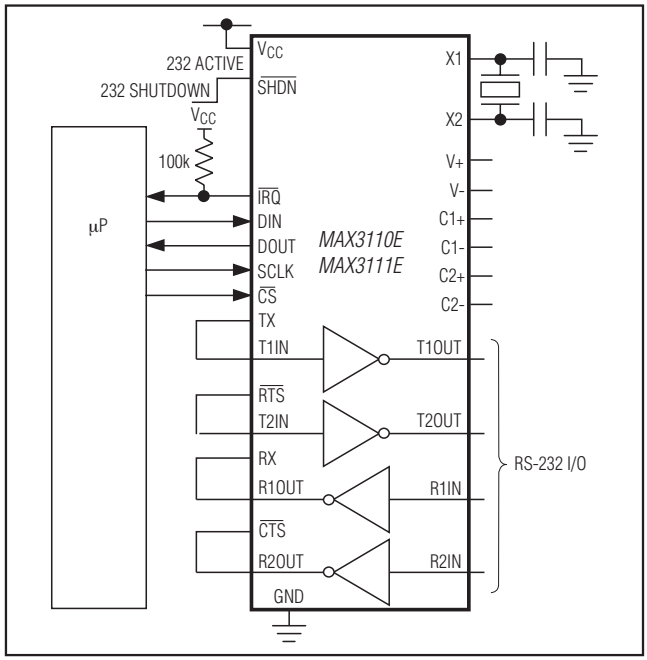


Figure 13. RS-232 Typical Operating Circuit

Table 9. Logic-Family Compatibility with Various Supply Voltages

LOGIC POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
5 (MAX3110E)	5	Compatible with all TTL and CMOS families
3.3 (MAX3111E)	3.3	Compatible with all CMOS families
5 (MAX3111E)	3.3	Compatible with ACT and HCT CMOS, and with AC, HC, or CD4000 CMOS

An IR and RS-232 typical operating circuit is shown in Figure 14. Since the MAX3110E/MAX3111E's internal UART has IrDA capability, a standard IR transceiver (the MAX3120) can be used to provide the IrDA communication. The two-driver/two-receiver RS-232 transceiver can be used with a software UART to provide RS-232 communication.

9-Bit Networks

The MAX3110E/MAX3111E support a common multidrop communication technique referred to as 9-bit mode. In this mode, the parity bit is set to indicate a message that contains a header with a destination address. The MAX3110E/MAX3111E's parity mask can be set to generate interrupts for this condition. Operating a network in this mode reduces the processing overhead of all nodes by enabling the slave controllers to ignore most message traffic. This relieves the remote processor to handle more useful tasks.

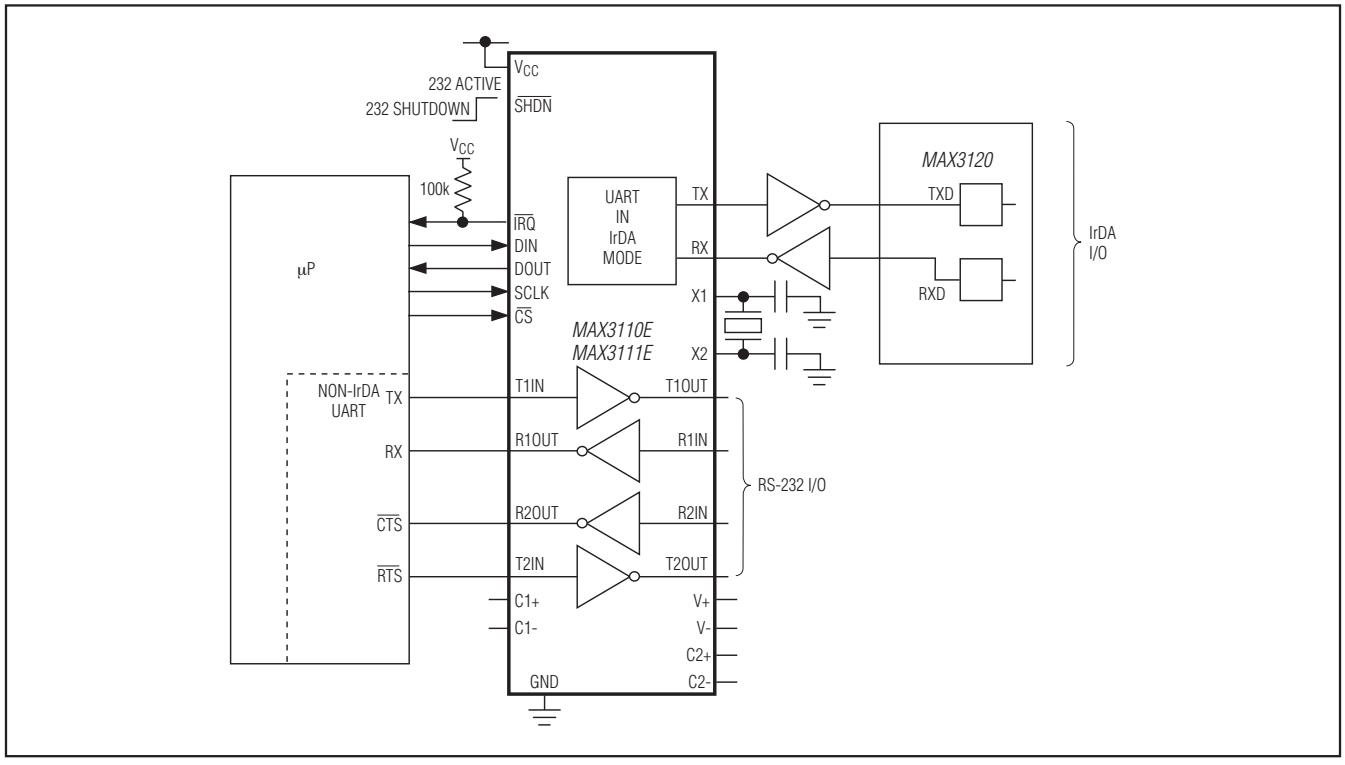


Figure 14. IR and RS-232 Typical Operating Circuit

In 9-bit mode, the MAX3110E/MAX3111E is set up with eight bits plus parity. The parity bit in all normal messages is clear but is set in an address-type message. The MAX3110E/MAX3111E's parity-interrupt mask generates an interrupt on high parity when enabled. When the master sends an address message with the parity bit set, all MAX3110E/MAX3111E nodes issue an interrupt. All nodes then retrieve the received byte to compare to their assigned address. Once addressed, the node continues to process each received byte. If the node was not addressed, it ignores all message traffic until a new address is sent out by the master.

The parity/9th-bit interrupt is controlled only by the data in the receive register and is not affected by data in the FIFO, so the most effective use of the parity/9th-bit interrupt is with FIFO disabled. With the FIFO disabled, received non-address words can be ignored and not even read from the UART. For more detailed information on 9-bit mode, refer to the MAX3100 data sheet.

SIR IrDA Mode

The MAX3110E/MAX3111E's IrDA mode can be used to communicate with other IrDA SIR-compatible devices or to reduce power consumption in opto-isolated applications.

In IrDA mode, a bit period is shortened to 3/16 of a baud period (1.61µs at 115,200 baud). A data zero is transmitted as a pulse of light (TX pin = logic low, RX pin = logic high), as shown in Figure 15.

In receive mode, the RX signal's sampling is done halfway into the transmission of a high level. The sampling is done once (instead of three times, as in normal mode). The MAX3110E/MAX3111E ignore pulses shorter than approximately 1/16 of the baud period. The IrDA device that is communicating with the MAX3110E/MAX3111E must be set to transmit pulses at 3/16 of the baud period. For compatibility with other IrDA devices, set the format to 8-bit data, one stop, no parity. For more detailed information on SIR IrDA mode, refer to the MAX3100 data sheet.

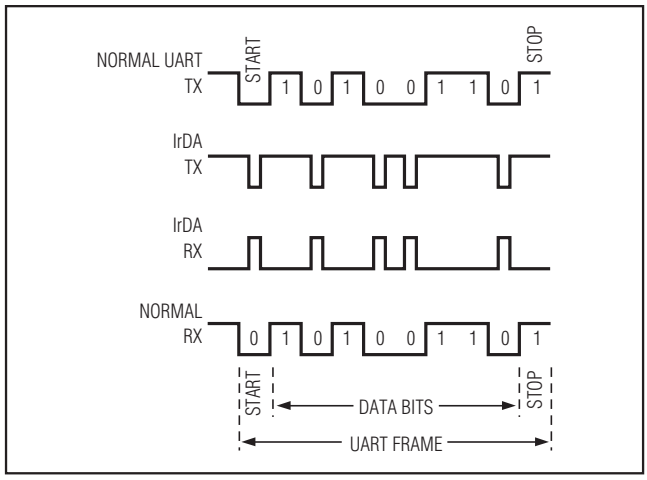


Figure 15. IrDA Timing

Layout and Power-Supply Considerations

The MAX3110E/MAX3111E require basic layout techniques and fundamental power supply considerations. The minimum requirements include: (1) placing a 1µF ceramic bypass capacitor as close as possible to V_{CC}, preferably right next to the V_{CC} lead or on the opposite side of the PCB directly below the V_{CC} lead; (2) using an internal ground plane within the PCB, returning all circuit grounds to this ground plane, or using a 'star' ground technique where all circuit grounds are returned to a common ground point at the 'GND' lead of the IC; (3) ensuring that the power source to the IC has a low inductive path and is high-frequency bypassed to absorb ESD events with significant changes in the supply voltage.

Listing 1. Outline for a MAX3110E/MAX3111E Software Driver

```
This is a C-language outline of an interrupt-driven software driver that interfaces
to a MAX3110E/MAX3111E, providing an intermediate layer between the bit-manipulation
subroutine and the familiar PutChar / GetChar subroutines.

User must supply code for managing the transmit and receive queues, as well as the
low-level hardware interface itself.  The interrupt control hardware must be
initialized before this driver is called.

char is an 8 bit character.   int is a 16 bit unsigned integer.
& is the bitwise Boolean AND operator.   | is the bitwise Boolean OR operator.

/* High level interface routine to put a character to the MAX3110E/MAX3111E. */
PutChar ( char c )
{
      EnQueue ( txqueue, c );
      /* enable the transmit-buffer-empty interrupt */
      config = config | 0x0800; /* set the TM bit */
      config = config | 0xC000; /* set bits 15 and 14 */
      MAX3110E/MAX3111E ( config );
}

/* High level interface routine to get a character from the MAX3110E/MAX3111E.
** Wait for a character to be received, if necessary.
*/
char GetChar ( )
{
      while ( IsQueueEmpty ( rxqueue ) )
            /* wait for data to be received */ ;
      return DeQueue ( rxqueue );
}

/* Configure the MAX3110E/MAX3111E with the specified baud rate.  */
ConfigureMAX3110E/MAX3111E ( int baud_rate_index )
{
      baud_rate_index = baud_rate_index & 0x000F; /* restrict to a 4 bit field */
      config = 0xC400 + baud_rate_index; /* enable received data interrupt */
      MAX3110E/MAX3111E ( config );
}


/* private variable that stores the configuration settings for the MAX3110E/MAX3111E
*/
int config;

/* Low level communication routine between the computer and the MAX3110E/MAX3111E.
** This is a PRIVATE routine to be used only within the driver software.
*/
int MAX3110E/MAX3111E ( int mosi )
{
      int miso;
      /* this is interface-specific.
      ** Transmit 16 bits of master-out, slave-in data, MSB first,
      ** while simultaneously receiving 16 bits of master-in, slave-out data.
      ** If and SPI hardware interface is available, use (CPOL=0,CPHA=0) mode.
      ** Lacking specialized hardware, just set and clear I/O bits to generate
      ** the waveform in figures 2 and 3 in the MAX3110E/MAX311E data sheet.
      */
      return miso; /* return 16 bits of master-in, slave-out data, MSB first */
}
```

Listing 1. Outline for a MAX3110E/MAX3111E Software Driver (continued)

```
/* This driver needs a txqueue transmit-data queue and a rxqueue receive-data queue.
** These can be ring buffers or any other kind of first-in, first-out data queue.
*/
EnQueue ( queue , char )
char DeQueue ( queue )
true/false IsQueueEmpty ( queue )



/*  Interrupt service routine called when the MAX3110EMAX3111E's INT pin falls to a
low level.
** This is a PRIVATE routine to be used only within the driver software.
*/
ServiceMAX3110E/MAX3111Eint ( )
{
      int rxdata;
      int txdata;
      char c;

      /* issue a READ DATA command to discover the cause of the interrupt */
      rxdata = MAX3110E/MAX3111E ( 0 );

      if ( rxdata & 0x8000 )  /* the R bit = 1 */
      {
            c = rxdata & 0x00FF; /* get the received character data */
            EnQueue ( rxqueue, c );
      }
      if ( rxdata & 0x4000 )  /* the T bit = 1 */
      {
            if ( IsQueueEmpty ( txqueue ) )
            {
                  /* mask the transmit-buffer-empty interrupt */
                  config = config & ~ 0x0800; /* clear the TM bit */
                  config = config | 0xC000; /* set bits 15 and 14 */
                  MAX3110E/MAX3111E ( config );
            }
            else /* transmit some data */
            {
                  /* issue a WRITE DATA command */
                  txdata = DeQueue ( txqueue );
                  c = txdata & 0x00FF; /* get the transmit character */
                  MAX3110E/MAX3111E ( 0x8000 | c );
            }
      }
} /* end of ServiceMAX3110E/MAX3111Eint */
```

SPI/MICROWIRE-Compatible UART and ±15kV ESD-Protected RS-232 Transceivers with Internal Capacitors

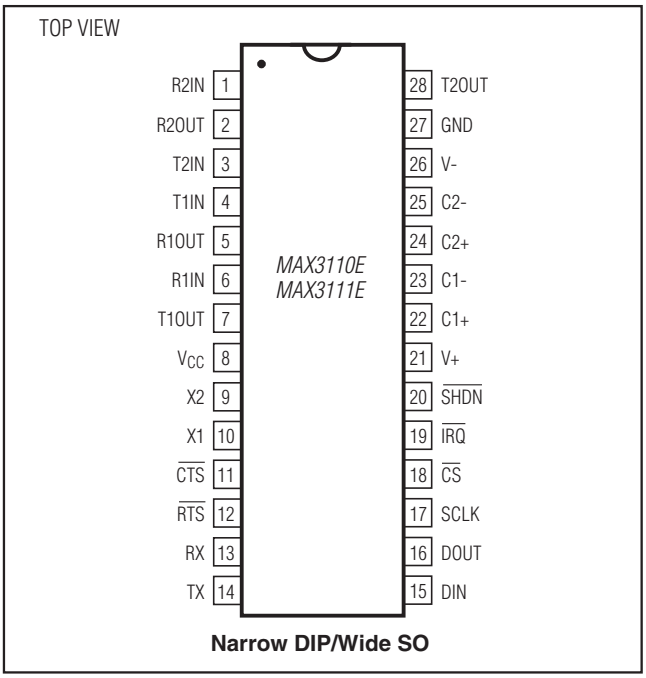
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	V_{CC} (V)
MAX3110EEWI	-40°C to +85°C	28 Wide SO	5
MAX3110EENI	-40°C to +85°C	28 Plastic DIP	5
MAX3111ECWI	0°C to +70°C	28 Wide SO	3.3
MAX3111ECNI	0°C to +70°C	28 Plastic DIP	3.3
MAX3111EEWI	-40°C to +85°C	28 Wide SO	3.3
MAX3111EENI	-40°C to +85°C	28 Plastic DIP	3.3

Chip Information

TRANSISTOR COUNT: 7977

Pin Configuration



Narrow DIP/Wide SO

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 Wide SO	—	21-0042
28 Plastic DIP	—	21-0043

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/99	Initial release.	—
1	12/05	Added the soldering temperature to the *Absolute Maximum Ratings*.	2

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Тел: +7 (812) 336 43 04 (многоканальный)
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