

2 Channel I2Cbus Multiplexer with interrupt logic

Features

- 1-of-2 bidirectional translating multiplexer
- I2C-bus interface logic
- Operating power supply voltage :1.65 V to 5.5 V
- Allows voltage level translation between 1.2V, 1.8V,2.5 V, 3.3 V and 5 V buses
- Low standby current
- Low Ron switches
- Channel selection via I2C bus
- Power-up with all multiplexer channels deselected
- Capacitance isolation when channel disabled
- No glitch on power-up
- Supports hot insertion
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 8000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SOIC-14W, TSSOP-14L

Description

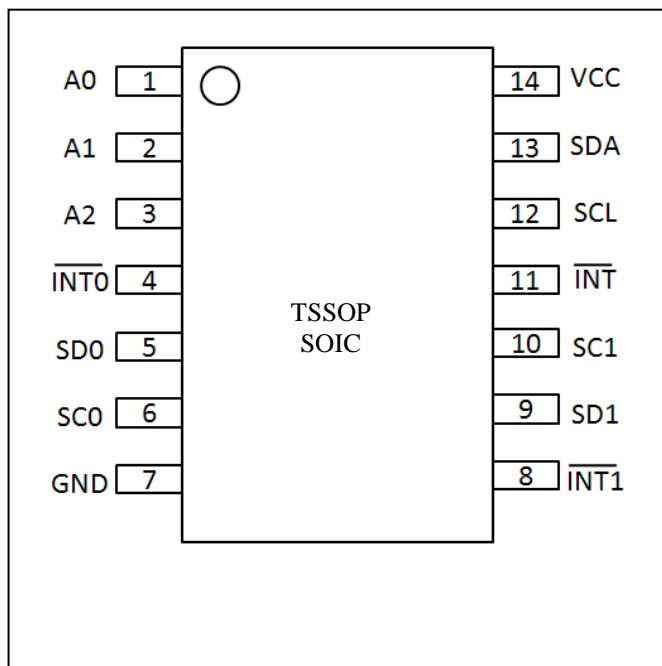
The PI4MSD5V9542A is a 1-of-2 bidirectional translating multiplexer, controlled via the I2C bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels.

Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Two interrupt inputs, INT0 and INT1, one for each of the SCx/SDx downstream pairs, are provided. One interrupt output, INT, which acts as an AND of the two interrupt inputs, is provided.

A power-on reset function puts the registers in their default state and initializes the I2C bus state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the VCC pin can be used to limit the maximum high voltage which will be passed by the PI4MSD5V9542A. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.2V, 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

Pin Configuration



Pin Description

| Pin No | Pin Name | Type | Description |
|--------|----------|--------|------------------------------|
| 1 | A0 | Input | address input 0 |
| 2 | A1 | Input | address input 1 |
| 3 | A2 | Input | address input 2 |
| 4 | INT0 | Input | active LOW interrupt input 0 |
| 5 | SD0 | I/O | serial data 0 |
| 6 | SC0 | I/O | serial clock 0 |
| 7 | GND | Ground | supply ground |
| 8 | INT1 | Input | active LOW interrupt input 1 |
| 9 | SD1 | I/O | serial data 1 |
| 10 | SC1 | I/O | serial clock 1 |
| 11 | INT | Output | active LOW interrupt output |
| 12 | SCL | I/O | serial clock line |
| 13 | SDA | I/O | serial data line |
| 14 | VCC | Power | supply voltage |

Block Diagram

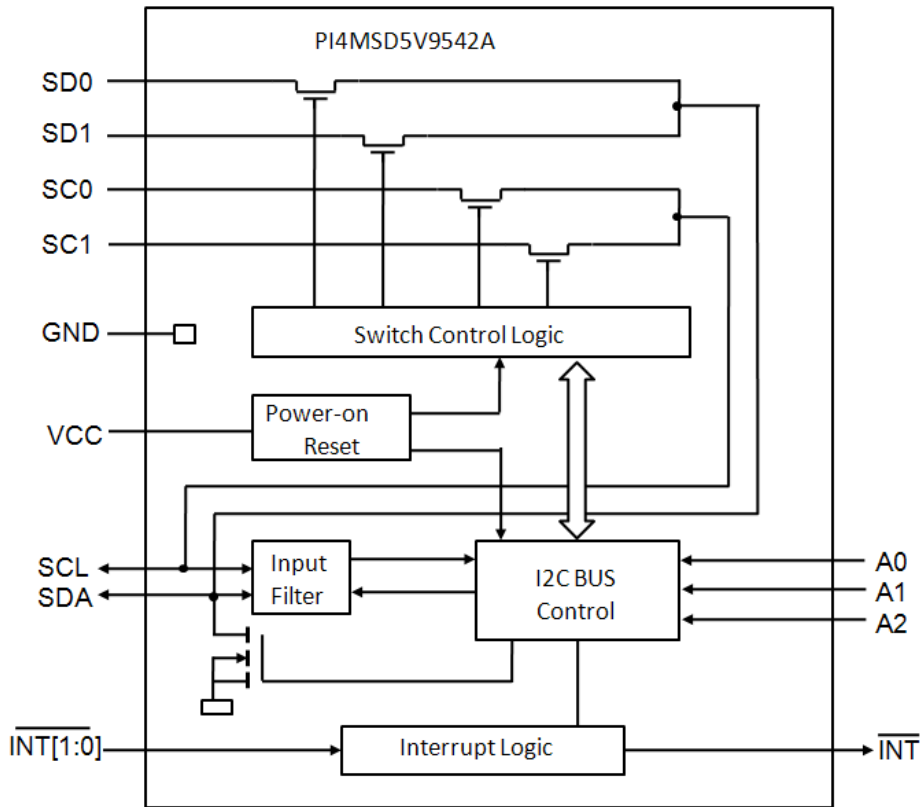


Figure 1: Block Diagram

Maximum Ratings

| | |
|--|-------------------|
| Storage Temperature | -55 °C to +125 °C |
| Supply Voltage port B | -0.5V to +6.0V |
| Supply Voltage port A | -0.5V to +6.0V |
| DC Input Voltage | -0.5V to +6.0V |
| Control Input Voltage (EN)..... | -0.5V to +6.0V |
| Total power dissipation ⁽¹⁾ | 100mW |
| Input current(EN,VCCA,VCCB,GND)..... | 50mA |
| ESD: HBM Mode | 8000V |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|---|------|-----|-----|------|
| V _{CC} | V _{CCA} Positive DC Supply Voltage | 1.65 | - | 5.5 | V |
| V _{EN} | Enable Control Pin Voltage | GND | - | 5.5 | V |
| V _{IO} | I/O Pin Voltage | GND | - | 5.5 | V |
| Δt / ΔV | Input transition rise or fall time | - | - | 10 | ns/V |
| T _A | Operating Temperature Range | -40 | - | +85 | °C |

DC Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $1.1\text{V} \leq V_{CC} \leq 3.6\text{V}$

| Symbol | Parameter | Conditions | VCC | Min | Typ | Max | Unit |
|------------------------------------|--------------------------|--|----------------|---------------------|-----|---------------------|---------------|
| Supply | | | | | | | |
| VCC | Supply Voltage | | | 1.65 | | 5.5 | V |
| ICC | supply current | operating mode; no load; $V_I = V_{CC}$ or GND; $f_{SCL} = 100\text{ kHz}$ | 3.6V to 5.5V | | 65 | 100 | μA |
| | | | 2.3V to 3.6V | | 20 | 50 | μA |
| | | | 1.65V to 2.3V | | 10 | 30 | μA |
| Istb | standby current | standby mode; $V_{CC} = 3.6\text{ V}$; no load; $V_I = V_{CC}$ or GND; $f_{SCL} = 0\text{ kHz}$ | 3.6V to 5.5V | | 0.3 | 1 | μA |
| | | | 2.3V to 3.6V | | 0.1 | 1 | μA |
| | | | 1.65V to 2.3V | | 0.1 | 1 | μA |
| VPOR ^[1] | power-on reset voltage | no load; $V_I = V_{CC}$ or GND | 3.6V to 5.5V | | 1.3 | 1.5 | V |
| Input SCL; input/output SDA | | | | | | | |
| V _{IL} | LOW-level input voltage | | 1.65V to 5.5V | -0.5 | | +0.3V _{CC} | V |
| V _{IH} | HIGH-level input voltage | | 1.65V to 2V | 0.75V _{CC} | | 6 | V |
| | | | 2V to 5.5V | 0.7V _{CC} | | 6 | V |
| I _{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$ | 1.65V to 5.5V | 3 | | - | mA |
| | | $V_{OL} = 0.6\text{ V}$ | 1.65V to 5.5V | 6 | | - | mA |
| I _{IL} | LOW-level input current | $V_I = \text{GND}$ | 1.65V to 5.5V | -1 | | +1 | μA |
| I _{IH} | HIGH-level input current | $V_I = V_{CC}$ | 1.65V to 5.5V | -1 | | +1 | μA |
| C _i | input capacitance | $V_I = \text{GND}$ | 1.65V to 5.5V | - | 9 | 10 | pF |
| Pass Gate | | | | | | | |
| Ron | ON-state resistance | $V_O = 0.4\text{ V}$; $I_O = 15\text{ mA}$ | 4.5 V to 5.5 V | 4 | 9 | 24 | Ω |
| | | | 3V to 3.6V | 5 | 11 | 31 | Ω |
| | | $V_O = 0.4\text{ V}$; $I_O = 10\text{ mA}$ | 2.3V to 2.7V | 7 | 16 | 55 | Ω |
| | | | 1.65V to 2V | 9 | 20 | 70 | Ω |
| V _{pass} | switch output voltage | $V_{in} = V_{CC}$; $I_{out} = -100\mu\text{A}$ | 5V | | 3.6 | | V |
| | | | 4.5 V to 5.5 V | 2.8 | | 4.5 | V |
| | | | 3.3V | | 2.2 | | V |
| | | | 3V to 3.6V | 1.6 | | 2.8 | V |
| | | | 2.5V | | 1.5 | | V |
| | | | 2.3V to 2.7V | 1.1 | | 2 | V |
| | | | 1.8V | | 0.9 | | V |
| 1.65V to 2V | 0.54 | | 1.3 | V | | | |

To be continued

Continued

| Symbol | Parameter | Conditions | VCC | Min | Typ | Max | Unit |
|--------------------------------------|---------------------------|-----------------------|---------------|--------------------|-----|---------------------|------|
| I_L | leakage current | $V_I = V_{CC}$ or GND | 1.65V to 5.5V | -1 | | +1 | pF |
| C_{io} | input/output capacitance | $V_I = V_{CC}$ or GND | 1.65V to 5.5V | | 3 | 5 | pF |
| Select inputs A0, A1, A2, INT0, INT1 | | | | | | | |
| V_{IL} | LOW-level input voltage | | 1.65V to 5.5V | -0.5 | | +0.3V _{CC} | V |
| V_{IH} | HIGH-level input voltage | | 1.65V to 5.5V | 0.7V _{CC} | | 6 | V |
| I_{LI} | input leakage current | $V_I = GND$ | 1.65V to 5.5V | -1 | | +1 | uA |
| C_i | input capacitance | $V_I = GND$ | 1.65V to 5.5V | | 3 | 5 | pF |
| INT output | | | | | | | |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4 V$ | 1.65V to 5.5V | 3 | | | mA |
| I_{OH} | HIGH-level output current | | 1.65V to 5.5V | | | +10 | uA |

Note: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.

AC Electrical characteristics

Tamb = - 40 °C to +85 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | VCC | Min | Typ | Max | Unit |
|--------------------|--------------------------------------|-----------------------------------|---------------|-----|-----|-----|------|
| $t_{PD}^{[1]}$ | propagation delay | from SDA to SDx, or SCL to SCx | 1.65V to 5.5V | | | 0.3 | ns |
| INT ^[2] | | | | | | | |
| t_{V_INT} | valid time from INTn to INT signal | | 1.65V to 5.5V | | | 4 | us |
| t_{D_INT} | delay time from INTn to INT inactive | | 1.65V to 5.5V | | | 2 | us |
| t_{REJ_L} | LOW-level rejection time | | 1.65V to 5.5V | 1 | | | us |
| t_{REJ_H} | HIGH-level rejection time | | 1.65V to 5.5V | 0.5 | | | us |

Note

[1] Pass gate propagation delay is calculated from the 20Ω typical Ron and the 15 pF load capacitance.

[2] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

I2C Interface Timing Requirements

| Symbol | Parameter | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNIT |
|---------------------|--|------------------------------------|------|--------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f _{SCL} | I2C clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{Low} | I2C clock high time | 4.7 | | 1.3 | | μs |
| t _{High} | I2C clock low time | 4 | | 0.6 | | μs |
| t _{SP} | I2C spike time | | 50 | | 50 | ns |
| t _{SU:DAT} | I2C serial-data setup time | 250 | | 100 | | ns |
| t _{HD:DAT} | I2C serial-data hold time | 0 ^[1] | | 0 ^[1] | | μs |
| t _r | I2C input rise time | | 1000 | | 300 | ns |
| t _f | I2C input fall time | | 300 | | 300 | ns |
| t _{BUF} | I2C bus free time between stop and start | 4.7 | | 1.3 | | μs |
| t _{SU:STA} | I2C start or repeated start condition setup | 4.7 | | 0.6 | | μs |
| t _{HD:STA} | I2C start or repeated start condition hold | 4 | | 0.6 | | μs |
| t _{SU:STO} | I2C stop condition setup | 4 | | 0.6 | | μs |
| t _{VD:DAT} | Valid-data time (high to low) ^[2] SCL low to SDA output low valid | | 1 | | 1 | μs |
| | Valid-data time (low to high) ^[2] SCL low to SDA output high valid | | 0.6 | | 0.6 | μs |
| t _{VD:ACK} | Valid-data time of ACK condition ACK signal from SCL low to SDA output low | | 1 | | 1 | μs |
| C _b | I2C bus capacitive load | | 400 | | 400 | pF |

Notes:

[1] A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the VIH min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

[2] Data taken using a 1-kΩ pullup resistor and 50-pF load Notes

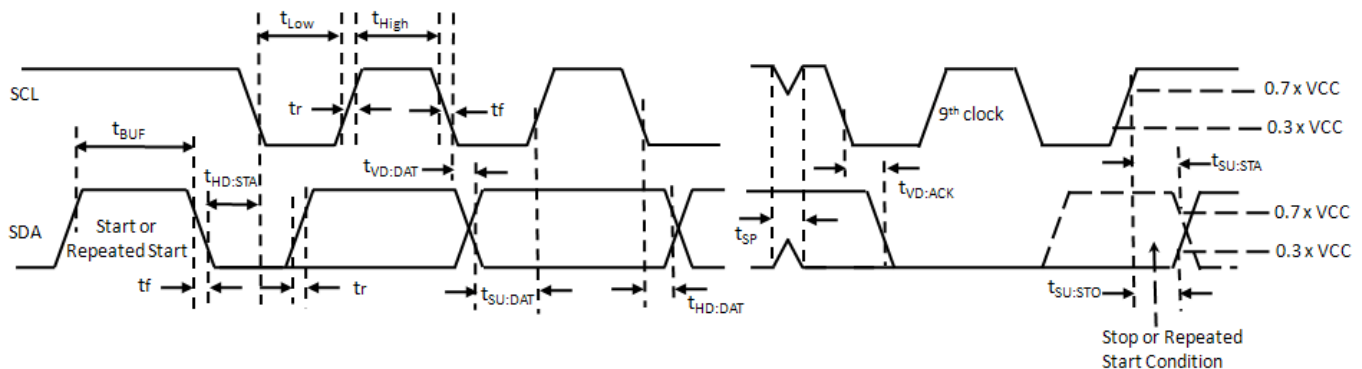


Figure 2. Definition of timing on the I2C-bus

Application

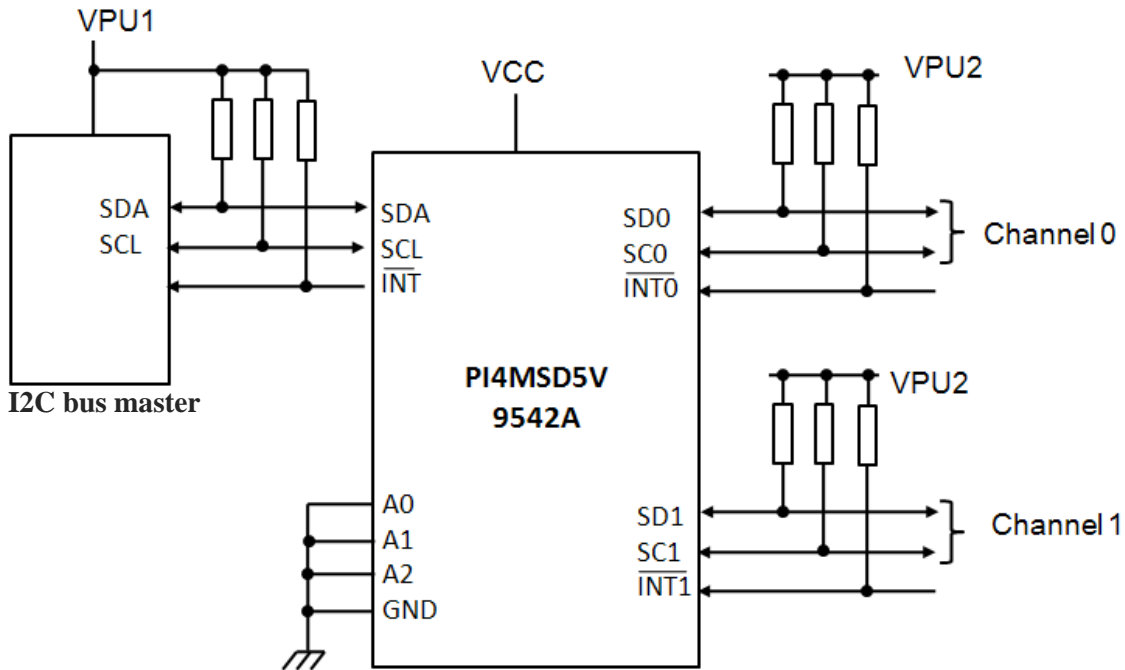


Figure 3. Typical Application

| VCC | VPU1 | VPU2 |
|------|-----------|-----------|
| 1.8V | 1.5V-5.5V | 1.2V-5.5V |
| 2.5V | 1.8V-5.5V | 1.8V-5.5V |
| 3.3V | 2.7V-5.5V | 2.7V-5.5V |
| 5V | 4.5V-5.5V | 4.5V-5.5V |

Note:
 If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.
 If the device generating the interrupt has a totem pole output structure and cannot be 3-stated, a pull-up resistor is not required.
 The interrupt inputs should not be left floating.

Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PI4MSD5V9542A is shown in Figure 4.

To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

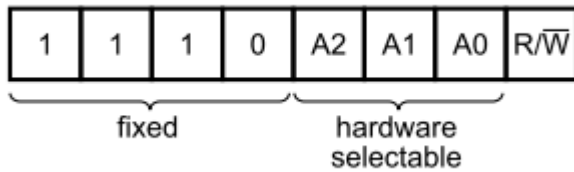


Figure 4: Device address

Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PI4MSD5V9542A which will be stored in the control register. If multiple bytes are received by the PI4MSD5V9542A, it will save the last byte received. This register can be written and read via the I2C-bus.

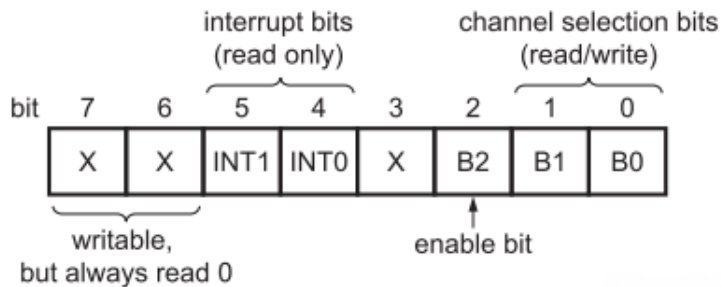


Figure 5: Control register

Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PI4MSD5V9542A has been addressed. The 3 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I2C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Bits INT0/, INT1/, D6 and D7 are all writable, but will read the chip status. INT0/ and INT1/ indicate the state of the corresponding interrupt input. D7 and D6 always read 0.

| D7 | D6 | INT1 | INT0 | D3 | B2 | B1 | B0 | Command |
|----|----|------|------|----|----|----|----|--|
| X | X | X | X | X | 0 | X | X | no channel selected |
| X | X | X | X | X | 1 | 0 | 0 | channel 0 enabled |
| X | X | X | X | X | 1 | 0 | 1 | channel 1 enabled |
| X | X | X | X | X | 1 | 1 | X | no channel selected |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | no channel selected; power-up default state |

Control register: Write—channel selection; Read—channel status.

Interrupt handling

The PI4MSD5V9542A provides 2 interrupt inputs, one for each channel and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PI4MSD5V9542A and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control byte.

Bits 5:4 of the control byte correspond to channel 1, channel 0 of the PI4MSD5V9542A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PI4MSD5V9542A and read the contents of the control byte to determine which channel contains the device generating the interrupt. The master can then reconfigure the PI4MSD5V9542A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt. The interrupt inputs may be used as general purpose inputs if the interrupt function is not required. If unused, interrupt input(s) must be connected to VCC through a pull-up resistor.

| D7 | D6 | INT1 | INT0 | D3 | B2 | B1 | B0 | Command |
|----|----|------|------|----|----|----|----|---------------------------|
| 0 | 0 | X | 0 | X | X | X | X | no interrupt on channel 0 |
| | | | 1 | | | | | interrupt on channel 0 |
| 0 | 0 | 0 | X | X | X | X | X | no interrupt on channel 1 |
| | | 1 | | | | | | interrupt on channel 1 |

Control register read — interrupt

Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4MSD5V9542A in a reset condition until VCC has reached VPOR. At this point, the reset condition is released and the PI4MSD5V9542A registers and I2C-bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, VCC must be lowered below 0.2 V for at least 5 us in order to reset the device.

Voltage translation

The pass gate transistors of the PI4MSD5V9542A are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I2C-bus to another.

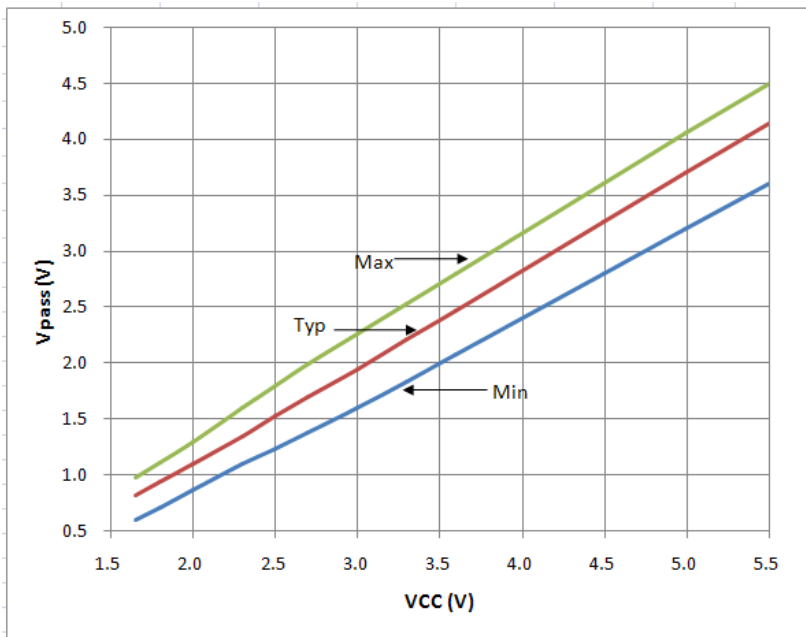


Figure 6: Vpass voltage VS Vcc

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section “DC Electrical characteristics” of this data sheet).

In order for the PI4MSD5V9542A to act as a voltage translator, the Vpass voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then Vpass should be equal to or below 2.7 V to clamp the downstream bus voltages effectively.

Looking at Figure 6, we see that Vpass (max) is at 2.7 V when the PI4MSD5V9542A supply voltage is 3.5 V or lower so the PI4MSD5V9542A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels

I2C BUS

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals

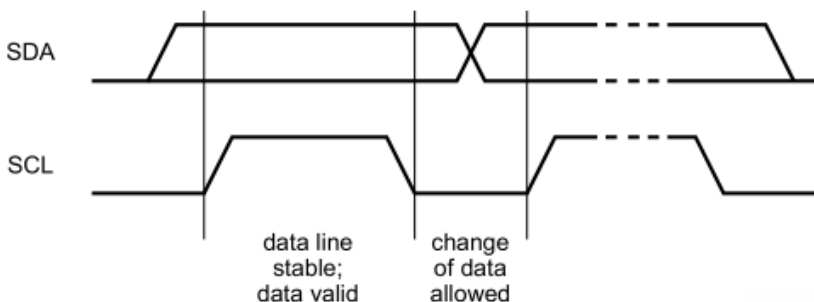


Figure 7: Bit Transfer

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P)

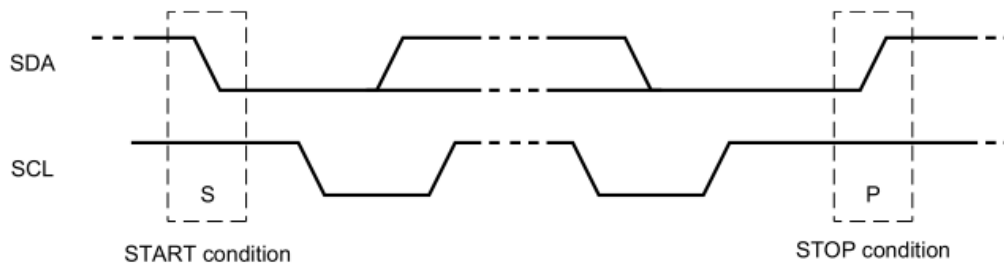


Figure 8. Definition of Start and Stop Conditions

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’

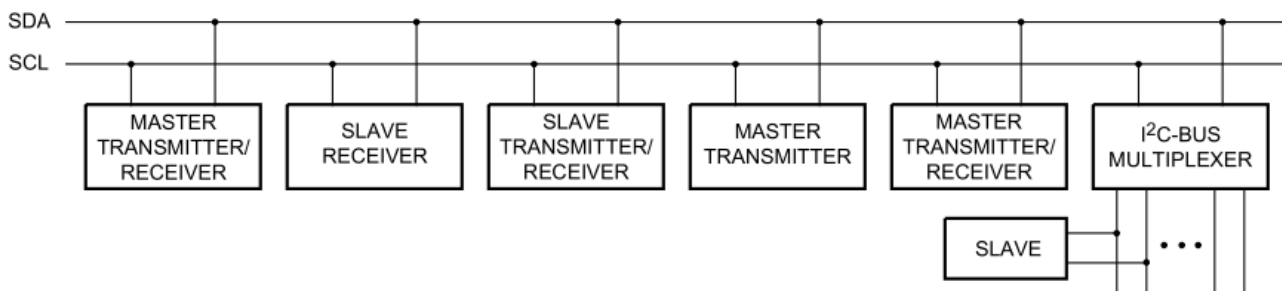


Figure 9. System Configuration

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

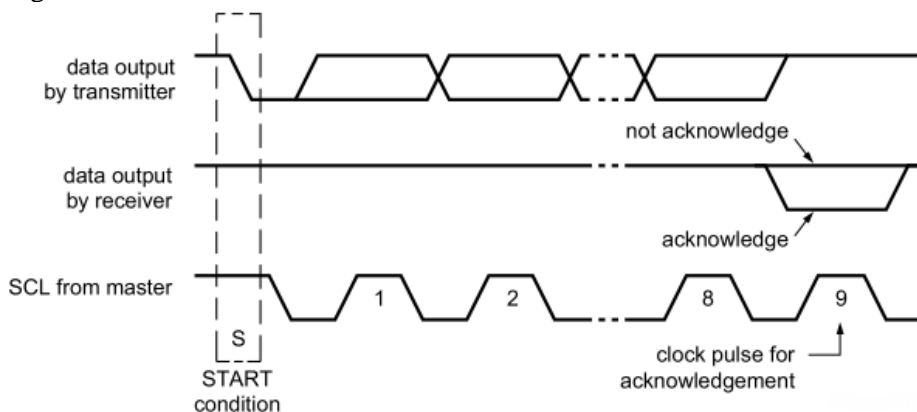


Figure 10. Acknowledgment on I2C Bus

Data is transmitted to the PI4MSD5V9542A control register using the write mode shown in bellow

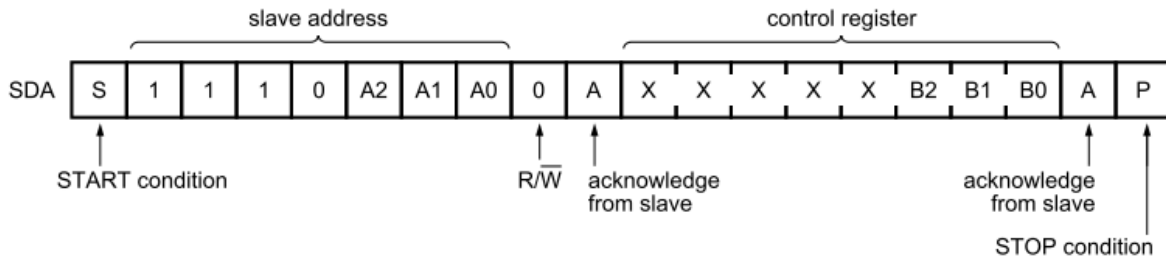


Figure 11. Write Control Register

Data is transmitted to the PI4MSD5V9542A control register using the write mode shown in bellow

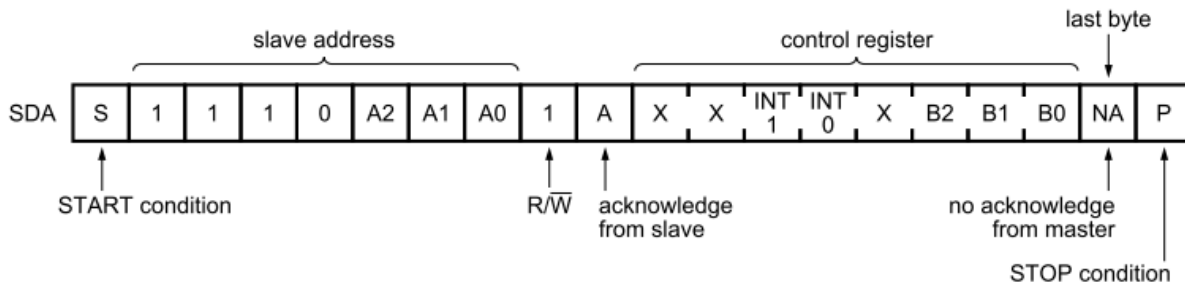
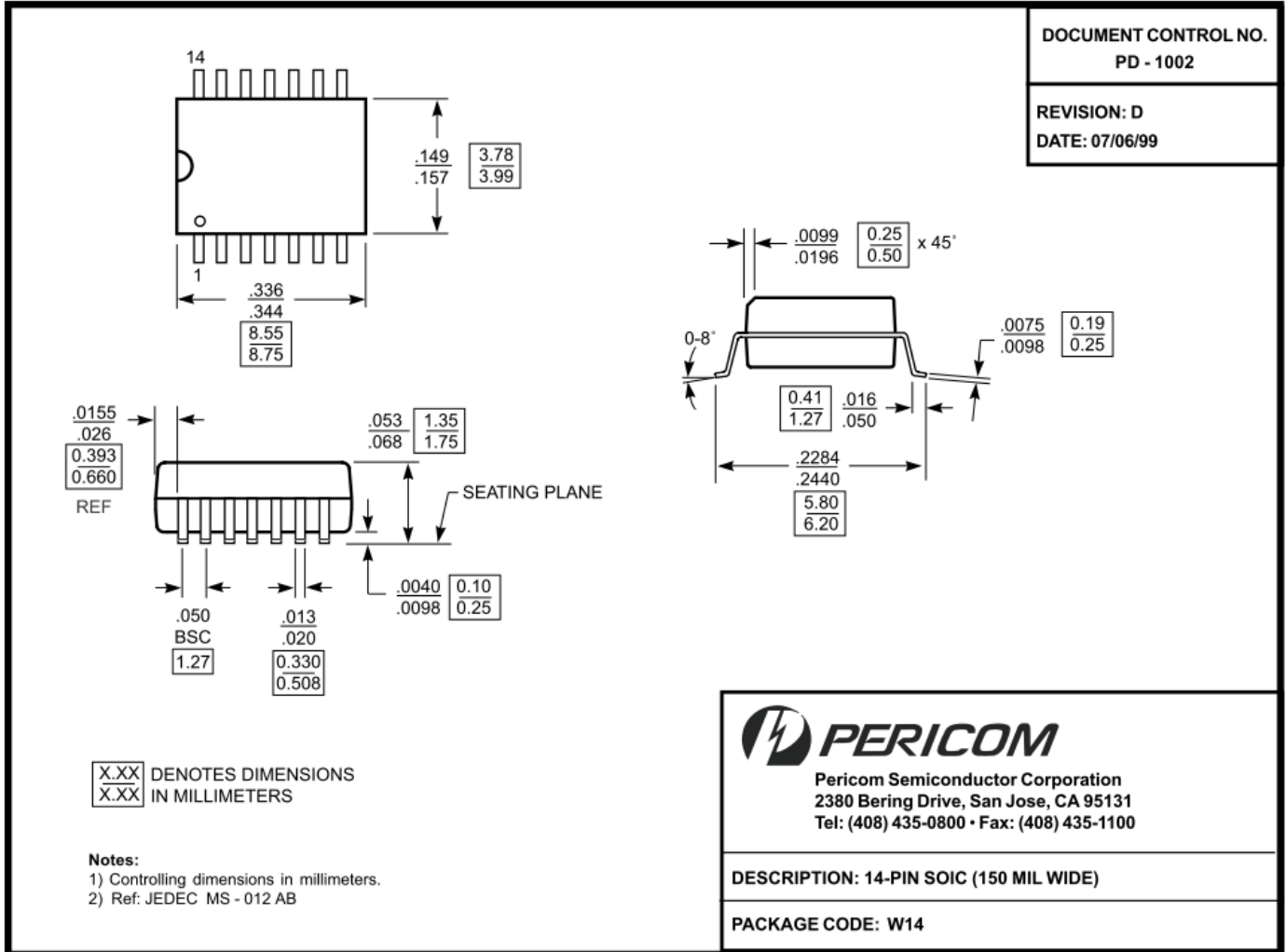


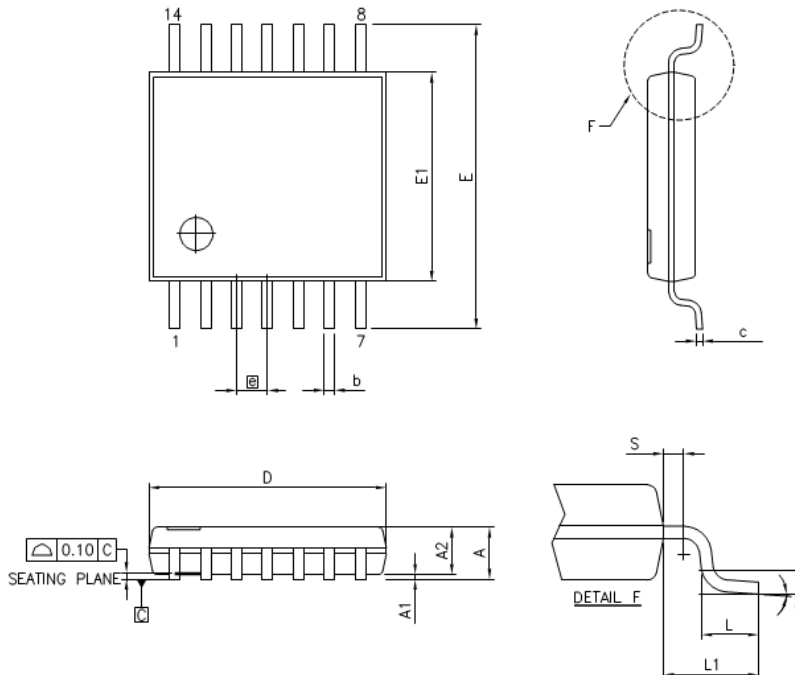
Figure 12. Read Control Register

Mechanical Information
SOIC-14(W)



Mechanical Information

TSSOP-14(L)




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---------|----------|------|------|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.80 | — | 1.05 |
| b | 0.19 | — | 0.30 |
| c | 0.09 | — | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.45 | 0.60 | 0.75 |
| S | 0.20 | — | — |
| θ | 0° | — | 8° |

Notes:

1. JEDEC: MO-153F/AB-1
2. Controlling dimensions in millimeters
3. Package Outline Exclusive of mold flash and metal burr

 DATE: 05/03/12

DESCRIPTION: 14-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1309 REVISION: D

Ordering Information

| Part No. | Package Code | Package |
|------------------|--------------|---|
| PI4MSD5V9542AWE | W | 14-Pin, 150 mil Wide SOIC |
| PI4MSD5V9542AWEX | W | 14-Pin, 150 mil Wide SOIC, Tape & Reel |
| PI4MSD5V9542ALE | L | 14-Pin, 173 mil Wide TSSOP |
| PI4MSD5V9542ALEX | L | 14-Pin, 173 mil Wide TSSOP, Tape & Reel |

Note:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru