19-4138; Rev 0; 10/08

EVALUATION KIT AVAILABLE

Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers

General Description

The MAX4810/MAX4811/MAX4812 integrated circuits generate high-voltage, high-frequency, unipolar or bipolar pulses from low-voltage logic inputs. These dual pulsers feature independent logic inputs, independent high-voltage pulser outputs with active clamps and independent high-voltage supply inputs.

The MAX4810/MAX4811/MAX4812 feature a 9Ω output impedance for the high-voltage outputs, and a 27Ω impedance for the active clamp. The high-voltage outputs are guaranteed to provide 1.3A output current.

All devices use three logic inputs per channel to control the positive and negative pulses and active clamp. Also included are two independent enable inputs. Disabling EN ensures the output MOSFETs are not accidentally turned on during fast power-supply ramping. This allows for faster ramp times and smaller delays between pulsing modes. A low-power shutdown mode reduces power consumption to less than 1µA. All digital inputs are CMOS compatible.

The MAX4810 includes clamp output overvoltage protection, while the MAX4811 features both pulser output and clamp output overvoltage protection. The MAX4812 does not provide overvoltage protection. See the *Ordering Information/Selector Guide*.

The MAX4810/MAX4811/MAX4812 are available in a 56-pin (7mm x 7mm), TQFN exposed-pad package and are specified over the 0°C to +70°C commercial temperature range.

Applications

- Ultrasound Medical Imaging
- Cleaning Equipment
- Flaw Detection
- Piezoelectric Drivers
- Test Instruments

Ordering Information/Selector Guide

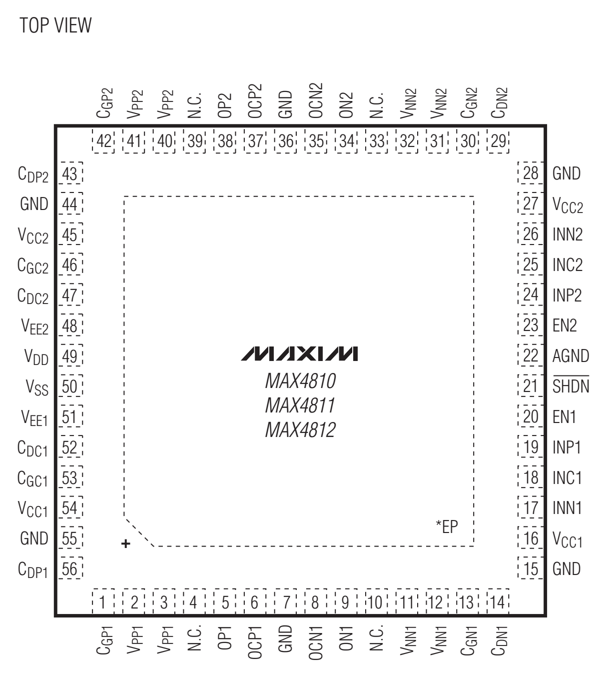
PART	PROTECTED OUTPUTS	OUTPUT CURRENT (A)	PIN-PACKAGE
MAX4810CTN+	OCP_, OCN_	1.3	56 TQFN-EP**
MAX4811CTN+	OCP_, OCN_, OP_, ON_	1.3	56 TQFN-EP**
MAX4812CTN+*	None	1.3	56 TQFN-EP**

Note: *All devices are specified over the 0°C to +70°C operating temperature range.*
+Denotes a lead-free/RoHS-compliant package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Features

- ♦ Highly Integrated, High-Voltage, High-Frequency Unipolar/Bipolar Pulser
- ♦ 9Ω Output Impedance and 1.3A (min) Output Current
- ♦ 27Ω Active Clamp
- ♦ Pulser and Clamp Overvoltage Protection (MAX4810/MAX4811)
- ♦ 0 to +220V Unipolar or ±110V Bipolar Outputs
- ♦ Matched Rise/Fall Times and Matched Propagation Delays
- ♦ CMOS-Compatible Logic Inputs
- ♦ 56-Pin, 7mm x 7mm, TQFN Package

Pin Configuration



TQFN
7mm x 7mm

*EP = EXPOSED PAD, CONNECT EP TO V_{SS}.

Warning: *The MAX4810/MAX4811/MAX4812 are designed to operate with high voltages. Exercise caution.*

Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{DD} Logic Supply Voltage.......................................-0.3V to +6V
$V_{CC\_}$ Output Driver Positive Supply Voltage..........-0.3V to +15V
$V_{EE\_}$ Output Driver Negative Supply Voltage.........-15V to +0.3V
$V_{PP\_}$ High Positive Supply Voltage.......................-0.3V to +230V
$V_{NN\_}$ High Negative Supply Voltage...................-230V to +0.3V
V_{SS} Voltage...($V_{PP\_}$ - 250V) to $V_{NN\_}$
V_{PP1} - V_{NN1}, V_{PP2} - V_{NN2} Supply Voltage............-0.6V to +250V
INP_, INN_, INC_, EN_, $\overline{SHDN}$ Logic Input...-0.3V to V_{DD} + 0.3V
$O_{P\_}$, $O_{CP\_}$, $O_{LN\_}$, $O_{N\_}$ ....(-0.3V + $V_{NN\_}$) to (-0.3V to $V_{PP\_}$)
$C_{GN\_}$ Voltage...........................(-0.3V + $V_{NN\_}$) to (+15V + $V_{NN\_}$)
$C_{GP\_}$ Voltage ....(+0.3V + $V_{PP\_}$) to (-15V + $V_{PP\_}$)
$C_{GC\_}$ Voltage..-15V to +15V
$C_{DC\_}$, $C_{DP\_}$, $C_{DN\_}$ Voltage.....................................-0.3V to $V_{CC\_}$
Peak Current per Output Channel 3.0A
Continuous Power Dissipation (T_A = +70°C) (Note 1)
56-Pin TQFN (derate 40mW/°C above +70°C) 3200mW
Thermal Resistance (Note 2)
θ_{JA}..25°C/W
θ_{JC}...0.8°C/W
Operating Temperature Range..............................0°C to +70°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: This specification is based on the thermal characteristic of the package, the maximum junction temperature, and the setup described by JEDEC 51. The maximum power dissipation for the MAX4810/MAX4811/MAX4812 might be limited by the thermal protection included in the device.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3) (See Figures 8, 9, and 10.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_{DD}, $V_{CC\_}$, $V_{EE\_}$, $V_{PP\_}$, $V_{NN\_}$)						
Logic Supply Voltage	V_{DD}		+2.7	+3	+6	V
Positive Drive Supply Voltage	$V_{CC\_}$		+4.75	+12	+12.6	V
Negative Drive Supply Voltage	$V_{EE\_}$		-12.6	-12	-4.75	V
High-Side Supply Voltage	$V_{PP\_}$		0		$V_{NN\_}$ + 220	V
Low-Side Supply Voltage	$V_{NN\_}$		-200		0	V
$V_{PP\_}$ - $V_{NN\_}$ Supply Voltage			0		+220	V
SUPPLY CURRENT (Single Channel)						
V_{DD} Supply Current	I_{DD}	$V_{INN\_}$/$V_{INP\_}$ = 0 , $V_{\overline{SHDN}}$ = 0			1	µA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz		100	200	
$V_{CC\_}$ Supply Current	$I_{CC\_}$	$V_{\overline{SHDN}}$ = 0, CH1 and CH2			1	µA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, CH1 and CH2		130	200	
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz, $V_{CC\_}$ = 5V, V_{DD} = 3V, only one channel switching		15		mA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz, $V_{CC\_}$ = 12V, V_{DD} = 3V, only one channel switching		36		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), V_{SS} ≤ the lower of V_{NN1} or V_{NN2}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3) (See Figures 8, 9, and 10.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{EE\_}$ Supply Current	$I_{EE\_}$	$V_{\overline{SHDN}}$ = 0, CH1 and CH2			25	µA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, CH1 and CH2			1	
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz, $V_{EE\_}$ = -5V, only one channel switching			200	
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz, $V_{EE\_}$ = -12V, only one channel switching			200	
$V_{PP\_}$ Supply Current	$I_{PP\_}$	$V_{\overline{SHDN}}$ = 0, CH1 and CH2			1	µA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, CH1 and CH2		90	160	
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, no load, only one channel switching		9		mA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{PP\_}$ = +80V, $V_{NN\_}$ = -80V, pulse repetition frequency = 10kHz, f = 10MHz, 4 periods, no load, only one channel switching		0.6		
$V_{NN\_}$ Supply Current	$I_{NN\_}$	$V_{\overline{SHDN}}$ = 0, CH1 and CH2			1	µA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, CH1 and CH2		40	80	
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{\overline{INP\_}}$, f = 5MHz, $V_{NN\_}$ = -5V, $V_{PP\_}$ = +5V, no load, only one channel switching		9		mA
		$V_{EN\_}$ = V_{DD}, $V_{\overline{SHDN}}$ = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{PP\_}$ = +80V, $V_{NN\_}$ = -80V, pulse repetition frequency = 10kHz, f = 10MHz, 4 periods, no load, only one channel switching		0.6		
LOGIC INPUTS (EN_, $\overline{\text{SHDN}}$, INN_, INP_, INC_)						
Low-Level Input Voltage	V_{IL}				0.25 x V_{DD}	V
High-Level Input Voltage	V_{IH}		0.75 x V_{DD}			V
Logic-Input Capacitance	C_{IN}			5		pF
Logic-Input Leakage	I_{IN}	V_{IN} = 0 or V_{DD}			±1	µA
OUTPUT (OUT_)						
OUT_ Output-Voltage Range	$V_{OUT\_}$	No load at OUT_	$V_{NN\_}$		$V_{PP\_}$	V
		Unprotected outputs (see the *Ordering Information/Selector Guide*), 100mA load	$V_{NN\_}$ + 1.5		$V_{PP\_}$ - 1.5	
		Protected outputs (see the *Ordering Information/Selector Guide*), 100mA load	$V_{NN\_}$ + 2.5		$V_{PP\_}$ - 2.5	
Low-Side Small-Signal Output Impedance	R_{OLS}	$I_{OP\_}$ = -100mA, $V_{CC\_}$ = +12V ±5%, DC-coupled		9	17	Ω
		$I_{OP\_}$ = -100mA, $V_{CC\_}$ = +5V ±5%, DC-coupled		9.5	18	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), V_{SS} ≤ the lower of V_{NN1} or V_{NN2}, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3) (See Figures 8, 9, and 10.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side Small-Signal Output Impedance	R_{OHS}	$I_{OP\_}$ = -100mA, $V_{CC\_}$ = +12V ±5%, DC-coupled		10.5	17	Ω
		$I_{OP\_}$ = -100mA, $V_{CC\_}$ = +5V ±5%, DC-coupled		12	18	
Low-Side Output Current	I_{OL}	$V_{CC\_}$ = +12V ±5%, $V_{OUT\_}$ - $V_{NN\_}$ = 100V	1.3			A
High-Side Output Current	I_{OH}	$V_{CC\_}$ = +12V ±5%, $V_{OUT\_}$ - $V_{PP\_}$ = 100V	1.3			A
Off-Output Capacitance	$C_{O(OFF)}$	OP_, ON_, OCP_ and OCN_ connected together, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V; MAX4810		45		pF
		OP_, ON_, OCP_ and OCN_ connected together, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V; MAX4811		75		
Off-Output Leakage Current	I_{LK}	$V_{NN\_}$ = -100V, $V_{PP\_}$ = 100V, EN_ = 0, OUT = -100V to +100V	-1		+1	µA
Low-Side Signal-Clamp Output Impedance	R_{CLS}	$I_{OCN\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$		22	50	Ω
		$I_{OCN\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = -$V_{CC\_}$		24	65	
High-Side Signal-Clamp Output Impedance	R_{CHS}	$I_{OCP\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$		28	50	Ω
		$I_{OCP\_}$ = -100mA, DC-coupled, $V_{CC\_}$ = +5V ±5%, $V_{EE\_}$ = -$V_{CC\_}$		38	65	
Low-Side Gate Short Impedance	R_{LSH}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$, I_{CGN} = 10mA, EN_ = 0			100	Ω
		$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$, I_{CGN} = 10mA, EN_ = V_{DD}	5	7.5	10	kΩ
High-Side Gate Short Impedance	R_{HSH}	$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$, I_{CGN} = 10mA, EN_ = 0			100	Ω
		$V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$, I_{CGN} = 10mA, EN_ = V_{DD}	5	7.5	10	kΩ
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}	Junction temperature rising		150		°C
Thermal-Shutdown Hysteresis				20		°C
DYNAMIC CHARACTERISTICS (R_L = 100Ω, C_L = 100pF, unless otherwise noted)						
Logic Input to Output Rise Propagation Delay	t_{PLH}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 4		15		ns
Logic Input to Output Fall Propagation Delay	t_{PHL}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 4		15		ns
Logic Input to Output Rise Propagation Delay	t_{POH}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 4		15		ns
Logic Input to Output Fall Propagation Delay	t_{POL}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 4		15		ns
Logic Input to Output-Rise Propagation Delay Clamp	t_{PLO}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 4		15		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +6V, $V_{CC\_}$ = +4.75V to +12.6V, $V_{EE\_}$ = -12.6V to -4.75V, $V_{NN\_}$ = -200V to 0, $V_{PP\_}$ = 0 to ($V_{NN\_}$ + 200V), $V_{SS} \leq$ the lower of V_{NN1} or V_{NN2}, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3) (See Figures 8, 9, and 10.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input to Output-Fall Propagation Delay Clamp	t_{PHO}	$V_{CC\_}$ = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, Figure 4		15		ns
OUT_ Rise Time (GND to $V_{PP\_}$)	t_{R0P}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 4		9	20	ns
OUT_ Rise Time ($V_{NN\_}$ to GND)	t_{RN0}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 4		17	35	ns
OUT_ Rise Time ($V_{NN\_}$ to $V_{PP\_}$)	t_{RNP}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 4		10.5	35	ns
OUT_ Fall Time (GND to $V_{NN\_}$)	t_{F0N}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 4		9	20	ns
OUT_ Fall Time ($V_{PP\_}$ to GND)	t_{FP0}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 4		17	35	ns
OUT_ Fall Time ($V_{PP\_}$ to $V_{NN\_}$)	t_{FPN}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$, Figure 4		10.5	35	ns
OUT Enable Time from EN (Figure 5)	t_{EN}	$V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			100	ns
		$V_{CC\_}$ = +5V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			150	
OUT Disable Time from EN (Figure 5)	t_{DI}	$V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			100	ns
		$V_{CC\_}$ = +5V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			150	
Clamp Enable Time from INC (Figure 6)	t_{EN-CL}	$V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			150	ns
		$V_{CC\_}$ = +5V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			180	
Clamp Disable Time from INC (Figure 6)	t_{DI-CL}	$V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			150	ns
		$V_{CC\_}$ = +5V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			150	
Short Enable Time from EN (Figure 7)	t_{EN_SH}	$V_{PP\_}$ = 12V, $V_{NN\_}$ = 0, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			1000	ns
		$V_{PP\_}$ = 5V, $V_{NN\_}$ = 0, $V_{CC\_}$ = +5V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			1000	
Short Disable Time from EN (Figure 7)	t_{DI_SH}	$V_{PP\_}$ = 12V, $V_{NN\_}$ = 0, $V_{CC\_}$ = +12V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			250	ns
		$V_{PP\_}$ = 5V, $V_{NN\_}$ = 0, $V_{CC\_}$ = +5V ± 5%, $V_{EE\_}$ = $-V_{CC\_}$			250	
INP_ to INN_ Overlap Tolerance				|3|		ns
Crosstalk		$V_{PP\_}$ = $V_{CC\_}$ = +5V, $V_{NN\_}$ = $V_{EE\_}$ = -5V, f = 5MHz		69		dB
2nd Harmonic Distortion	2HD	$V_{PP\_}$ = $V_{NN\_}$ = 100V, f_{OUT} = 5MHz, $V_{CC\_}$ = 12V		-48		dB
RMS Output Jitter	t_J	$V_{CC\_}$ = 12V		9		ps

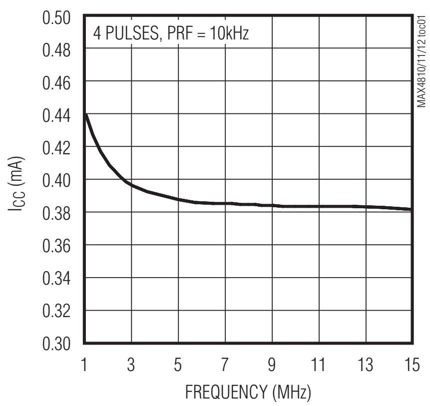
Note 3: Specifications are guaranteed for the stated global conditions, unless otherwise noted and are 100% production tested at T_A = +25°C and T_A = +70°C. Specifications at T_A = 0°C are guaranteed by design.

Note 4: 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

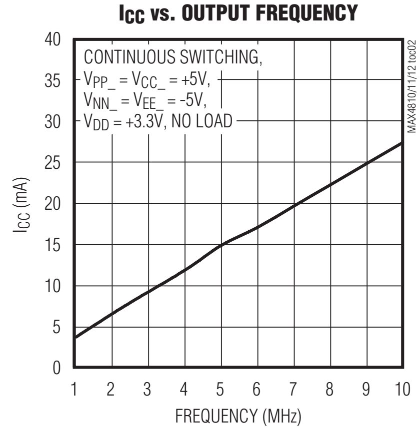
Typical Operating Characteristics

(V_{DD} = +3.3V, $V_{CC\_}$ = +12V, $V_{EE\_}$ = -12V, V_{SS} = -100V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, f_{OUT} = 5MHz, T_A = +25°C, unless otherwise noted.)

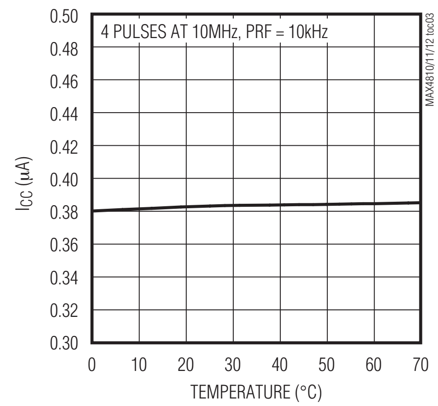
I_{CC} vs. OUTPUT FREQUENCY



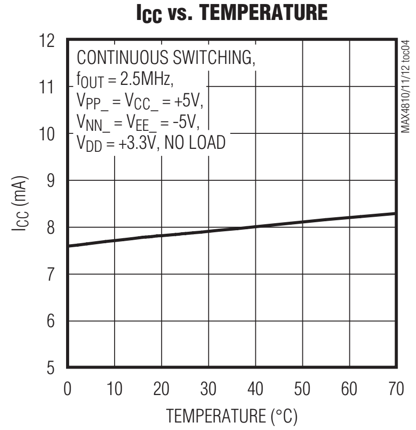
I_{CC} vs. OUTPUT FREQUENCY



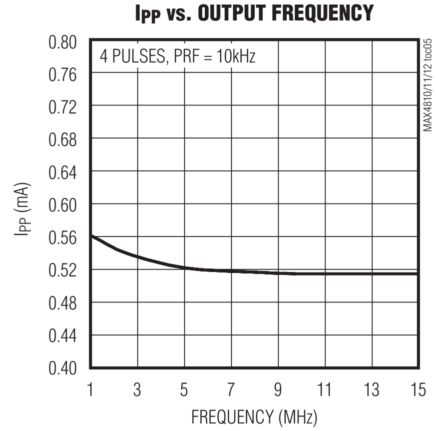
I_{CC} vs. TEMPERATURE



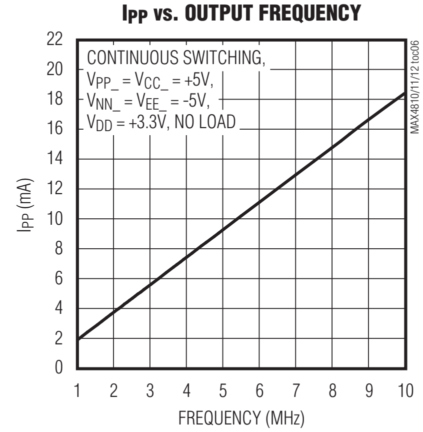
I_{CC} vs. TEMPERATURE



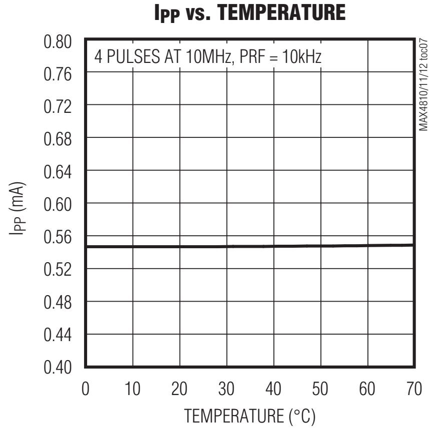
I_{PP} vs. OUTPUT FREQUENCY



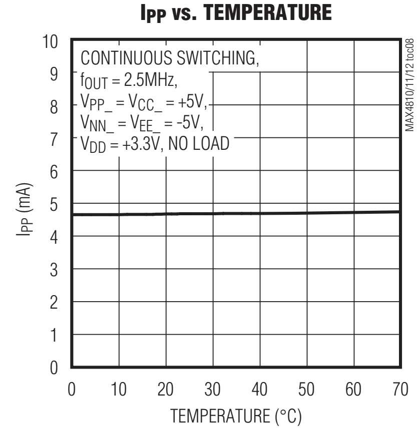
I_{PP} vs. OUTPUT FREQUENCY



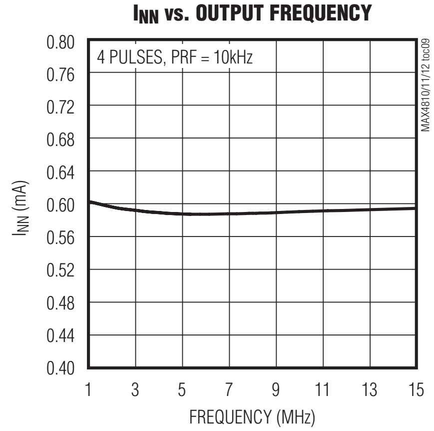
I_{PP} vs. TEMPERATURE



I_{PP} vs. TEMPERATURE



I_{NN} vs. OUTPUT FREQUENCY

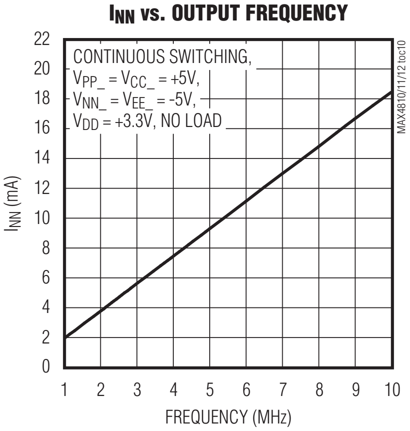


Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers

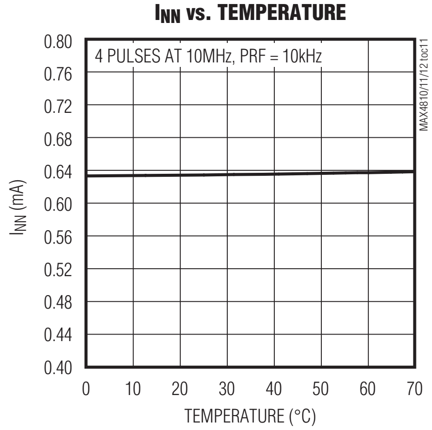
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, $V_{CC\_}$ = +12V, $V_{EE\_}$ = -12V, V_{SS} = -100V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, f_{OUT} = 5MHz, T_A = +25°C, unless otherwise noted.)

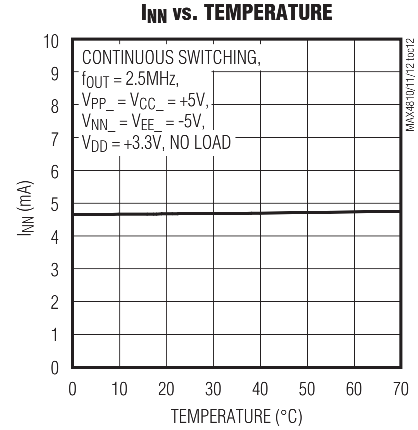
I_{NN} vs. OUTPUT FREQUENCY



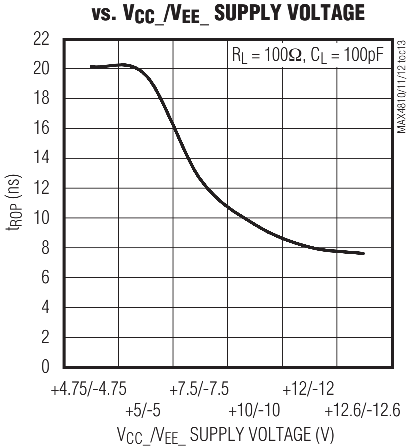
I_{NN} vs. TEMPERATURE



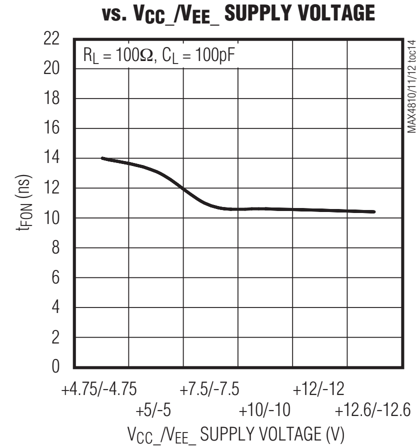
I_{NN} vs. TEMPERATURE



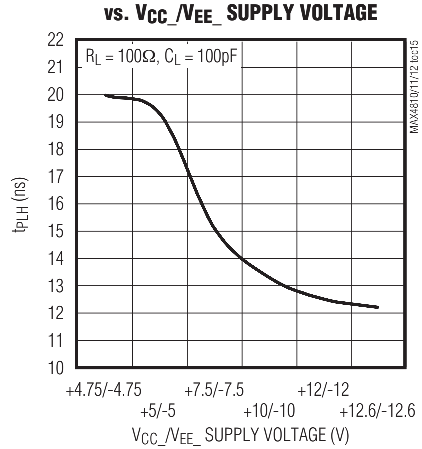
OUT RISE TIME (GND TO $V_{PP\_}$) vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



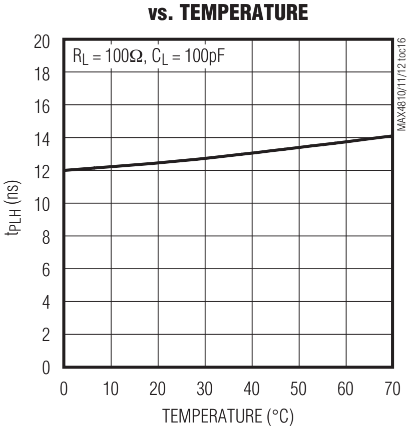
OUT FALL TIME (GND TO $V_{NN\_}$) vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



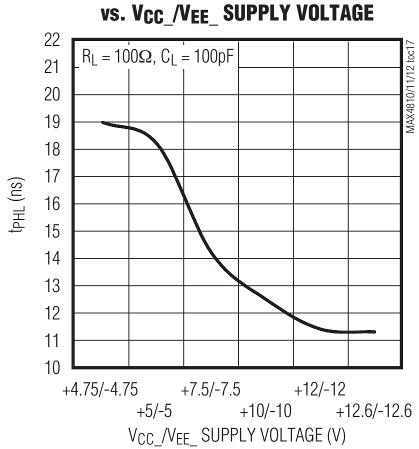
INP-TO-OUT RISE PROPAGATION DELAY vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



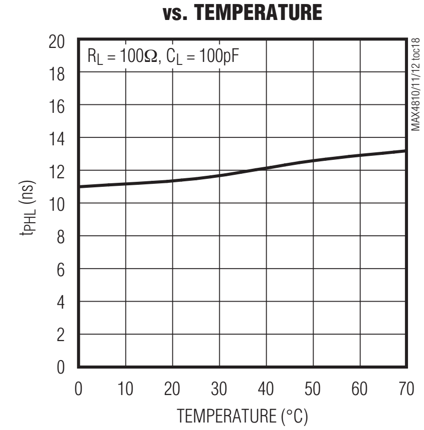
INP-TO-OUT RISE PROPAGATION DELAY vs. TEMPERATURE



INP-TO-OUT FALL PROPAGATION DELAY vs. $V_{CC\_}/V_{EE\_}$ SUPPLY VOLTAGE



INP-TO-OUT FALL PROPAGATION DELAY vs. TEMPERATURE



Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers

Pin Description

PIN	NAME	FUNCTION
1	C_{GP1}	Channel 1 High-Side Gate Input. Connect a 1nF to 10nF capacitor between C_{DP1} and C_{GP1} as close as possible to the device.
2 , 3	V_{PP1}	Channel 1 High-Side Positive Supply Voltage Input. Bypass V_{PP1} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
4, 10, 33, 39	N.C.	No Connection. Not connected internally.
5	OP1	Channel 1 High-Side Drain Output
6	OCP1	Channel 1 High-Side Clamp Output
7, 15, 28, 36, 44, 55	GND	Ground
8	OCN1	Channel 1 Low-Side Clamp Output
9	ON1	Channel 1 Low-Side Drain Output
11, 12	V_{NN1}	Channel 1 High-Side Negative Supply Voltage Input. Bypass V_{NN1} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
13	C_{GN1}	Channel 1 Low-Side Gate Input. Connect a 1nF to 10nF capacitor between C_{DN1} and C_{GN1} as close as possible to the device.
14	C_{DN1}	Channel 1 Low-Side Driver Output. Connect a 1nF to 10nF capacitor between C_{DN1} and C_{GN1} as close as possible to the device.
16, 54	V_{CC1}	Channel 1 Gate-Drive Supply Voltage Input. Bypass V_{CC1} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
17	INN1	Channel 1 Low-Side Logic Input (Table 1)
18	INC1	Channel 1 Clamp Logic Input. Clamps OCP1 and OCN1 are turned on when INC1 is high and when INP1 and INN1 are low (see Table 1).
19	INP1	Channel 1 High-Side Logic Input (Table 1)
20	EN1	Channel 1 Enable Logic Input. Drive EN1 high to enable OP1 and ON1. Pull EN1 low to turn on the gate-source short circuit (see Table 1).
21	$\overline{\text{SHDN}}$	Shutdown Logic Input (Table 1)
22	AGND	Analog Ground. Must be connected to common GND.
23	EN2	Channel 2 Enable Logic Input. Drive EN2 high to enable OP2 and ON2. Pull EN2 low to turn on the gate-source short circuit. See Table 1.
24	INP2	Channel 2 High-Side Logic Input (Table 1)
25	INC2	Channel 2 Clamp Logic Input. Clamps OCP2 and OCN2 are turned on when INC2 is high and when INP2 and INN2 are low. See Table 1.
26	INN2	Channel 2 Low-Side Logic Input (Table 1)
27, 45	V_{CC2}	Channel 2 Gate-Drive Supply Voltage Input. Bypass V_{CC2} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
29	C_{DN2}	Channel 2 Low-Side Driver Output. Connect a 1nF to 10nF capacitor between C_{DN2} and C_{GN2} as close as possible to the device.
30	C_{GN2}	Channel 2 Low-Side Gate Input. Connect a 1nF to 10nF capacitor between C_{DN2} and C_{GN2} as close as possible to the device.

Pin Description (continued)

PIN	NAME	FUNCTION
31, 32	V_{NN2}	Channel 2 High-Side Negative Supply Voltage Input. Bypass V_{NN2} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
34	ON2	Channel 2 Low-Side Drain Output
35	OCN2	Channel 2 Low-Side Clamp Output
37	OCP2	Channel 2 High-Side Clamp Output
38	OP2	Channel 2 High-Side Drain Output
40, 41	V_{PP2}	Channel 2 High-Side Supply Voltage Input. Bypass V_{PP2} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
42	C_{GP2}	Channel 2 High-Side Gate Input. Connect a 1nF to 10nF capacitor between C_{DP2} and C_{GP2} as close as possible to the device.
43	C_{DP2}	Channel 2 High-Side Driver Output. Connect a 1nF to 10nF capacitor between C_{DP2} and C_{GP2} as close as possible to the device.
46	C_{GC2}	Channel 2 High-Side Clamp Gate Input. Connect a 1nF to 10nF capacitor between C_{DC2} and C_{GC2} as close as possible to the device.
47	C_{DC2}	Channel 2 High-Side Clamp Driver Output. Connect a 1nF to 10nF capacitor between C_{DC2} and C_{GC2} as close as possible to the device.
48	V_{EE2}	Channel 2 Negative Supply Input. $\|V_{EE2}\| \leq V_{CC2}$. Gate Drive Supply Voltage for the OCP clamp. Bypass V_{EE2} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
49	V_{DD}	Logic Supply Voltage Input. Bypass V_{DD} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
50	V_{SS}	Substrate Voltage. Connect V_{SS} to a voltage equal to or more negative than the more negative of V_{NN1} or V_{NN2}.
51	V_{EE1}	Channel 1 Negative Supply Input. $\|V_{EE1}\| \leq V_{CC1}$. Gate Drive Supply Voltage for the OCP clamp. Bypass V_{EE1} to GND with a 0.1µF as close as possible to the device. See the *Power Supplies and Bypassing* section. Depending on the output, additional bypassing may be required.
52	C_{DC1}	Channel 1 High-Side Clamp Driver Output. Connect a 1nF to 10nF capacitor between C_{DC1} and C_{GC1} as close as possible to the device.
53	C_{GC1}	Channel 1 High-Side Clamp Gate Input. Connect a 1nF to 10nF capacitor between C_{DC1} and C_{GC1} as close as possible to the device.
56	C_{DP1}	Channel 1 High-Side Driver Output. Connect a 1nF to 10nF capacitor between C_{DP1} and C_{GP1} as close as possible to the device.
—	EP	Exposed Pad. EP must be connected to V_{SS}. Do not use EP as the only V_{SS} connection for the device.

Detailed Description

The MAX4810/MAX4811/MAX4812 are dual high-voltage, high-speed pulsers that can be independently configured for either unipolar or bipolar pulse outputs. These devices have independent logic inputs for full pulse control and independent active clamps. The clamp input, INC_, can be set high to activate the clamp automatically when the device is not pulsing to the positive or negative high-voltage supplies.

Logic Inputs (INP_, INN_, INC_, EN_, $\overline{\text{SHDN}}$)

The MAX4810/MAX4811/MAX4812 have a total of nine logic input signals. SHDN controls power-up and power-down of the device. There are two sets of INP_, INN_, INC_, and EN_ signals: one for each channel. INP_

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Table 1. Truth Table

INPUTS					OUTPUTS			STATE
$\overline{SDHN}$	EN_	INP_	INN_	INC_	OP_	ON_	OCP_, OCN_	
0	X	X	X	0	High impedance	High impedance	High impedance	Powered down, INP_/INN_ disabled, gate-source short disabled
0	X	X	X	1	High impedance	High impedance	GND	Powered down, INP_/INN_ disabled, gate-source short disabled
1	0	X	X	0	High impedance	High impedance	High impedance	Powered up, INP_/INN_ disabled, gate-source short enabled
1	0	X	X	1	High impedance	High impedance	GND	Powered up, INP_/INN_ disabled, gate-source short enabled
1	1	0	0	0	High impedance	High impedance	High impedance	Powered up, all inputs enabled, gate-source short disabled
1	1	0	0	1	High impedance	High impedance	GND	Powered up, all inputs enabled, gate-source short disabled
1	1	0	1	X	High impedance	$V_{NN\_}$	High impedance	Powered up, all inputs enabled, gate-source short disabled
1	1	1	0	X	$V_{PP\_}$	High impedance	High impedance	Powered up, all inputs enabled, gate-source short disabled
1	1	1	1	X	$V_{PP\_}$	$V_{NN\_}$	High impedance	Not allowed (3ns maximum overlap)

X = Don't care.
0 = Logic-low.
1 = Logic-high.

controls the on and off states of the high side FET, INN_ controls the on and off states of the low side FET, INC_ controls the active clamp and EN_ controls the gate to source short. These signals give complete control of the output stage of each driver (see Table 1 for all logic combinations).

The MAX4810/MAX4811/MAX4812 logic inputs are CMOS logic compatible and the logic level are referenced to V_{DD} for maximum flexibility. The low 5pF (typ) input capacitance of the logic inputs reduces loading and increases switching speed.

High-Voltage Output Protection (MAX4811 Only)

The high-voltage outputs of the MAX4811 feature an integrated overvoltage protection circuit that allows the user to implement multilevel pulsing by connecting the outputs of multiple pulser channels in parallel. Internal diodes in series with the ON_ and OP_ outputs prevent the body diode of the high-side and low-side FETs from switching on when a voltage greater than $V_{NN\_}$ or $V_{PP\_}$ is present on the output. See Figure 2.

Active Clamps

The MAX4810/MAX4811/MAX4812 feature an active clamp circuit to improve pulse quality and reduce 2nd harmonic output. The clamp circuit consists of an N-channel (DC-coupled) and a P-channel (AC and DC delay coupled) high-voltage FETs that are switched on or off by the logic clamp input (INC_). The MAX4810/MAX4811 feature protected clamp devices, allowing the clamp circuit to be used in bipolar pulsing circuits (see Figures 1 and 2). A diode in series with the OCN_ output prevents the body diode of the low-side FET from turning on when a voltage lower than GND is present. Another diode in series with the OCP_ output prevents the body diode of the high-side FET from turning on when a voltage higher than ground is present. The MAX4812 does not have diode protection on the clamp outputs. Thus, the device is suitable for use in circuits where only unipolar pulsing is required.

The user can connect the active clamp input (INC_) to a logic-high voltage and drive only the INP_ and INN_ inputs to minimize the number of signals used to drive the device. In this case, whenever both the INP_ and INN_ inputs are low and the INC_ input is high, the active clamp circuit pulls the output to GND through the OCP_ and OCN_ outputs (see Table 1 for more information).

Power-Supply Ramping and Gate-Source Short Circuit

The MAX4810/MAX4811/MAX4812 include a gate-source short circuit that is controlled by the enable input (EN_). When $\overline{SHDN}$ is high and EN is low, a 60Ω switch shorts together the gate and source of the high-side output FET. At the same time, a similar switch shorts the gate and source of the low-side output FET (Table 1). The gate-source short circuit prevents accidental turn-on of the output FETs due to the ramping voltage on $V_{PP\_}$ and $V_{NN\_}$, and allows for faster ramping rates and smaller delay times between pulsing modes.

Shutdown Mode

$\overline{SHDN}$ is common to both channel 1 and channel 2 and powers up or down the device. Drive $\overline{SHDN}$ low to power down all internal circuits (except the clamp circuits). When $\overline{SHDN}$ is low, the device is in the lowest power state (1µA) and the gate-source short circuit is disabled. The device takes 1µs (typ) to become active when $\overline{SHDN}$ is disabled.

Thermal Protection

A thermal shutdown circuit with a typical threshold of +150°C prevents damage due to excessive power dissipation. When the junction temperature exceeds T_J = +150°C, all outputs are disabled. Normal operation typically resumes after the IC's junction temperature drops below +130°C.

Applications Information

AC-Coupling Capacitor Selection

The value of all AC-coupling capacitors (between $C_{DP\_}$ and C_{GP}, and between $C_{DN\_}$ and $C_{GN\_}$) should be between 1nF to 10nF. The voltage rating of the capacitor should be at least as high as $V_{PP\_}$. The capacitors should be placed as close as possible to the device.

Because INP_ and part of INC_ are AC-coupled to the output devices, they cannot be driven high indefinitely when the device is active.

Power Dissipation

The power dissipation of the MAX4810/MAX4811/MAX4812 consists of three major components caused by the current consumption from $V_{CC\_}$, $V_{PP\_}$, and $V_{NN\_}$. The sum of these components ($P_{VCC\_}$, $P_{VPP\_}$ and $P_{VNN\_}$) must be kept below the maximum power-dissipation limit. See the *Typical Operating Characteristics* section for more information on typical supply currents versus switching frequencies.

The device consumes most of the supply current from $V_{CC\_}$ supply to charge and discharge internal nodes such as the gate capacitance of the high-side FET (C_P) and the low-side FET (C_N). Neglecting the small quiescent supply current and a small amount of current used to charge and discharge the capacitances at the internal gate clamp FETs, the power consumption can be estimated as follows:

$$P_{VCC} = \left[\left(C_N \times V_{CC\_}{}^2 \times f_{IN}\right) + \left(C_P \times V_{CC\_}{}^2 \times f_{IN}\right)\right] \times \left(BRF \times BTD\right)$$

$$f_{IN} = f_{INN} + f_{INP}$$

Where f_{INN} and f_{INP} are the switching frequency of the inputs INN, INP respectively, and where BRF is the burst repitition frequency and BTD is the burst time duration. The typical value of the gate capacitances of the power FET are C_N = 0.2nF, C_P = 0.4nF.

For an output load that has a resistance of R_L and capacitance of C_L, the MAX4810/MAX4811/MAX4812 power dissipation can be estimated as follows (assume square wave output and neglect the resistance of the switches):

$$P_{VPP} = \left\{\left[\left(C_O + C_L\right) \times f_{IN} \times \left(V_{PP\_} - V_{NN\_}\right)^2\right] + \left[\frac{V_{PP\_}{}^2}{R_L} \times \frac{1}{2}\right] \times \left(BRF \times BTD\right)\right\}$$

where C_O is the output capacitance of the device.

Power Supplies and Bypassing

The MAX4810/MAX4811/MAX4812 operate from independent supply voltage sets (only V_{DD} and V_{SS} are common to both channels). The logic input circuit operates from a +2.7V to +6V single supply (V_{DD}). The level-shift driver dual supplies, $V_{CC\_}/V_{EE\_}$ operate from ±4.75V to ±12.6V.

The $V_{PP\_}/V_{NN\_}$ high-side and low-side supplies are driven from a single positive supply up to +220V, from a single negative supply up to -200V, or from ±110V dual supplies. Either $V_{PP\_}$ or $V_{NN\_}$ can be set at 0. Bypass each supply input to ground with a 0.1µF capacitor as close as possible to the device.

Depending on the load of the input, additional bypassing may be needed to keep the output of $V_{NN\_}$ and $V_{PP\_}$ stable during output transitions. For example, with

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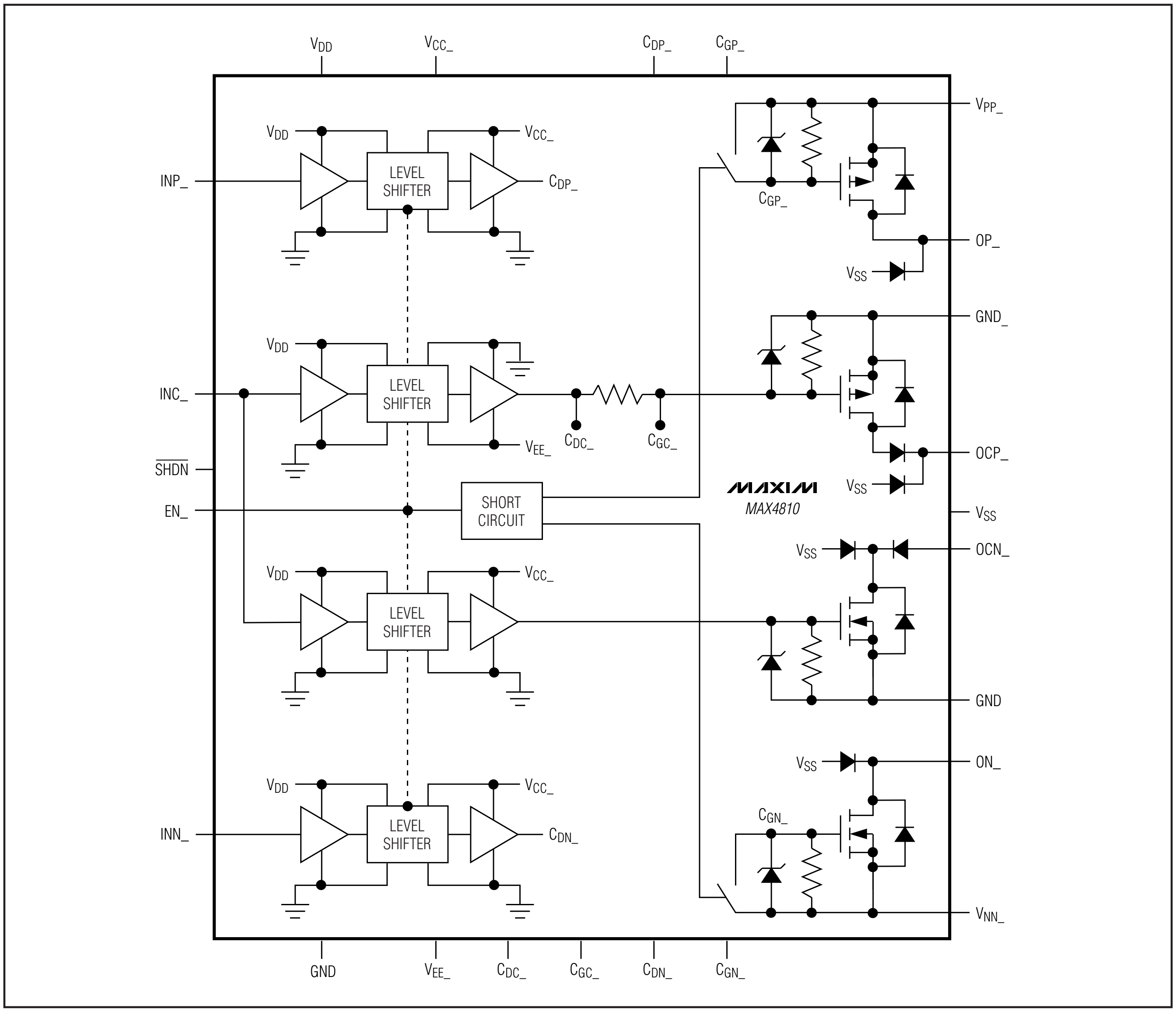

Figure 1. MAX4810 Simplified Functional Diagram for One Channel

C_{OUT} = 100pF and R_{OUT} = 100Ω load, additional 10µF (typ) capacitor is recommended. V_{SS} is the substrate voltage and must be connected to a voltage equal to or more negative than the more negative voltage of V_{NN1} or V_{NN2}.

Exposed Pad and Layout Concerns

The MAX4810/MAX4811/MAX4812 provide an exposed pad (EP) underneath the TQFN package for improved thermal performance. EP is internally connected to V_{SS}. Connect EP to V_{SS} externally and do not run traces under the package to avoid possible short circuits. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through to the solder-side copper by several plated holes to a large heat spreading copper area to conduct heat away from the device.

The MAX4810/MAX4811/MAX4812 high-speed pulsers require low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize

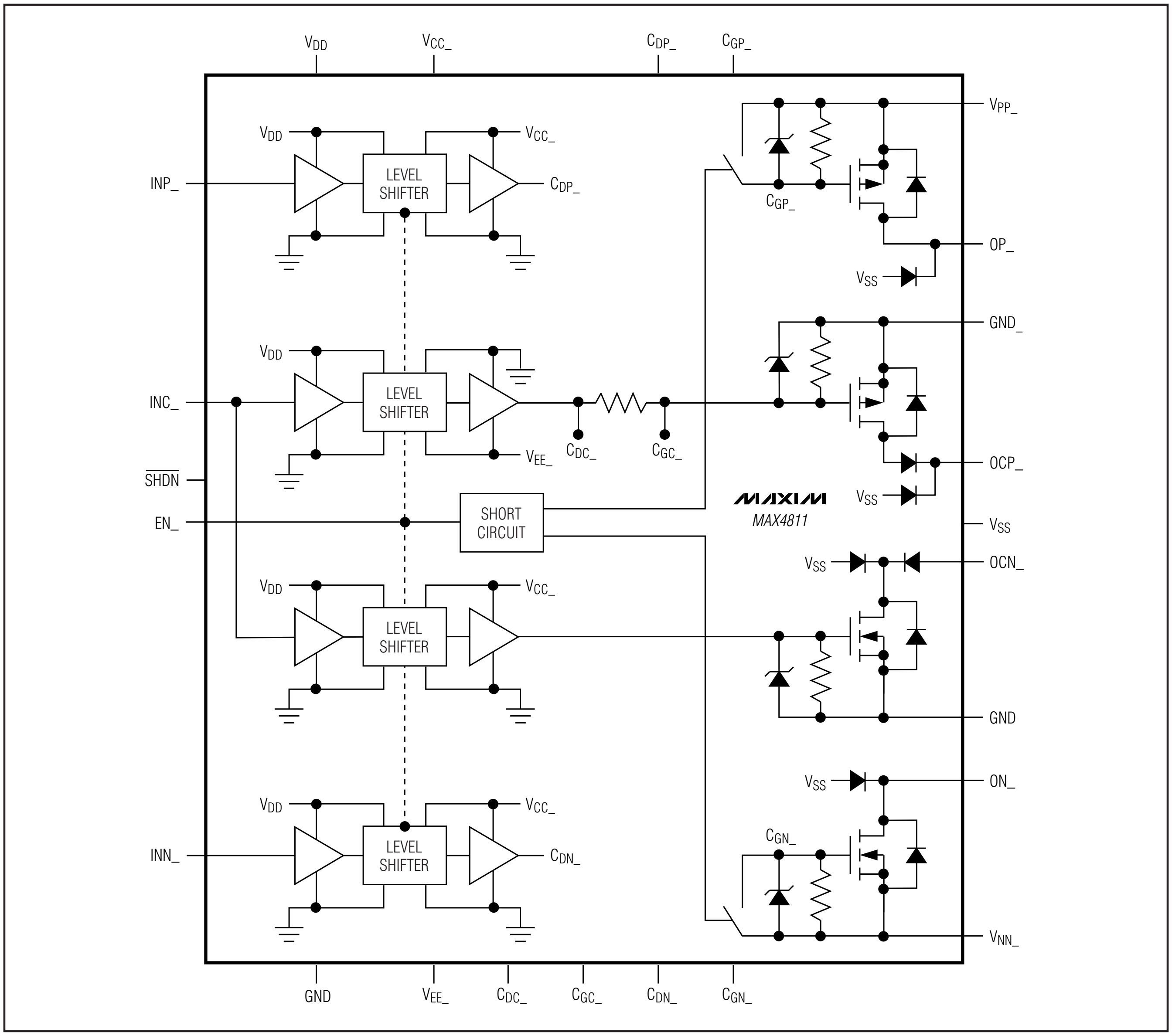

Figure 2. MAX4811 Simplified Functional Diagram for One Channel

trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

Supply Sequencing

V_{SS} must be lower than or equal to the more negative voltage of V_{NN1} or V_{NN2} at all times. No other power-supply sequencing is required for the MAX4810/MAX4811/MAX4812.

Typical Application Circuits

Figures 8, 9, and 10 show typical applications for the MAX4810/MAX4811/MAX4812. Figure 8 shows the MAX4810 used in a bipolar pulsing connection. Figure 9 shows the MAX4811 in a five-level pulsing application, and Figure 10 shows the MAX4812 used in a unipolar application.

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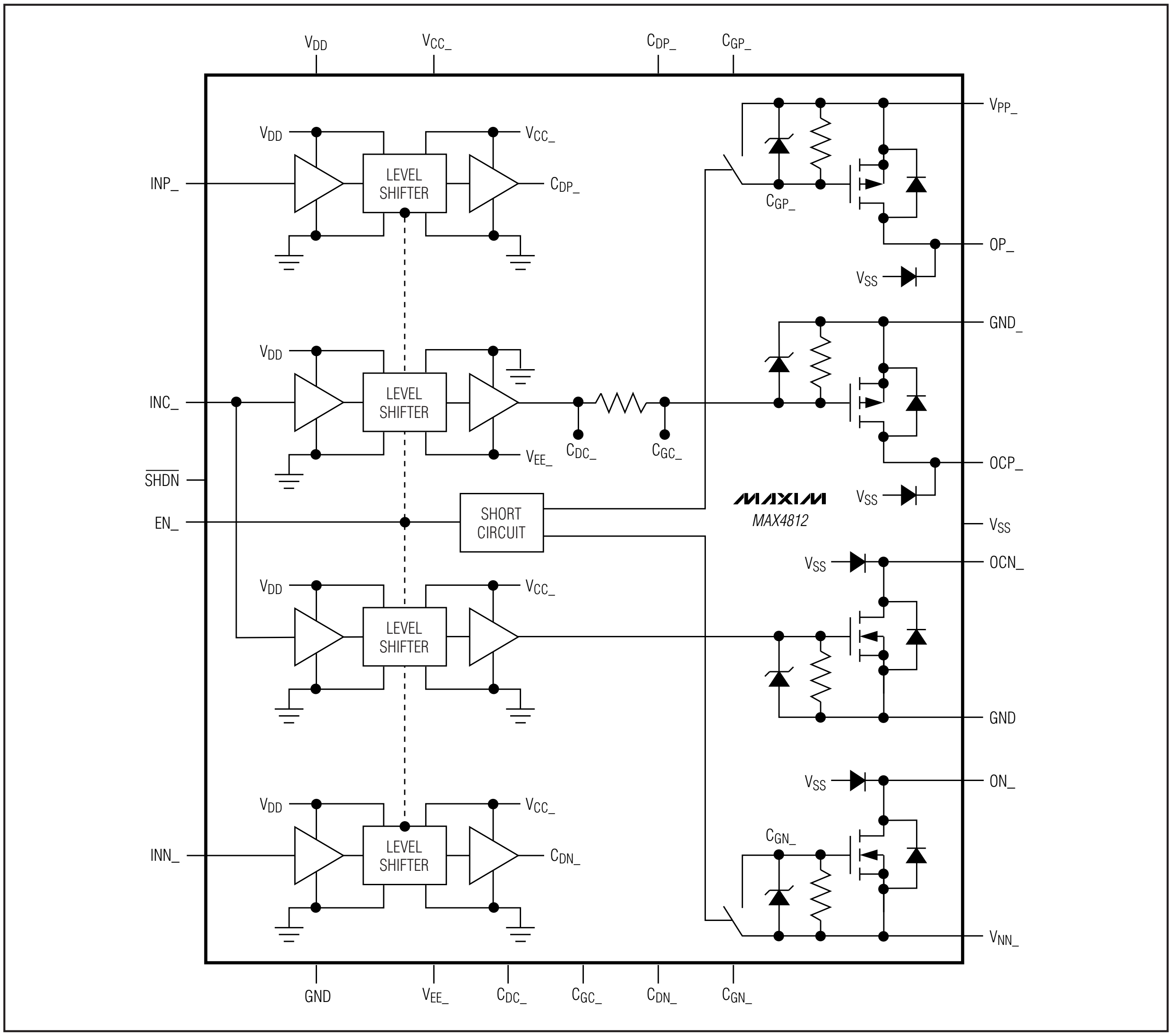

Figure 3. MAX4812 Simplified Functional Diagram for One Channel

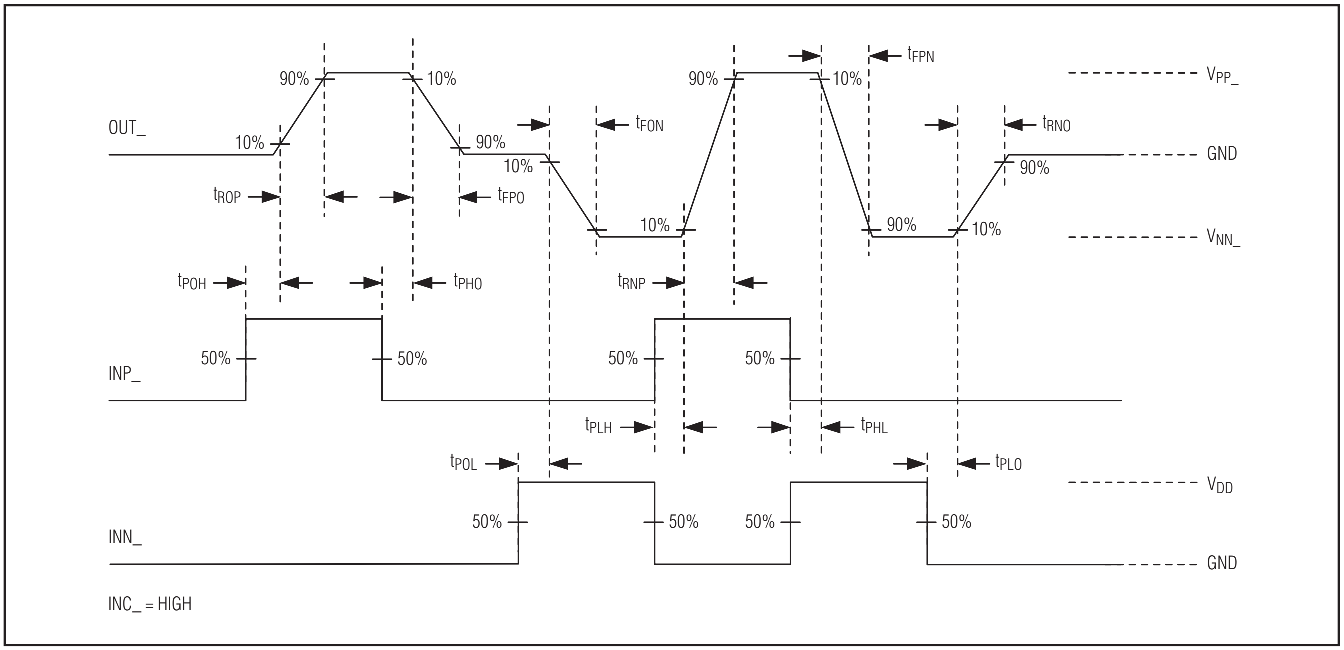

Figure 4. Detailed Timing (R_L = 100Ω, C_L = 100pF)

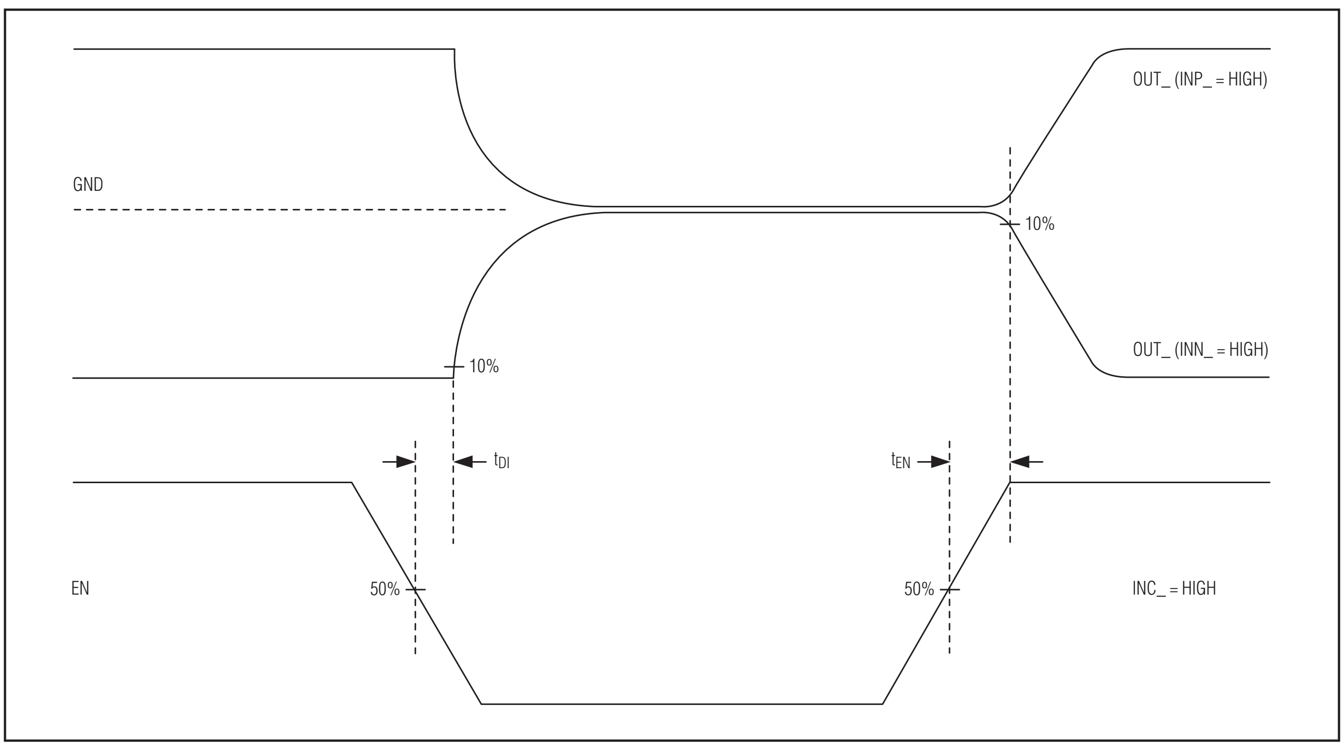

Figure 5. Enable Timing (R_L = 100Ω, C_L = 100pF)

Dual, Unipolar/Bipolar, High-Voltage Digital Pulsers

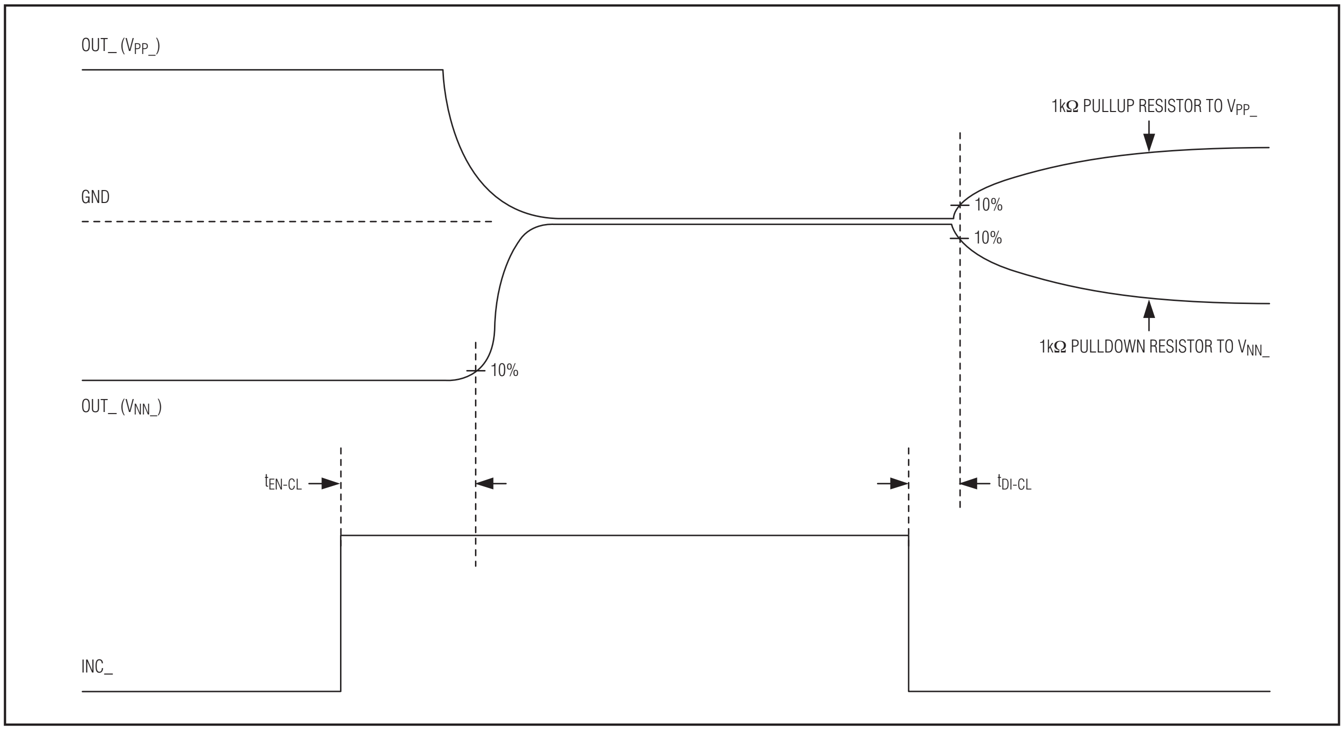

Figure 6. Active Clamp Timing

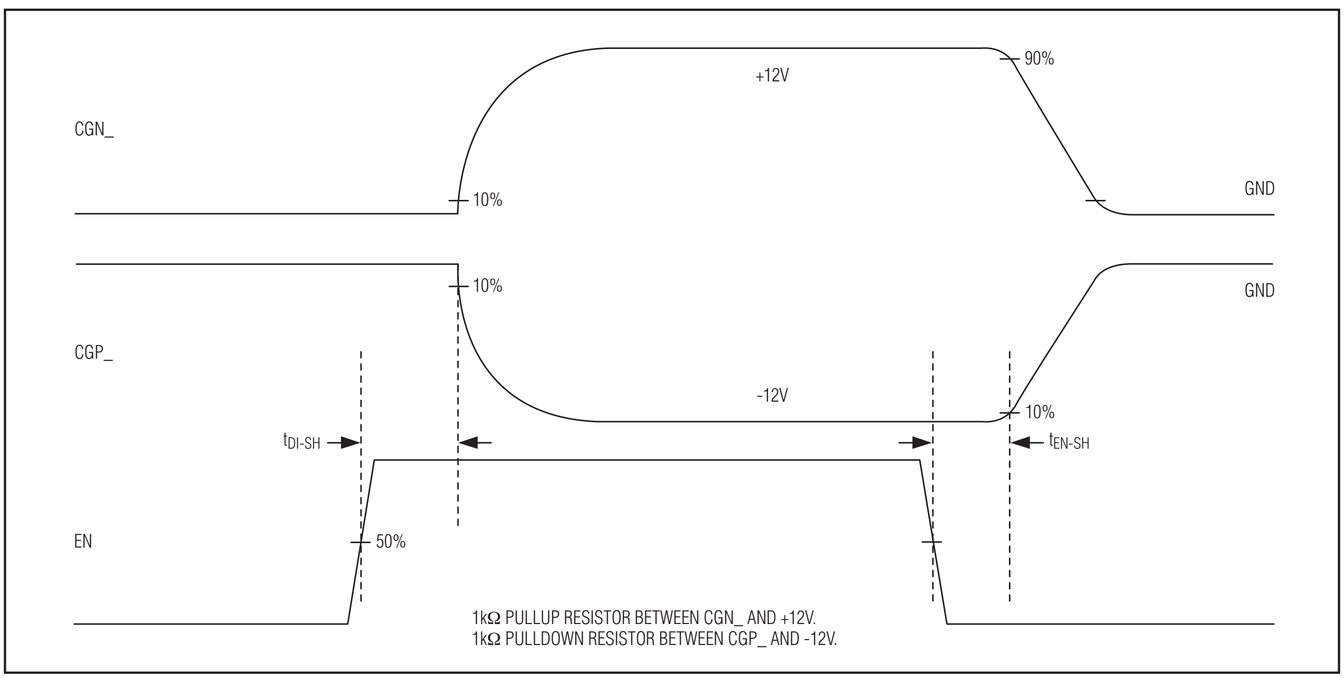

Figure 7. Short-Circuit Timing

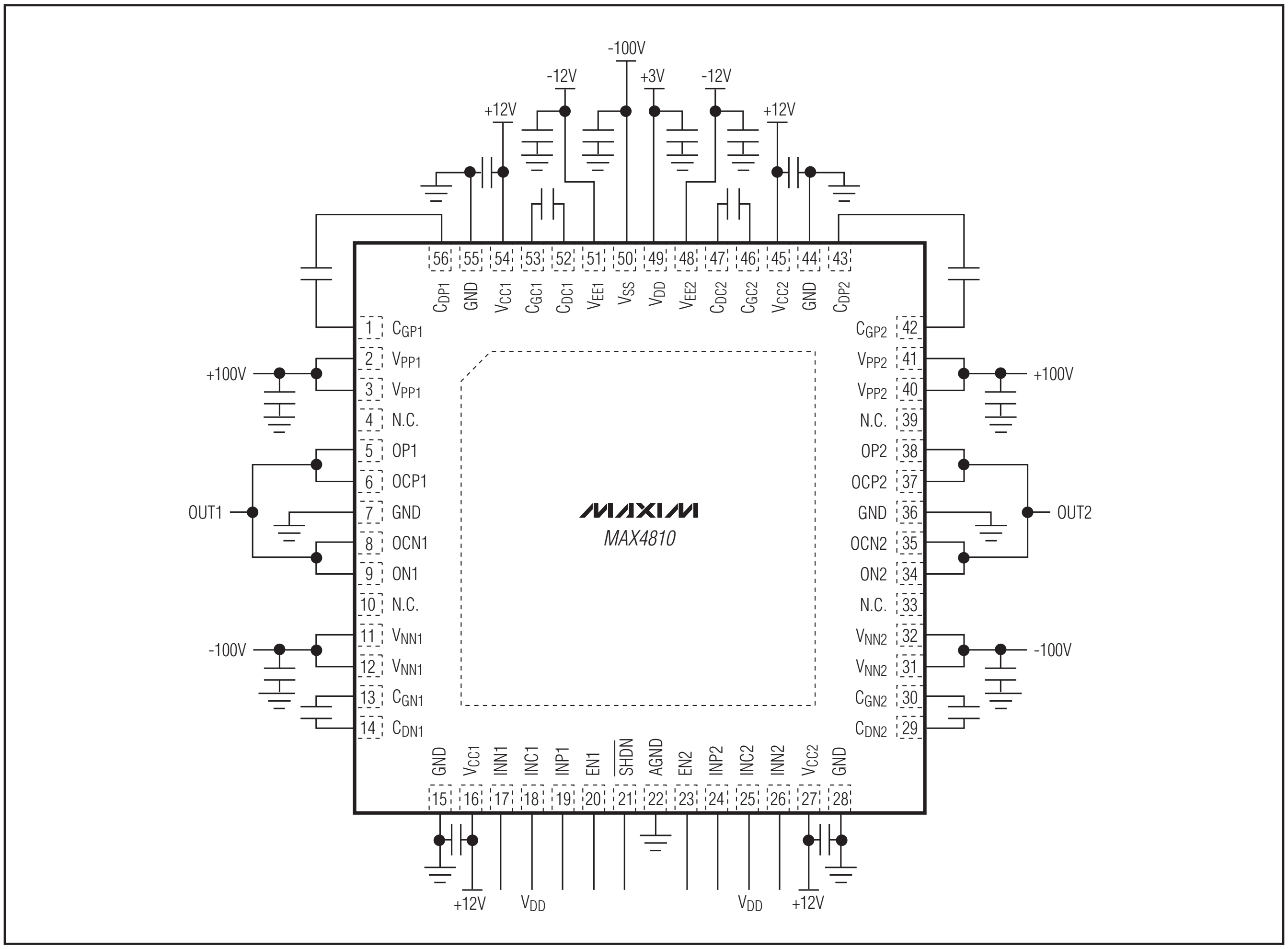

Figure 8. MAX4810: Dual Bipolar Pulsing, ±100V, GND

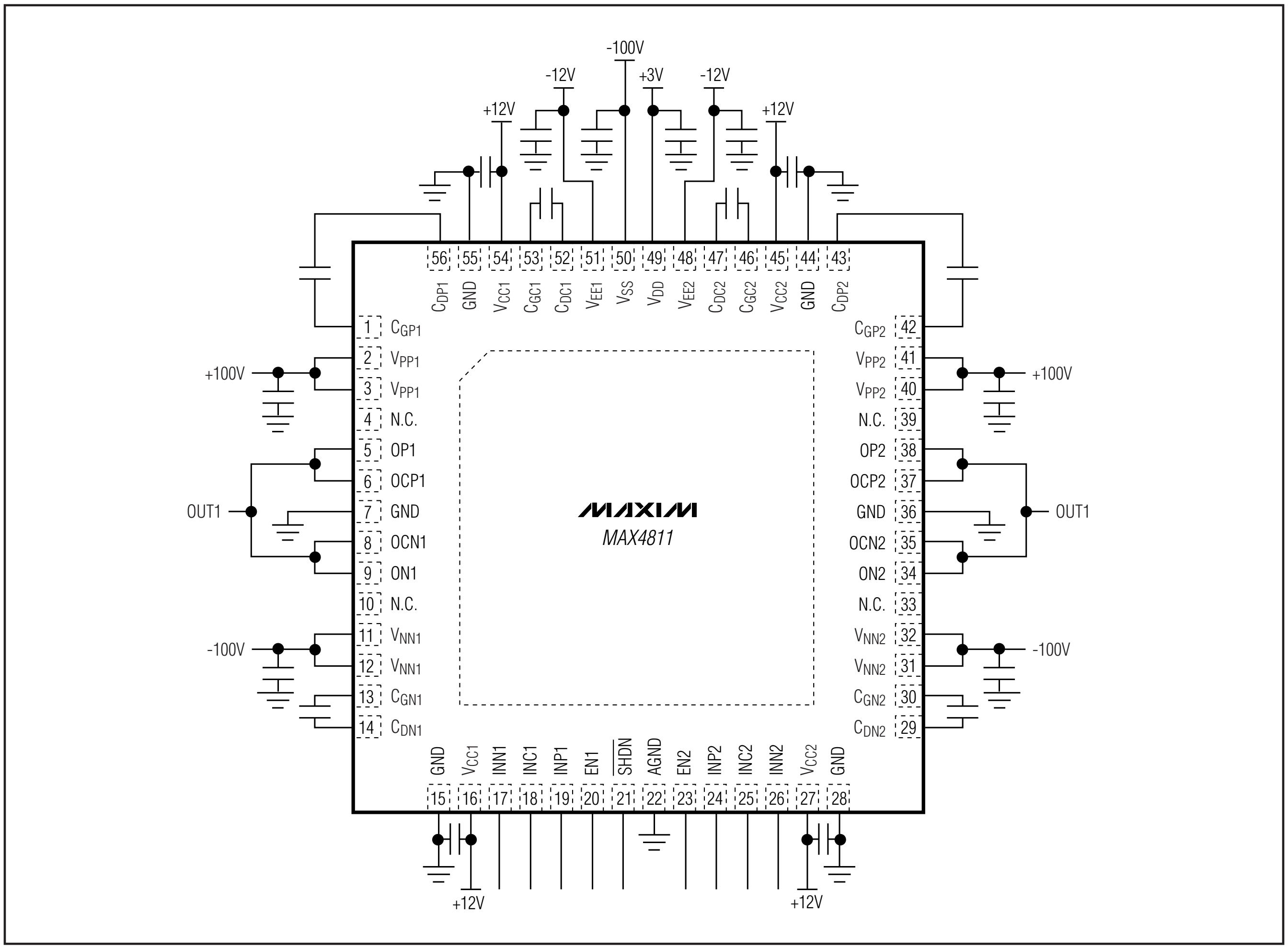

Figure 9. MAX4811: Five-Level Pulsing, ±100V, ±50V, GND

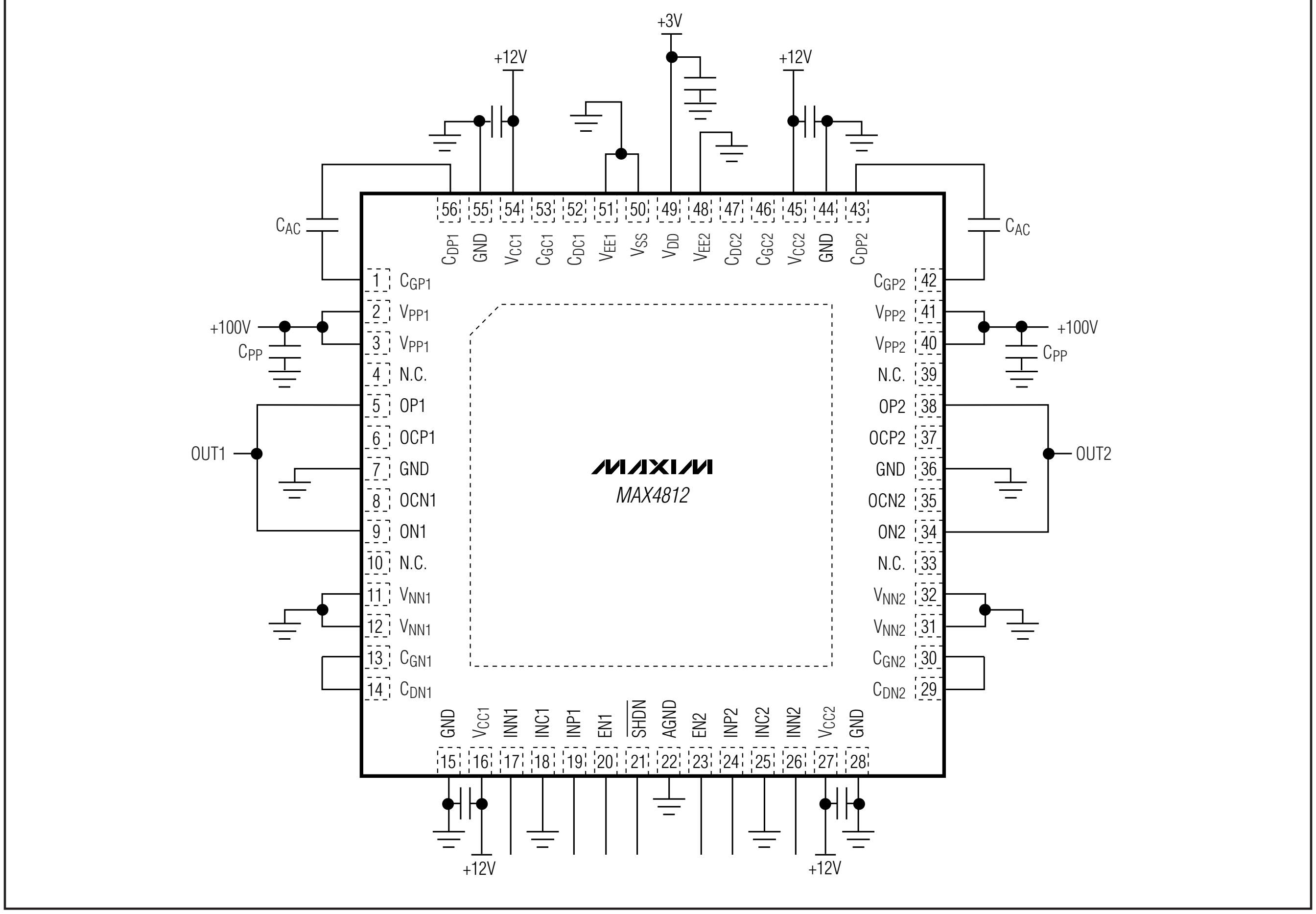

Figure 10. MAX4812: Dual Unipolar Pulsing, +100V, GND

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN	T5677-1	21-0144