30 V, 7.5 MHz, Low Bias Current, Single-Supply, RRO, Precision Op Amp

Data Sheet

ADA4622-2

FEATURES

Next generation of the AD822
Wide bandwidth: 8 MHz typical
High slew rate: +23 V/µs/−18 V/µs typical
Low input bias current: ±10 pA maximum at T_A = 25°C
Low offset voltage
- **A grade: ±0.8 mV maximum at T_A = 25°C**
- **B grade: ±0.35 mV maximum at T_A = 25°C**

Low offset voltage drift
- **A grade: ±2 µV/°C typical, ±15 µV/°C maximum**
- **B grade: ±2 µV/°C typical, ±5 µV/°C maximum**

Input voltage range includes Pin V−
Rail-to-rail output
Input electromagnetic interference (EMI) filters
- **90 dB typical at f = 1000 MHz and f = 2400 MHz**

Industry-standard package and pinouts

APPLICATIONS

High output impedance sensor interfaces
Photodiode sensor interfaces
Transimpedance amplifiers
ADC drivers
Precision filters and signal conditioning

PIN CONFIGURATION

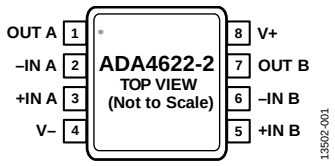

Figure 1. 8-Lead MSOP (RM Suffix) Pin Configuration (See the Pin Configurations and Function Descriptions Section for Additional Pin Configurations)

GENERAL DESCRIPTION

The ADA4622-2 is the next generation of the AD822 single-supply, rail-to-rail output (RRO), precision junction field effect transistors (JFET) input op amp. The ADA4622-2 includes many improvements that make it desirable as an upgrade without compromising the flexibility and ease of use that makes the AD822 useful for a wide variety of applications.

The input voltage range includes the negative supply and the output swings rail-to-rail. Input EMI filters are added to increase the signal robustness in the face of closely located switching noise sources.

The speed in terms of bandwidth and slew rate is increased along with a strong output drive to improve settling time performance and enable the device to drive the inputs of modern single-ended, successive approximation register (SAR) analog-to-digital converters (ADCs).

Voltage noise is reduced; broadband noise is reduced by 25% and 1/f is reduced by half while keeping the supply current the same as the AD822. DC precision in the ADA4622-2 improved from the AD822 with half the offset and a maximum thermal drift specification added to the ADA4622-2. The common-mode rejection ratio (CMRR) is improved from the AD822 to make the ADA4622-2 more suitable when used in noninverting gain and difference amplifier configurations.

The ADA4622-2 is specified for operation over the extended industrial temperature range of −40°C to +125°C and operates from 5 V to 30 V with specifications at +5 V, ±5 V, and ±15 V. The ADA4622-2 is available in 8-lead SOIC, 8-lead MSOP, and 8-lead LFCSP packages.

Rev. A
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REVISION HISTORY

2/16—Rev. 0 to Rev. A

Added 8-Lead LFCSP ... Universal
Changes to General Description Section ... 1
Changes to Settling Time to 0.1% Parameter and Settling Time to 0.01% Parameter, Table 1 ... 4
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Added Pin Configurations and Function Descriptions Section, Figure 2, Figure 3, Table 6, Figure 4, and Table 7; Renumbered Sequentially ... 10
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10/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, V_{SY} = ±15 V

Supply voltage (V_{SY}) = ±15 V, common-mode voltage (V_{CM}) = output voltage (V_{OUT}) = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
A Grade				0.04	±0.8	mV
		−40°C < T_A < +125°C			±2	mV
B Grade				0.04	±0.35	mV
		−40°C < T_A < +125°C			±0.8	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
A Grade		−40°C < T_A < +125°C		±2	±15	μV/°C
B Grade		−40°C < T_A < +125°C		±2	±5	μV/°C
Input Bias Current	I_B			2	±10	pA
		−40°C < T_A < +125°C			±1.5	nA
		V_{CM} = V−		−15		pA
Input Offset Current	I_{OS}				±10	pA
		−40°C < T_A < +125°C			±0.5	nA
Input Voltage Range	IVR		(V−) − 0.2		(V+) − 1	V
Common-Mode Rejection Ratio	CMRR					
A Grade		V_{CM} = V− to (V+) − 3 V	84	100		dB
		−40°C < T_A < +125°C	81			dB
B Grade		V_{CM} = V− to (V+) − 3 V	87	100		dB
		−40°C < T_A < +125°C	85			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_{OUT} = −14.5 V to +14.5 V	117	122		dB
		−40°C < T_A < +125°C	109			dB
		R_L = 1 kΩ, V_{OUT} = −14 V to +14 V	102	110		dB
		−40°C < T_A < +125°C	93			dB
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		10^{13}		Ω
	R_{CM}	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	I_{SOURCE} = 1 mA	50	30		mV
		−40°C < T_A < +125°C	100			mV
		I_{SOURCE} = 15 mA	700	500		mV
		−40°C < T_A < +125°C	900			mV
Low	V_{OL}	I_{SINK} = 1 mA		45	65	mV
		−40°C < T_A < +125°C			120	mV
		I_{SINK} = 15 mA		315	450	mV
		−40°C < T_A < +125°C			750	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		20		mA
Short-Circuit Current	I_{SC}	Sourcing		42		mA
		Sinking		−51		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, gain (A_V) = 1		0.1		Ω
		A_V = 10		0.4		Ω
		A_V = 100		3		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4 V to ±18 V	87	103		dB
		−40°C < T_A < +125°C	81			dB
Supply Current per Amplifier	I_{SY}			665	700	µA
		−40°C < T_A < +125°C			725	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = ±12.5 V, R_L = 2 kΩ, load capacitor (C_L) = 100 pF, A_V = 1				
		Low to high transition		23		V/µs
		High to low transition		−18		V/µs
Gain Bandwidth Product	GBP	A_V = 100		8		MHz
Unity-Gain Crossover	UGC	A_V = 1		7		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		15.5		MHz
Phase Margin	ΦM			53		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 10 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		1.5		µs
Settling Time to 0.01%	t_S	V_{IN} = 10 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		2		µs
EMI REJECTION RATIO	EMIRR	V_{IN} = 100 mV p-p				
f = 1000 MHz				90		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.75		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		30		nV/√Hz
		f = 100 Hz		15		nV/√Hz
		f = 1 kHz		12.5		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, input voltage (V_{IN}) = 7 V rms at 1 kHz				
Bandwidth (BW) = 80 kHz				0.0003		%
BW = 500 kHz				0.00035		%
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				2.5		µV/°C
Input Bias Current				0.5	5	pA
CROSSTALK	C_S	R_L = 5 kΩ, V_{IN} = 20 V p-p				
		f = 1 kHz		−112		dB
		f = 100 kHz		−72		dB

ELECTRICAL CHARACTERISTICS, V_{SY} = ±5 V

V_{SY} = ±5 V, V_{CM} = V_{OUT} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
A Grade				0.04	±0.8	mV
		−40°C < T_A < +125°C			±2	mV
B Grade				0.04	±0.35	mV
		−40°C < T_A < +125°C			±0.8	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
A Grade		−40°C < T_A < +125°C		±2	±15	μV/°C
B Grade		−40°C < T_A < +125°C		±2	±5	μV/°C
Input Bias Current	I_B			2	±10	pA
		−40°C < T_A < +125°C			±1.5	nA
		V_{CM} = V−		−5		pA
Input Offset Current	I_{OS}				±10	pA
		−40°C < T_A < +125°C			±0.5	nA
Input Voltage Range	IVR		(V−) − 0.2		(V+) − 1	V
Common-Mode Rejection Ratio	CMRR					
A Grade		V_{CM} = V− to (V+) − 3 V	75	91		dB
		−40°C < T_A < +125°C	73			dB
B Grade		V_{CM} = V− to (V+) − 3 V	78	91		dB
		−40°C < T_A < +125°C	75			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_{OUT} = −4.4 V to +4.4 V	113	118		dB
		−40°C < T_A < +125°C	105			dB
		R_L = 1 kΩ, V_{OUT} = −4.4 V to +4.4 V	100	105		dB
		−40°C < T_A < +125°C	91			dB
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		10^{13}		Ω
	R_{CM}	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	I_{SOURCE} = 1 mA	50	30		mV
		−40°C < T_A < +125°C	100			mV
		I_{SOURCE} = 15 mA	700	490		mV
		−40°C < T_A < +125°C	900			mV
Low	V_{OL}	I_{SINK} = 1 mA		45	65	mV
		−40°C < T_A < +125°C			120	mV
		I_{SINK} = 15 mA		315	450	mV
		−40°C < T_A < +125°C			750	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		20		mA
Short-Circuit Current	I_{SC}	Sourcing		31		mA
		Sinking		−40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
		A_V = 10		0.4		Ω
		A_V = 100		4		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4 V to ±18 V	87	103		dB
		−40°C < T_A < +125°C	81			dB
Supply Current per Amplifier	I_{SY}			610	675	µA
		−40°C < T_A < +125°C			700	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = ±3 V, R_L = 2 kΩ, C_L = 100 pF, A_V = 1				
		Low to high transition		21		V/µs
		High to low transition		−16		V/µs
Gain Bandwidth Product	GBP	A_V = 100		7.8		MHz
Unity-Gain Crossover	UGC	A_V = 1		6.5		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		10		MHz
Phase Margin	ΦM			50		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 8 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		1.5		µs
Settling Time to 0.01%	t_S	V_{IN} = 8 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		2		µs
EMI REJECTION RATIO	EMIRR	V_{IN} = 100 mV p-p				
f = 1000 MHz				90		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.75		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		30		nV/√Hz
		f = 100 Hz		15		nV/√Hz
		f = 1 kHz		12.5		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, V_{IN} = 1.5 V rms at 1 kHz				
BW = 80 kHz				0.0005		%
BW = 500 kHz				0.0008		%
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				2.5		µV/°C
Input Bias Current				0.5	5	pA
CROSSTALK	C_S	R_L = 5 kΩ, V_{IN} = 6 V p-p				
		f = 1 kHz		−112		dB
		f = 100 kHz		−72		dB

ELECTRICAL CHARACTERISTICS, V_{SY} = 5 V

V_{SY} = 5 V, V_{CM} = 0 V, V_{OUT} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
A Grade				0.04	±0.8	mV
		−40°C < T_A < +125°C			±2	mV
B Grade				0.04	±0.35	mV
		−40°C < T_A < +125°C			±0.8	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
A Grade		−40°C < T_A < +125°C		±2	±15	μV/°C
B Grade		−40°C < T_A < +125°C		±2	±5	μV/°C
Input Bias Current	I_B			2	±10	pA
		−40°C < T_A < +125°C			±1.5	nA
Input Offset Current	I_{OS}				±10	pA
		−40°C < T_A < +125°C			±0.5	nA
Input Voltage Range	IVR		(V−) − 0.2		(V+) − 1	V
Common-Mode Rejection Ratio	CMRR					
A Grade		V_{CM} = V− to (V+) − 3 V	70	87		dB
		−40°C < T_A < +125°C	67			dB
B Grade		V_{CM} = V− to (V+) − 3 V	73	87		dB
		−40°C < T_A < +125°C	70			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ to V−, V_{OUT} = 0.2 V to 4.6 V	110	115		dB
		−40°C < T_A < +125°C	99			dB
		R_L = 1 kΩ to V−, V_{OUT} = 0.2 V to 4.6 V	96	104		dB
		−40°C < T_A < +125°C	87			dB
Input Capacitance	C_{INDM}	Differential mode		0.4		pF
	C_{INCM}	Common mode		3.6		pF
Input Resistance	R_{DIFF}	Differential mode		10^{13}		Ω
	R_{CM}	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	I_{SOURCE} = 1 mA	50	30		mV
		−40°C < T_A < +125°C	100			mV
		I_{SOURCE} = 15 mA	700	500		mV
		−40°C < T_A < +125°C	900			mV
Low	V_{OL}	I_{SINK} = 1 mA		45	65	mV
		−40°C < T_A < +125°C			120	mV
		I_{SINK} = 15 mA		310	450	mV
		−40°C < T_A < +125°C			750	mV
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		20		mA
Short-Circuit Current	I_{SC}	Sourcing		27		mA
		Sinking		−35		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
		A_V = 10		0.6		Ω
		A_V = 100		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4 V to 15 V	80	95		dB
		−40°C < T_A < +125°C	74			dB
Supply Current per Amplifier	I_{SY}			600	650	μA
		−40°C < T_A < +125°C			675	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = 0.5 V to 3.5 V, R_L = 2 kΩ, C_L = 100 pF, A_V = 1				
		Low to high transition		20		V/µs
		High to low transition		−15		V/µs
Gain Bandwidth Product	GBP	A_V = 100		7.2		MHz
Unity-Gain Crossover	UGC	A_V = 1		6		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		9		MHz
Phase Margin	ΦM			50		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		1.5		µs
Settling Time to 0.01%	t_S	V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		2.0		µs
EMI REJECTION RATIO	EMIRR	V_{IN} = 100 mV p-p				
f = 1000 MHz				90		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.75		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		30		nV/√Hz
		f = 100 Hz		15		nV/√Hz
		f = 1 kHz		12.5		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, V_{IN} = 0.5 V rms at 1 kHz				
BW = 80 kHz				0.0025		%
BW = 500 kHz				0.0025		%
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				2.5		µV/°C
Input Bias Current				0.5	5	pA
CROSSTALK	C_S	R_L = 5 kΩ, V_{IN} = 3 V p-p				
		f = 1 kHz		−112		dB
		f = 100 kHz		−72		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	(V–) – 0.3 V to (V+) + 0.2 V
Differential Input Voltage	36 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
ESD Rating, Human Body Model (HBM)	4 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance[1]

Package Type	θ_{JA}	Unit
8-Lead SOIC		
1-Layer JEDEC Board	180	°C/W
2-Layer JEDEC Board	120	°C/W
8-Lead MSOP		
1-Layer JEDEC Board	265	°C/W
2-Layer JEDEC Board	185	°C/W
8-Lead LFCSP		
1-Layer JEDEC Board	272	°C/W
2-Layer JEDEC Board	145	°C/W
2-Layer JEDEC Board with 2 × 2 Vias	55	°C/W

[1] Thermal impedance simulated values are based on a JEDEC thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

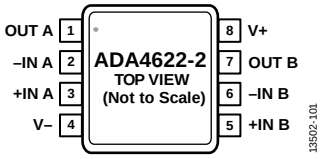


Figure 2. 8-Lead MSOP Pin Configuration

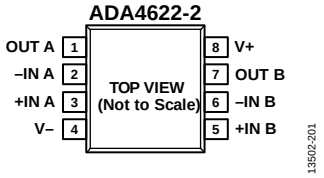


Figure 3. 8-Lead SOIC Pin Configuration

Table 6. 8-Lead SOIC and 8-Lead MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	–IN A	Inverting Input, Channel A
3	+IN A	Noninverting Input, Channel A
4	V–	Negative Supply Voltage
5	+IN B	Noninverting Input, Channel B
6	–IN B	Inverting Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply Voltage

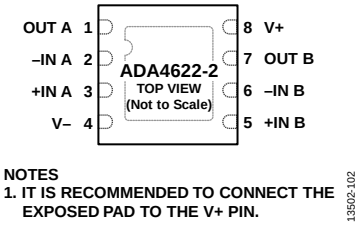


Figure 4. 8-Lead LFCSP Pin Configuration

Table 7. 8-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	–IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V–	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	–IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.
EPAD	EPAD	Exposed Pad. It is recommended to connect the exposed pad to the V+ pin.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

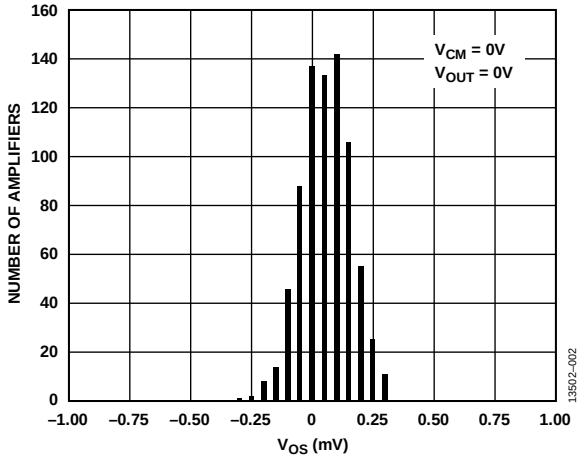


Figure 5. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

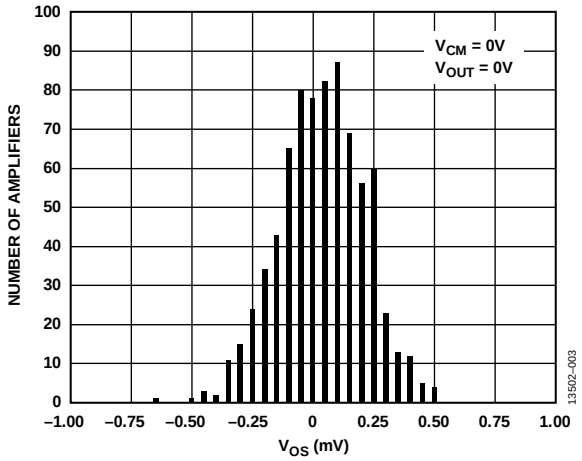


Figure 6. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

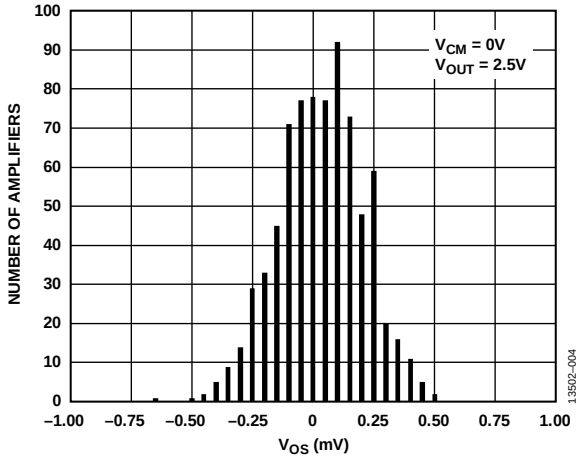


Figure 7. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = 5 V

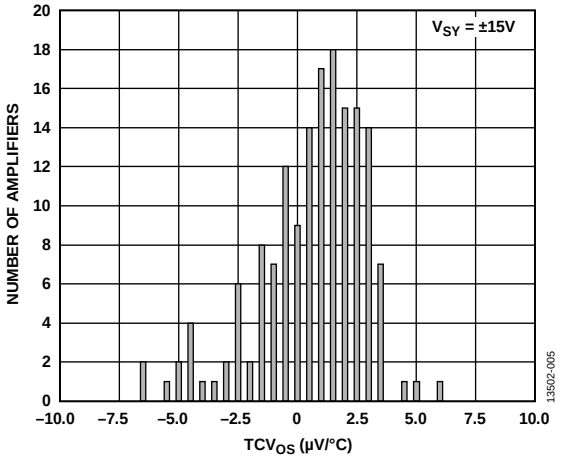


Figure 8. Input Offset Voltage Drift (TCV_{OS}) Distribution (−40°C to +85°C), V_{SY} = ±15 V

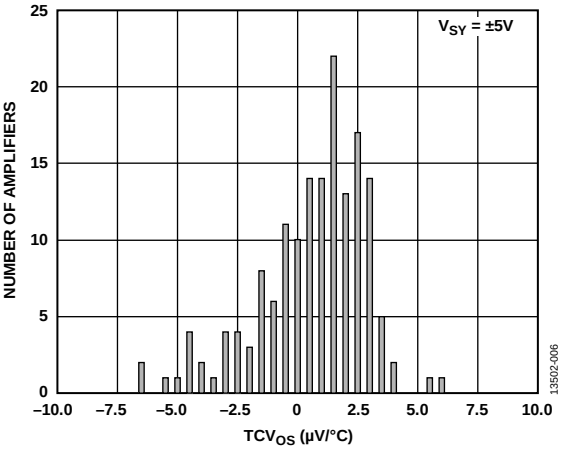


Figure 9. Input Offset Voltage Drift (TCV_{OS}) Distribution (−40°C to +125°C), V_{SY} = ±5 V

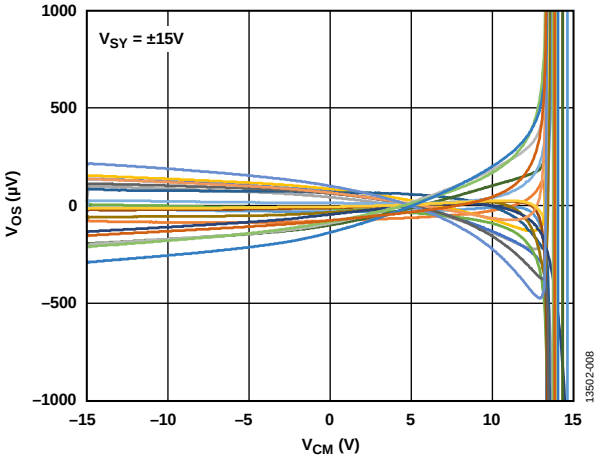


Figure 10. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±15 V

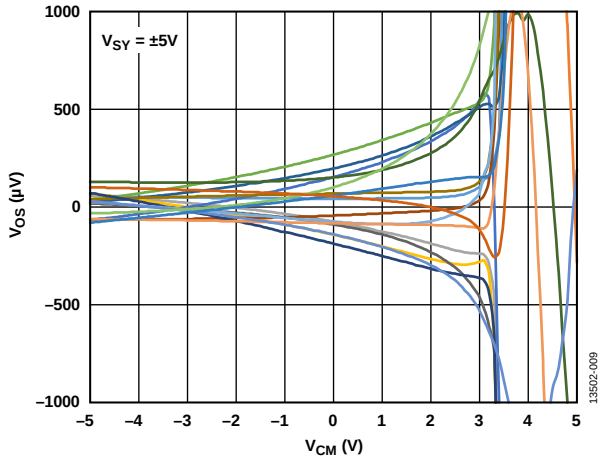


Figure 11. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±5 V

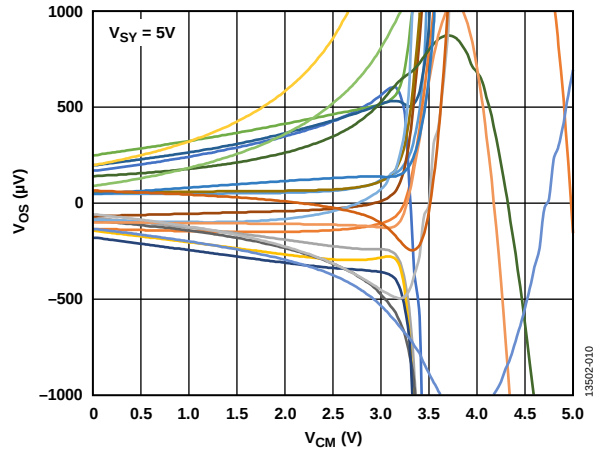


Figure 12. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 5 V

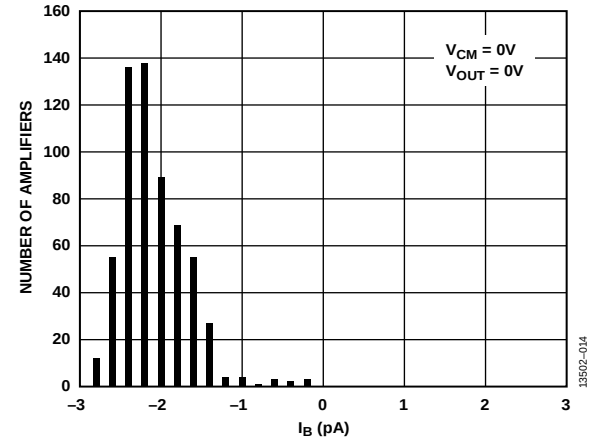


Figure 13. Input Bias Current (I_B) Distribution, V_{SY} = ±15 V

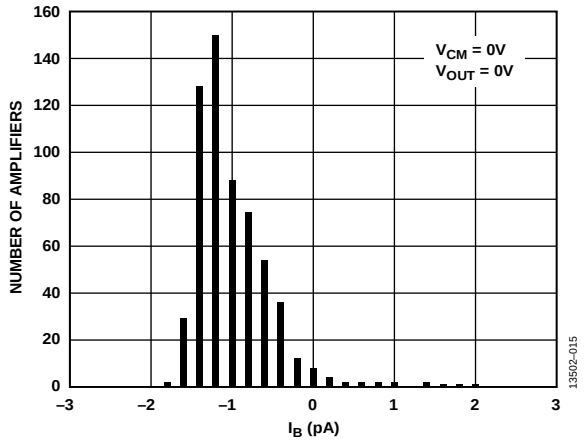


Figure 14. Input Bias Current (I_B) Distribution, V_{SY} = ±5 V

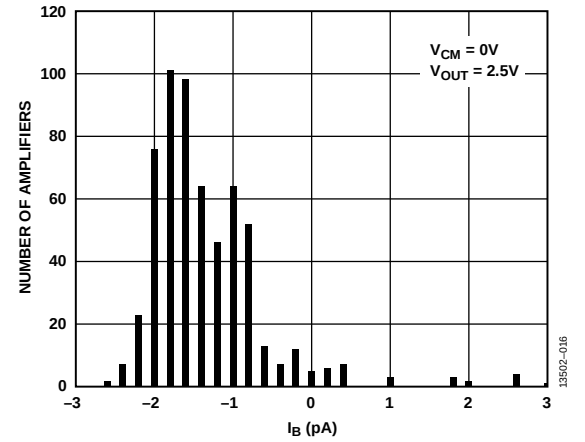


Figure 15. Input Bias Current (I_B) Distribution, V_{SY} = 5 V

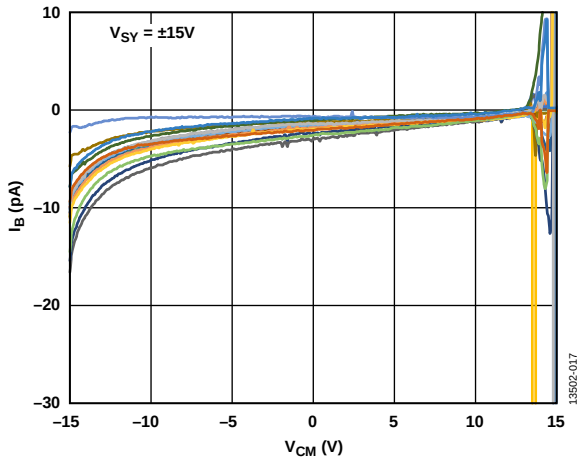


Figure 16. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), V_{SY} = ±15 V

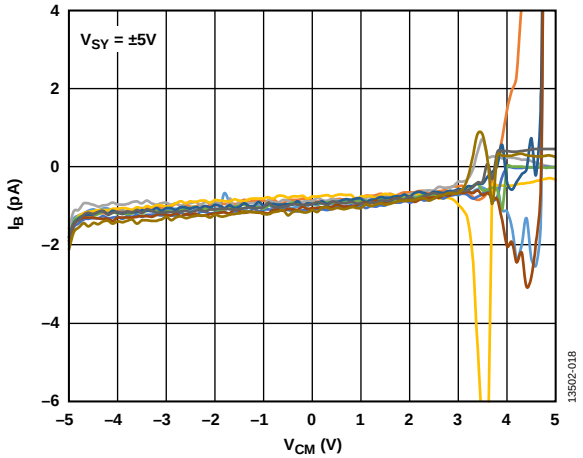


Figure 17. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), V_{SY} = ±5 V

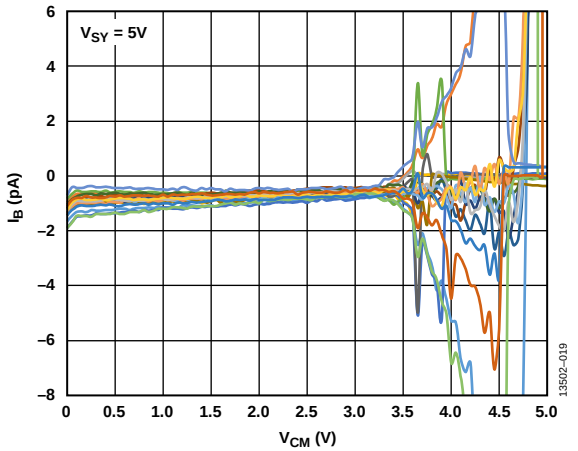


Figure 18. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), V_{SY} = 5 V

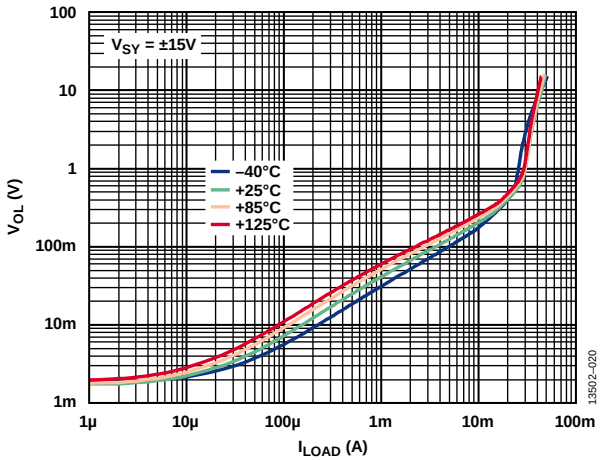


Figure 19. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = ±15 V

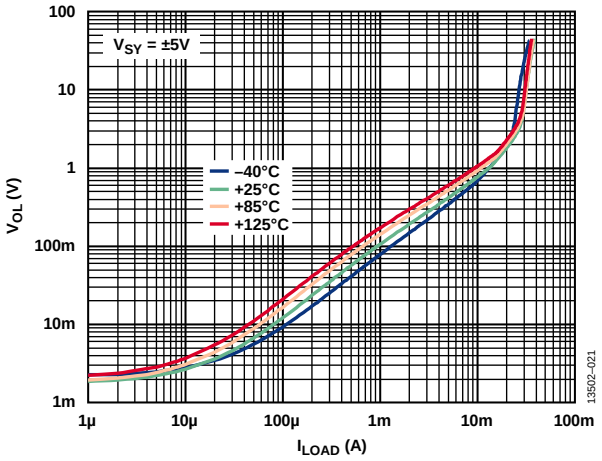


Figure 20. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = ±5 V

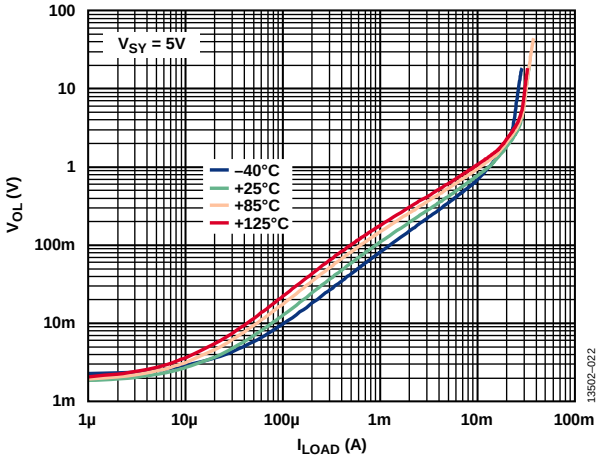


Figure 21. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = 5 V

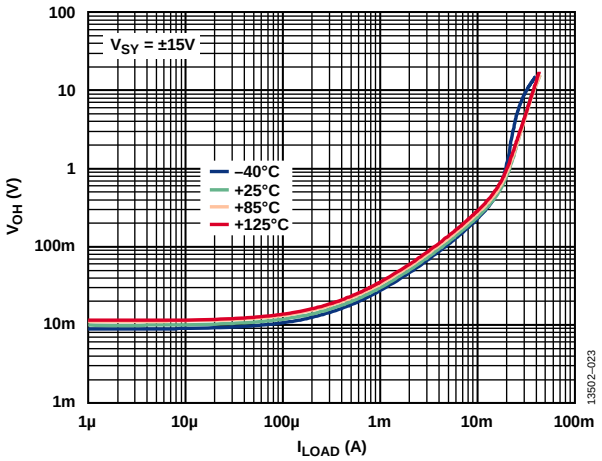


Figure 22. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = ±15 V

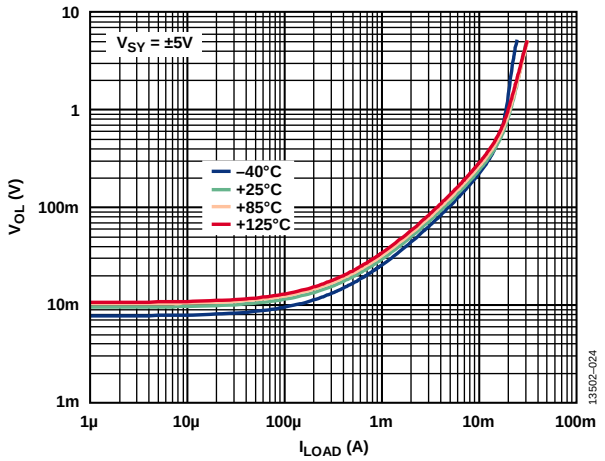


Figure 23. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = ±5 V

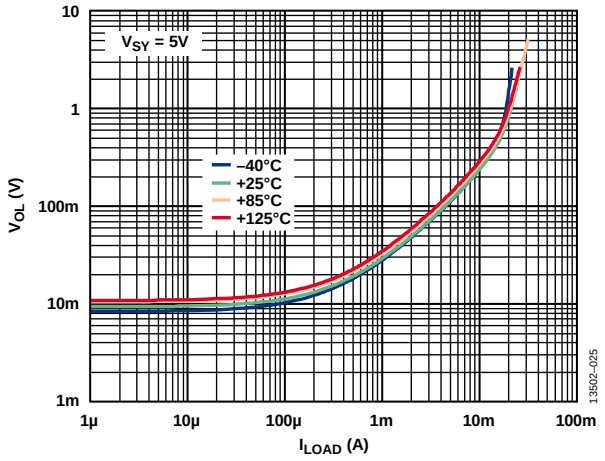


Figure 24. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, V_{SY} = 5 V

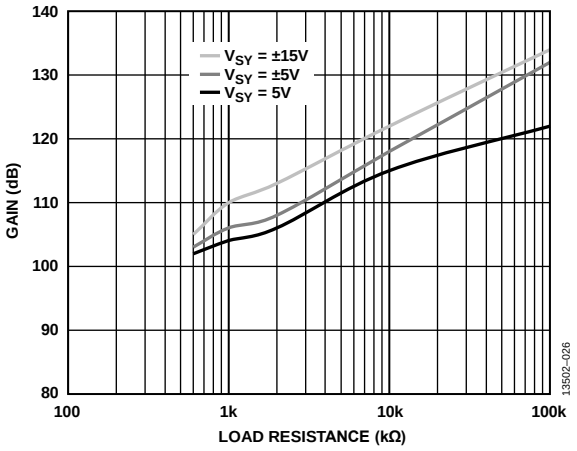


Figure 25. Open-Loop Gain (A_{VO}) vs. Load Resistance

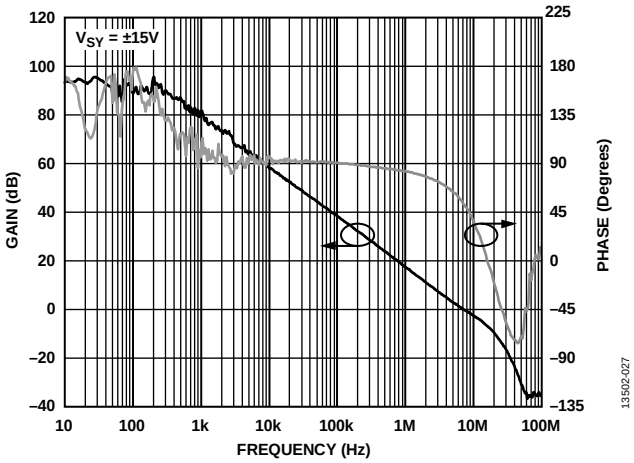


Figure 26. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±15 V

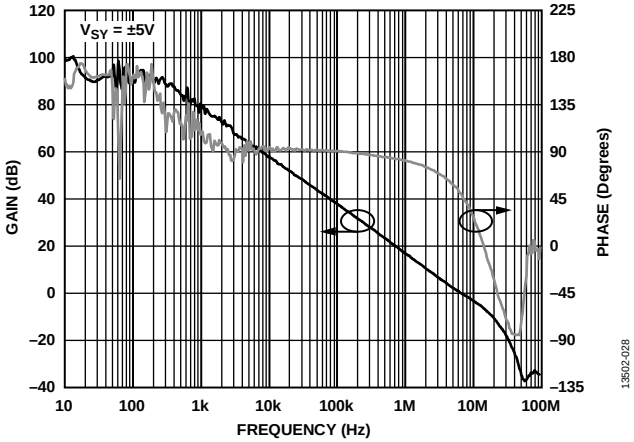


Figure 27. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±5 V

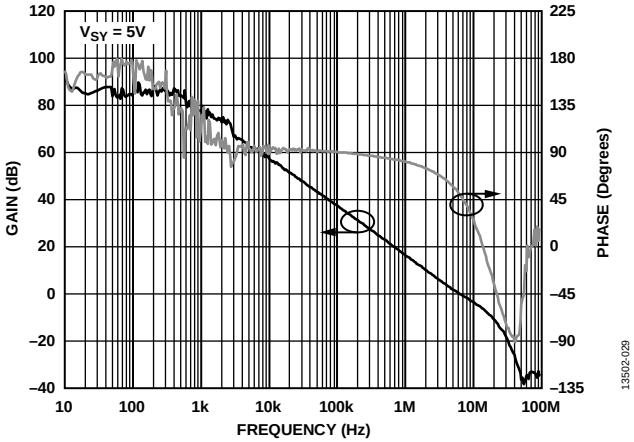


Figure 28. Open-Loop Gain and Phase vs. Frequency, V_{SY} = 5 V

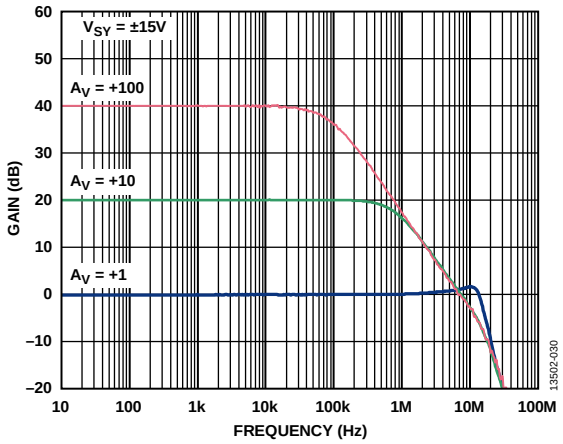


Figure 29. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

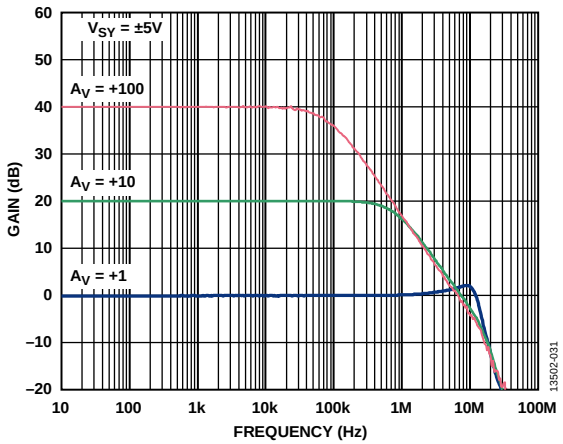


Figure 30. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

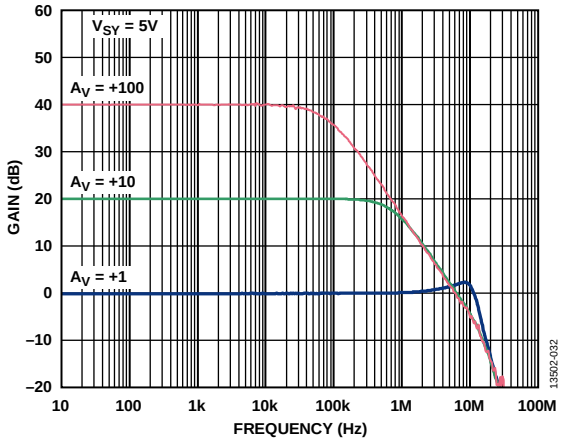


Figure 31. Closed-Loop Gain vs. Frequency, V_{SY} = 5 V

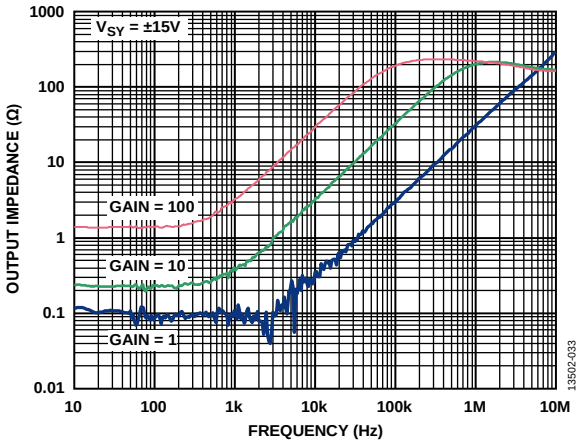


Figure 32. Output Impedance vs. Frequency, V_{SY} = ±15 V

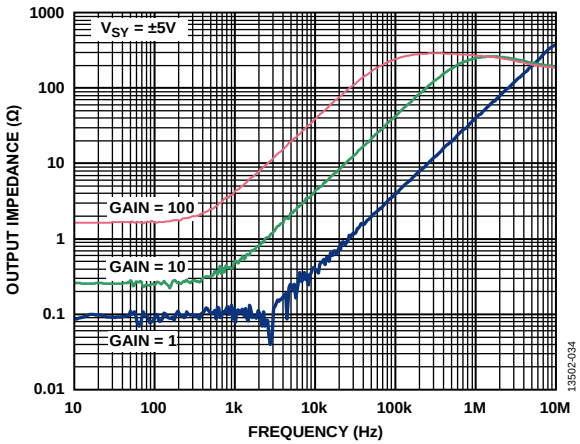


Figure 33. Output Impedance vs. Frequency, V_{SY} = ±5 V

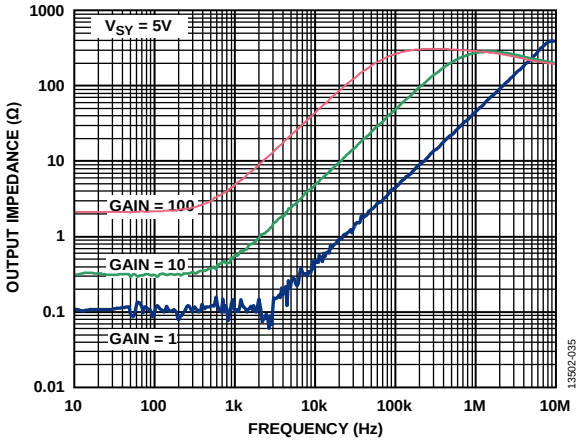


Figure 34. Output Impedance vs. Frequency, V_{SY} = 5 V

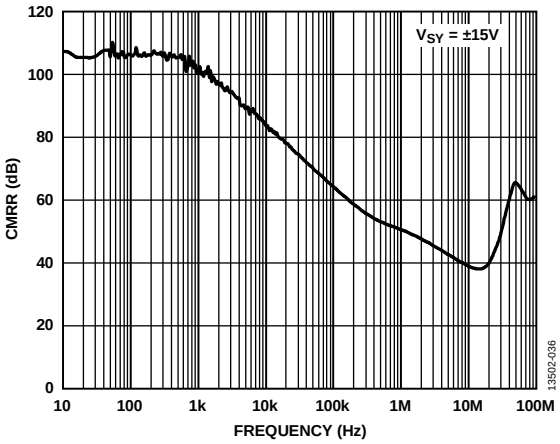


Figure 35. CMRR vs. Frequency, V_{SY} = ±15 V

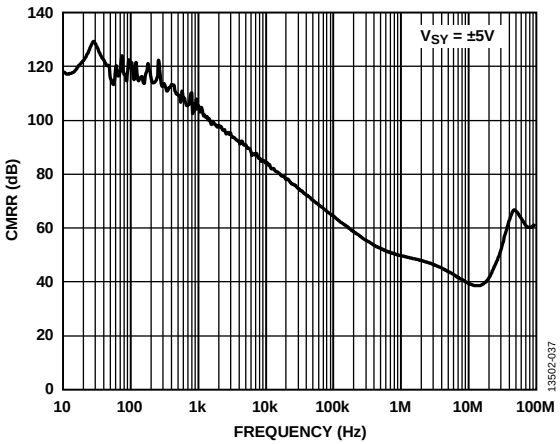


Figure 36. CMRR vs. Frequency, V_{SY} = ±5 V

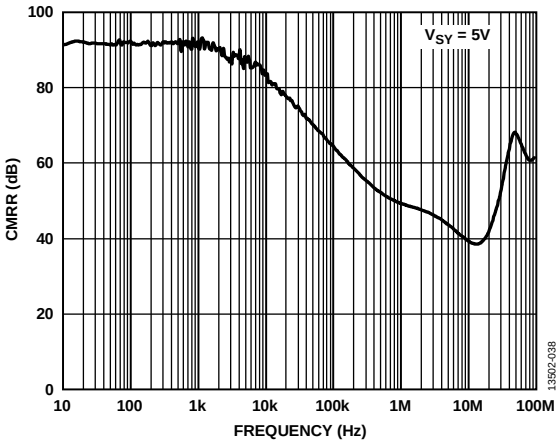


Figure 37. CMRR vs. Frequency, V_{SY} = 5 V

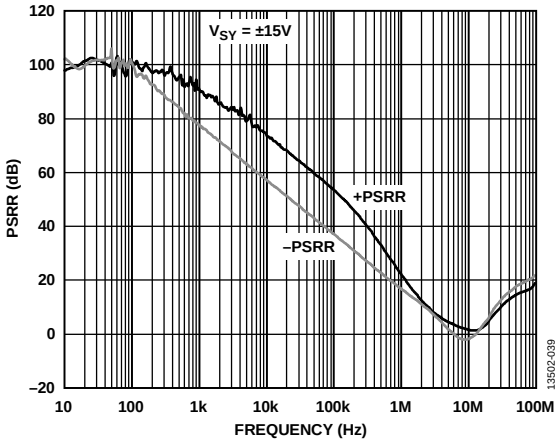


Figure 38. PSRR vs. Frequency, V_{SY} = ±15 V

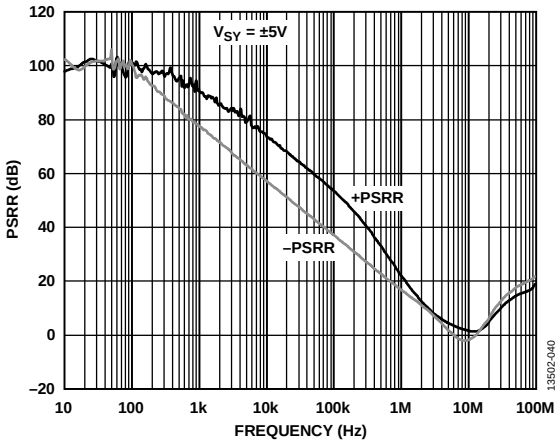


Figure 39. PSRR vs. Frequency, V_{SY} = ±5 V

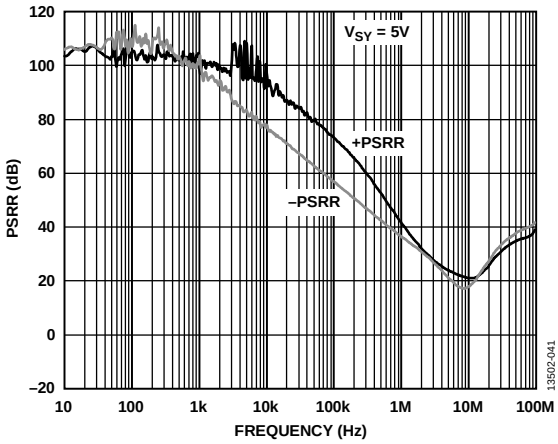


Figure 40. PSRR vs. Frequency, V_{SY} = 5 V

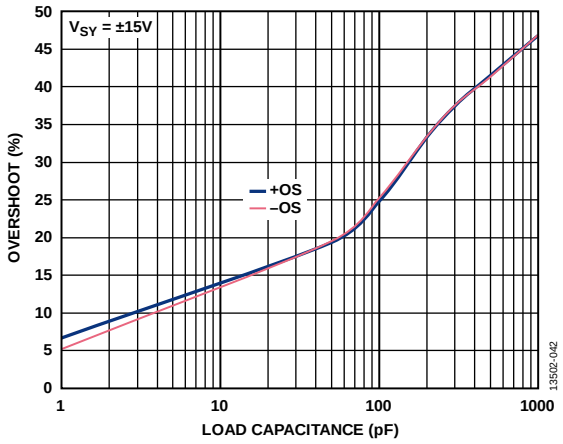


Figure 41. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = ±15 V

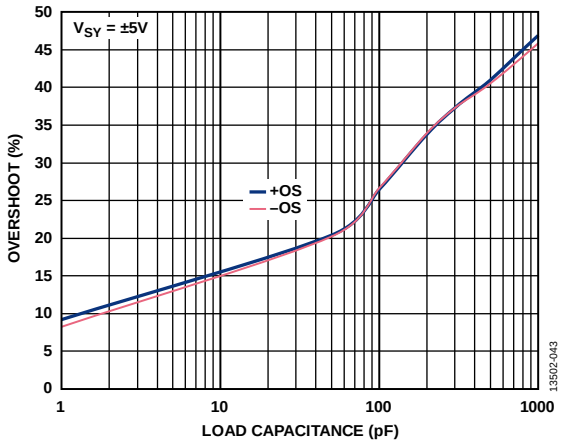


Figure 42. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = ±5 V

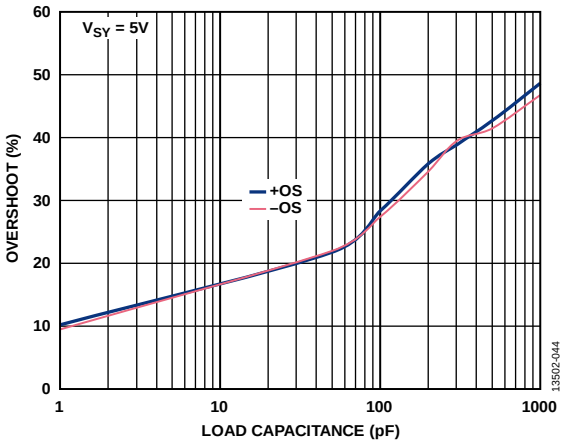


Figure 43. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = 5 V

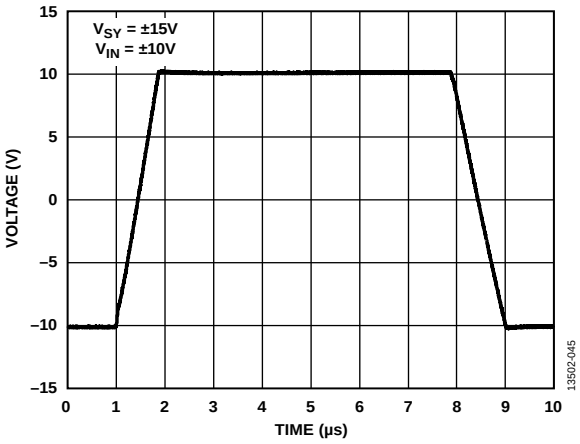


Figure 44. Large Signal Transient Response, V_{SY} = ±15 V

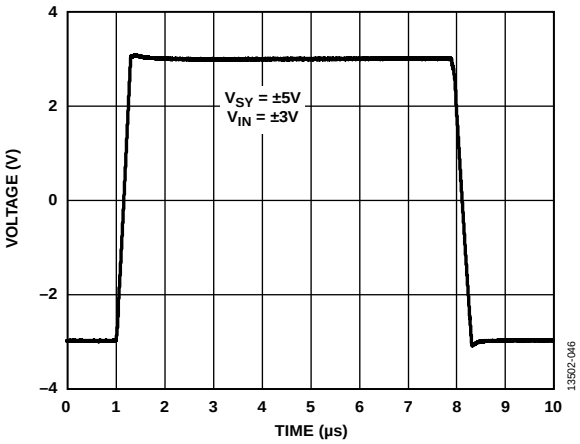


Figure 45. Large Signal Transient Response, V_{SY} = ±5 V

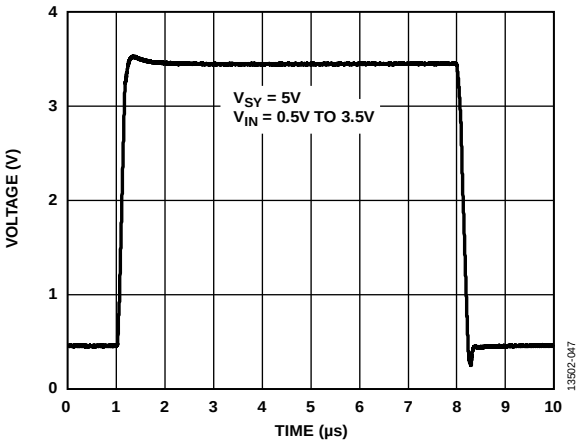


Figure 46. Large Signal Transient Response, V_{SY} = 5 V

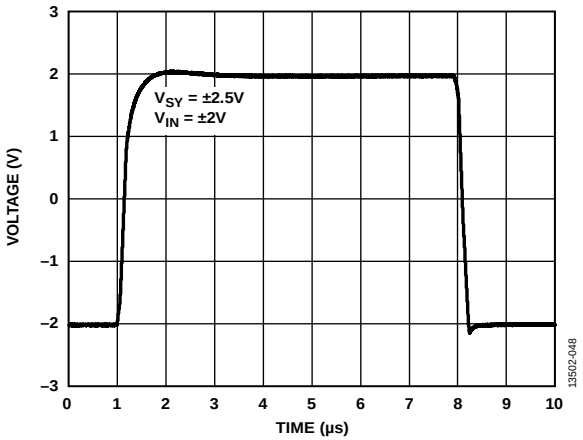


Figure 47. Large Signal Transient Response, V_{SY} = ±2.5 V

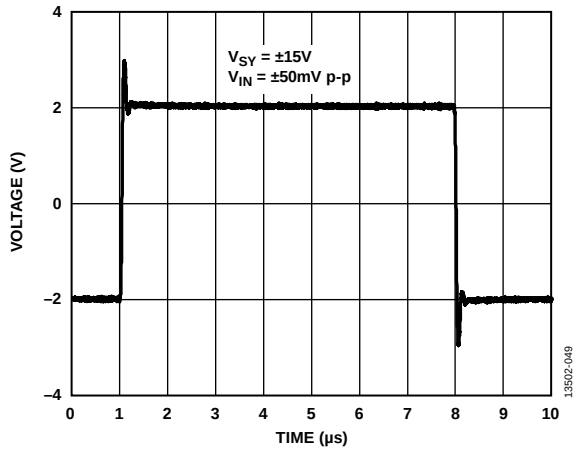


Figure 48. Small Signal Transient Response, V_{SY} = ±15 V

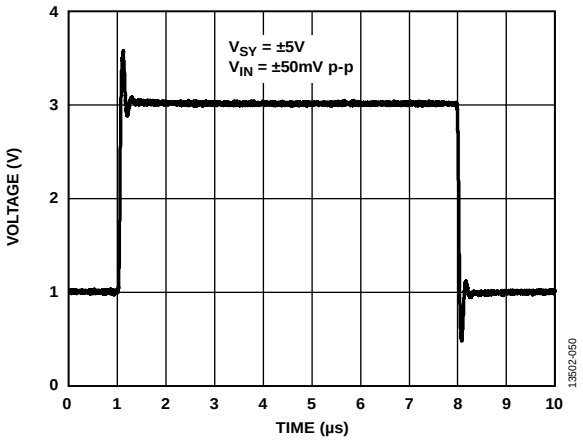


Figure 49. Small Signal Transient Response, V_{SY} = ±5 V

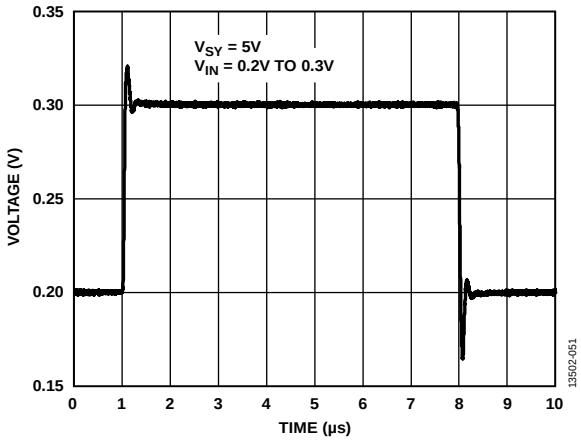


Figure 50. Small Signal Transient Response, V_{SY} = 5 V

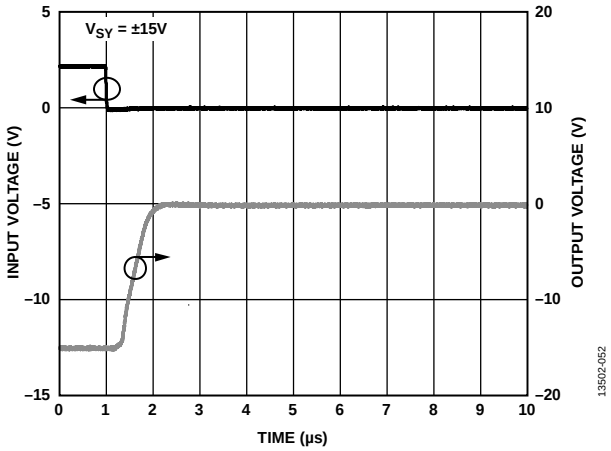


Figure 51. Negative Overload Recovery, A_V = −10, V_{SY} = ±15 V

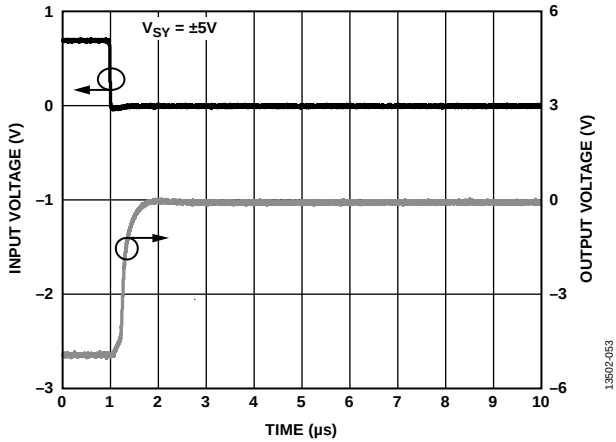


Figure 52. Negative Overload Recovery, A_V = −10, V_{SY} = ±5 V

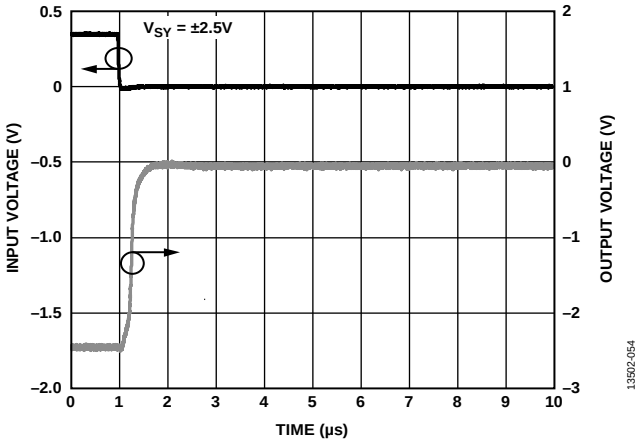


Figure 53. Negative Overload Recovery, $A_V = -10$, $V_{SY} = \pm 2.5$ V

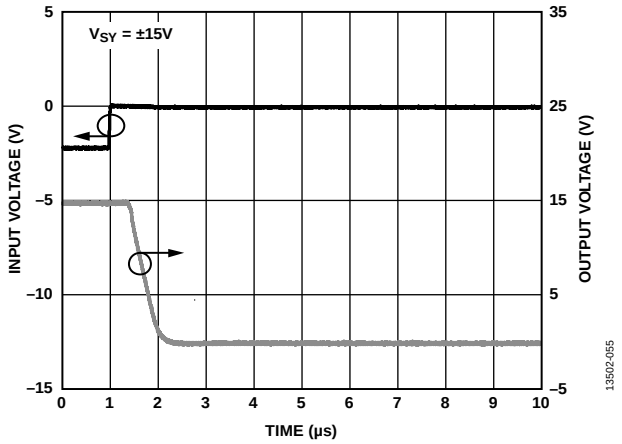


Figure 54. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm 15$ V

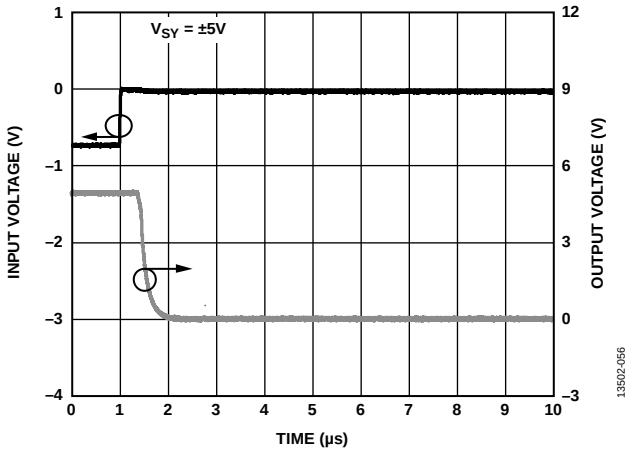


Figure 55. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm 5$ V

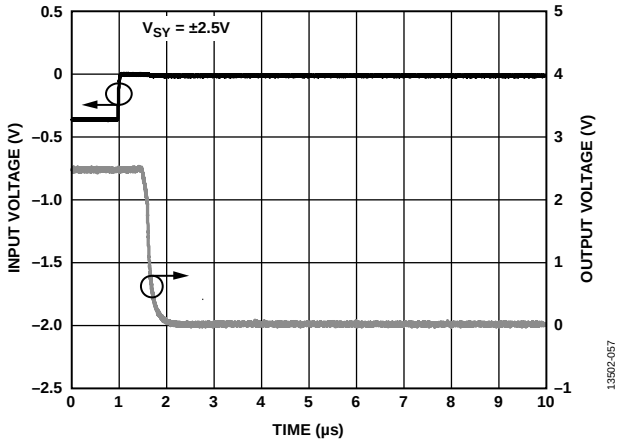


Figure 56. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm 2.5$ V

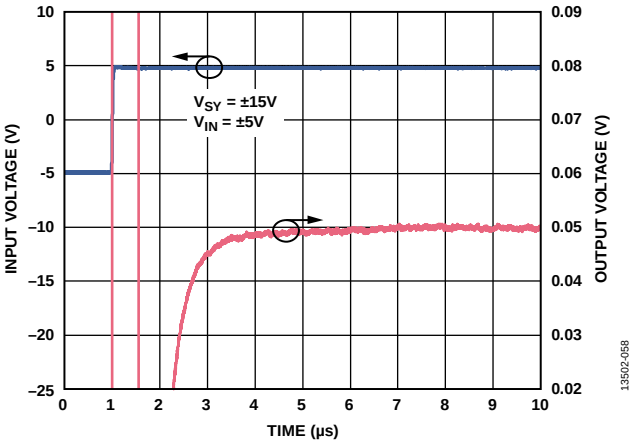


Figure 57. Positive Settling Time, $A_V = -10$, $V_{SY} = \pm 15$ V

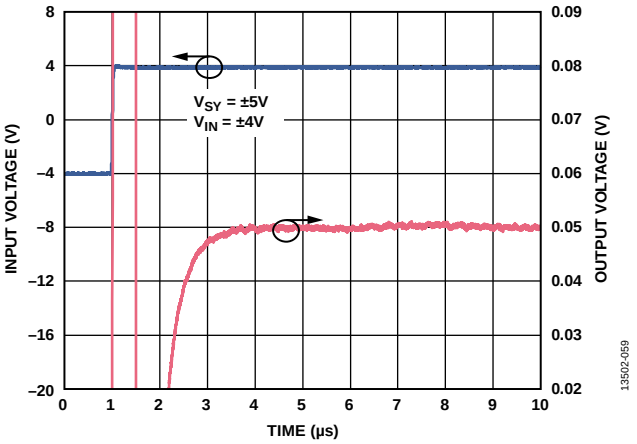


Figure 58. Positive Settling Time, $A_V = -10$, $V_{SY} = \pm 5$ V

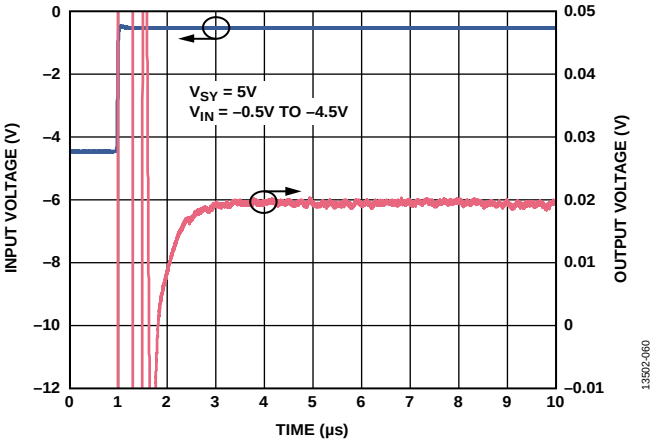


Figure 59. Positive Settling Time, $A_V = -10$, $V_{SY} = 5$ V

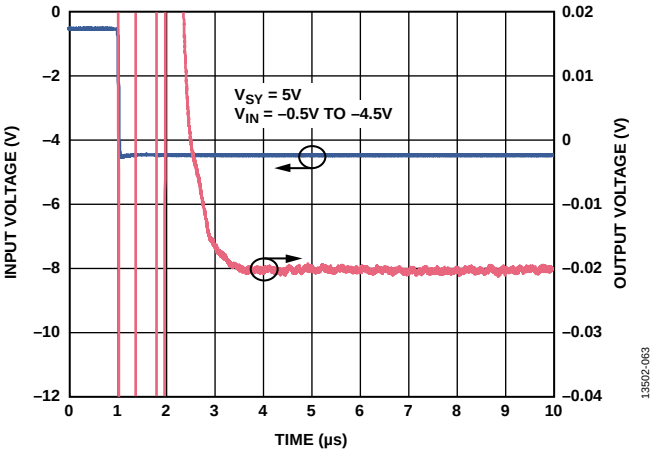


Figure 62. Negative Setting Time, $A_V = -10$, $V_{SY} = 5$ V

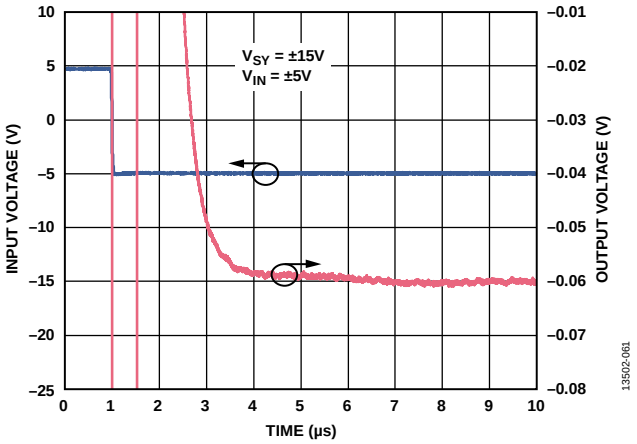


Figure 60. Negative Setting Time, $A_V = -10$, $V_{SY} = \pm 15$ V

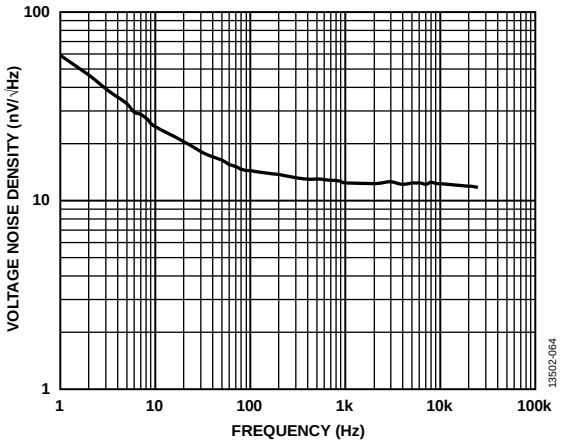


Figure 63. Voltage Noise Density, $V_{SY} = \pm 15$ V

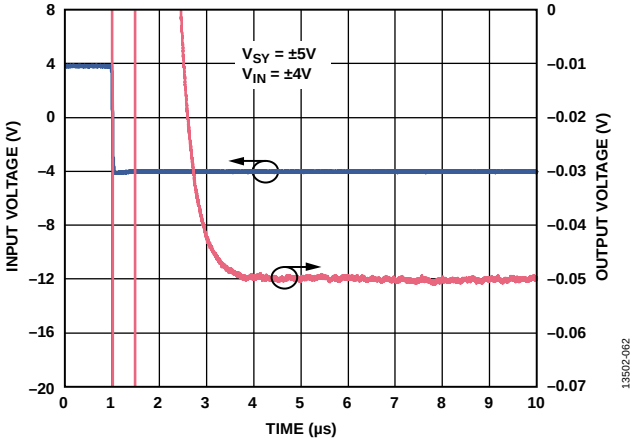


Figure 61. Negative Setting Time, $A_V = -10$, $V_{SY} = \pm 5$ V

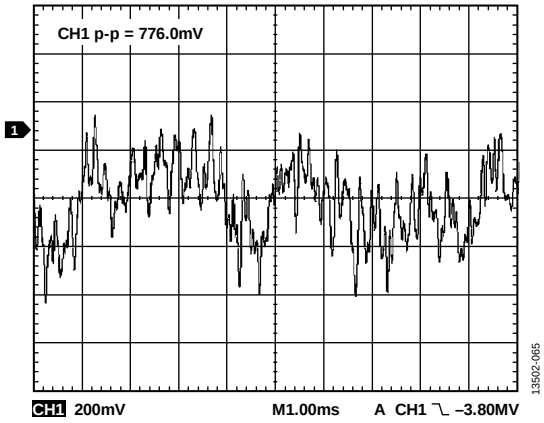


Figure 64. 0.1 Hz to 10 Hz Noise, $V_{SY} = \pm 15$ V

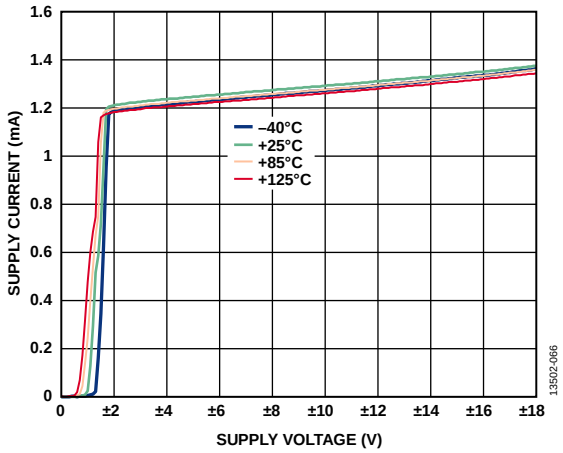


Figure 65. Supply Current (I_{SY}) vs. Supply Voltage (V_{SY}) for Various Temperatures

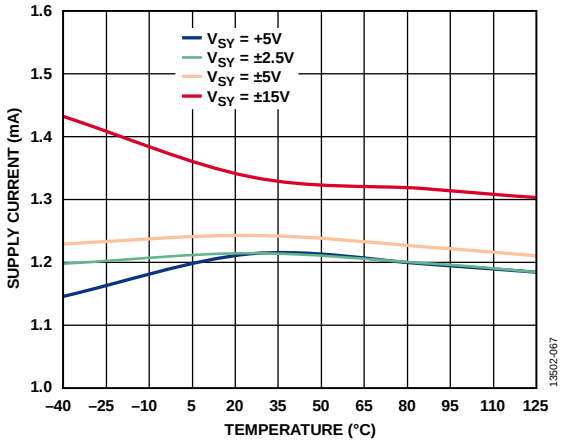


Figure 66. Supply Current (I_{SY}) vs. Temperature for Various Supply Voltages

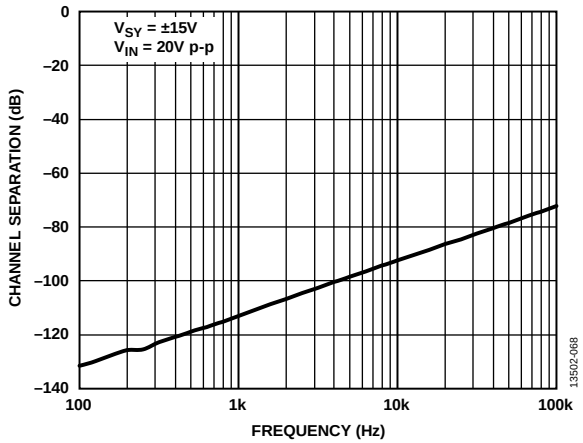


Figure 67. Channel Separation vs. Frequency, V_{SY} = ±15 V

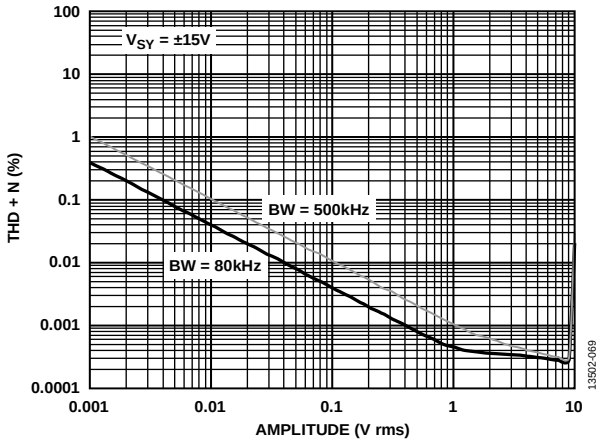


Figure 68. THD + Noise vs. Amplitude, V_{SY} = ±15 V

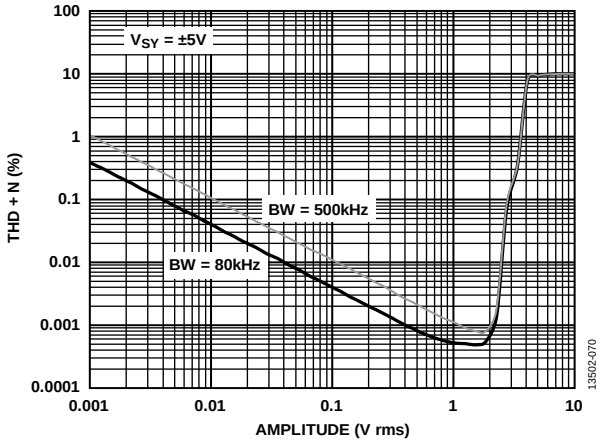


Figure 69. THD + Noise vs. Amplitude, V_{SY} = ±5 V

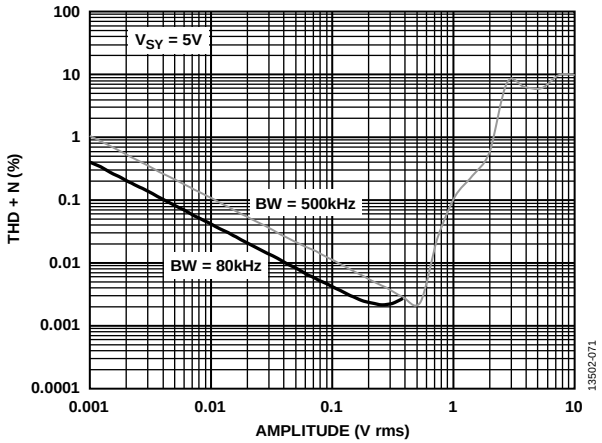


Figure 70. THD + Noise vs. Amplitude, V_{SY} = 5 V

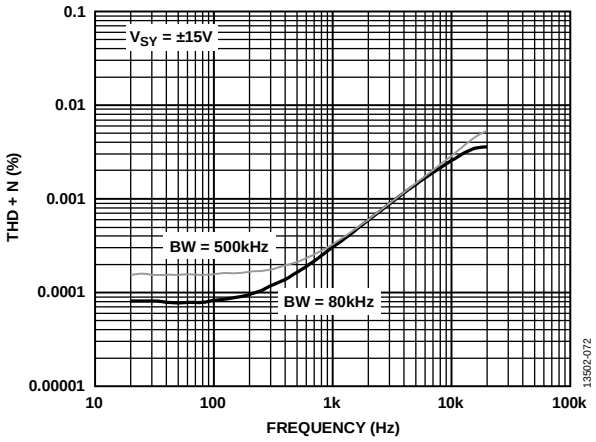


Figure 71. THD + Noise vs. Frequency, V_{SY} = ±15 V

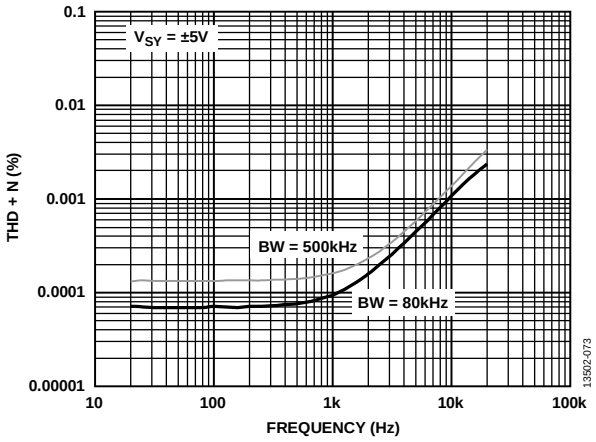


Figure 72. THD + Noise vs. Frequency, V_{SY} = ±5 V

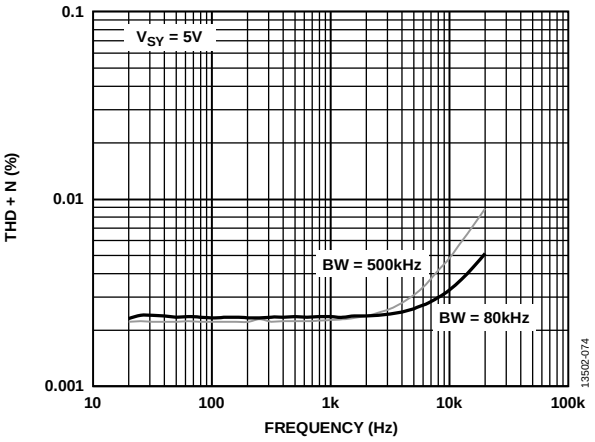


Figure 73. THD + Noise vs. Frequency, V_{SY} = 5 V

THEORY OF OPERATION

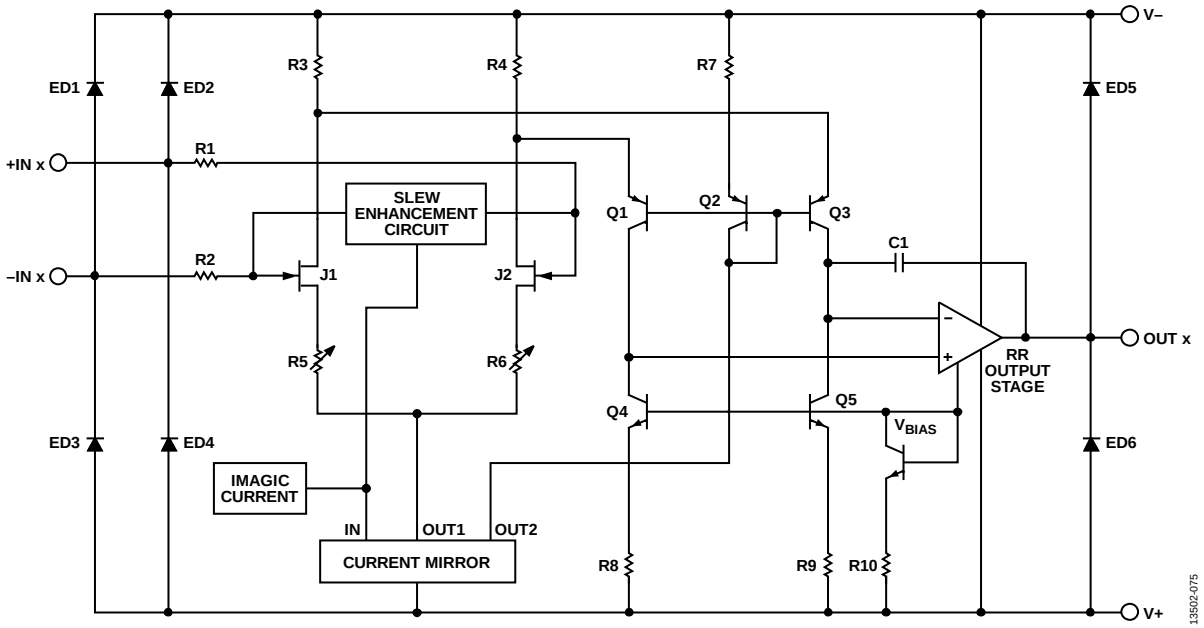


Figure 74. Simplified Circuit Diagram

INPUT CHARACTERISTICS

The ADA4622-2 input stage consists of N-channel, JFETs that provide low offset, low noise, and high impedance. The minimum input common-mode voltage extends from −0.2 mV below V− to 1 V less than V+. Driving the input closer to the positive rail causes loss of amplifier bandwidth and increased common-mode voltage error. Figure 75 shows the rounding of the output due to the loss of bandwidth. The input and output are superimposed.

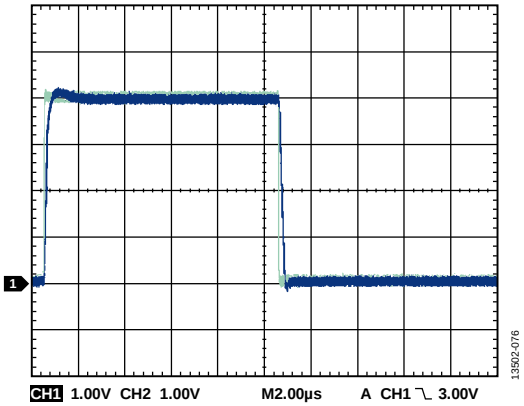


Figure 75. Bandwidth Limiting due to Headroom Requirements

The ADA4622-2 does not exhibit phase reversal for input voltages up to V+. For input voltages greater than V+, a 10 kΩ resistor in series with the noninverting input prevents phase reversal at the expense of higher noise (see Figure 76).

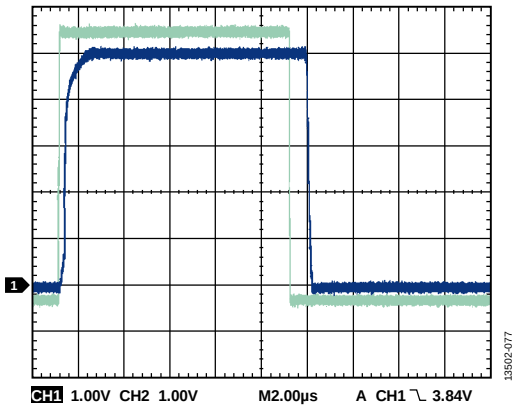


Figure 76. No Phase Reversal

Because the input stage uses N-channel JFETs, the input current during normal operation is negative. However, the input bias current changes direction as the input voltage approaches V+ due to internal junctions becoming forward biased (see Figure 77).

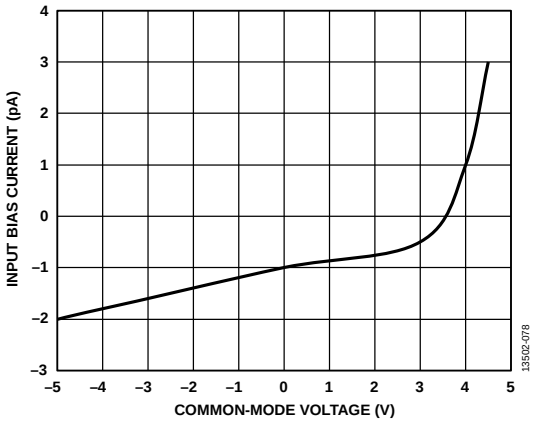


Figure 77. Input Bias Current vs. Common-Mode Voltage with ±5 V Supply

The ADA4622-2 is designed for 12 nV/√Hz wideband input voltage noise density and maintains low noise performance at low frequencies (see Figure 78). This noise performance, along with the low input current as well as low current noise, means that the ADA4622-2 contributes negligible noise for applications with a source resistance greater than 10 kΩ and at signal bandwidths greater than 1 kHz.

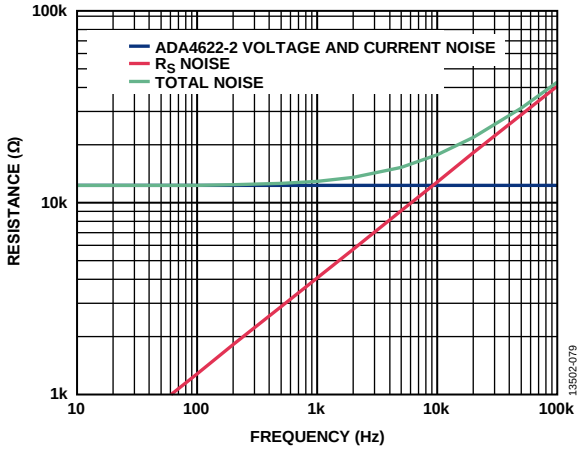


Figure 78. Total Noise vs. Source Resistance

Input Overvoltage Protection

The ADA4622-2 has internal protective circuitry that allows voltages as high as 0.3 V beyond the supplies applied at the input of either terminal without causing damage. Use a current limiting resistor in series with the input of the ADA4622-2 if the input voltage exceeds 0.3 V beyond the amplifier supply rails. If the overvoltage condition persists for more than a few seconds, the amplifier can be damaged.

For higher input voltages, determine the resistor value by

$$\frac{V_{IN} - V_{SY}}{R_S} \leq 10 \text{ mA}$$

where:
V_{IN} is the input voltage.
V_{SY} is the voltage of either the V+ pin or the V− pin.
R_S is the series resistor.

With a very low input bias current of ±1.5 nA maximum up to 125°C, higher resistor values can be used in series with the inputs without introducing large offset errors. A 1 kΩ series resistor allows the ADA4622-2 to withstand 10 V of continuous overvoltage and increases the noise by a negligible amount. A 5 kΩ resistor protects the inputs from voltages as high as 25 V beyond the supplies and adds less than 10 µV to the amplifier offset voltage.

EMI Rejection Ratio

Figure 79 shows the electromagnetic interference rejection ratio (EMIRR) vs. frequency for the ADA4622-2.

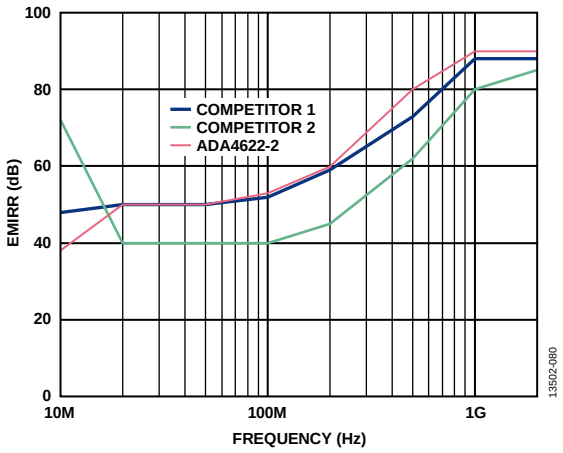


Figure 79. EMI Rejection Ratio (EMIRR) vs. Frequency

OUTPUT CHARACTERISTICS

The ADA4622-2 unique bipolar rail-to-rail output stage swings within 10 mV of the supplies with no external resistive load.

The ADA4622-2 approximate output saturation resistance is 24 Ω, sourcing or sinking. Use the output impedance to estimate the output saturation voltage when driving heavier loads. As an example, when driving 5 mA, the saturation voltage from either rail is roughly 120 mV.

If the ADA4622-2 output drives hard against the output saturation voltage, it recovers within 1.2 µs of the input, returning to the linear operating region of the amplifier (see Figure 51 and Figure 54).

Capacitive Load Drive Capability

Direct capacitive loads interact with the effective output impedance of the ADA4622-2 to form an additional pole in the amplifier feedback loop, which causes excessive peaking on the pulse response or loss of stability. The worst case condition is when the device uses a single 5 V supply in a unity-gain configuration. Figure 80 shows the pulse response of the ADA4622-2 driving 500 pF directly.

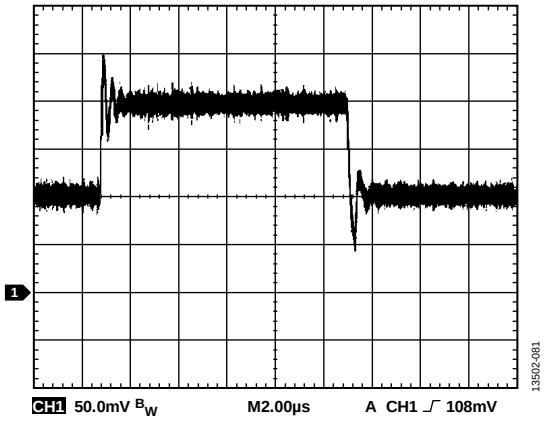


Figure 80. Pulse Response with 500 pF Load Capacitance

APPLICATIONS INFORMATION

RECOMMENDED POWER SOLUTION

The ADA4622-2 can be operated from ±2.5 V to ±15 volt dual supply or 5 V to 30 V single supply.The ADP7118 and ADP7182 are recommended to generate the clean positive and negative rails for the ADA4622-2. Both low dropout regulators (LDOs) are available in fixed output voltage or adjustable output voltage versions. To generate the input voltages for the LDOs, the ADP5070 dc-to-dc switching regulator is recommended. Figure 81 shows the recommended power solution configuration for the ADA4622-2.

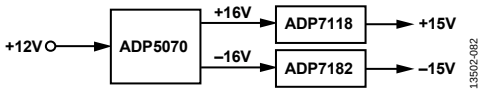


Figure 81. Power Solution Configuration for the ADA4622-2

Table 8. Recommended Power Management Devices

Product	Description
ADP5070	DC-to-DC switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO regulator
ADP7182	−28 V, −200 mA, low noise, linear regulator

MAXIMUM POWER DISSIPATION

The maximum power the ADA4622-2 can safely dissipate is limited by the associated rise in junction temperature. For plastic packages, the maximum safe junction temperature is 150°C. If this maximum temperature is exceeded, reduce the die temperature to restore proper circuit operation. Leaving the device in the overheated condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the Absolute Maximum Ratings and Thermal Resistance specifications.

SECOND-ORDER LOW-PASS FILTER

Figure 82 shows the ADA4622-2 configured as a second-order, Butterworth, low-pass filter. With the values as shown, the corner frequency equals 200 kHz. Component selection is shown in the following equations:

$$R1 = R2 = \text{User Selected } (\text{Typical Values: } 10\ \text{k}\Omega \text{ to } 100\ \text{k}\Omega)$$

$$C1 = \frac{1.414}{2\pi f_{CUTOFF} \times R1}$$

$$C2 = \frac{0.707}{2\pi f_{CUTOFF} \times R1}$$

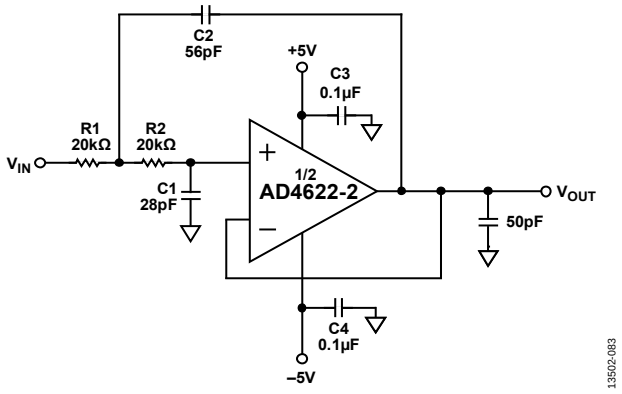


Figure 82. Second-Order, Butterworth, Low-Pass Filter

A plot of the filter is shown in Figure 83; greater than 35 dB of high frequency rejection is achieved.

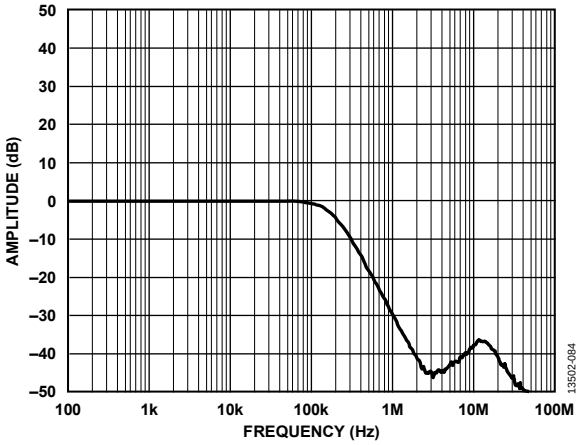


Figure 83. Frequency Response of the Filter

WIDEBAND PHOTODIODE PREAMPLIFIER

The ADA4622-2 is an excellent choice for photodiode preamplifier application. The low input bias current minimizes the dc error at the preamplifier output. In addition, the high gain bandwidth product and low input capacitance maximizes the signal bandwidth of the photodiode preamplifier. Figure 84 shows the ADA4622-2 as a current to voltage (I to V) converter with an electrical model of a photodiode.

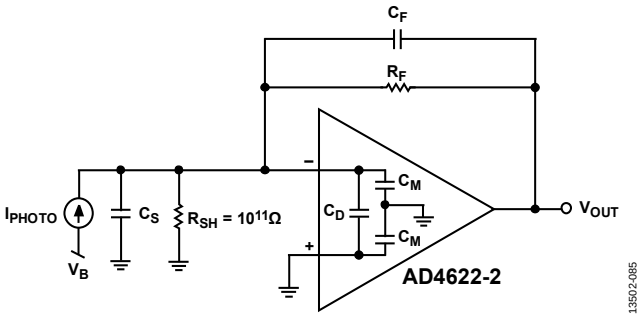


Figure 84. Wideband Photodiode Preamplifier

The transimpedance gain of the photodiode preamplifier is described by the following basic transfer function:

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F}$$

where
I_{PHOTO} is the output current of the photodiode.
The parallel combination of R_F and C_F sets the signal bandwidth (see the I to V gain curve in Figure 86).
s refers to the s-plane.

Note that R_F must be set so the maximum attainable output voltage corresponds to the maximum diode output current, I_{PHOTO}, which allows use of the full output swing. The attainable signal bandwidth with this photodiode preamplifier is a function of R_F, the gain bandwidth product (f_{GBP}) of the amplifier, and the total capacitance at the amplifier summing junction, including C_S and the amplifier input capacitance, C_D and C_M. R_F and the total capacitance produce a pole with loop frequency (f_P).

$$f_P = \frac{1}{2\pi R_F C_S}$$

With the additional pole from the amplifier open-loop response, the two-pole system results in peaking and instability due to an insufficient phase margin (see Figure 85).

Adding C_F creates a zero in the loop transmission that compensates for the effect of the input pole. This stabilizes the photodiode preamplifier design because of the increased phase margin. Adding C_F also sets the signal bandwidth (see Figure 86). The signal bandwidth and the zero frequency are determined by

$$f_Z = \frac{1}{2\pi R_F C_F}$$

where f_Z is the zero frequency.

Setting the zero at the f_X frequency maximizes the signal bandwidth with a 45° phase margin. Because f_X is the geometric mean of f_P and f_{GBP}, it can be calculated by

$$f_X = \sqrt{f_P \times f_{GBP}}$$

Combining these equations, the value of C_F that produces f_X is defined by

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times f_{GBP}}}$$

The frequency response in this case shows about 2 dB of peaking and 15% overshoot. Doubling C_F and halving the bandwidth results in a flat frequency response with about 5% transient overshoot.

The dominant sources of output noise in the wideband photodiode preamplifier design are the input voltage noise of the amplifier, V_{NOISE}, and the resistor noise due to R_F. The gray curve in Figure 86 shows the noise gain over frequencies for the photodiode preamplifier. Calculate the noise bandwidth at the f_N frequency by

$$f_N = \frac{f_{GBP}}{(C_S + C_F)/C_F}$$

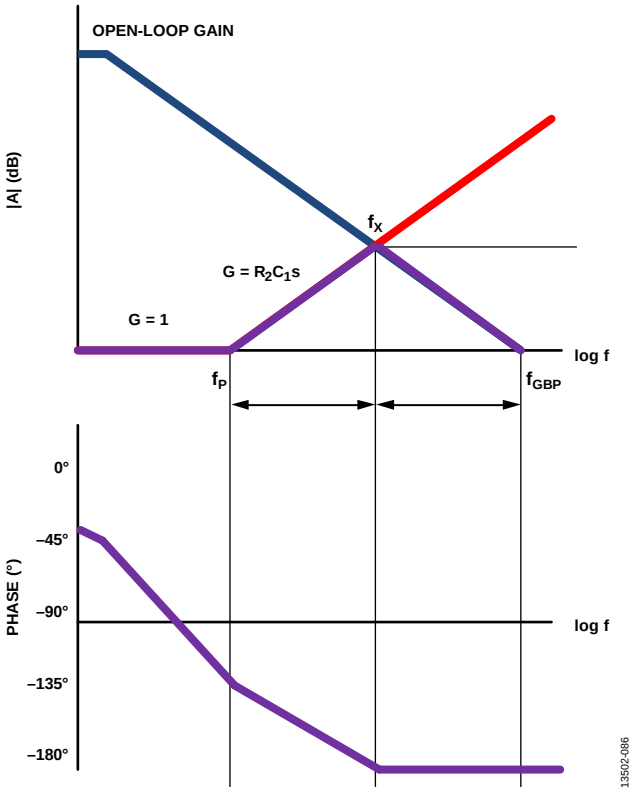


Figure 85. Gain and Phase Plot of the Transimpedance Amplifier Design, Without Compensation

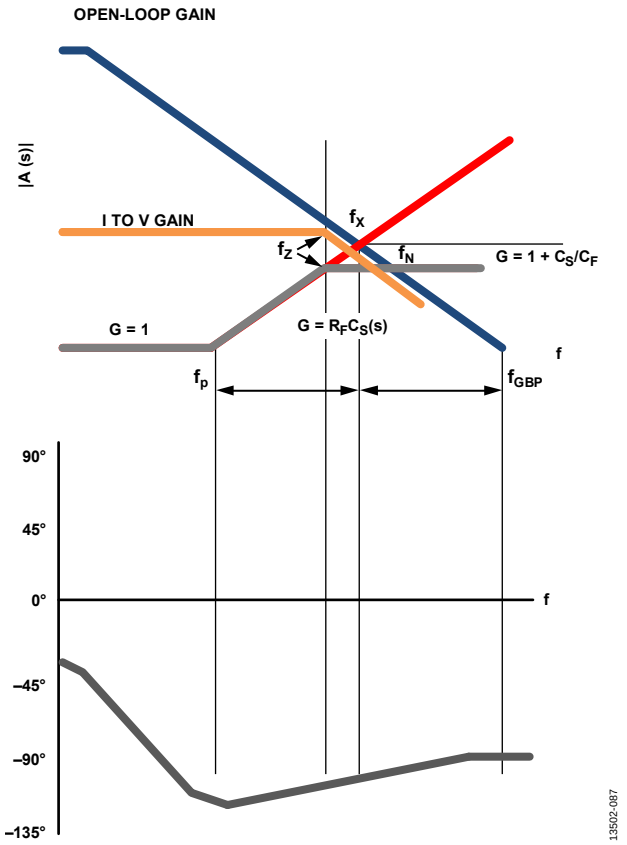


Figure 86. Gain and Phase Plot of the Transimpedance Amplifier Design with Compensation

Figure 87 shows the ADA4622-2 configured as a transimpedance photodiode amplifier. The amplifier is used in conjunction with a photodiode detector with an input capacitance of 5 pF. Figure 88 shows the transimpedance response of the ADA4622-2 when I_{PHOTO} is 1 µA p-p. The amplifier has a bandwidth of 2 MHz when it is maximized for a 45° phase margin with C_F = 2 pF. Note that with the PCB parasitics added to C_F, the peaking is only 0.5 dB and the bandwidth is slightly reduced.

Increasing C_F to 3 pF completely eliminates the peaking. However, increasing C_F to 3 pF reduces the bandwidth to 1 MHz.

Table 9 shows the noise sources and total output noise for the photodiode preamplifier, where the preamplifier is configured to have a 45° phase margin for maximum bandwidth and $f_Z = f_X = f_N$ in this case.

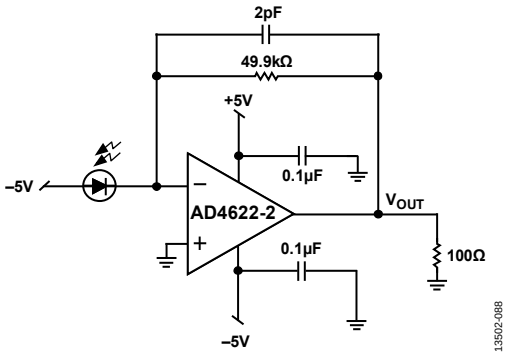


Figure 87. Photodiode Preamplifier

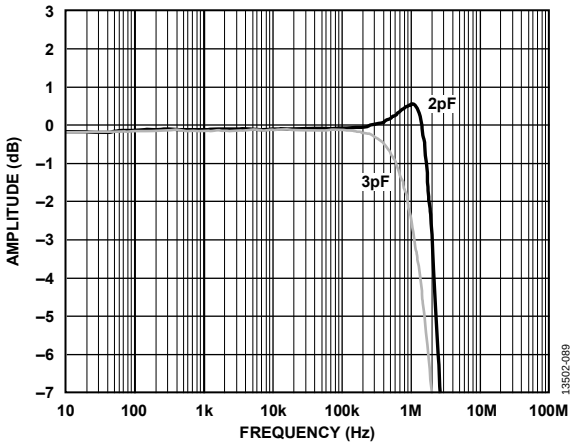


Figure 88. Photodiode Preamplifier Frequency Response

Table 9. RMS Noise Contributions of the Photodiode Preamplifier

Contributor	Expression	RMS Noise (µV)[1]
R_F	$\sqrt{4kT \times R_F \times f_N \times \frac{\pi}{2}}$	50.8
V_{NOISE}	$V_{NOISE} \times \sqrt{\frac{(C_S + C_M + C_F + C_D)}{C_F}} \times \sqrt{\frac{\pi}{2} \times f_N}$	131.6
Root Sum Square (RSS) Total	$\sqrt{R_F^2 \times V_{NOISE}^2}$	141

[1] RMS noise with R_F = 50 kΩ, C_S = 5 pF, C_F = 2 pF, C_M = 3.7 pF, and C_D = 0.4 pF.

PEAK DETECTOR

A peak detector captures the peak value of a signal and produces an output equal to it. By taking advantage of the dc precision and super low input bias current of the JFET input amplifiers, such as the ADA4622-2, a highly accurate peak detector can be built, as shown in Figure 89.

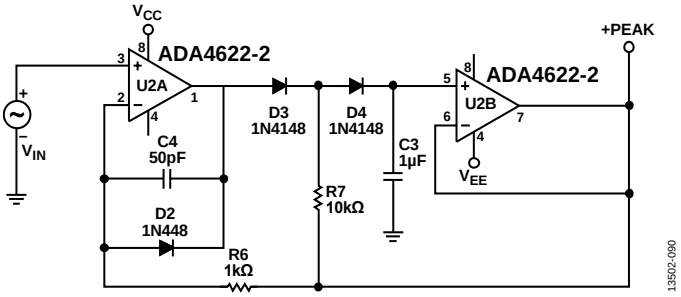


Figure 89. Positive Peak Detector

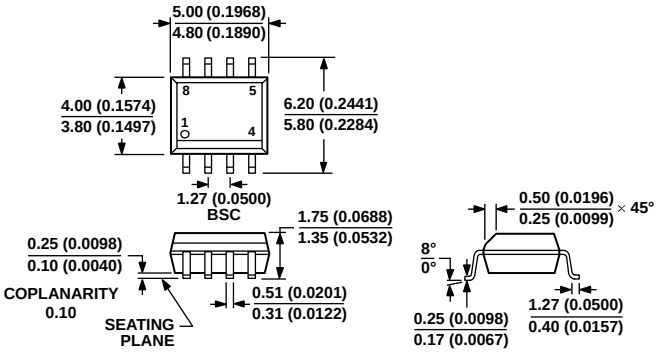
In this application, D3 and D4 act as unidirectional current switches that open when the output is kept constant in hold mode.

To detect a positive peak, U2A drives C3 through D3 and drives D4 until C3 is charged to a voltage equal to the input peak value.

Feedback from the output of the U2B (positive peak) through R6 limits the output voltage of U2A. After detecting the peak, the output of U2A swings low but is clamped by D2. D3 reverses bias and the common node of D3, D4, and R7 is held to a voltage equal to positive peak by R7. The voltage across D4 is 0 V; therefore, the leakage is small. The bias current of U2B is also small. With almost no leakage, C3 has a long hold time.

The ADA4622-2, shown in Figure 89, is a perfect fit for building a peak detector because U2A requires dc precision and high output current during fast peaks and U2B requires low input bias current (I_B) to minimize capacitance discharge between peaks. A low leakage and low dielectric absorption capacitor, such as polystyrene or polypropylene, is required for C3. Reversing the diode directions causes the circuit to detect negative peaks.

OUTLINE DIMENSIONS

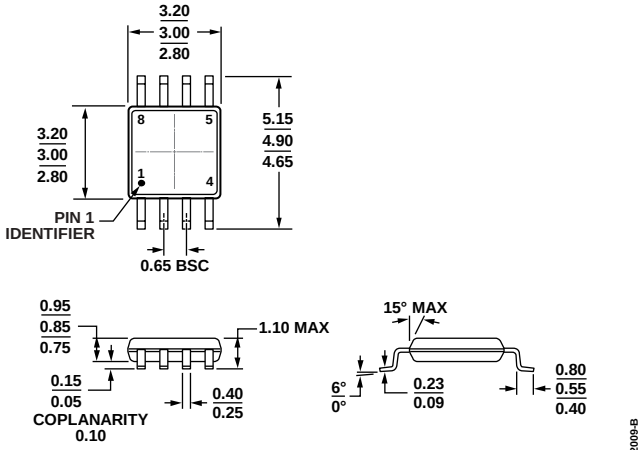


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 90. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 91. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

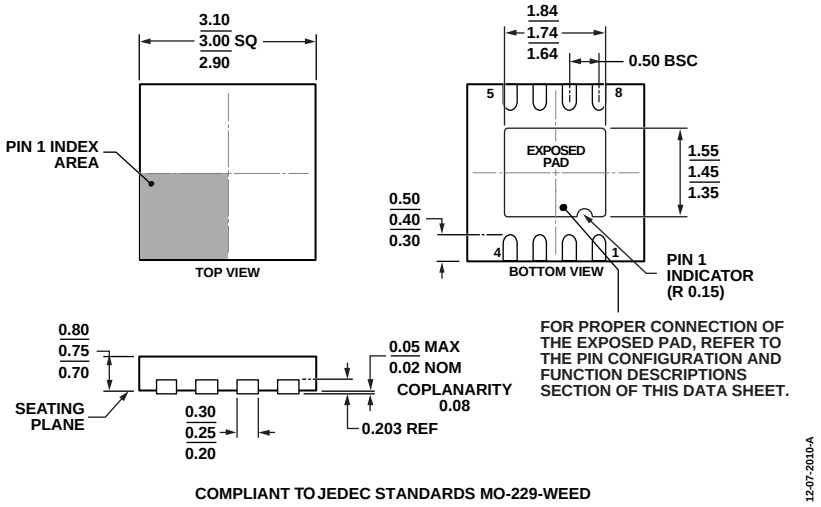


Figure 92. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4622-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A3D
ADA4622-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A3D
ADA4622-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A3D
ADA4622-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A3D
ADA4622-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A3D
ADA4622-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4622-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4622-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4622-2BRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4622-2BRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4622-2BRZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Compliant Part.

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D13502-0-2/16(A)

ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

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