NXH5104

4 Mbit Serial SPI EEPROM

Rev. 6.3 — 3 July 2019 Product data sheet

1 General description

The NXP Semiconductors NXH5104 is a 4 Mbit serial electrically erasable and programmable read-only memory (EEPROM). It provides byte level and page level serial EEPROM functions, sector level protection and power-down functions. The device has been developed for low-power low-voltage applications and is provided with a serial peripheral interface (SPI) compatible interface.

2 Features and benefits

- Compact wafer-level chip-scale package (WLCSP) package
- – 7.8 mm^2, 380 µm thick
  – 13 bumps with 400 µm pitch
- Integrated power management unit (PMU)
- – V_{DD} supply range 1.0 V to 2.0 V
  – $V_{DD(IO)}$ supply range: V_{DD} to 2.6 V
  – Direct operation from ZnAir, NiMH, Silver-Zinc batteries
  – Active peak current limiting
- Low current consumption
- – Average power down current < 5 µA
  – Average read current 0.6 mA (V_{DD} = $V_{DD(IO)}$ = 1.8 V, F_{SPI} =5 MHz)
  – Average write current 0.7 mA (V_{DD} = $V_{DD(IO)}$ = 1.8 V, F_{SPI} = 5 MHz)
- Low-power CMOS technology
- Auxiliary supply voltage enabling direct LED drive
- Self-timed program cycle
- – 256 byte page write buffer
  – Partial page write allowed
- Write protect
- – Quarter, half or entire memory array
- Serial peripheral interface (SPI)
- – Speed up to 5 MHz for 1.2 V signaling level
  – Speed up to 10 MHz for 1.8 V signaling level
  – SPI mode 0 (0,0) and 3 (1,1) support
  – SPI 3-wire support for SPI mode 0
- Fixed high supply mode for faster start-up
- Space-saving 2.80 mm × 2.74 mm wafer-level chip-scale package (WLCSP)
- Highly integrated: 1 external cap
- High reliability
- – 10-year data retention
  – 500 000 program cycles
  – Wear-out management

- Operating temperature −20 °C to +85 °C
- Support for different supply configurations
- Device ID and Unique ID
- Pb-free and RoHS compliant

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NXH5104UK/A1	WLCSP13	wafer level chip-scale package; 13 bumps; 2.74 mm × 2.80 mm × 0.38 mm	SOT1461-1

4 Block diagram

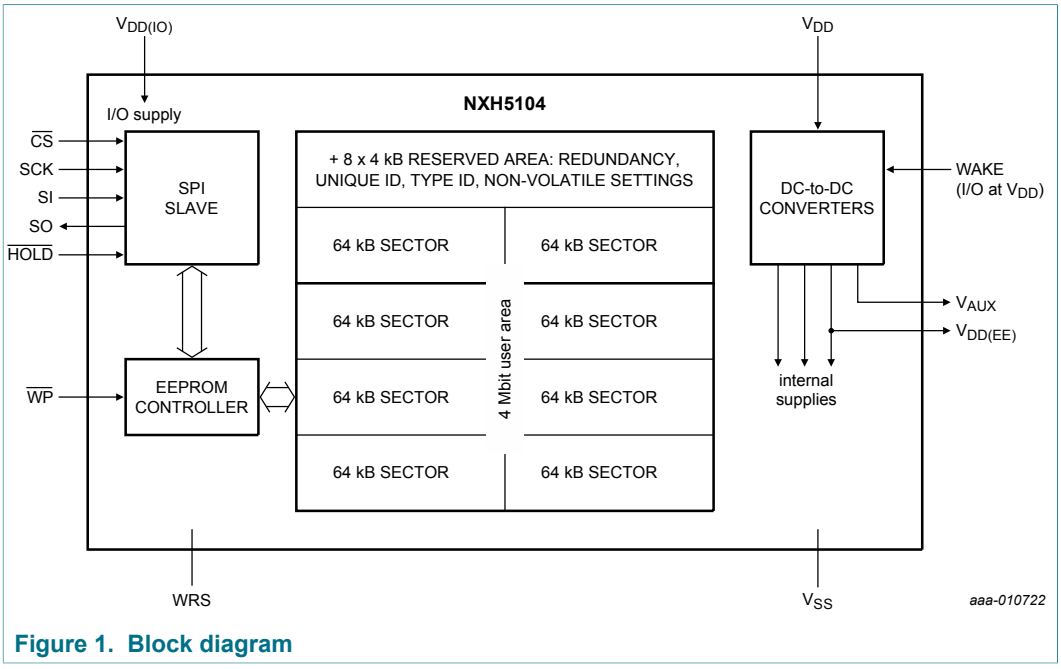


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

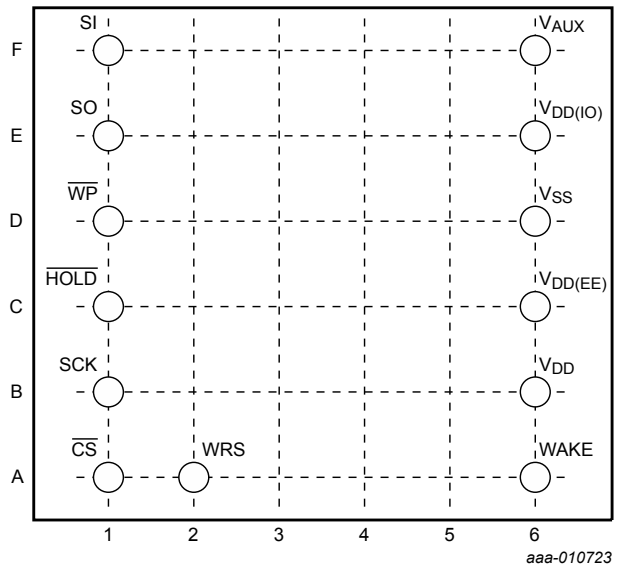


Figure 2. NXH5104 13 bump SPI package configuration (bottom view)

5.2 Pin description

Table 2. Bump allocation table

Bump	Symbol	Type	Description
Supply			
B6	V_{DD}	PWR	primary supply input. The V_{DD} pin is used to supply the source voltage to the device. Operations at invalid V_{DD} voltages may produce spurious results and should not be attempted.
E6	$V_{DD(IO)}$	PWR	input/output supply input. The $V_{DD(IO)}$ pin is used to supply the IO voltage to the device and hence defines the signaling voltage of the SPI slave interface. The voltage level of $V_{DD(IO)}$ must be equal or higher than V_{DD}.
C6	$V_{DD(EE)}$	PWR	EEPROM array supply output. In wide range supply mode, this pin requires a 470 nF decoupling capacitor. In fixed high supply (FHS) mode, this pin must be pulled HIGH with a 1 MΩ resistor to V_{DD}.
F6	V_{AUX}	PWR	auxiliary supply output. This pin provides a configurable voltage source for supplying other devices. Section 6.3 describes this functionality. A separate application note (Ref. 2) provides more detailed usage information.
Ground			
D6	V_{SS}	GND	analog/digital ground. Connect to the system GND.

Bump	Symbol	Type	Description
Configuration			
D1	$\overline{WP}$	DI	write-protect pin. This pin is used to prevent inadvertent writes to the EEPROM array. When connected to GND, the device is write protected. When connected to $V_{DD(IO)}$, the device is not write protected.
A2	WRS	DI	wide-range supply pin. This pin configures the supply mode of the device. When connected to $V_{DD(IO)}$, the chosen supply mode is the wide range supply mode. When connected to GND, the chosen supply mode is the fixed high supply mode. In this latter mode, a higher minimum voltage is required on V_{DD}, as described in Section 6.4.
Control			
A6	WAKE	DI	wake-up/power-down control input. To disable this functionality, the WAKE pin must be connected to GND. The SPI slave chip select input can then be used to wake up the device. To enable the WAKE functionality, the WAKE pin must be actively driven and may not be left unconnected nor floating. The input voltage level is referenced to V_{DD}.
SPI			
A1	$\overline{CS}$	DI	SPI slave chip select. • When the device is active, asserting the $\overline{CS}$ pin enables the device SPI interface. A HIGH-to-LOW transition on the $\overline{CS}$ pin initiates an SPI transaction. A LOW-to-HIGH transition ends the transaction. When the $\overline{CS}$ signal is deasserted, the SPI SO output pin is in a HIGH impedance state and commands issued to the device are not accepted. When the device is active, the signaling level is referenced to $V_{DD(IO)}$. • When the device is in power down, asserting the $\overline{CS}$ pin wakes up the device. Keeping the $\overline{CS}$ pin asserted while the device is waking-up, can stall the booting process. So, deassert the pin after minimum 200 ns. see Section 6.2 for more information. To wake up the device, the input level is referenced to V_{DD}.
E1	SO	DO	SPI slave serial data output. The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. The SO pin is in a high impedance state whenever the device is not selected. The signaling level is referenced to $V_{DD(IO)}$.For EMI, it is required to pull up the SO line at some place in the system: either the SPI master has an internal weak pull-up, either an external pull-up resistor is required.
F1	SI	DI	SPI slave serial data input. The SI pin is used the shift opcodes, addresses, and data into the device and latched on the rising edge of SCK. The signaling level is referenced to $V_{DD(IO)}$.
B1	SCK	DI	SPI clock input.

Bump	Symbol	Type	Description
C1	$\overline{HOLD}$	DI	SPI HOLD. The $\overline{HOLD}$ pin can be used to pause an on-going SPI transaction. More information on usage can be found in Section 6.1.1. The signaling level is referenced to $V_{DD(IO)}$. To disable this functionality, the $\overline{HOLD}$ pin must be connected to $V_{DD(IO)}$.

6 Functional description

6.1 SPI interface

The NXP Semiconductors NXH5104 acts as a slave device on the serial peripheral interface (SPI) bus. It supports mode 0 (0,0) and mode 3 (1,1) transfers at standard clock speeds up to 5 MHz. It also supports high-speed operation up to 10 MHz when $V_{DD(IO)}$ exceeds 1.8 V. Incoming data on the SI pin is latched on the rising edge of SCK. Outgoing data output on the SO pin is output on the falling edge of SCK. A leading or trailing falling edge of SCK is discarded.

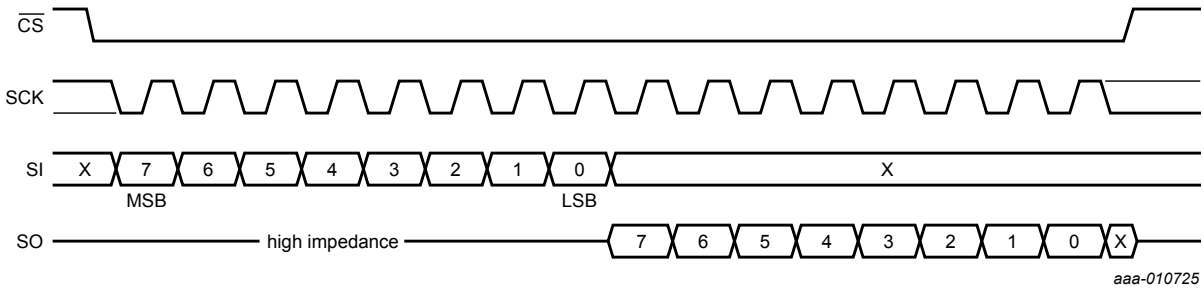


Figure 3. SPI mode 0/3

Transactions are byte-oriented, counting an integer multiple of 8-bit words, whereby the most significant bit (MSB) is transmitted first, least significant bit (LSB) last. The master initiates a transaction by asserting $\overline{CS}$ low and terminates it by de-asserting $\overline{CS}$ high, even if it is a single-byte command.

The command byte is the first byte transmitted by the master and received by the slave on the SI line after asserting low the $\overline{CS}$ pin.

6.1.1 SPI transaction hold

A $\overline{HOLD}$ input is provided as an extension to the SPI interface. It enables the host to suspend an ongoing transaction such as performing a high priority transaction with another slave device.

While $\overline{HOLD}$ is asserted low, the device releases the SO line to a high impedance state and discards any transitions on SCK and SI lines. The $\overline{CS}$ line however, must remain asserted. When the $\overline{HOLD}$ input is deasserted high, the suspended transaction resumes.

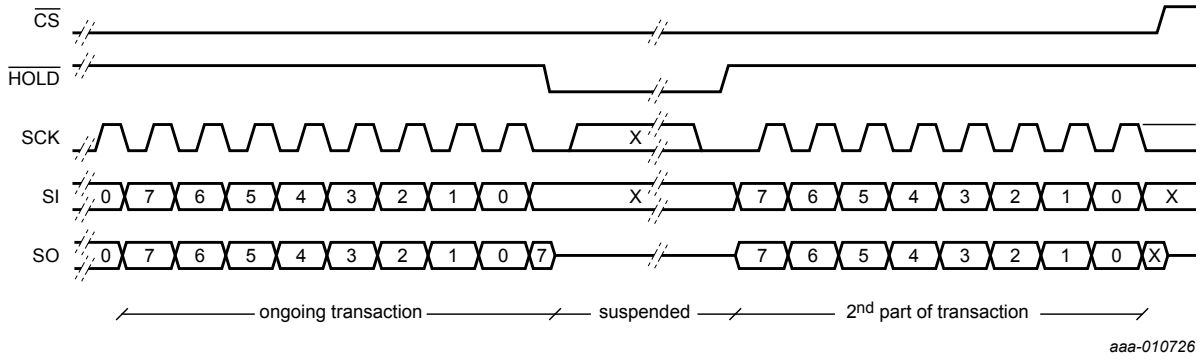


Figure 4. SPI transaction hold

When SCK is stable, the $\overline{HOLD}$ input must be asserted low. It must be deasserted during the same clock phase as it was asserted.

The $\overline{HOLD}$ input must be asserted after the last bit of a byte has been asserted on SI (see Figure 4).

If this feature is not used, the $\overline{HOLD}$ input must be tied to $V_{DD(IO)}$.

6.1.2 Overview commands

The NXP Semiconductors NXH5104 uses 8-bit commands. For some of these commands, the device needs time to execute the action during which no new commands can be serviced. These commands are referred to as extended operation commands (EOC). For instance, the WRITE command is an EOC. The WRITE command triggers an erase-program cycle during which other commands are not serviced.

The host must poll readiness by issuing RDSR commands and must observe if the $\overline{RDY}$ bit is asserted low.

If an invalid command byte is received, the command is ignored and the SO line remains in a high impedance state.

There are two types of write accesses: volatile and persistent. When a setting is written volatile, the change takes effect, but this setting reinitializes with its default value after a device power cycle. When a setting is written persistent, the change takes effect and the updated value is automatically loaded after a device power cycle.

Table 3. SPI command set overview

Command	Value	Description	EOC	Reference
WRSR	01h	write status register	yes	Table 12
WRITE	02h	write data bytes to memory array	yes	Table 7
READ	03h	read data bytes from memory array	no	Table 4
WRDI	04h	disable write operations	no	Table 9
RDSR	05h	read status register	no	Table 17
WREN	06h	enable write operations	no	Table 8
RDID	83h	read device ID and unique ID	no	Table 18
RDR	F9h	read response	no	Table 20
STBY	E0h	standby command	yes	Table 26

Command	Value	Description	EOC	Reference
SLEEP	E1h	sleep command	yes	Table 25
PWDN	E2h	power-down command	yes	Table 24
VWXSR	E3h	volatile write of extended status register	yes	Table 15
PWXSR	E4h	persistent write of extended status register	yes	Table 16
VAUXVW	E5h	volatile write of auxiliary supply configuration register (VAUXCFG)	yes	Table 27
VAUXPW	E6h	persistent write of auxiliary supply configuration register (VAUXCFG)	yes	Table 28
VAUXR	E7h	prepares a read auxiliary supply configuration register (VAUXCFG). To read the auxiliary supply configuration register value, use the RDR (Read Response) command.	yes	Table 29
WOIR	E8h	prepares a read of wear out status register. To read the wear-out status register value, use the RDR (Read Response) command.	yes	Table 21
RVDD	E9h	prepares a read of the V_{DD} supply voltage level. To read back the prepared data, use the RDR (Read Response) command.	yes	Table 23

6.1.3 SPI read operation (READ)

A read operation of the memory array is initiated when the SPI master issues a READ command, followed by the sector byte and the 16-bit address. The latter defines the offset within the chosen sector.

The NXP Semiconductor NXH5104 contains eight sectors; hence the SA field contains 3 bits. The remaining most-significant bits of the sector byte must be zero!

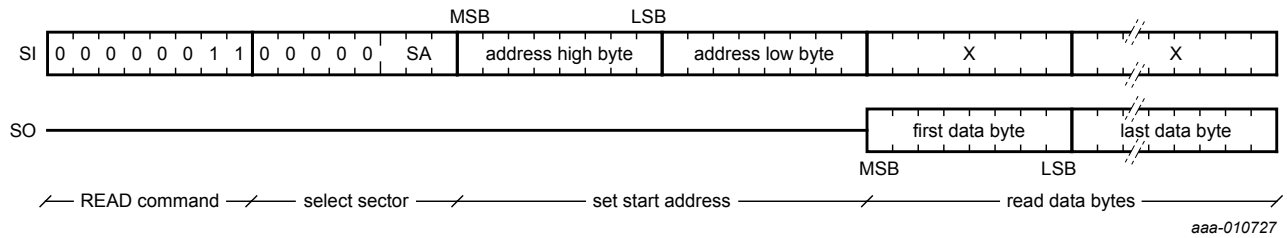


Figure 5. SPI read operation

Immediately following the last address byte (READ command), the device starts driving the SO line. It transmits consecutive data bytes read from the memory array, starting at the selected memory location, until the $\overline{CS}$ input is asserted HIGH.

During read operations, the internal address counter auto-increments. What happens at a sector boundary depends on the setting of the RAWMODE field of the extended status register (see Table 14). When RAWSEC is chosen, the address automatically wraps at the sector boundary. When RAWFULL is chosen, the address automatically increments beyond the sector boundary to the next sector.

If a previous program operation is in progress, the memory read/write operation is prohibited (treated as an invalid command).

A READ command is only allowed on sectors which are in power-up mode.

Table 4. SPI READ command

Byte	Access	Command	Value	Description
0	W	READ	03h	read data bytes from memory
1:3	W	SPI_AR	-	address register
4:...	R	DATA	-	data bytes

6.1.4 SPI write protection

To prevent inadvertent writes to the memory array and status register, software and hardware protection mechanisms are included in the device.

The following protection is available for writing to the EEPROM memory array:

- The write enable bit (WEN) must be first set by issuing a write enable (WREN) command. It is cleared by issuing a write disable (WRDI) command. The write enable bit is also automatically cleared at power-up, after each WRITE command, and when the status register is written (WRSR or PWXSR).
- The corresponding sector protection bit SP(n) must be disabled.
- If a program operation is still in progress ($\overline{RDY}$ = 1), writes are prohibited.

Table 5. SPI memory array write protection

$\overline{RDY}$	WEN	WREN	$\overline{WP}$	SP(n)	WRITE command [1]
1	X	X	X	X	prohibited
X	0	X	X	X	prohibited
X	X	X	X	1	prohibited
0	1	X	X	0	allowed

[1] When prohibited, the WRITE command is treated as an invalid command.

The following protection is available for writing to the status register:

- The write enable bit (WEN) must be set by issuing a write enable (WREN) command. It is cleared by issuing a write disable (WRDI) command. It is also automatically cleared at power-up, after each WRITE instruction and when the status register is written (WRSR or PWXSR).
- If the nonvolatile WPEN bit is set and the $\overline{WP}$ input is asserted low, hardware write protection is enabled.
- If a program operation is still in progress ($\overline{RDY}$ = 1), writes are discarded.

Table 6. SPI Status register write protection

$\overline{RDY}$	WEN	WPEN	$\overline{WP}$	SP(n)	WRSR or PWXSR commands [1]
1	X	X	X	X	prohibited
X	0	X	X	X	prohibited
0	1	1	0	X	prohibited
0	1	0	X	X	allowed

$\overline{RDY}$	WEN	WPEN	$\overline{WP}$	SP(n)	WRSR or PWXSR commands [1]
0	1	X	1	X	allowed

[1] When prohibited, the WRSR and PWXSR commands are treated as invalid commands.

Because the granularity of the write protection mechanisms is sector-based, it is recommended to store different types of data (e.g. firmware instructions versus data logging) in separate sectors.

6.1.5 SPI write operation (WRITE)

Since the write enable bit (WEN) is cleared after each write operation, a write enable (WREN) command must precede each WRITE command. The write enable (WREN) command and write disable command (WRDI) are single-byte commands.

A write operation is initiated when the master issues a WRITE command followed by 3 bytes. The first byte selects the sector, and the remaining 2 bytes set the 16-bit address pointer (offset within the sector).

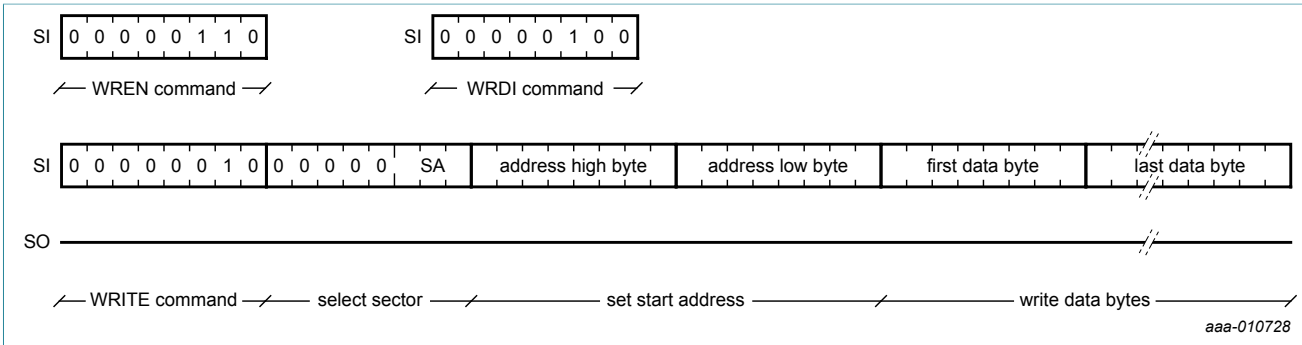


Figure 6. SPI write operation

Following the address bytes, any number of data bytes between 1 and 256 transmitted by the master, are written to the page write buffer. The write transfer is completed by asserting $\overline{CS}$ high, upon which an internal self-timed program cycle is started.

The eight lower bits of the address counter, corresponding to the offset within the page buffer, auto-increment after each byte is written via SPI. Hence, the current address wraps at page boundary. If more than 256 data bytes are transferred via SPI, all bytes from byte 256 are discarded.

A write operation must be preceded by setting the write enable bit (see Section 6.1.4).

A write operation is initiated when the master issues a WRITE command byte followed by the sector byte and the 16 bit (2 bytes) address. The latter defines the offset within the chosen sector.

The NXP Semiconductors NXH5104 contains eight sectors; hence the SA field contains 3 bit. The remaining most significant bits of the sector byte must be logic 0!

If more than 256 data bytes are transferred through the SPI slave interface, these additional bytes are discarded.

Table 7. SPI WRITE command: write data bytes to memory

Byte	Access	Command/Data	Value	Description
0	W	WRITE	02h	write data bytes to memory.
1:3	W	SPI_AR	-	address register.
4:...	R	DATA	-	data bytes.

Table 8. SPI WREN command: enable write operations

Byte	Access	Command/Data	Value	Description
0	W	WREN	06h	enable write operations

Table 9. SPI WRDI command: disable write operations

Byte	Access	Command/Data	Value	Description
0	W	WRDI	04h	disable write operations

Table 10. SPI address register (SPI_AR)

Bits	Access [1]	Field	Value	Description
23:19	W	-	00000b	fixed SPI prefix. These bits should be written as zeros
18:16	W	SA_0	000b	sector address bits. Sector 0
		SA_1	001b	sector address bits. Sector 1
		SA_2	010b	sector address bits. Sector 2
		SA_3	011b	sector address bits. Sector 3
		SA_4	100b	sector address bits. Sector 4
		SA_5	101b	sector address bits. Sector 5
		SA_6	110b	sector address bits. Sector 6
		SA_7	111b	sector address bits. Sector 7
15:8	W	AH	-	high address bit
7:0	W	AL	-	low address bit

[1] W = volatile writable.

A write operation consists of an erase cycle followed by a programming cycle. To ensure the endurance, an adaptive trimming algorithm checks if the erase cycle was successful. If not, another erase cycle is started at a higher (internal) supply level. This process leads to a programming time, which can be considerably longer than the typical programming time (see Table 36). It is highly recommended to poll completion through the RDSR command. As soon as the write operation is completed, the host can continue and issue new commands.

6.1.6 SPI status register

The status register (SR) is accessible through the RDSR and WRSR instructions. It can be read at any time to poll the device RDY status bit. The other bits of the status register are not updated when the RDY is indicating busy state. They can be overwritten using the WRSR instruction. Under applicable write protection conditions (see Section 6.1.4), the WRSR command initiates a write of the status register

The status register can be accessed as part of the extended status register (XSR).

Table 11. SPI status register

Bits	Access [1]	Field	Value [2]	Description
-	R/P	SR	(00h)	status register.
7	R/P	WPEN	(0b)	write protect enable bit.
6:4	R	-	(000b)	(reserved).
3:2	R/P	SP	(00b)	sector protection.
		SPNONE	00b	sector protection disabled.
		SPQUART	01b	protect sector 6 and 7 (upper quarter).
		SPHALF	10b	protect sectors 4 to 7 (upper half).
		SPALL	11b	protect all sectors.
1	R [3]	WEN	(0b)	write enable bit.
0	R	$\overline{\text{RDY}}$	(0b)	ready status bit.

[1] R = readable, P = persistent writable.
[2] Default manufacturing values between brackets.
[3] The WREN/WRDI commands set/clear the WEN bit.

Table 12. SPI write status register

Byte	Access	Command/Data	Value	Description
0	W	WRSR	01h	write status register.
1	P	SR	-	status register.

Table 13. SPI read status register

Byte	Access	Command/Data	Value	Description
0	W	RDSR	05h	read status register.
1	R	SR	-	status register.

6.1.7 SPI extended status register

An extended, 32-bit status register (XSR) can be read using the same RDSR command. The upper (first) byte corresponds to the 8-bit status register (SR). Reading beyond this first byte provides access to extended features/settings of the device.

Two functions support writing to the extended status register:

- VWXSR: Volatile write of the XSR. Only the fields indicated with W are writing.
- PWXSR: Persistent write of the XSR. Only the fields indicated with P are writing.

Manufacturing default R/W/P fields are indicated (between brackets). A persistent write can configure the device in a mode which is unrecoverable. It is recommended that the host programs the preferred settings once at initial start-up.

Table 14. SPI XSR: extended status register

Bits	Access [1]	Field	Value [2]	Description
-	R/W/P	XSR	(0010h)	extended status register
31:24	R/P	SR	(00h)	status register
23:16	R/W/P	SPD	(00h)	sector power-down
		bit 23	1b	power-down sector 7
		bit 22	1b	power-down sector 6
		bit 21	1b	power-down sector 5
		bit 20	1b	power-down sector 4
		bit 19	1b	power-down sector 3
		bit 18	1b	power-down sector 2
		bit 17	1b	power-down sector 1
		bit 16	1b	power-down sector 0
15:14	W	PMI	(00b)	power mode indicator
		PMSB	00b	standby.
		PMS	01b	sleep
13:12	R/W/P	IOMODE	(00b)	select $V_{DD(IO)}$ mode
			0xb	$V_{DD(IO)} = V_{DD}$.
			10b	$V_{DD(IO)}$ is fixed, > 1.5 V
			11b	$V_{DD(IO)}$ is fixed, < 1.5 V
11:8	R	-	(00b)	(reserved).
7	R	WOI	(0b)	wear-out indication
		WOIOK	0b	no wear-out, indication OK
		WOINOK	1b	wear-out, indication not OK
6:5	R	PSTAT	(00b)	result of last program operation
		PNONE	00b	no program cycle has been started
		PSUCCESS	01b	program cycle succeeded
		PABORT	10b	program cycle aborted
		PWORN	11b	page is worn out

Bits	Access [1]	Field	Value [2]	Description
4	R/W/P	RAWMODE	(1b)	read address wrapping mode
		RAWSEC	0b	wrap address at sector boundary
		RAWFULL	1b	read across sector boundary
3	R/W/P	WPPOL	(0b)	write protect input polarity
		PLOW	0b	active low polarity
		PHIGH	1b	active high polarity
2:0	R	-	(000b)	(reserved)

[1] R = readable, W = volatile writable, P = persistent writable.
[2] Default manufacturing values between brackets.

Table 15. SPI VWXSR command: volatile write extended status register

Byte	Access	Command/Data	Value	Description
0	W	VWXSR	E3h	volatile write extended status register.
1:4	W	XSR	-	extended status register.

Table 16. SPI PWXSR command: persistent write extended status register

Byte	Access	Command/Data	Value	Description
0	W	PWXSR	E4h	persistent write extended status register.
1:4	W	XSR	-	extended status register.

Table 17. SPI read status register

Byte	Access	Command/Data	Value	Description
0	W	RDSR	05h	read status register.
1:4	R	XSR	-	extended status register.

6.1.8 SPI device identification

Device identification data comprises a fixed device ID as well as a unique ID. The identifiers can be retrieved using the RDID command. This command can only be applied if sector 0 is powered-up.

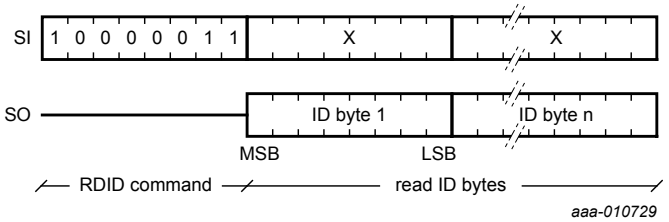


Figure 7. Device identification

Table 18. SPI RDID command: read device ID and unique ID

Byte	Access	Command/Data	Value	Description
0	W	RDID	83h	read device ID and unique ID
1:3	R	DEVID	(001010h)	device ID
4:15	R	UID	-	unique ID.

Table 19. SPI device ID

Bits	Access	Field	Value	Description
-	R	DEVID	(001010h)	device ID
23:12	R	MFG	(001h)	manufacturing identification
11:3	R	PART	(000000010b)	part identification
2:0	R	REV	(000b)	revision number

6.1.9 SPI read response (RDR)

Reads a 32-bit register after the extended commands: VAUXR or WOIR.

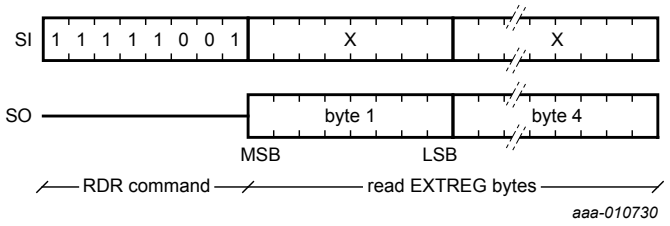


Figure 8. Read response

Table 20. SPI RDR command: read response

Byte	Access	Command/Data	Value	Description
0	W	RDR	F9h	read extended register.
1:4	R	EXTREG	-	extended register.

6.1.10 SPI wear-out status register (WOIR)

If the bit WOI in the XSR is set, a part of the EEPROM has reached its maximal endurance level. The host can request more details by consulting the wear-out status register (WOSR).

The register gives details informing which sector has reached the maximal endurance level.

The command WOIR prepares the wear-out status register.

The host must poll readiness by issuing RDSR commands and observing that the $\overline{\text{RDY}}$ bit is asserted low. To read the wear-out status register value, use RDR.

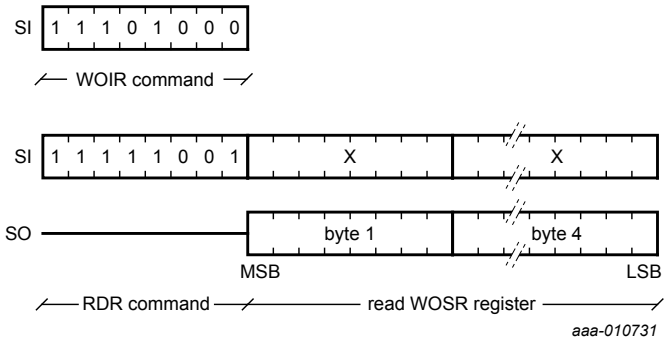


Figure 9. SPI wear-out status read sequence

Table 21. SPI wear-out status register

Bits	Access	Field	Value	Description
-	R	WOSR	-	wear-out status register.
31:24	R	SPD	(00h)	wear-out indicator.
		bit 31	1b	wear-out of sector 7 when set to 1.
		bit 30	1b	wear-out of sector 6 when set to 1.
		bit 29	1b	wear-out of sector 5 when set to 1.
		bit 28	1b	wear-out of sector 4 when set to 1.
		bit 27	1b	wear-out of sector 3 when set to 1.
		bit 26	1b	wear-out of sector 2 when set to 1.
		bit 25	1b	wear-out of sector 1 when set to 1.
		bit 24	1b	wear-out of sector 0 when set to 1.
23:0	R	-	undefined	(reserved).

Table 22. SPI RDR command: read response

Byte	Access	Command/Data	Value	Description
0	W	WOIR	E8h	Prepares a read of the wear-out status register. To read the wear-out status register value, use RDR.

When writing a single byte, the full 32-bit data word containing this byte is cycled (erased and programmed) and eventually wears out. However, the internal adaptive algorithm for guaranteeing the endurance works on pages. So, when a user wears out a word by only repeatedly writing to only this location, it effectively wears out the full 128 bytes page.

6.1.11 SPI read of the V_{DD} supply (RVDD)

After the device receives the SPI read of the V_{DD} supply command, a response can be eventually read in the response register.

The command RVDD prepares the read of the V_{DD} supply.

The host must poll readiness by issuing RDSR commands and observing whether the $\overline{RDY}$ bit is asserted low.

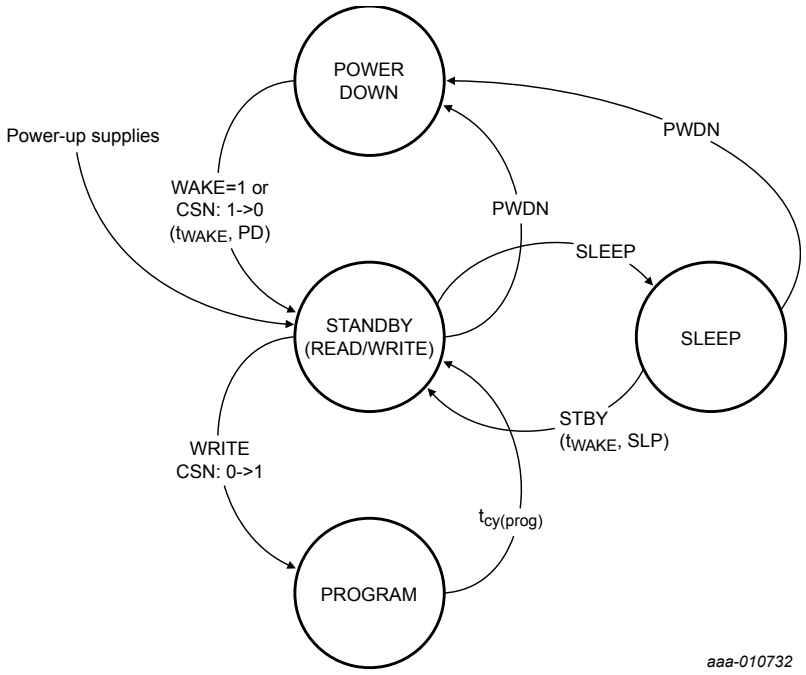
To read the value of the V_{DD} supply, use RDR.

Table 23. SPI read of the V_{DD} supply

Bits	Access	Field	Value	Description
7:4	R	RVDD	(0h)	V_{DD} supply voltage level
			0h	0.850 V to 0.950 V
			1h	0.925 V to 1.025 V
			2h	1.000 V to 1.100 V
			3h	1.050 V to 1.150 V
			4h	1.150 V to 1.250 V
			5h	1.200 V to 1.300 V
			6h	1.250 V to 1.350 V
			7h	1.350 V to 1.450 V
			8h	1.400 V to 1.500 V
			9h	1.500 V to 1.600 V
			Ah	1.550 V to 1.650 V
			Bh	1.650 V to 1.750 V
			Ch	1.700 V to 1.800 V
			Dh	1.800 V to 1.900 V
			Eh	1.850 V to 1.950 V
			Fh	1.900 V to 2.000 V
3:0	-	(reserved)	(0h)	-

6.2 Power modes

To conserve power, the NXH5104 features scalable power modes as illustrated below.



1. PDWN, SLEEP, STBY, WRITE are host commands.
2. WAKE and $\overline{CS}$ are input pins.
3. WAKE signal should be = 1 during at least $t_{wake(pd)}$ to transition cleanly from POWER DOWN state to STANDBY state.
4. In SLEEP state, the device is only responding to a limited number of host commands (STBY, PWDN, and RDSR). The V_{aux} supply is not available in this mode.
5. Transition to PROGRAM state occurs after the host reverts $\overline{CS}$ to high and the device is presented with the complete page or word to be written.
6. Program cycle time t_{prog} depends on whether a full 256 bytes sector or half sector is being written.

Figure 10. Power modes

6.2.1 Boot

When V_{DD} is supplied, the device boots in the standby mode by default.

Keeping the $\overline{CS}$ pin asserted during that phase can stall the booting process. So, as soon as V_{bat} and V_{IO} are supplied and stable, deassert the $\overline{CS}$ pin.

When the CS pin is deasserted, and after the wake-up time $t_{wake(pd)}$ has elapsed, the device is active and ready to process requests. To test if the device is ready, poll the RDY bit.

To move the device to sleep mode or power-down mode, give the sleep command or power-down command over the SPI interface.

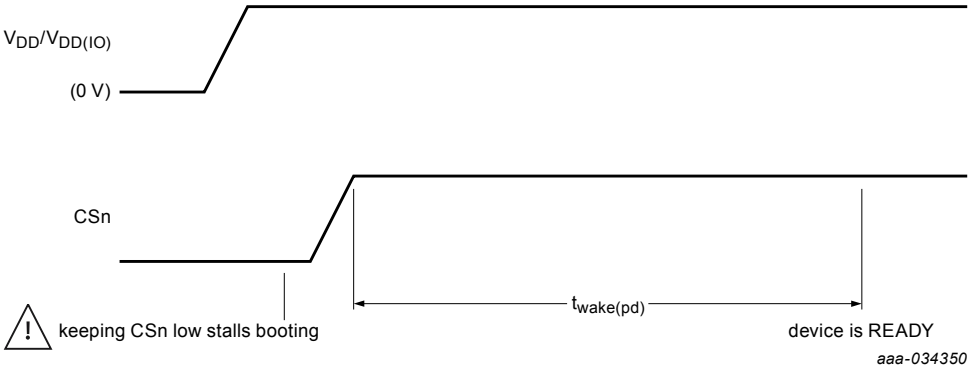


Figure 11. External supply ramp-up and CSn handling

6.2.2 Power-down

When the CS pin is asserted low, the device starts ramping-up its (internal) supplies.

Keeping the $\overline{CS}$ pin asserted while the device is waking up can stall the booting process. So, deassert the pin after minimum 200 ns.

When the CS pin is deasserted, and after the wake-up time $t_{wake(pd)}$ has elapsed, the device is active and ready to process requests. To test if the device is ready, poll the RDY bit.

Wake up using the $\overline{CS}$ pin

When the $\overline{CS}$ pin is asserted low, the device starts to ramp up its (internal) supplies. Keeping the $\overline{CS}$ pin asserted while the device is waking up can stall the booting process. So, deassert the pin after minimum 200 ns. When the $\overline{CS}$ pin is deasserted and after the wake-up time $t_{wake(pd)}$ has elapsed, the device is active and ready to process requests. To test if the device is active and ready, poll the RDY bit. This detection mechanism becomes active 1 ms after applying V_{DD}.

Wake-up using the WAKE pin

If the WAKE pin is de-asserted (low) at start-up, the device remains in power-down mode until the WAKE pin is asserted high.

When the WAKE pin is asserted high, the device ramps-up its supplies. After wake-up time $t_{wake(pd)}$, the supplies are stable and the device becomes active and ready to process requests. The $\overline{RDY}$ bit can be used to test that it is ready.

Note: *The wake must be asserted low again before reverting to the power-down mode.*

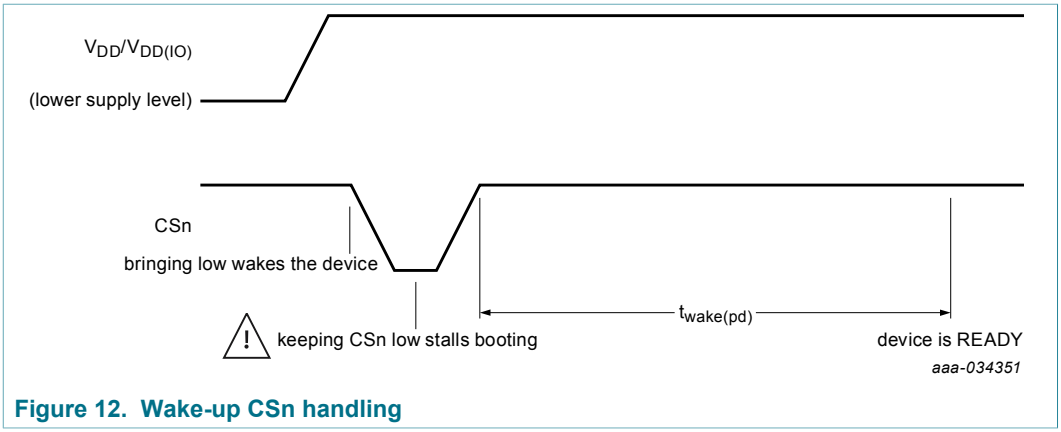


Figure 12. Wake-up CSn handling

When a PDWN command is issued, the device enters power-down mode.

It takes t_{pd} for the device to finalize the shut-down sequence. Do not to disturb this process and keep $\overline{CS}$ deasserted.

If a program cycle is still in progress, the PDWN command is ignored. The $\overline{RDY}$ bit can first be polled to check if the command is valid.

Table 24. SPI PDWN: power-down command

Byte	Access	Command	Value	Description
0	W	PWDN	E2h	power-down command.

6.2.3 Sleep

Sleep mode is a power-saving mode in which the EEPROM array is powered down. However, internally generated supplies are maintained and the serial interfaces remain responsive to a limited set of host commands. The auxiliary supply voltage (V_{aux}) cannot be maintained. For more information, see the application note: V_{AUX} - Auxiliary voltage supply (Ref. 2). This mode enables faster activation ($t_{wake(sleep)}$) compared to sleep mode and power-down mode. When a SLEEP command is issued, the device enters sleep mode. If a program cycle is still in progress, the SLEEP command is ignored. The $\overline{RDY}$ bit can first be polled to check if the command is valid.

When in sleep mode, the device only responds to STBY, RDSR, and PDWN commands. The V_{aux} supply is not available in sleep mode.

Table 25. SPI SLEEP: Sleep command

Byte	Access	Command	Value	Description
0	W	SLEEP	E1h	sleep command.

6.2.4 Standby

In standby mode, the EEPROM remains powered and ready to process read/write requests.

When an STBY command is issued in sleep mode, the device ramps-up its internal supplies. After wake-up time $t_{wake(sleep)}$, the supplies are stable and the enabled EEPROM array sectors are switched to power-on state. The enabled EEPROM array sectors are configured in the XSR register (non-user area).The device becomes active and ready to process read/write requests. Polling the $\overline{RDY}$ bit can be used to test it.

Wake-up from sleep mode is faster ($t_{wake(sleep)}$) as it does not involve ramp-up of the supplies. It does involve switching the enabled EEPROM sectors to the Power-on state.

In standby mode, the EEPROM array can be read and written with READ and WRITE commands.

Table 26. SPI STBY: standby command

Byte	Access	Command	Value	Description
0	W	STBY	E0h	standby command.

6.3 Auxiliary supply

The auxiliary supply voltage (V_{aux}) is a configurable DC-to-DC supply, generated from the primary supply voltage (V_{DD}) for supplying an external auxiliary component. It is configured using the VAUXVW, VAUXPW, and VAUXR commands that configure the VAUXCFG register.

For performing a volatile write (VAUXVW) of the V_{AUX} configuration register, no preceding WREN command is required. If there is a persistent write (VAUXPW), a preceding WREN command is required.

Table 27. SPI VAUXVW command: volatile write auxiliary supply configuration

Byte	Access	Command/Data	Value	Description
0	W	VAUXVW	E5h	volatile write auxiliary supply configuration.
1:4	W	VAUXCFG	-	auxiliary supply configuration register.

Table 28. SPI VAUXPW command: persistent write auxiliary supply configuration

Byte	Access	Command/Data	Value	Description
0	W	VAUXPW	E6h	persistent write auxiliary supply configuration register; persistent write of the configuration register which is used for initialization after reset.
1:4	P	VAUXCFG	-	auxiliary supply configuration register.

Table 29. SPI VAUXR command: read auxiliary supply configuration

Byte	Access	Command/Data	Value	Description
0	W	VAUXR	E7h	prepares a read auxiliary supply register; to read the auxiliary supply configuration register value, use RDR.

Table 30. SPI auxiliary supply configuration

Bits	Access	Field	Value	Description
31:17	-	-	-	(reserved)
16	R/W/P	VAUXEN	(0b)	auxiliary supply enable
		VAUXEN_DIS	0b	disabled
		VAUXEN_EN	1b	enabled.
15	R/W/P	VAUXBY	(0b)	auxiliary supply bypass mode
		VAUXBY_DIS	0b	disabled
		VAUXBY_EN	1b	enabled
14	R/W/P	VAUXRATIO	(0b)	auxiliary supply ratio setting
			0b	ratio 2
			1b	ratio 3
13	-	-	-	(reserved)
12:11	R/W/P	VAUXDS	(00b)	auxiliary supply drive strength
			00b	1/4 of drive strength
			01b	2/4 of drive strength
			10b	3/4 of drive strength
			11b	4/4 of drive strength
10:8	R/W/P	VAUXDF	(000b)	auxiliary supply clock divider
			000b	maximum clock speed
			001b	clock divided by 2
			010b	clock divided by 4
			011b	clock divided by 8
			100b	clock divided by 16
			101b	clock divided by 32
			110b	clock divided by 64
			111b	clock divided by 128
7	R/W/P	VAUXREG	(0b)	auxiliary supply enable voltage regulation
			0b	disabled (open loop).
			1b	enabled (closed loop).
6:0	R/W/P	VAUXV	(0b)	auxiliary supply comparator mode
			00h	minimum (1.5 V)
			7Fh	maximum (3.3 V)

Note: *Details of the V_{aux} principle and operation can be found in the separate application note: V_{AUX} - Auxiliary voltage supply (Ref. 2).*

6.4 Supply mode

There are two V_{DD} supply modes available. The wide range supply pin (WRS) selects the supply mode.

If the supplied V_{DD} of the device is a regulated voltage always above 1.65 V, it is possible to use the fixed high supply (FHS) mode. In this mode, the DC-to-DC converter that is used to generate the EEPROM array voltage ($V_{DD(EE)}$) is bypassed. The rise time of this supply is hence almost instantaneous, reducing the overall start-up time of the device by approximately 1.5 ms. See Section 9 for the actual values. To select the fixed high supply mode, the WRS pin must be connected to GND.

If the minimum supplied V_{DD} of the device cannot be guaranteed to be above 1.65 V, the wide range supply mode can be used. To select the wide range supply mode, the WRS pin must be connected to $V_{DD(IO)}$.

6.5 Error-correcting code ECC)

The NXH5104 features an ECC to improve reliability. It provides six parity bits for every 32 data bits so that a 38-bit word in memory represents four data bytes internally. Single bit read errors within a word are corrected.

Since the NXP Semiconductors NXH5104 supports byte level access, it is only allowed to write part of the four data bytes that make up a word. However, if a partial word is modified, the entire word is updated and endures a program cycle. To benefit from the qualified endurance optimally (500 000 program cycles), write entire words (multiples of 4 bytes at word boundaries) within a single transaction.

6.6 Current measurements

The most interesting modes impacting the current consumption of the NXP Semiconductors NXH5104 are the READ and the WRITE mode. Measurements performed for these modes are shown in this section. The current has been measured using a differential voltage amplifier across the 10 Ω resistor, as shown in the schematic. The scale for all following graphs is 1 mA/division.

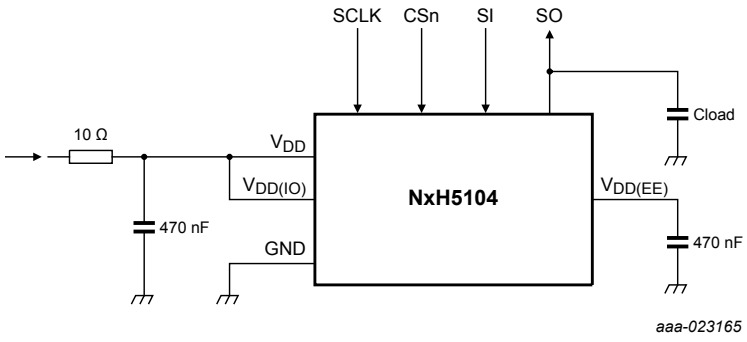
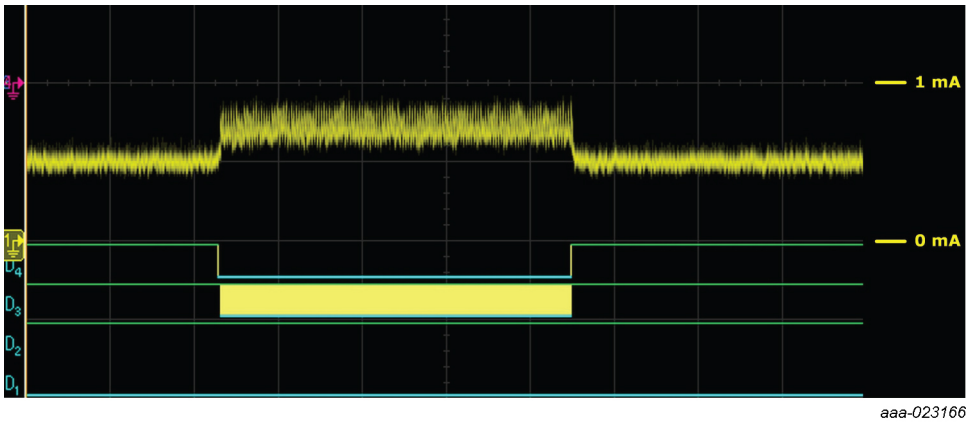


Figure 13. Current measurement configuration

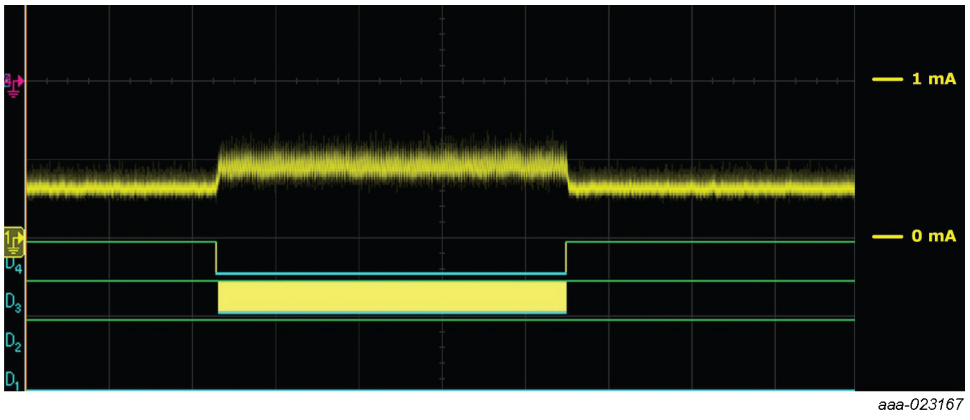
6.6.1 Read

The following graphs depict a READ operation, with varying levels of supply. Take note that the capacitive load (C_{load}) on the SO line dominates $I_{DD(IO)}$.



$V_{DD} = V_{DD(IO)}$ = 1.2 V, FSPI = 5 MHz, pink = CSn, yellow = $I_{DD} + I_{DD(IO)}$, purple = $V_{DD(EE)}$

Figure 14. Read operation with 1.2 V supply

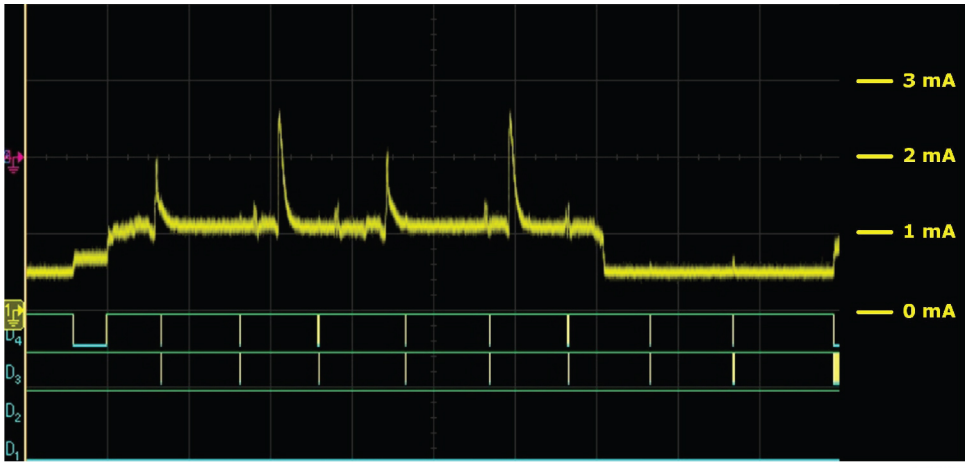


$V_{DD} = V_{DD(IO)}$ = 1.8 V, FSPI = 5 MHz, pink = CSn, yellow = $I_{DD} + I_{DD(IO)}$, purple = $V_{DD(EE)}$

Figure 15. Read operation with 1.8 V supply

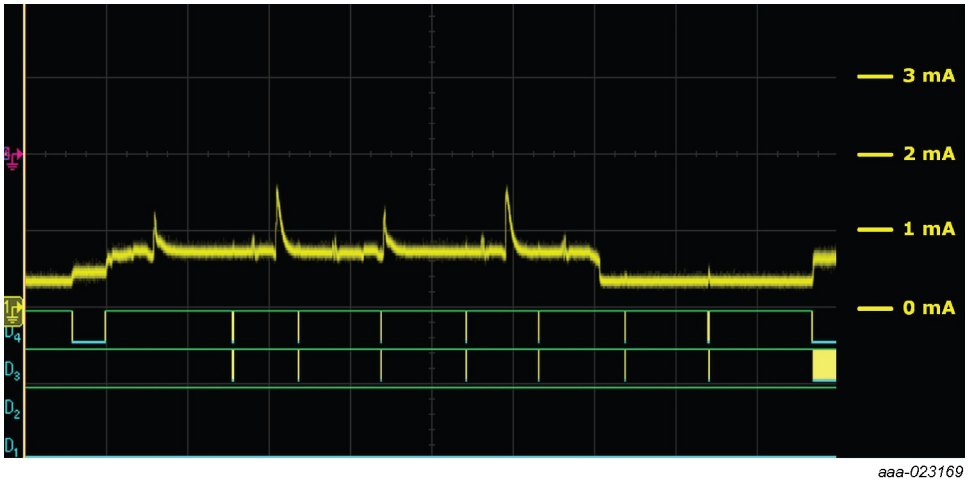
6.6.2 Write

The following graphs depict a WRITE operation, with varying levels of supply.



$V_{DD} = V_{DD(IO)} = 1.2$ V, FSPI = 5 MHz, pink = CSn, yellow = $I_{DD} + I_{DD(IO)}$, purple = $V_{DD(EE)}$

Figure 16. Write operation with 1.2 V supply



$V_{DD} = V_{DD(IO)} = 1.8$ V, FSPI = 5 MHz, pink = CSn, yellow = $I_{DD} + I_{DD(IO)}$, purple= $V_{DD(EE)}$

Figure 17. Write operation with 1.8 V supply

7 Limiting values

Table 31. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			−50	+150	°C
V_{DD}	supply voltage		[1]	-0.5	+2.4	V
$V_{DD(IO)}$	input/output supply voltage			−0.5	+5.2	V
V_{aux}	auxiliary voltage			−0.5	+5.2	V
V_{ESD}	electrostatic discharge voltage	human body model	[2]	-	2	kV
		charged device model	[3]	-	500	V
I_{lu}	latch-up current		[4]	-	±100	µA

[1] Maximum voltage for a lifetime of 1 hour at 60 °C, with 0.01 % failure rate and 95 % confidence bound.
[2] In accordance with JESD22-A114.
[3] In accordance with JESD22-C101.
[4] In accordance with JESD78.

7.1 Recommended operating conditions

Table 32. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{oper}	operating temperature			−20	+25	+85	°C
V_{DD}	supply voltage		[1]	1.0	1.2	2.0	V
$V_{DD(IO)}$	input/output supply voltage			1.0	V_{DD}	2.6	V
$V_{DD(IO)(1V2)}$	input/output supply voltage (1.2 V)	1.2 V signaling		1.08	1.2	1.9	V
$V_{DD(IO)(1V8)}$	input/output supply voltage (1.8 V)	1.8 V signaling		1.62	1.8	2.6	V

[1] During the READ and WRITE command execution the V_{DD} is allowed to dip to 0.9 V.

8 Static characteristics

Table 33. Static characteristics-1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Auxiliary supply						
V_{aux}	auxiliary voltage	regulation range	1.5	1.8	3.3	V
		regulation step	-	3.75	-	mV
$I_{aux(ext)}$	external auxiliary current	standby/active mode	-	0.75	2.0	mA
		pass-through mode	-	-	2.0	mA

Table 34. Static characteristics-2

Current from V_{DD}, excluding external current sourced through supply or I/O pads.

Symbol	Parameter	Conditions		1.2 V		1.8 V		Unit
				Typ	Max	Typ	Max	
$I_{DD(pd)}$	average power-down supply current			-	5	-	5	µA
$I_{DD(sleep)}$	average sleep supply current			80	-	70	-	µA
$I_{DD(stb)}$	average standby supply current	all sectors powered down	[1]	400	-	350	-	µA
		4 sectors active	[1]	635	-	475	-	µA
		all sectors active	[1]	870	-	600	-	µA
$I_{DD(RW)}$	average read supply current	4 sectors active and 5 MHz SPI	[1]	800	-	600	-	µA
$I_{DD(prog)}$	average write supply current	4 sectors active and 5 MHz SPI	[1]	1.1	-	0.7	-	mA

[1] Sectors powered down according to the SPD field in the External Status Register (XSR).

Table 35. Static characteristics-3

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltages and currents						
$V_{DD(EEPROM)}$	EEPROM supply voltage		1.5	1.6	2.0	V
Input characteristics[1]						
V_{IH}	HIGH-level input voltage		0.7 × V_S	-	2.6	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.3 × V_S	V
V_{hys}	hysteresis voltage		0.1 × V_S	-	-	V
Output characteristics 1.2 V signaling						
I_{OH}	HIGH-level output current	current sourcing capability; V_{OH} = 0.8 × $V_{DD(IO)(1V2)}$	2.0	-	-	mA
I_{OL}	LOW-level output current	current sinking capability; V_{OL} = 0.2 × $V_{DD(IO)(1V2)}$	2.0	-	-	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output characteristics 1.8 V signaling						
I_{OH}	HIGH-level output current	current sourcing capability; $V_{OH} = 0.8 \times V_{DD(IO)(1V8)}$	4.0	-	-	mA
I_{OL}	LOW-level output current	current sinking capability; $V_{OL} = 0.2 \times V_{DD(IO)(1V8)}$	4.0	-	-	mA

[1] For WAKE pin and WRS pin, $V_S = V_{DD}$. For all other I/Os, $V_S = V_{DD(IO)}$.

9 Dynamic characteristics

Table 36. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output characteristics – 1.2 V signaling							
$t_{r(io)}$	input/output rise time		[1]	1.0	-	10	ns
$t_{f(io)}$	input/output fall time		[1]	1.0	-	10	ns
Output characteristics 1.8 V signaling							
$t_{r(io)}$	input/output rise time		[1]	1.0	-	10	ns
$t_{f(io)}$	input/output fall time		[1]	1.0	-	10	ns
Input characteristics							
f_{SPI}	SPI frequency	1.2 V signaling	[2]	5	-	-	MHz
		1.8 V signaling	[2]	10	-	-	MHz
Reliability							
$N_{endu(W)}$	write endurance	number of program cycles	[3]	500 000	-	-	cycles
$t_{ret(data)}$	data retention time			10	-	-	years
Input characteristics							
t_{prog}	programming time	full 256 Byte sector	[4]	-	6.4	-	ms
		half sector		-	3.7	-	ms
$t_{wake(pd)}$	power-down mode wake-up time	Wide Range Supply mode		-	5	-	ms
		Fixed High Supply mode		-	3.5	-	ms
t_{pd}	power-down time			-	-	750	µs
$t_{wake(sleep)}$	sleep mode wake-up time			-	500	-	µs

[1] 5 nH bond wire inductance and 15 pF external capacitive load.
[2] $V_{DD} > 1.0$ V.
[3] Endurance qualified at page level.
[4] The programming time is consisting out of an erase cycle followed by a program cycle. To guarantee the endurance, an adaptive trimming algorithm could retry erasing, which leads to a longer programming time. The typical value given is for a programming time without erase retry. Very rarely (on average once in 200,000 write operations) such an additional erase/program cycle is performed, which increases the programming time to 11.3 ms. The user is strongly advised to use the available control flow. This control flow always provides the shortest access time by polling completion of the programming operation by using the RDSR command.

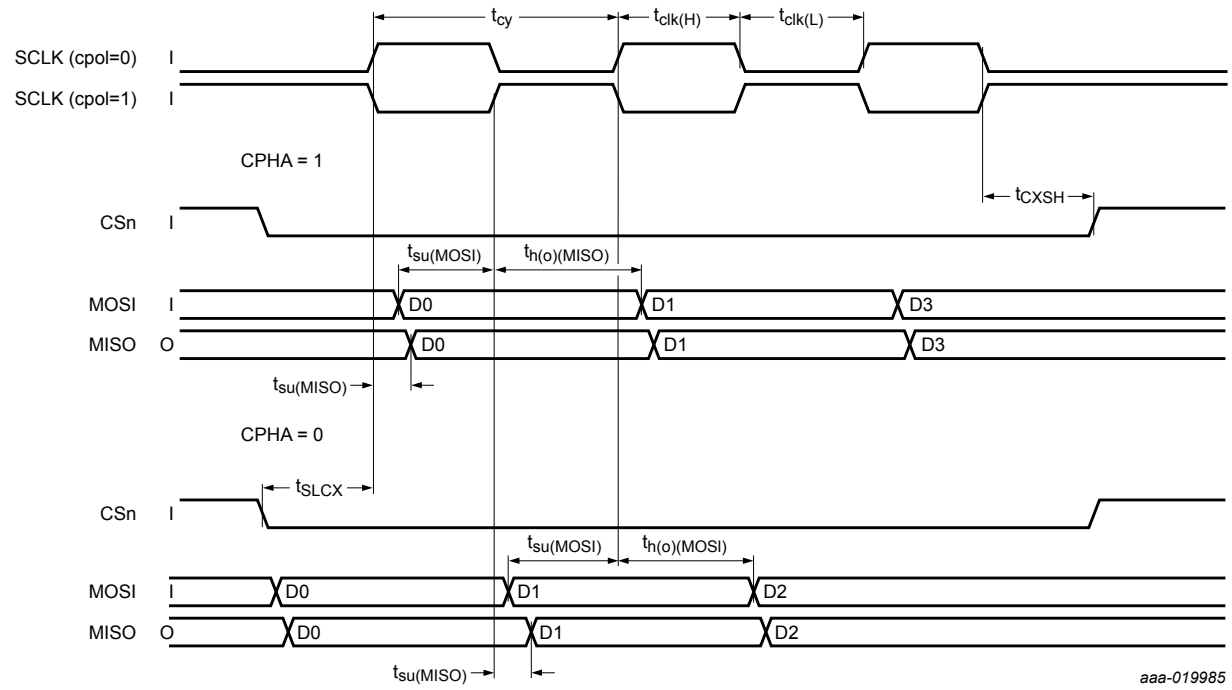


Figure 18. SPI slave timing

Table 37. SPI slave timing - 1.8 V signaling level

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{cy}	cycle time	$V_{DD(IO)}$ = 1.8 V, C_{LOAD} = 4 pF	100	-	-	ns
$t_{clk(H)}$	clock HIGH time		50	-	-	ns
$t_{clk(L)}$	clock LOW time		50	-	-	ns
t_{su}	set-up time	To the rising edge of PCLK. MOSI	20	-	-	ns
$t_{h(o)}$	output hold time	MOSI	20	-	-	ns
$t_{d(o)}$	output delay time	MISO	-	-	22.5	ns
t_{SLCX}	chip select LOW to clock changing		50	-	-	ns
t_{CXSH}	clock changing to chip select HIGH		50	-	-	ns

Table 38. SPI slave timing - 1.2 V signaling level

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{cy}	cycle time	$V_{DD(IO)}$= 1.2 V, C_{LOAD} = 4 pF	200	-	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	-	ns
$t_{clk(L)}$	clock LOW time		100	-	-	ns
t_{su}	set-up time	To the rising edge of PCLK. MOSI	20	-	-	ns
$t_{h(o)}$	output hold time	MOSI	20	-	-	ns
$t_{d(o)}$	output delay time	MISO	-	-	64.0	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SLCX}	chip select LOW to clock changing		100	-	-	ns
t_{CXSH}	clock changing to chip select HIGH		100	-	-	ns

10 Application information

The primary supply input (V_{DD}) accepts a voltage in range 1.0 V to 2.0 V and supports battery powered operation with various battery chemistries. Three configurations are demonstrated to connect the input/output supply ($V_{DD(IO)}$).

The auxiliary supply (V_{aux}) is available as an independent, configurable supply for auxiliary components.

In the following application diagrams, a 470 nF decoupling capacitor is proposed for decoupling V_{DD} and $V_{DD(IO)}$. This value is not strictly mandatory, another value may be chosen depending on the system integration.

10.1 Configuration 1 - Wide range single supply

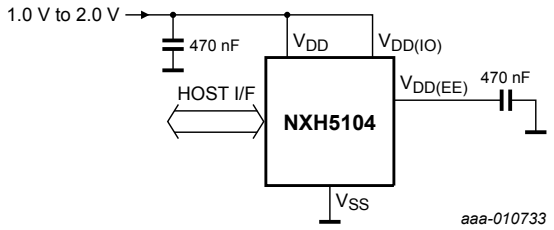


Figure 19. Single supply

According to application configuration 1 (Figure 19), the input/output signaling voltage ($V_{DD(IO)}$) can equal the primary supply. It enables single supply operation according to the specified voltage range.

10.2 Configuration 2 - Wide range dual supply

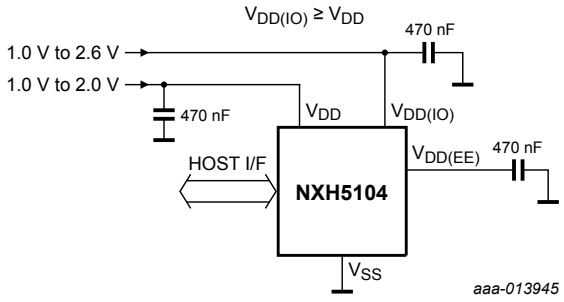


Figure 20. Dual supply

For configuration 2 (Figure 20), the input/output supply is different from the primary supply. The primary supply is typically connected to the battery. The input/output supply can be disabled while the primary supply stays powered. As long as the device is not powered down, the input/output supply must be valid.

10.3 Configuration 3 - Fixed high supply mode

If the V_{DD} is > 1.65 V in the WRS mode, configurations 1 (Figure 19) and 2 (Figure 20) can be used. In this case, capacitor C1 is not required.

If V_{DD} is a regulated voltage always above 1.65 V, it is possible to use the WRS mode. In this mode. In this mode, the DC-to-DC converter used to generate the V_{EE} voltage is bypassed. For this reason, the rise of this supply is almost instantaneous, reducing the overall start-up time of the device by approximately 1.5 ms. See Section 9 for the actual values.

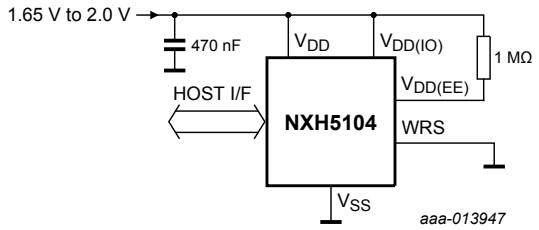


Figure 21. General-purpose 1.8 V supply

10.4 Configuration 4 - Auxiliary supply feeding $V_{DD(IO)}$

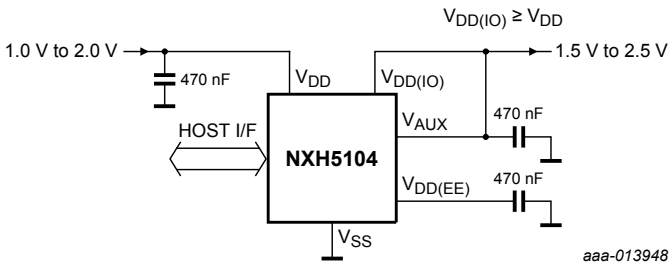


Figure 22. Auxiliary I/O supply

In this configuration, the auxiliary output V_{aux} can be used to feed $V_{DD(IO)}$. The V_{aux} output requires a 470 nF decoupling capacitor.

10.5 Application diagram - driving an LED

Figure 23 shows the application diagram for driving an LED. An additional capacitor may be required between V_{aux} and ground, depending on the application.

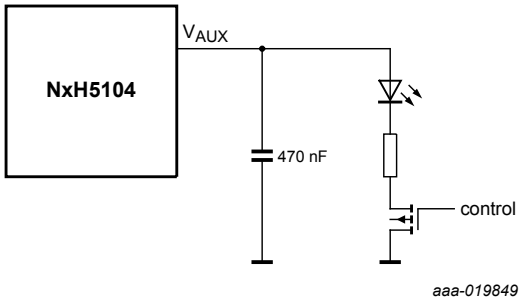


Figure 23. Application diagram for driving an LED

11 Packing information

Default packing for the WLCSP devices is tape and reel according to T1 taping orientation as depicted below.

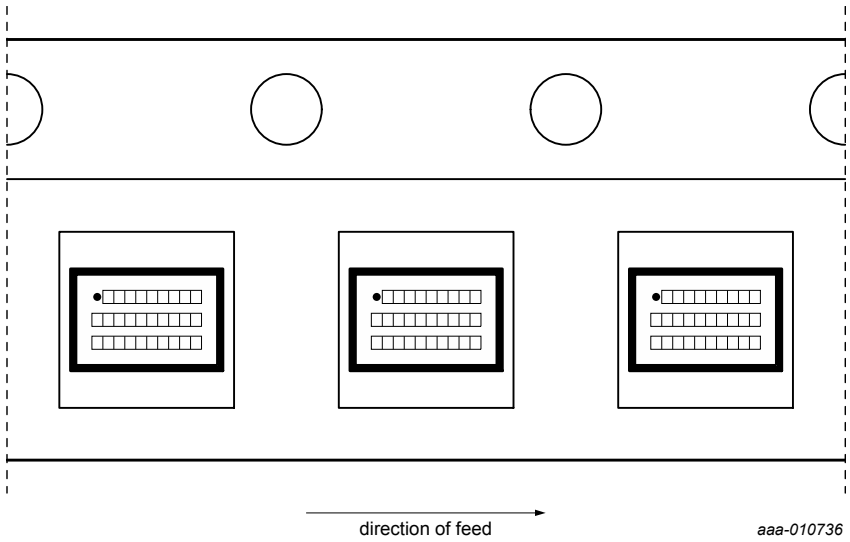


Figure 24. Tape and reel product orientation

Table 39. Die marking

Line	Description	Example
A	Device	NxH5104A1
B	Lot number - Wafer number	P6T659-03
C	Fab - year - week	E TDyyww
D	X-Y coordinates	03 xxx yyyy

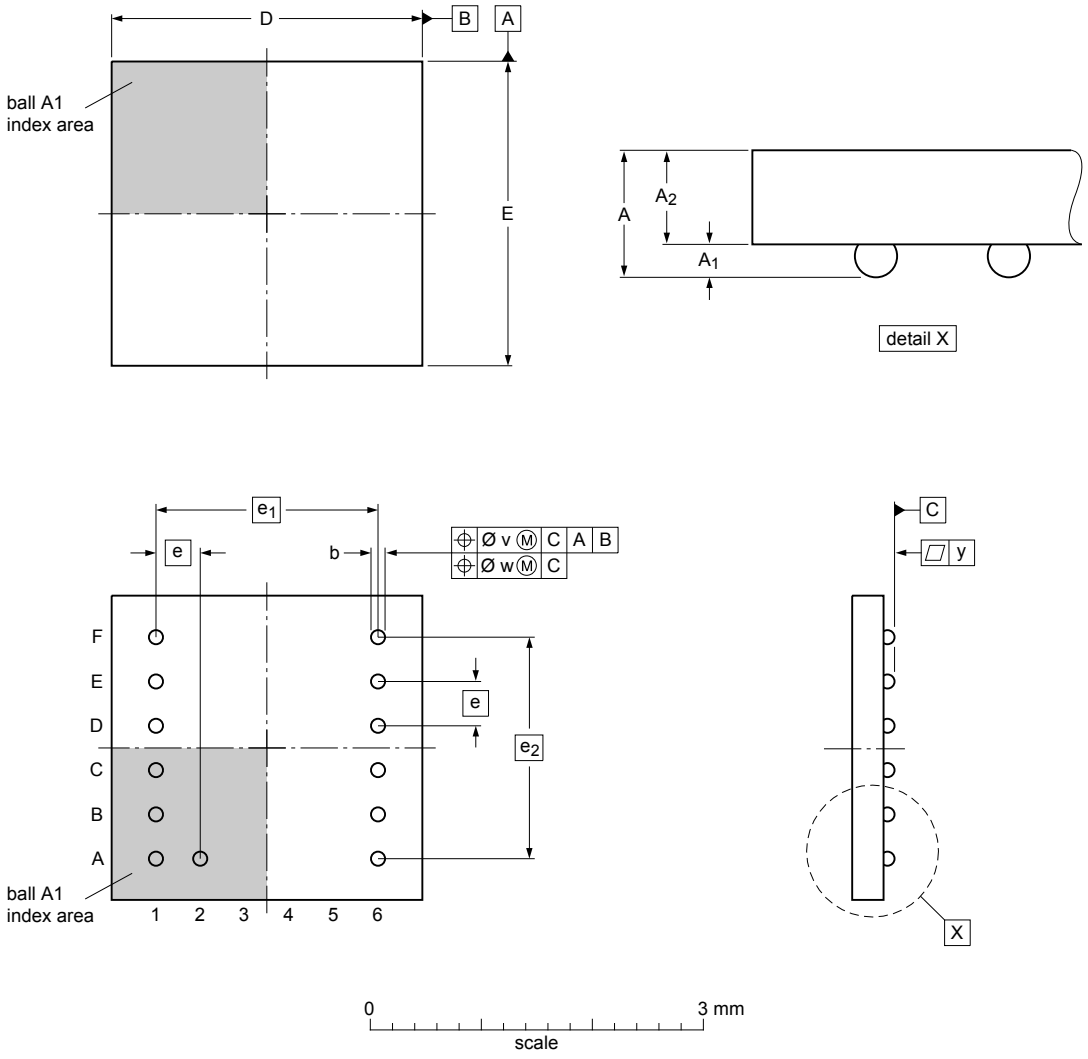
11.1 Physical specification

Table 40. Physical specification

Item		Specification	Remark
Solder bump	Material	Plating: SnAg1.8	Lead-free

12 Package outline

WLCSP13: wafer level chip-scale package; 13 bumps; 2.74 x 2.80 x 0.38 mm **SOT1461-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
max	0.42	0.115	0.305	0.140	2.83	2.77						
mm nom	0.38	0.100	0.280	0.125	2.80	2.74	0.4	2.0	2.0	0.15	0.05	0.02
min	0.34	0.085	0.255	0.110	2.77	2.71						

sot1461-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1461-1		- - -				~~15-09-29~~ 16-08-08

Figure 25. Package outline SOT1461-1 (WLCSP13)

13 Handling information

See the Flip chip application note (Ref. 1) for detailed instructions on handling, soldering and mounting WLCSP packaged devices.

14 Abbreviations

Table 41. Abbreviations

Acronym	Description
EEPROM	electrically erasable and programmable read-only memory.
EOC	extended operation command
LDO	low dropout regulator.
RoHS	restriction of hazardous substances (directive 2002/95/EC).
SPI	serial peripheral interface.
SR	status register
WLCSP	wafer-level chip-scale Package.
WOSR	wear-out status register
XSR	extended status register

15 References

[1] **AN11761 application note** — Flip chip; 2016, NXP Semiconductors
Available on: http://www.nxp.com/documents/application_note/AN11761.pdf

[2] **AN11660 application note** — V_{AUX} - Auxiliary voltage supply; 2016, NXP Semiconductors

16 Revision history

Table 42. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXH5104 v.6.3	20190703	Product data sheet	-	NXH5104 v.6.2
Modifications:	• Section 5.2 "Pin description" has been updated. • Section 6.2.1 "Power modes → Boot" has been updated. • Section 6.2.2 "Power modes → Power down" has been updated. • Section 9 "Dynamic characteristics" has been updated.			
NXH5104 v.6.2	20170516	Product data sheet	-	NXH5104 v.6.1
Modifications:	• The title of the data sheet has changed from "4 Mbit Serial EEPROM" to "4 Mbit Serial SPI EEPROM". • Section 6.1.10 has been updated.			
NXH5104 v.6.1	20170308	Product data sheet	-	NXH5104 v.6
Modifications:	• Section 3 has been updated. • Section 12 has been updated. • Section 15 has been updated.			
NXH5104 v.6	20170111	Product data sheet	-	NXH5104 v.5
Modifications	• Addition to section describing SPI write protection • Data sheet promoted to Product			
NXH5104 v.5	201609289	Objective data sheet	-	NXH5104 v.4
Modifications	• Reference [1] changed • POD updated • Security status changed to Company Public			
NXH5104 v.4	20160805	Objective data sheet	-	NXH5104 v.3
NXH5104 v.3	20151110	Objective data sheet	-	NXH5104 v.2
NXH5104 v.2	20141211	Objective data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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