

LTC4229

Single Ideal Diode and Hot Swap Controller

DESCRIPTION

Demonstration circuit 2060A is a single-rail circuit with an ideal diode and Hot Swap™ functionality provided by the LTC®4229, ideal diode and Hot Swap controller. The main components of this circuit are two series connected N-channel MOSFETs, a power sense resistor, a few passive components, nine jumpers for selection of alternative operation modes, and four LEDs for visual indication of the controller signals. One of the MOSFETs operates as an ideal diode and the other one as a Hot Swap power switch.

DC2060A facilitates evaluation of the LTC4229 in the different operation modes such as supply ramp-up, steady state, overcurrent faults, and power supply switchover. Power supply switchover mode can be realized when the LTC4229 controller operates in a prioritizer set up or when a second ideal diode circuit is added.

The DC2060A circuit is assembled to operate with a 12V supply and 10A maximum current load. The operating voltage can be easily readjusted for any voltage between 2.9V and 18V.

Pads on key nodes are intended to be used as test points.

The LTC4229 controller has two independent pins (SENSE⁺ and SENSE⁻) for the current sense signal. That simplifies using two configurations with the series connection of the ideal diode MOSFET and Hot Swap MOSFET. The ability of the LTC4229 to regulate the ideal diode voltage between the IN and DSNS pins allows the use of two distinctive paths

for the ideal diode voltage regulation. The combination of both features allows the implementation of four different configurations.

The typical configuration (as DC2060A is populated by default) has the ideal diode MOSFET ahead of the Hot Swap MOSFET with voltage regulation across the ideal diode MOSFET. There is an option to use two back-to-back MOSFETs instead of one ideal diode MOSFET to prevent powering the load before the gate voltage of the ideal diode MOSFET ramps up.

The LTC4229 provides voltage regulation to the ideal diode across the single ideal diode MOSFET or across three series connected components: ideal diode MOSFET, sense resistor, and Hot Swap MOSFET.

The bottom side of the board includes pads for an alternative configuration with the Hot Swap MOSFET located ahead of the ideal diode.

Provision is made for the selection of ideal diode regulation components: single ideal diode MOSFET or series connected ideal diode MOSFET, sense resistor, and Hot Swap MOSFET.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Hot Swap						
V _{NOM}	Demo Board Rail Voltage		9.8	12.0	15.2	V
I _{LIM}	Assembled Circuit Current Limit	FB = 1.23V, V _{OUT} ≥ 10.5V FB = 0, V _{OUT} < 2.5V	8.9 2.4	10.0 3.3	11.2 4.3	A A
S	Output Voltage Slew Rate with No Load		630	950	1300	V/s
Ideal Diode						
ΔV _{FWD(REG)}	Forward Regulation Voltage (V _{IN} - V _{DSNS})		35	50	65	mV

dc2060af

OPERATING PRINCIPLES

The LTC4229 functions as an ideal diode with inrush current limiting and overcurrent protection by controlling two external N-channel MOSFETs (Q2 and Q3) in a power path.

All component designators refer to the DC2060A schematic.

An internal charge pump provides energy for both MOSFET gate drivers through their individual current sources. Each MOSFET has an ON/OFF control: Q2 with DOFF pin signal (JP9) and Q3 with \overline{EN} pin signal (JP7).

The LTC4229 regulates the voltage between the IN pin and the diode sense pin (DSNS), so the DSNS connection defines the power path node in which the ideal diode regulates the voltage. There is an option (JP2) to connect the DSNS pin to Q2 drain or to the OUT node. Selection of this connection should be accompanied by a suitable signal at the DCFG pin. The proper signal is reached by placing the shunt of the jumper DC_CFG(JP8) in the proper position.

Table 1 demonstrates possible power path topologies for DC2060A and conditions necessary to achieve them.

The LTC4229 precision comparators are used to monitor the input voltage for both UV and OV conditions. Enabling the ideal diode functionality with the DOFF pin (low) forces the ideal diode gate drive amplifier to monitor the voltage between the IN and DSNS pins. Sensing the large forward voltage drop, the gate drive amplifier quickly pulls up DGATE turning the ideal diode MOSFET on.

High pull-up current of the ideal diode MOSFET guarantees minimum voltage droop during supply switchover and a short turn-on time.

Enabling the Hot Swap control with the \overline{EN} pin (low) initiates a debounce time interval, which can be fixed at 100ms, or 8.9ms to 17.5ms set by the capacitor C9 on the DTMR pin.

The foldback current limit and electronic circuit breaker of the Hot Swap MOSFET protect the input rail against short circuit faults and excessive load.

After the debounce time, a 10 μ A current source from the charge pump ramps up the HGATE pin. When the Hot Swap MOSFET Q3 turns on, the maximum current is limited to a level set by an external sense resistor RS1 (or RS2 in the optional application with Q4 MOSFET).

When both MOSFETs Q2 and Q3 (or Q4 and Q5 in the optional application) are turned on, the gate drive amplifier controls DGATE to servo the forward voltage drop across the MOSFET Q2 (or both MOSFETs and sense resistor) to 65mV. If the load current causes more than 65mV of voltage drop, the gate voltage rises to enhance the ideal diode MOSFET.

If the MOSFETs are conducting, and an input supply is shorted, a large reverse current starts flowing from the load to the input. The gate drive amplifier detects this failure condition as soon as it appears and turns the ideal diode MOSFET Q2 off, by pulling down the DGATE pin. The HGATE pin continues pulling high and keeps the MOSFET Q3 on.

OPERATING PRINCIPLES

Power Jacks with Connected Turrets

J1, J3 GND: Supply ground terminal and load terminal connection.

J2 SENSE⁺: Node for connection of external ideal diode circuit or external supply.

J4 IN: Supply input; do not exceed 18V.

J5 OUT: Load terminal connection.

Turrets Connected with Controller Pins and LEDs Indicating Its State

DFLT, RED LED D2: Controller $\overline{\text{DFLT}}$ pin.

DSTAT, GREEN LED D3: Controller $\overline{\text{DSTAT}}$ pin.

FAULT, RED LED D4: Controller $\overline{\text{FAULT}}$ pin.

PWRGD, GREEN LED D5: Controller $\overline{\text{PWRGD}}$ pin.

Turrets Connected with Controller Pins and Other

UV: Controller UV pin.

OV: Controller OV pin.

EN: Controller $\overline{\text{EN}}$ pin.

DOFF: Controller DOFF pin.

PRI: Node for a prioritizer implementation.

GND and PROBE GND: Ground pins for instrumental measurements.

Jumpers

JP1, FB_SEL: Use 12V position for 12V rail operation voltage; use 5V position for 5V rail operation voltage; use V_{CC} position for disabling the foldback characteristic.

JP2, DS_SEL: Use SENSE⁺ position for ideal diode MOSFET voltage regulation across the MOSFET power terminal; use OUT position for ideal diode MOSFET voltage regulation across the series connected ideal diode MOSFET, sense resistor, and Hot Swap MOSFET.

JP3, DSTAT_SEL: Use DOFF position to increase $\overline{\text{DSTAT}}$ pin hysteresis from 20mV to 100mV (with 2.2k for R14, R13 = 20k, R15 = 56.2k).

JP4, VIN_SEL: Use V_{IN} position to provide signal to the UV pin from input supply; use V_S^+ position to provide signal to the UV pin from SENSE⁺ node.

JP5, DEBOUNCE: Use 100ms position for 100ms debounce time; use ADJ position for debounce time defined by external capacitor C9.

JP6, RETRY: Use LATCH position to latch off after fault; use RETRY position to try turning on again after a fault with time off set by FTMR capacitor; if JP6 is not installed, auto-retry duty cycle after a fault is less than 0.1%.

JP7, EN_SEL: Use $\overline{\text{EN}}$ position to connect controller $\overline{\text{EN}}$ pin to GND; use DIS_EXT position to connect $\overline{\text{EN}}$ pin to EN turret for external signaling.

JP8, DC_CFG: Use 1-DIODE position to regulate a diode voltage across the ideal diode MOSFET; use 3-COMP position to regulate a diode voltage across three components (ideal diode MOSFET, sense resistor and Hot Swap MOSFET).

JP9, DIODE_OFF: Use ON position to activate ideal diode functionality; use OFF_EXT position to connect DOFF pin to DOFF turret for external.

OPERATING PRINCIPLES

Table 1. Configuration Table

SIDE	NUMBER	CONFIGURATION	JUMPER POSITION
Top Board Side	1		JP8 = 1-DIODE JP2 = SENSE ⁺
	2		JP8 = 3-COMP JP2 = OUT
Bottom Board Side	3		JP8 = 3-COMP JP2 = OUT
	4		JP8 = 1-DIODE JP2 = OUT

QUICK START PROCEDURE

Demonstration circuit DC2060A can be easily set up to evaluate the performance of the LTC4229. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

Hot Swap Functionality Test

Initially the jumpers should be installed in the following positions:

- JP1 (FB_SEL) 12V
- JP2 (DS_SEL) SENSE⁺
- JP3 (DSTAT_SEL) NC
- JP4 (VIN_SEL) VS⁺

- JP5 (DEBOUNCE) ADJ
- JP6 (RETRY) LATCH
- JP7 (EN_SEL) DIS_EXT
- JP8 (DC_CFG) 1-DIODE
- JP9 (DIODE_OFF) ON

The test is performed by measuring the parameters in the three different operation modes:

- Power-up with no load connected
- Current limit operation after successful power-up mode
- Power-up with a shorted output

QUICK START PROCEDURE

1. Connect a 12V power supply to the board input turrets IN and GND. Do not load the output. Use the current probe to monitor current into the wire between the 12V supply and board turret. Place the voltage probes on the OUT turret.

Provide the \overline{EN} signal by changing the shunt position of JP7 and observe the transient. The output voltage rise time should be in the range of 9.2ms to 19ms. The PWRGD green LED (D5) should light up. Turn off the rail with JP7.

2. Initially adjust the electronic load to 2.0Ω to 2.5Ω (in the constant resistive mode) and connect it to the board OUT and GND turrets. Turn on the rail and slowly increase the load current up to the circuit breaker threshold level. The current limit range should be from 8.9A to 11.2A. Reset the controller by turning off the rail voltage.

3. Short the output to ground with a wire. Place the current probe on this wire. Turn on the rail and record the current shape. The maximum current should be in the 2.4A to 4.3A range while the fault timer capacitor is ramping from 0.9ms to 1.8ms. After a fault, the Hot Swap MOSFET will be off approximately 50 times longer.

Ideal Diode Functionality Test

An additional 12V regulated power supply and a Schottky diode are needed for this test.

Connect the positive terminal of this supply through the Schottky diode to the DC2060A SENSE+ jack and the negative terminal to GND. Place a voltmeter between the IN and SENSE+ turrets to measure the difference between the two input voltages. Activate both rails and keep a load of around 1A to 3A. Adjust the input voltage levels and verify that when the difference between the input voltages exceeds 65mV only one rail powers the load.

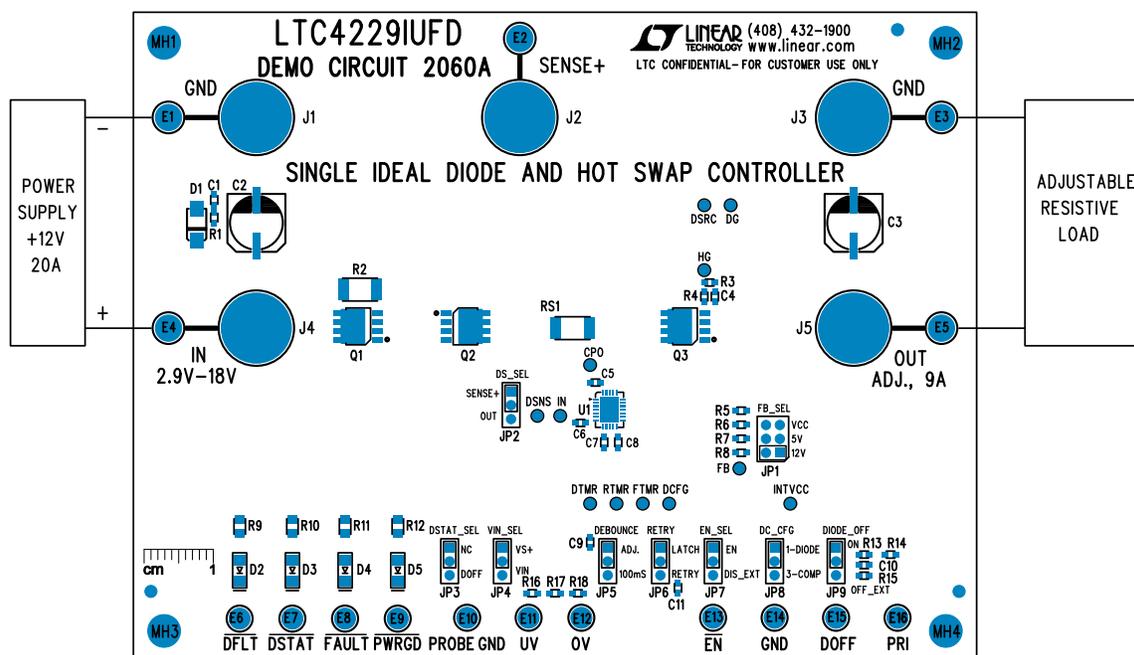


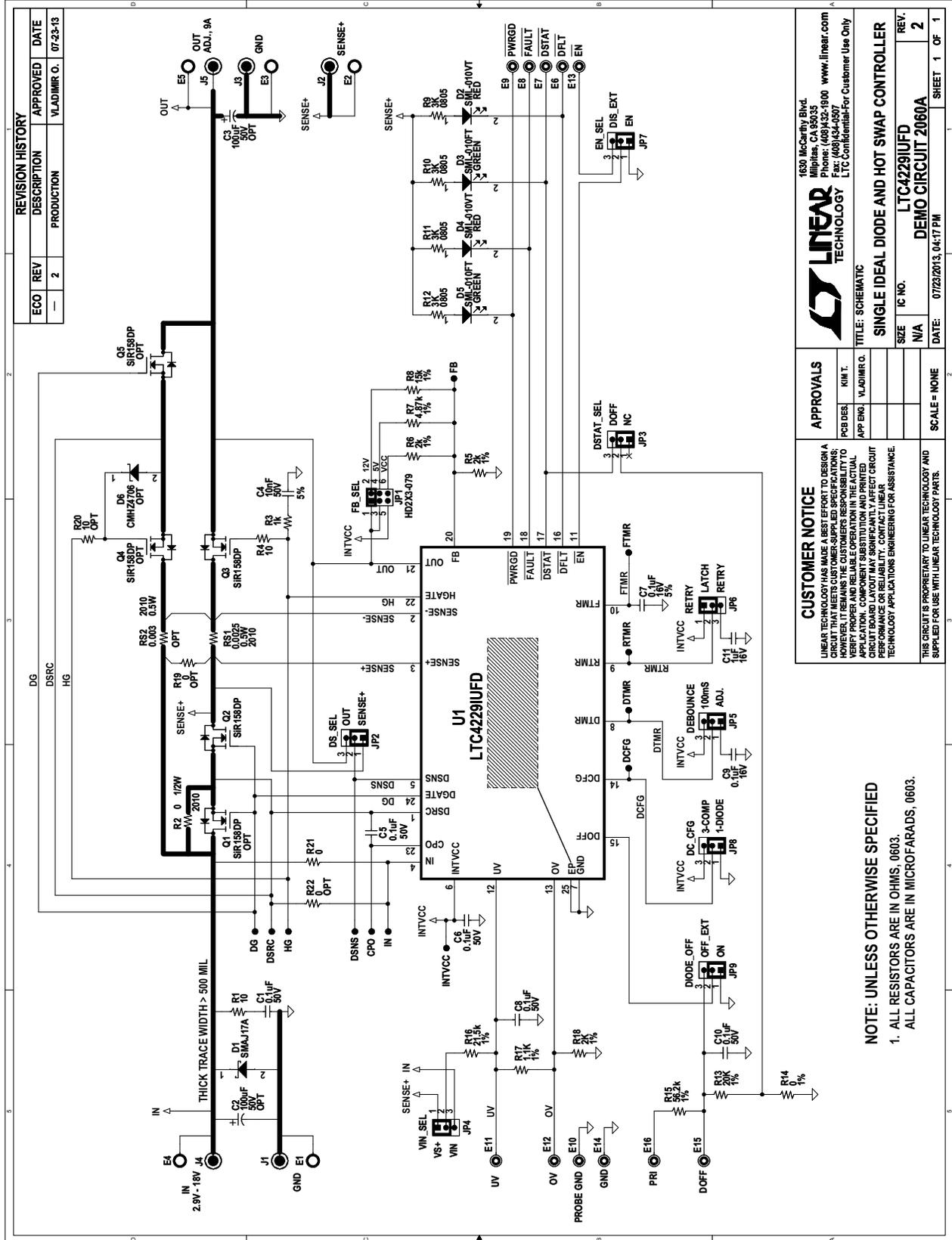
Figure 1. DC2060A Measurement Setup

DEMO MANUAL DC2060A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	5	C1, C5, C6, C8, C10	CAP., X7R, 0.1 μ F, 50V, 0603	AVX, 06035C104KAT2A
2	0	C2, C3	CAP., ALUMINUM, 100 μ F 50V, OPT	SUN ELECT., 50CE100BS
3	1	C4	CAP., X7R, 10nF, 50V, 0603	AVX, 06035C103KAT2A
4	2	C7, C9	CAP., X7R, 0.1 μ F, 16V, 5%, 0603	AVX, 0603YC104JAT2A
5	1	C11	CAP., X7R, 1 μ F, 16V, 10%, 0603	AVX, 0603YC105KAT2A
6	1	D1	DIODE, VOLTAGE SUPP. 19V 5%, SMA-DIODE	VISHAY, SMAJ17A-E3
7	2	D2, D4	LED, SMT RED	ROHM, SML-010VTT86L
8	2	D3, D5	LED, SMT GREEN	ROHM, SML-010FTT86L
9	0	D6	DIODE, CMHZ4706, SOD123	OPT
10	5	E1, E2, E3, E4, E5	TP, .094"	MILL-MAX, 2501-2-00-80-00-00-07-0
11	11	E6-E16	TP, .064"	MILL-MAX, 2308-2-00-80-00-00-07-0
12	1	JP1	JMP, HD2X3, .079CC	SULLINS, NRPN032PAEN-RC
13	8	JP2-JP9	JMP, HD1X3, .079CC	SULLINS, NRPN031PAEN-RC
14	5	J1, J2, J3, J4, J5	JACK, BANANA	KEYSTONE, 575-4
15	0	Q1, Q4, Q5	MOSFET, N-CH, 30V, SiR158DP, SO8-POWERPAK	OPT
16	2	Q2, Q3	MOSFET, N-CH, 30V, SO8-POWERPAK	VISHAY, SiR158DP-T1-GE3
17	1	RS1	RES., CHIP, 0.0025 Ω , 3/4W, 1%, 2010	VISHAY, WSL20102L5000FEA
18	0	RS2	RES., CHIP, 0.003 Ω , 3/4W, 1%, 2010, OPT	OPT
19	2	R1, R4	RES., CHIP, 10 Ω , 1%, 0603	VISHAY, CRCW060310R0FKEA
20	1	R2	RES., CHIP, 0 Ω , 3/4W, 2010	VISHAY, CRCW20100000FKEF
21	1	R3	RES., CHIP, 1k, 5%, 0603	VISHAY, CRCW06031K00JKEA
22	3	R5, R6, R18	RES., CHIP, 2k, 1%, 0603	VISHAY, CRCW06032K00FKEA
23	1	R7	RES., CHIP, 4.87k, 1%, 0603	VISHAY, CRCW06034K87FKEA
24	1	R8	RES., CHIP, 15k, 1%, 0603	VISHAY, CRCW060315K0FKEA
25	4	R9, R10, R11, R12	RES., CHIP, 3k, 1%, 0805	VISHAY, CRCW08053K00FKEA
26	1	R13	RES., CHIP, 20k, 1%, 0603	VISHAY, CRCW060320K0FKEA
27	2	R14, R21	RES., CHIP, 0 Ω , 1/16W, 0603	VISHAY, CRCW06030000Z0EDA
28	1	R15	RES., CHIP, 56.2k, 1%, 0603	VISHAY, CRCW060356K2FKEA
29	1	R16	RES., CHIP, 21.5k, 1%, 0603	VISHAY, CRCW060321K5FKEA
30	1	R17	RES., CHIP, 1.1k, 1%, 0603	VISHAY, CRCW06031K10FKEA
31	0	R19, R22	RES., CHIP, 0 Ω , 0603	OPT
32	0	R20	RES., CHIP, 10 Ω , 0603	OPT
33	1	U1	IC., Hot Swap, QFN24UFD-4X5	LINEAR TECH., LTC4229IUFD
34	9	SHUNTS (SEE ASSY DWG)	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
35	4	MH1-MH4	STANDOFF, NYLON, 0.50, 1/2"	KEYSTONE, 8833 (SNAP ON)
36	2		STENCILS FOR BOTH SIDES	STENCIL DC2060A-2

SCHEMATIC DIAGRAM



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APPROVALS

PCB DES.	KIM T.
APP ENG.	VLADIMIR O.

TITLE: SCHEMATIC

SIZE IC NO. N/A

SCALE = NONE

DATE: 07/23/2013, 04:17 PM

SHEET 1 OF 1

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NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 0603.
 ALL CAPACITORS ARE IN MICROFARADS, 0603.

DEMO MANUAL DC2060A

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