

# 74LVC16373A; 74LVCH16373A

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Rev. 9 — 15 February 2019

Product data sheet

## 1. General description

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The 74LVC16373A and 74LVCH16373A are 16-bit D-type transparent latches featuring separate D-type inputs with bus hold (74LVCH16373A only) for each latch and 3-state outputs for bus-oriented applications. One Latch Enable (LE) input and one Output Enable ( $\overline{OE}$ ) are provided for each octal. Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The device consists of two sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition, the latches are transparent, that is, the latch outputs change each time its corresponding D-input changes. The latches store the information that was present at the D-inputs one set-up time ( $t_{su}$ ) preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches. Bus hold on the data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features and benefits

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- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16373A only)
- High-impedance when  $V_{CC} = 0$  V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM ANSI/ESDA/Jedec JS-002 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

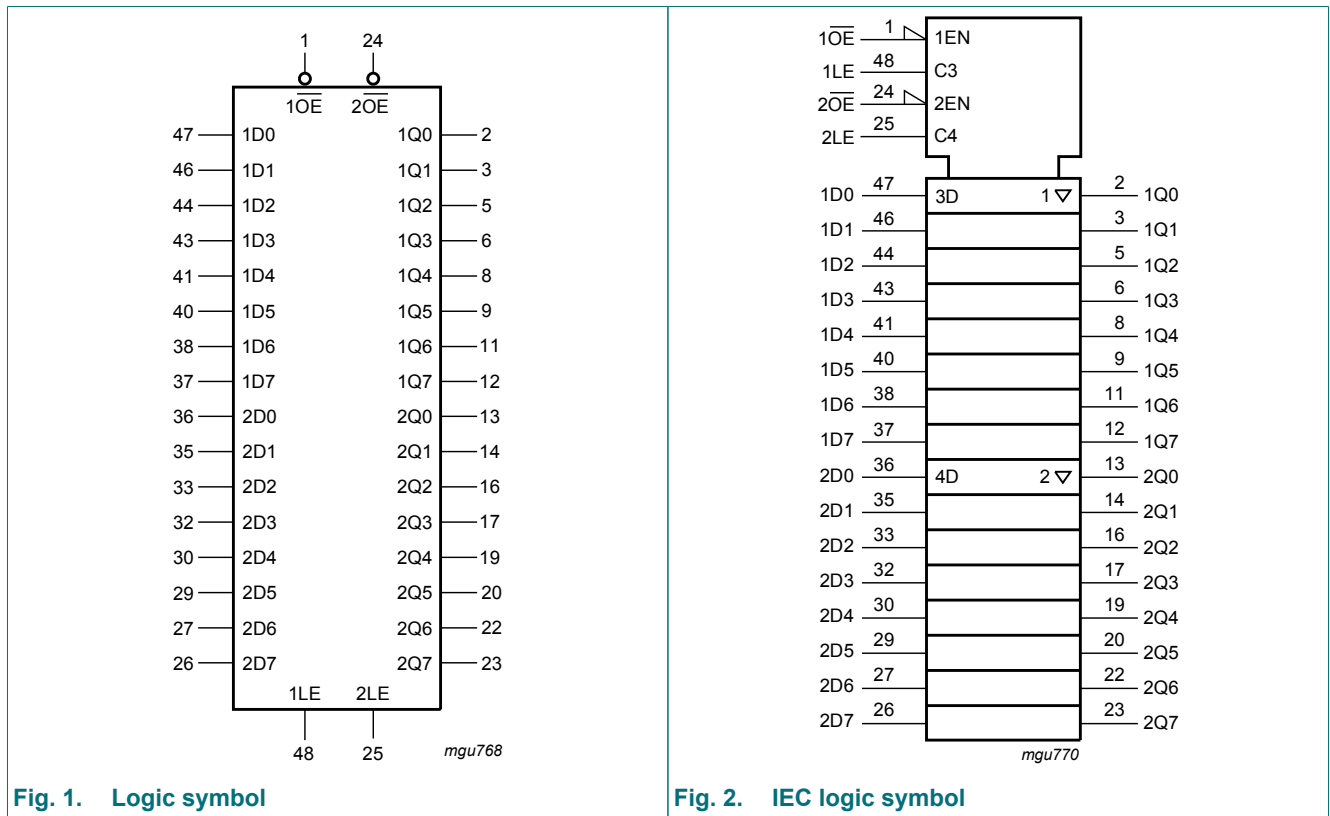
### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC16373ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16373ADGG				
74LVC16373ADL	-40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVC16373ADGV	-40 °C to +125 °C	TSSOP48 [1]	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74LVCH16373ADGV				

[1] Also known as TVSOP48.

### 4. Functional diagram



16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

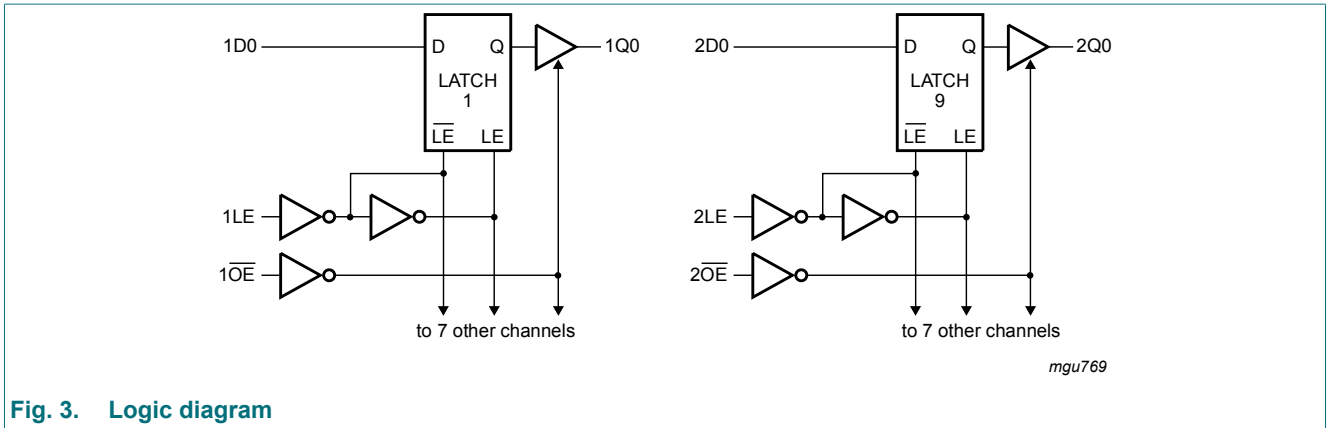


Fig. 3. Logic diagram

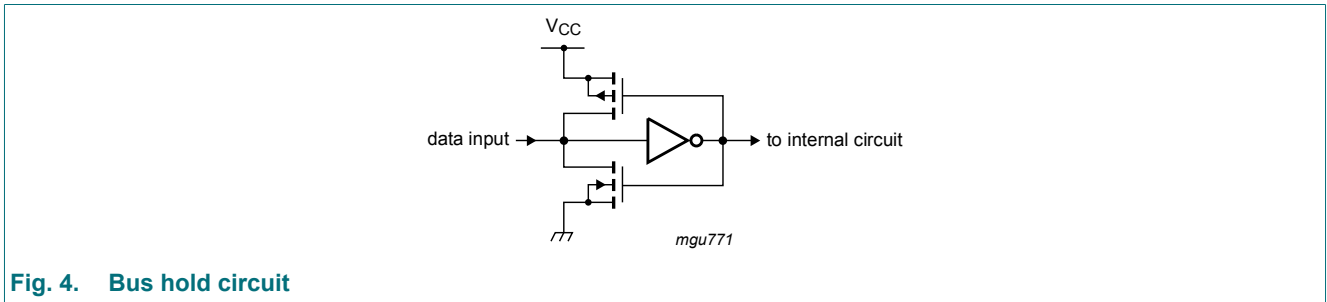
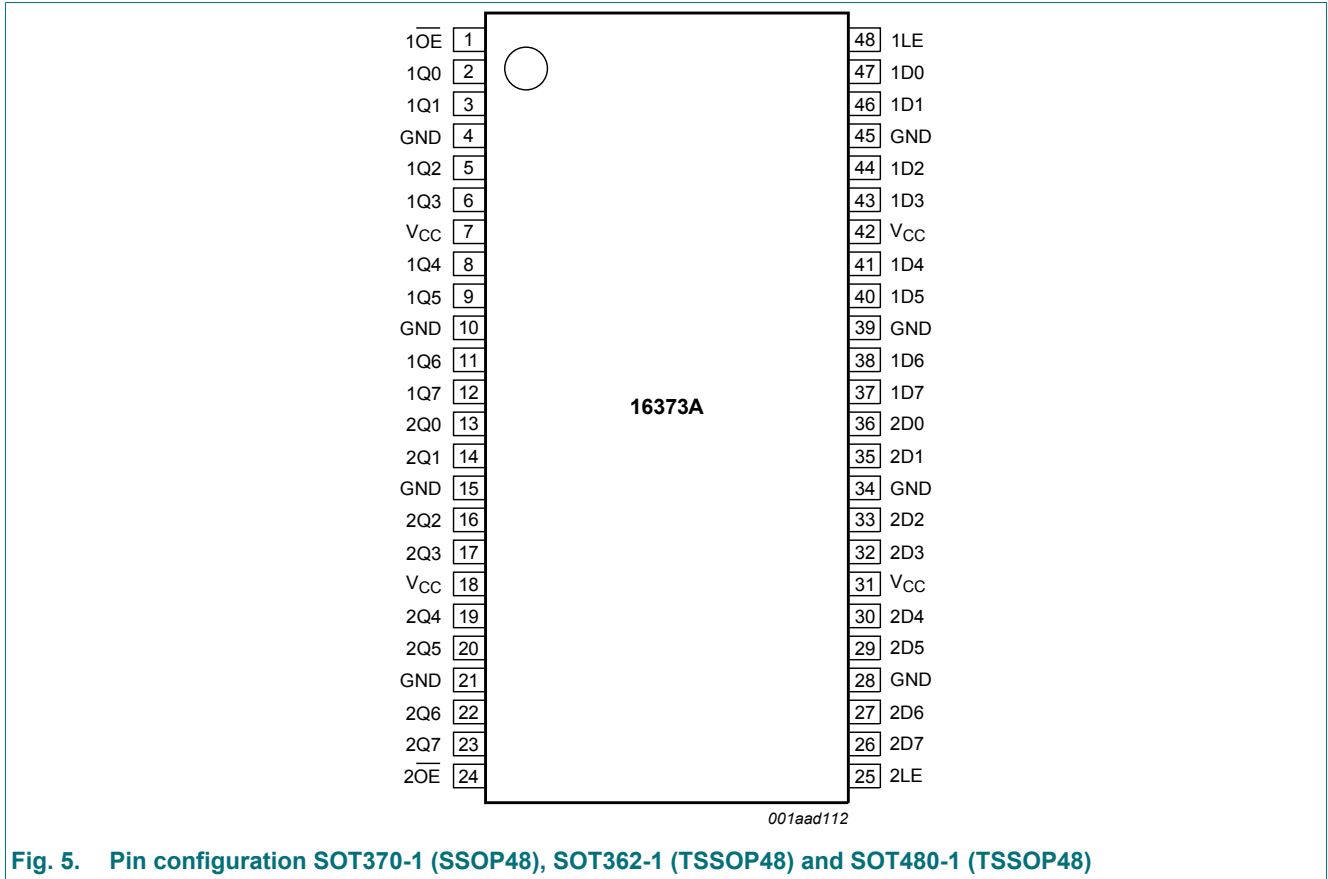


Fig. 4. Bus hold circuit

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 24	output enable input (active LOW)
1LE, 2LE	48, 25	latch enable input (active HIGH)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data output
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data output
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	data input
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	data input

## 6. Functional description

**Table 3. Function table**

Per section of eight bits.

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH to LOW LE transition

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH to LOW LE transition

Z = high-impedance OFF-state

Operating modes	Input			Internal latch	Output nQ0 to nQ7
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC}$	supply voltage		-0.5	+6.5	V	
$I_{IK}$	input clamping current	$V_I < 0$	-50	-	mA	
$V_I$	input voltage	[1]	-0.5	+6.5	V	
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA	
$V_O$	output voltage	output HIGH or LOW state	[2]	-0.5	$V_{CC} + 0.5$	V
		output 3-state	[2]	-0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA	
$I_{CC}$	supply current		-	100	mA	
$I_{GND}$	ground current		-100	-	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C, the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
	I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V	

## 16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$I_I$	input leakage current	$V_{CC} = 3.6\text{ V}$ ; $V_I = 5.5\text{ V}$ or GND [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 3.6\text{ V}$ ; $V_O = 5.5\text{ V}$ or GND [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 5.5\text{ V}$	-	$\pm 0.1$	$\pm 10$	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.1	20	-	80	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ ; $V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$	-	5	500	-	5000	$\mu\text{A}$
$C_I$	input capacitance	$V_{CC} = 0\text{ V}$ to $3.6\text{ V}$ ; $V_I = \text{GND}$ to $V_{CC}$	-	5.0	-	-	-	pF
$I_{BHL}$	bus hold LOW current	$V_{CC} = 1.65$ ; $V_I = 0.58\text{ V}$ [3] [4]	10	-	-	10	-	$\mu\text{A}$
		$V_{CC} = 2.3$ ; $V_I = 0.7\text{ V}$	30	-	-	25	-	$\mu\text{A}$
		$V_{CC} = 3.0$ ; $V_I = 0.8\text{ V}$	75	-	-	60	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 1.65$ ; $V_I = 1.07\text{ V}$ [3] [4]	-10	-	-	-10	-	$\mu\text{A}$
		$V_{CC} = 2.3$ ; $V_I = 1.7\text{ V}$	-30	-	-	-25	-	$\mu\text{A}$
		$V_{CC} = 3.0$ ; $V_I = 2.0\text{ V}$	-75	-	-	-60	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 1.95\text{ V}$ [3] [5]	200	-	-	200	-	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V}$	300	-	-	300	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	500	-	-	500	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 1.95\text{ V}$ [3] [5]	-200	-	-	-200	-	$\mu\text{A}$
		$V_{CC} = 2.7\text{ V}$	-300	-	-	-300	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	-500	-	-	-500	-	$\mu\text{A}$

[1] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  (unless stated otherwise) and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

[2] The bus hold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input pin.

[3] Valid for data inputs (74LVCH16373A) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified  $V_I$  level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	Dn to Qn; see Fig. 6 [2]						
		$V_{CC} = 1.2\text{ V}$	-	12	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	5.4	11.4	1.5	13.2	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.9	5.7	1.0	6.6	ns
		$V_{CC} = 2.7\text{ V}$	1.5	2.9	4.9	1.5	6.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.4	4.4	1.0	5.5	ns
		LE to Qn; see Fig. 7						
		$V_{CC} = 1.2\text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.0	6.4	12.4	2.0	14.4	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.5	3.4	6.1	1.5	7.1	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.0	5.3	1.5	7.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	2.9	4.8	1.5	6.0	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see Fig. 8 [2]						
		$V_{CC} = 1.2\text{ V}$	-	18	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	5.5	12.4	1.5	14.3	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.1	6.6	1.0	7.6	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.3	5.7	1.5	7.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.5	4.9	1.0	6.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see Fig. 8 [2]						
		$V_{CC} = 1.2\text{ V}$	-	11	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.8	4.5	9.1	2.8	10.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.5	5.1	1.0	6.0	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.3	6.3	1.5	8.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.1	5.4	1.5	7.0	ns
$t_W$	pulse width	LE HIGH; see Fig. 7						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7\text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.0	2.0	-	3.0	-	ns
$t_{su}$	set-up time	Dn to LE; see Fig. 9						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.5	-	-	2.5	-	ns
		$V_{CC} = 2.7\text{ V}$	2.0	-	-	2.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	1.0	-	2.0	-	ns
$t_h$	hold time	Dn to LE; see Fig. 9						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.5	-	-	2.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.0	-	-	2.0	-	ns
		$V_{CC} = 2.7\text{ V}$	0.9	-	-	0.9	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	+0.9	-1.0	-	+0.9	-	ns

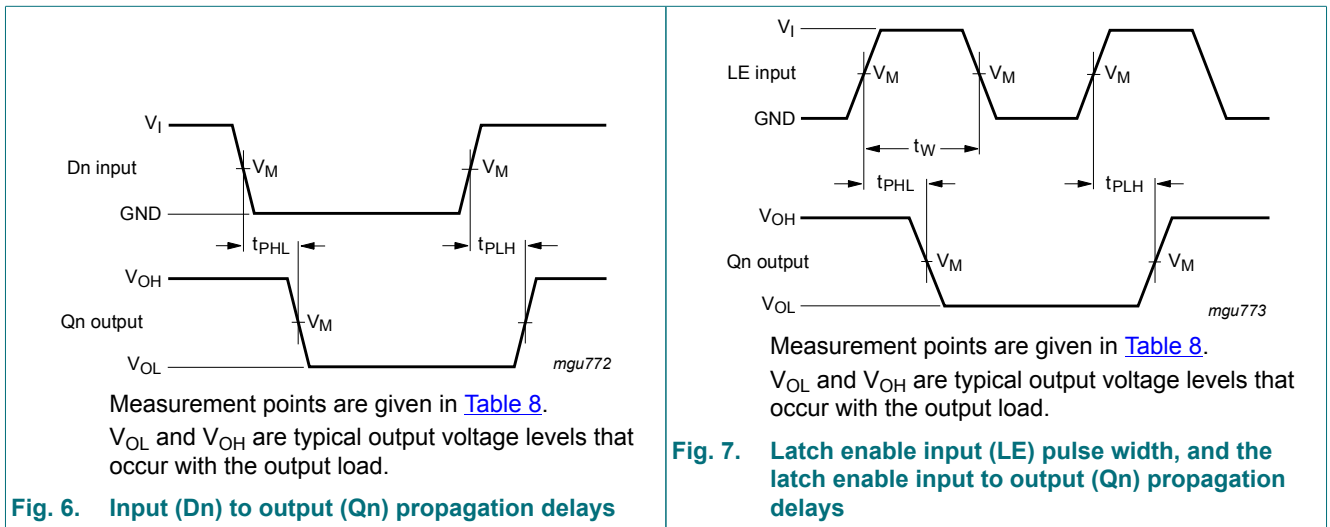


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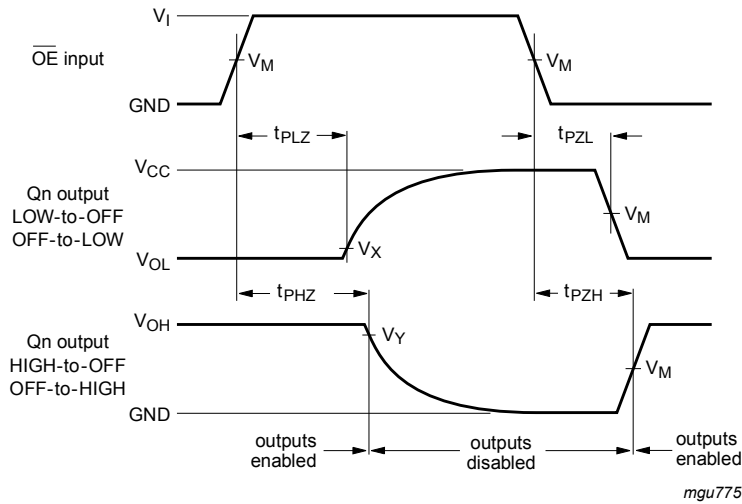
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	-	1.0	-	1.5	ns
$C_{PD}$	power dissipation capacitance	per input; $V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	10.8	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	13.0	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	15.0	-	-	-	pF

- [1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V}$  and  $3.3\text{ V}$  respectively.
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in Volts  
 $N$  = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

10.1. Waveforms and test circuit



16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 8. 3-state enable and disable times**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 9. Data set-up and hold times for the Dn input to the LE input**

**Table 8. Measurement points**

Supply voltage	Input		Output		
	$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

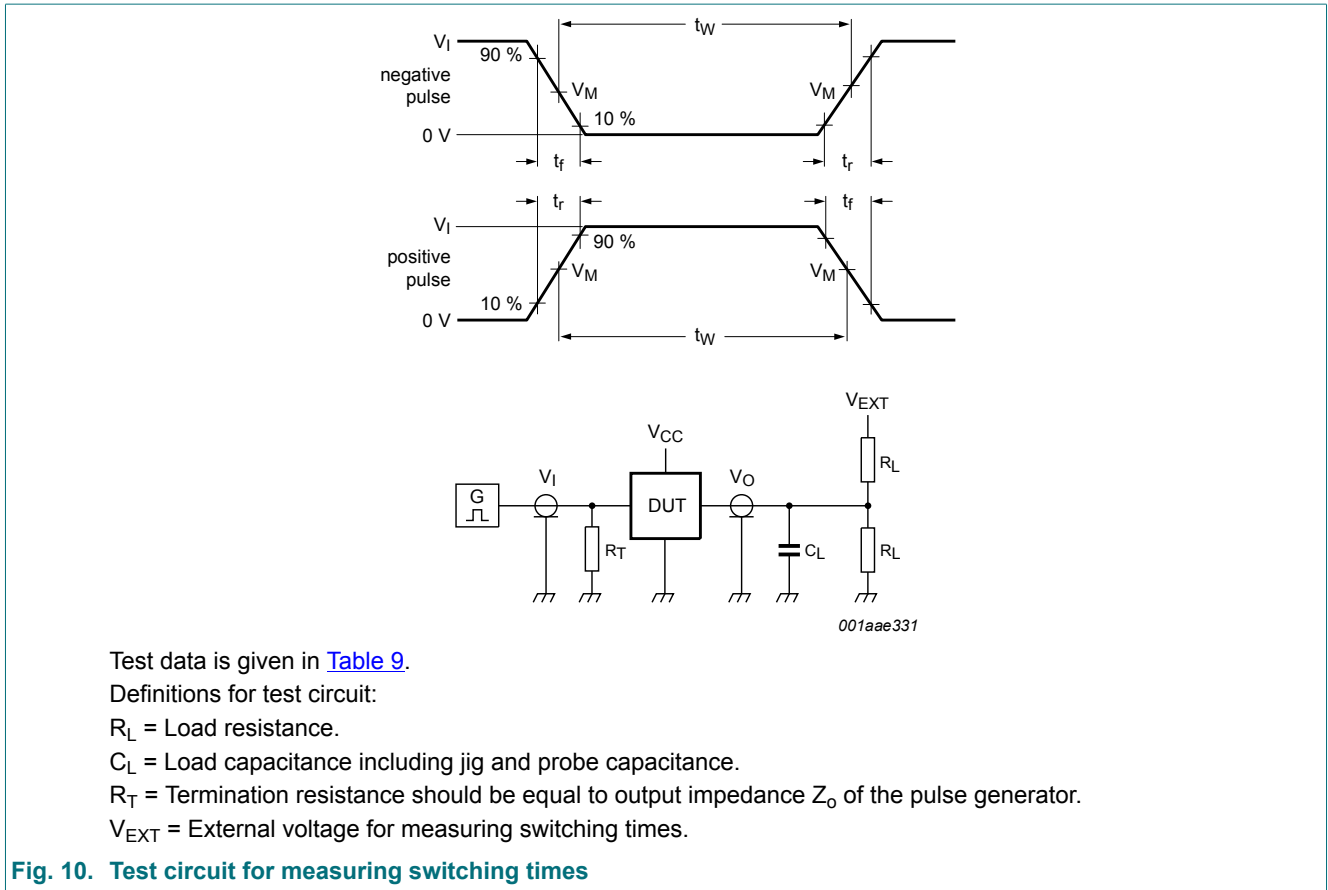


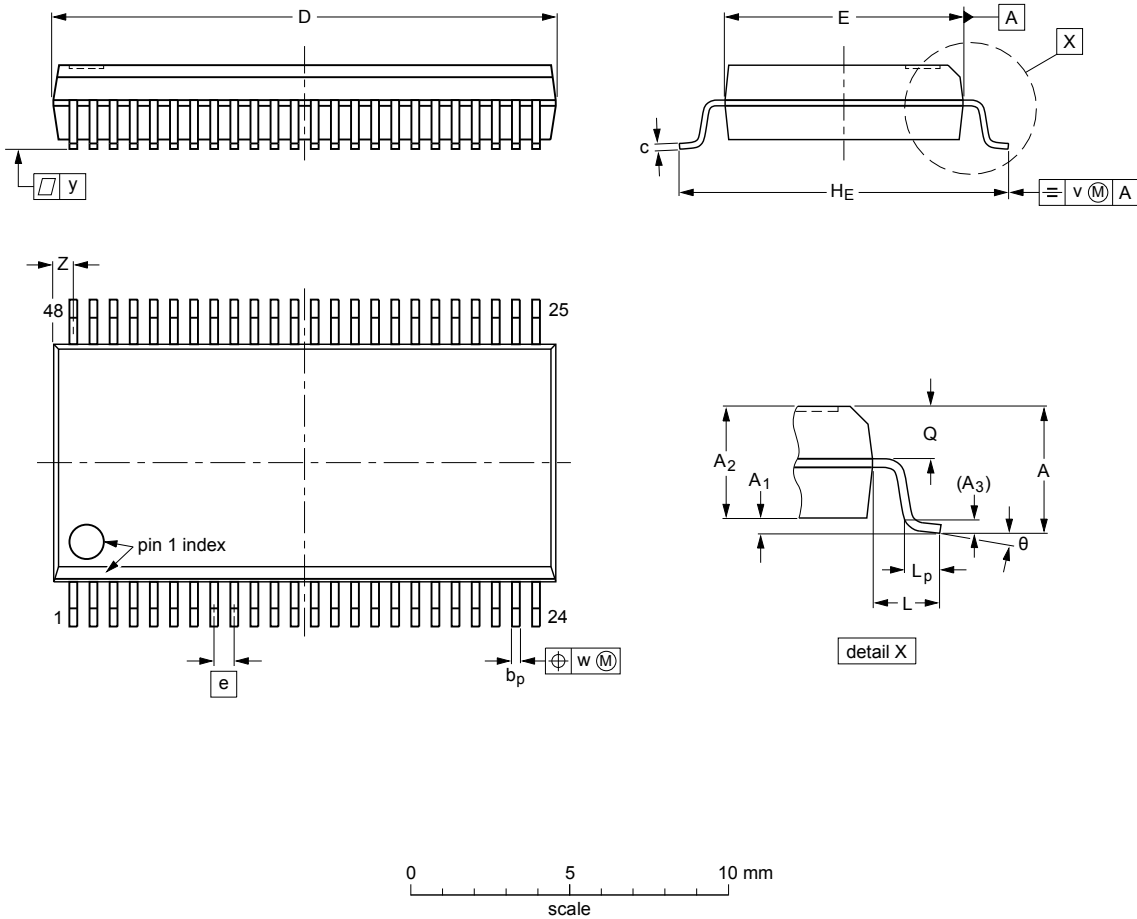
Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

11. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

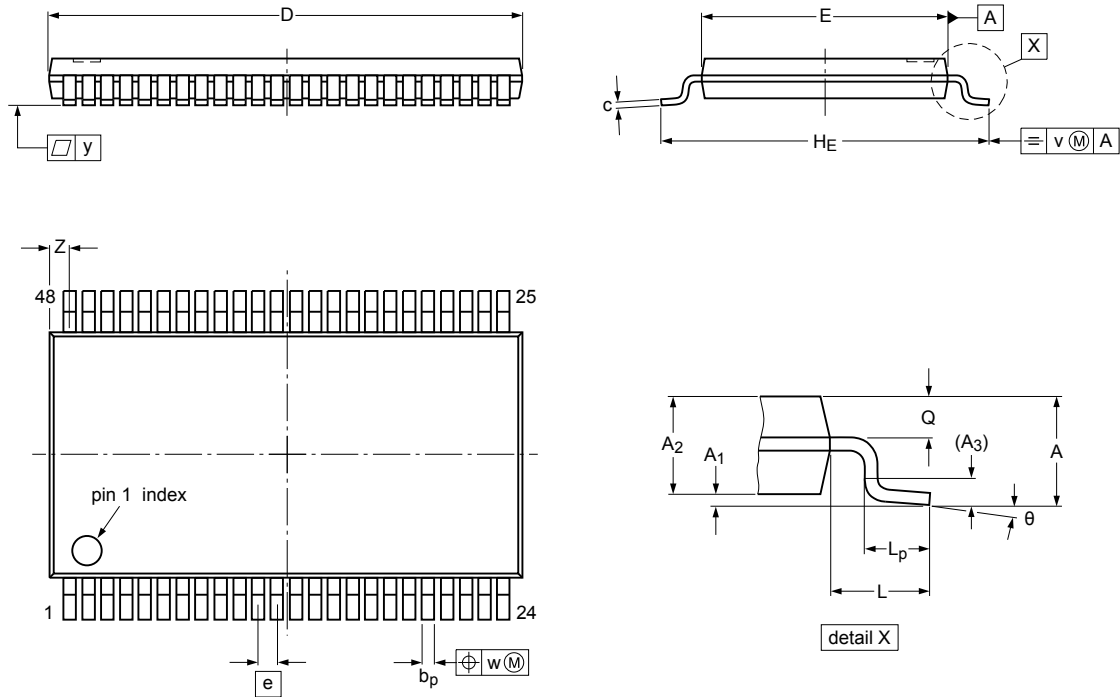
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

Fig. 11. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ	
max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50		0.25	0.08	0.1	0.8	8°
nom	1.2			0.25					0.5		1								
min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

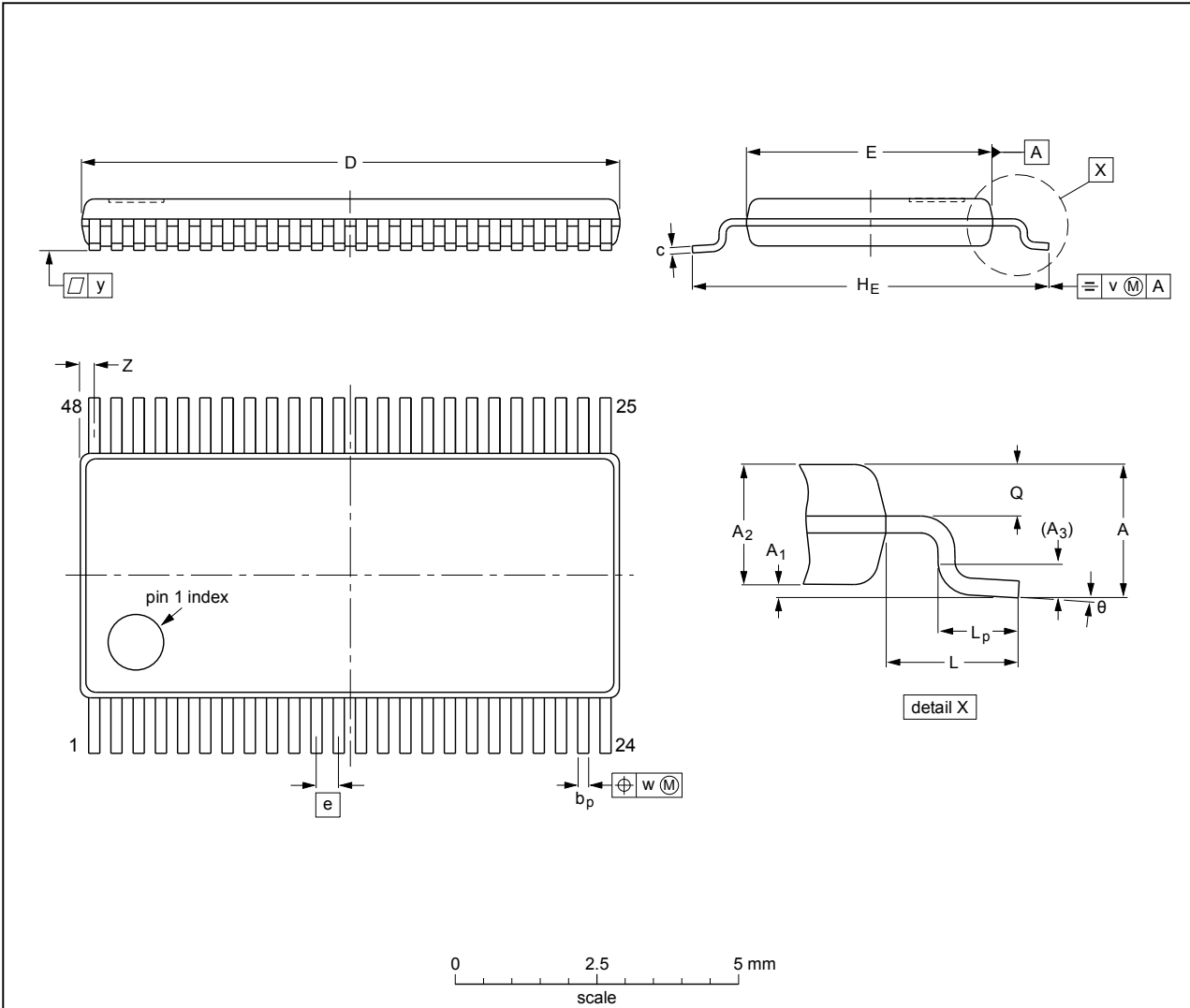
sot362-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-03-02-19- 13-08-05

Fig. 12. Package outline SOT362-1 (TSSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm

SOT480-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.8 9.6	4.5 4.3	0.4	6.6 6.2	1	0.7 0.5	0.4 0.3	0.2	0.07	0.08	0.4 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT480-1		MO-153				99-12-27 03-02-18

Fig. 13. Package outline SOT480-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16373A v.9	20190215	Product data sheet	-	74LVC_LVCH16373A v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74LVCH16373ADL (SOT370-1) removed.</li> <li>Type numbers 74LVC16373ADGV and 74LVCH16373ADGV (SOT480-1) added.</li> </ul>			
74LVC_LVCH16373A v.8	20140106	Product data sheet	-	74LVC_LVCH16373A v.7
Modifications:	<ul style="list-style-type: none"> <li>General description corrected (errata).</li> </ul>			
74LVC_LVCH16373A v.7	20130118	Product data sheet	-	74LVC_LVCH16373A v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH16373A v.6	20031208	Product specification	-	74LVC_LVCH16373A v.5
74LVC_LVCH16373A v.5	20021002	Product specification	-	74LVC_H16373A v.4
74LVC_H16373A v.4	19980317	Product specification	-	74LVC16373A_74LVCH16373A v.3
74LVC16373A_74LVCH16373A v.3	19980317	Product specification	-	74LVC16373A v.2
74LVC16373A v.2	19970822	Product specification	-	74LVC16373A v.1
74LVC16373A v.1	19960108	-	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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