

DEM-OPA-SO-2D Demonstration Fixture

1 Description

The DEM-OPA-SO-2D demonstration fixture is a generic, unpopulated printed circuit board (PCB) for dual high-speed operational amplifiers with disable in SO-14 packages. [Figure 1](#) shows the package pinout for this PCB. For more information on these op amps, as well as good PCB layout techniques, see the individual amplifier data sheets.

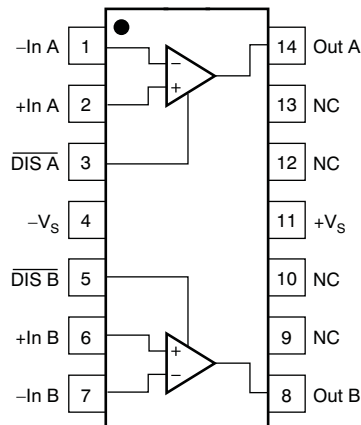


Figure 1. SO Package Pinout, Top View

2 Circuit

The circuit schematic in [Figure 2](#) shows the connections for all possible components. Each configuration uses only some of the components.

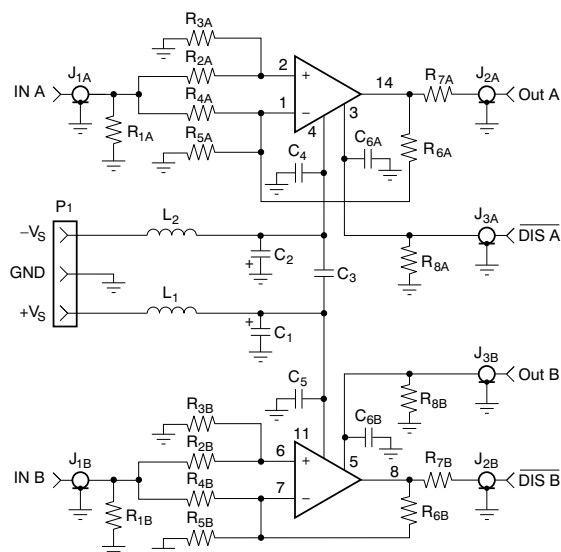


Figure 2. Schematic for DEM-OPA-SO-2D

3 Components

Components that have RF performance similar to the ones listed in [Table 1](#) may be substituted.

Table 1. Component Descriptions

PART	DESCRIPTION
C ₁ , C ₂	Tantalum Chip Capacitor, SMD EIA Size 3528, 20V
C ₃ – C _{6B}	Multilayer Ceramic Chip Capacitor, SMD 1206, 50V
J _{1A} – J _{3B}	SMA or SMB Board Jack (Amphenol 901-144-8)
L ₁ , L ₂	EMI-Suppression Ferrite Chip, SMD 1206 (Steward LI 1206 B 900 R)
P ₁	Terminal Block, 3.5mm Centers (On-Shore Technology ED555/3DS)
R _{1A} – R _{8B}	Metal Film Chip Resistor, SMD 1206, 1/8W

R₁ and R₇ set the I/O impedance; R₂ through R₆ set the gain; R₈ and C₆ set up the disable pin; and C₁ through C₅ are supply bypass capacitors. C₃ is optional; it adds a bypass between the supplies that improves distortion performance for some models. L₁ and L₂ are ferrite chips that can reduce interactions with the power supply at high frequencies. If not desired, they can be replaced with 0Ω resistors.

For single-supply operation, do not connect L₂; otherwise, the -V_S input to P₁ would be at ground potential.

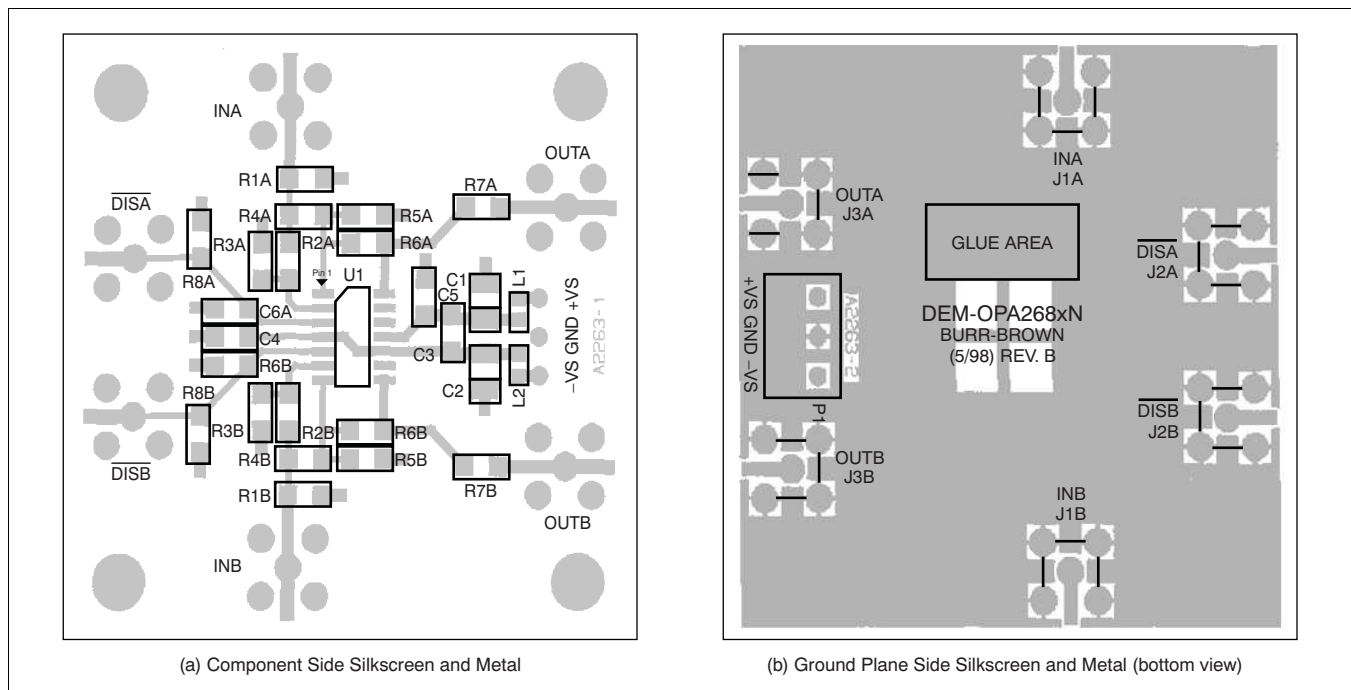
Disable Pin—Pins 3 and 5 disable op amps A and B when low. [Table 2](#) shows different ways to set up the voltage on these pins.

Table 2. Disable Pin

CONFIGURATION	R_g	C_6
External Service	49.9 Ω	Open
On	Open	0.1 μ F
Off	0 Ω	Open

4 Board Layout

This demonstration fixture is a two-layer PCB. (See [Figure 3.](#)) It uses both a ground plane and power traces on the inner layers. The ground plane has been opened up around op amp pins that are sensitive to capacitive loading. Power-supply traces are laid out to keep current loop areas to a minimum. The SMA (or SMB) connectors may be mounted either vertically or horizontally onto the board edge. The location and type of capacitors used for power-supply bypassing are crucial for high-frequency amplifiers. The tantalum capacitors, C_1 and C_2 , do not need to be close to pins 11 and 4 on the PCB and may be shared with other amplifiers. See the individual op amp data sheet for more information on proper board layout techniques and component selection.



- (1) The board name shown in the silkscreen is DEM-OPA268xN with the Burr-Brown Revision B design finalized in May 1998.

Figure 3. DEM-OPA-SO-2D Demonstration Board Layout

5 Measurement Tips

This demonstration fixture, with the component values shown, is designed to operate in a 50Ω environment; most data sheet plots are obtained under these conditions. It is easy to change the component values for different input and output impedance levels. However, do not use high-impedance probes; they represent a heavy capacitive load to the op amp, and will alter the amplifier response. Instead, use low-impedance ($\leq 500\Omega$) probes with adequate bandwidth. The probe input capacitance and resistance set an upper limit on the measurement bandwidth. If a high-impedance probe must be used, place a 100Ω resistor on the probe tip to isolate its capacitance from the circuit.

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