

1.5V Drive Nch+Pch MOSFET

US6M11

●Structure

Silicon N-channel MOSFET /
Silicon P-channel MOSFET

●Features

- 1) Nch MOSFET and Pch MOSFET are put in TUMT6 package.
- 2) Low on-resistance.
- 3) Low voltage drive (1.5V drive).
- 4) Built-in G-S Protection Diode.

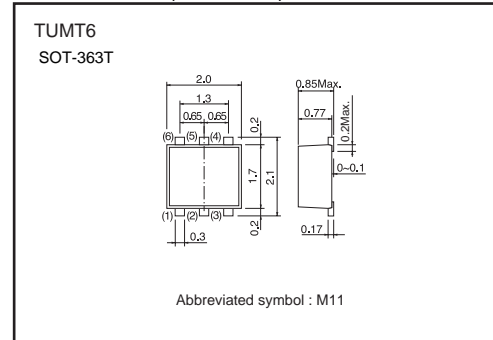
●Applications

Switching

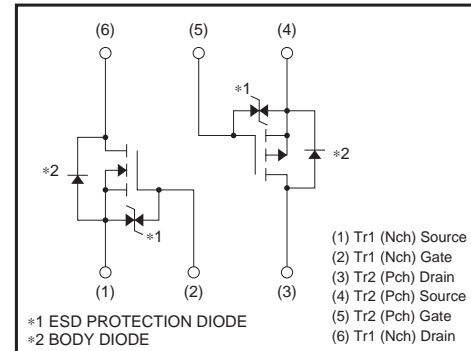
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6M11		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : Nchannel	Tr2 : Pchannel	
Drain-source voltage	V_{DSS}	20	-12	V
Gate-source voltage	V_{GSS}	± 10	± 10	V
Drain current	Continuous	I_D	± 1.5	A
	Pulsed	I_{DP}^{*1}	± 6	A
Source current (Body diode)	Continuous	I_S	0.5	A
	Pulsed	I_{SP}^{*1}	6	A
Power dissipation	P_D^{*2}	1.0		W / TOTAL
		0.7		W / ELEMENT
Channel temperature	T_{ch}	150		°C
Range of storage temperature	T_{stg}	-55 to +150		°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}^{*}$	125	°C/W / TOTAL
		179	°C/W / ELEMENT

* Mounted on a ceramic board

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●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} = ±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	20	–	–	V	I _D = 1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	1	μA	V _{DS} = 20V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	0.3	–	1.0	V	V _{DS} = 10V, I _D = 1mA
Static drain-source on-state resistance	R _{DS(on)*}	–	130	180	mΩ	I _D = 1.5A, V _{GS} = 4.5V
		–	170	240	mΩ	I _D = 1.5A, V _{GS} = 2.5V
		–	220	310	mΩ	I _D = 0.8A, V _{GS} = 1.8V
		–	300	600	mΩ	I _D = 0.3A, V _{GS} = 1.5V
Forward transfer admittance	Y _{fs} *	1.6	–	–	S	V _{DS} = 10V, I _D = 1.5A
Input capacitance	C _{iss}	–	110	–	pF	V _{DS} = 10V
Output capacitance	C _{oss}	–	18	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	15	–	pF	f=1MHz
Turn-on delay time	t _{d(on)*}	–	5	–	ns	V _{DD} ≐ 10V
Rise time	t _r *	–	5	–	ns	I _D = 1A
Turn-off delay time	t _{d(off)*}	–	20	–	ns	V _{GS} = 4.5V
Fall time	t _f *	–	3	–	ns	R _L ≐ 10Ω
Total gate charge	Q _g *	–	1.8	–	nC	V _{DD} ≐ 10V, V _{GS} = 4.5V
Gate-source charge	Q _{gs} *	–	0.3	–	nC	I _D = 1.5A
Gate-drain charge	Q _{gd} *	–	0.3	–	nC	R _L ≐ 6.7Ω, R _G = 10Ω

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	1.2	V	I _S = 1.5A, V _{GS} =0V

*Pulsed

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●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} = ±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	–12	–	–	V	I _D = –1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} = –12V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	–0.3	–	–1.0	V	V _{DS} = –6V, I _D = –1mA
Static drain-source on-state resistance	R _{DS(on)*}	–	190	260	mΩ	I _D = –1.3A, V _{GS} = –4.5V
		–	280	390	mΩ	I _D = –0.6A, V _{GS} = –2.5V
		–	400	600	mΩ	I _D = –0.6A, V _{GS} = –1.8V
		–	530	1060	mΩ	I _D = –0.2A, V _{GS} = –1.5V
Forward transfer admittance	Y _{fs} *	1.4	–	–	S	V _{DS} = –6V, I _D = –1.3A
Input capacitance	C _{iss}	–	290	–	pF	V _{DS} = –6V
Output capacitance	C _{oss}	–	28	–	pF	V _{GS} = 0V
Reverse transfer capacitance	C _{rss}	–	21	–	pF	f=1MHz
Turn-on delay time	t _{d(on)*}	–	8	–	ns	V _{DD} ≐ –6V
Rise time	t _r *	–	10	–	ns	I _D = –0.6A
Turn-off delay time	t _{d(off)*}	–	30	–	ns	V _{GS} = –4.5V
Fall time	t _f *	–	9	–	ns	R _L ≐ 10Ω
Total gate charge	Q _g *	–	2.4	–	nC	V _{DD} ≐ –6V, V _{GS} = –4.5V
Gate-source charge	Q _{gs} *	–	0.6	–	nC	I _D = –1.3A
Gate-drain charge	Q _{gd} *	–	0.4	–	nC	R _L ≐ 4.6Ω, R _G = 10Ω

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	–1.2	V	I _S = –1.3A, V _{GS} =0V

*Pulsed

●Electrical characteristic curves

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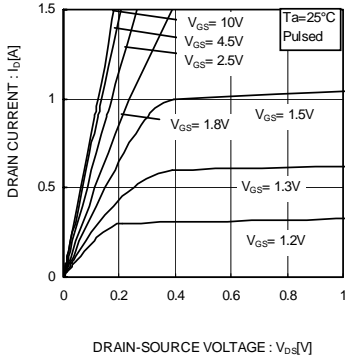


Fig.1 Typical Output Characteristics(I)

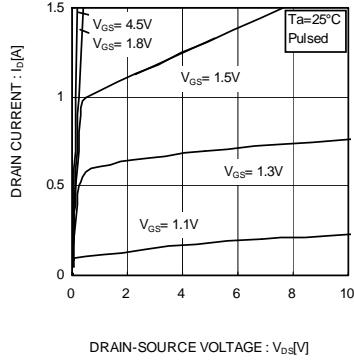


Fig.2 Typical Output Characteristics(II)

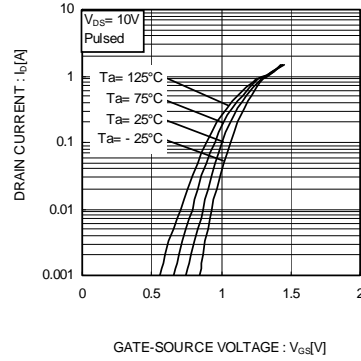


Fig.3 Typical Transfer Characteristics

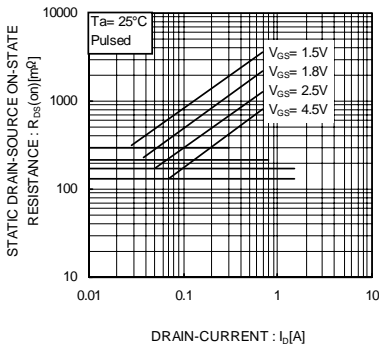


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

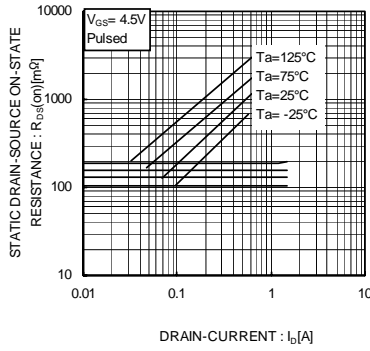


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

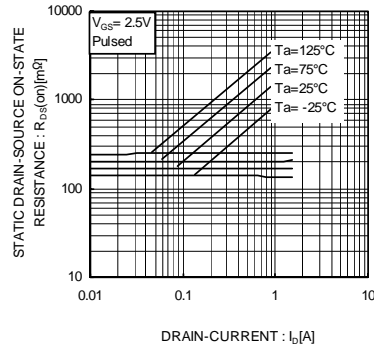


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

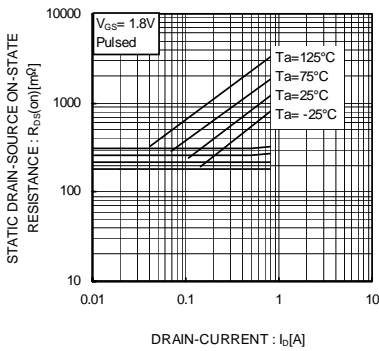


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

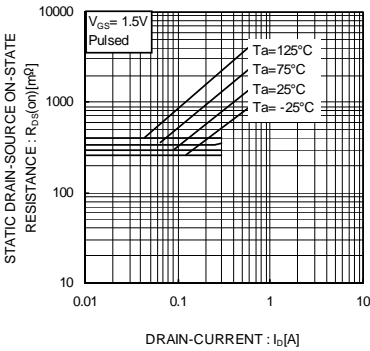


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

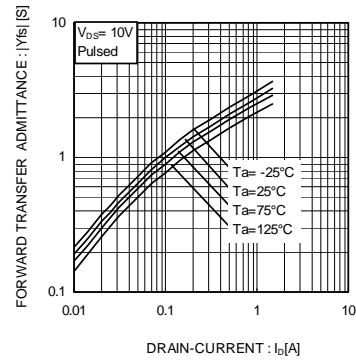


Fig.9 Forward Transfer Admittance vs. Drain Current

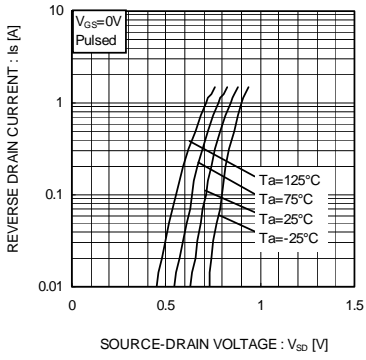


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

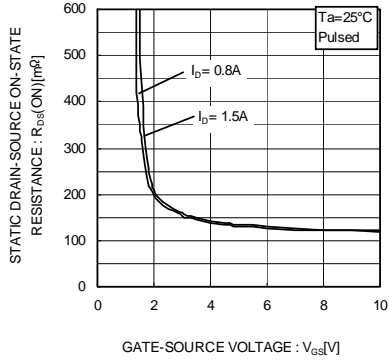


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

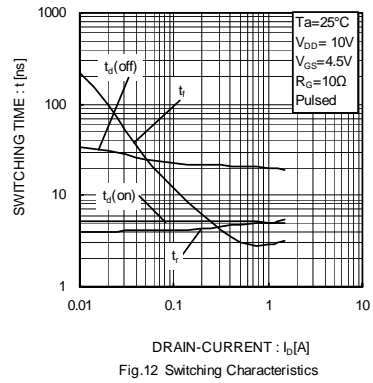


Fig.12 Switching Characteristics

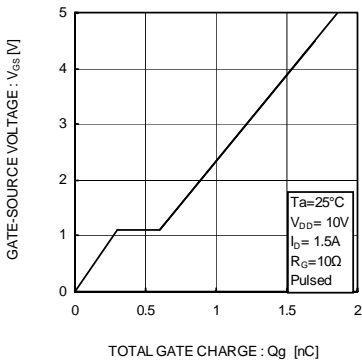


Fig.13 Dynamic Input Characteristics

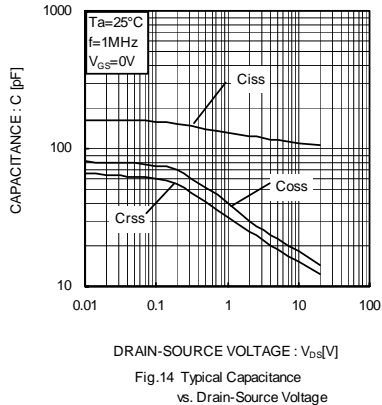


Fig.14 Typical Capacitance vs. Drain-Source Voltage

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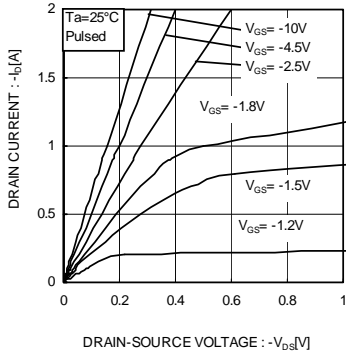


Fig.1 Typical output characteristics (I)

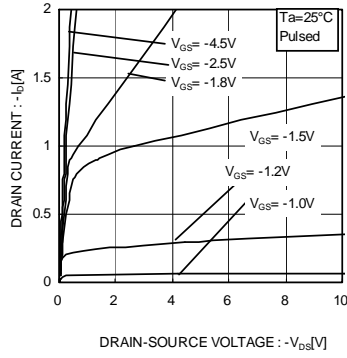


Fig.2 Typical output characteristics (II)

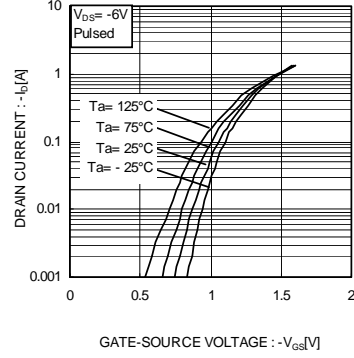


Fig.3 Typical Transfer Characteristics

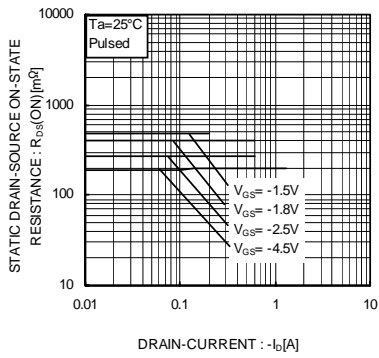


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

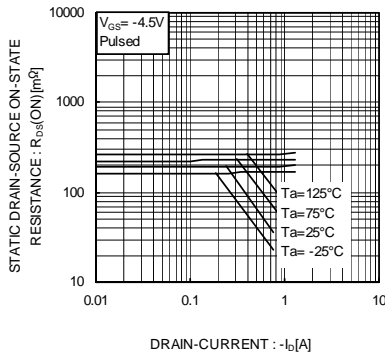


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

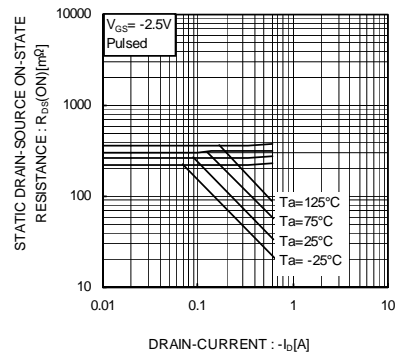


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

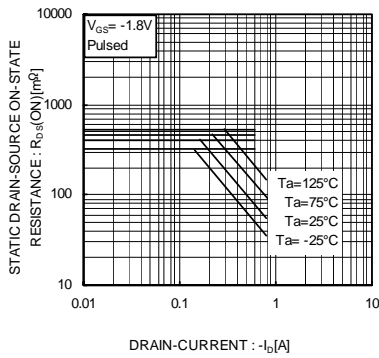


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

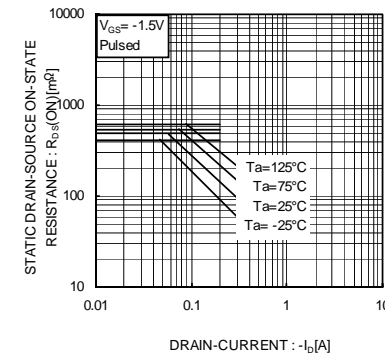


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (IV)

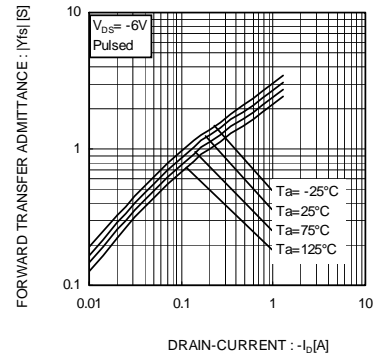
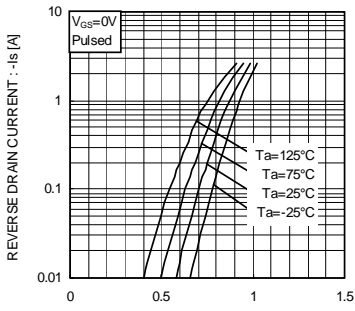
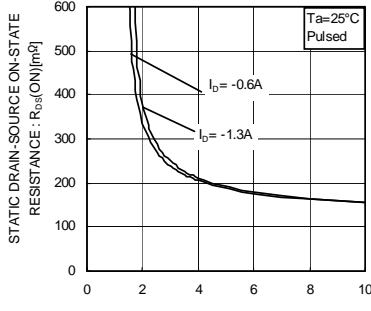


Fig.9 Forward Transfer Admittance vs. Drain Current



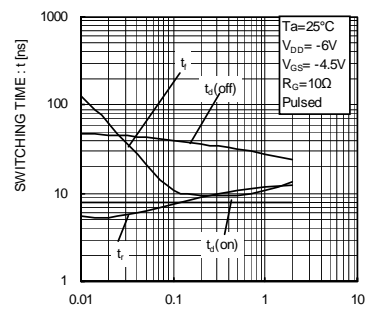
SOURCE-DRAIN VOLTAGE : $-V_{sd}$ [V]

Fig.10 Reverse Drain Current vs. Source-Drain Voltage



GATE-SOURCE VOLTAGE : $-V_{gs}$ [V]

Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage



DRAIN-CURRENT : $-I_b$ [A]

Fig.12 Switching Characteristics

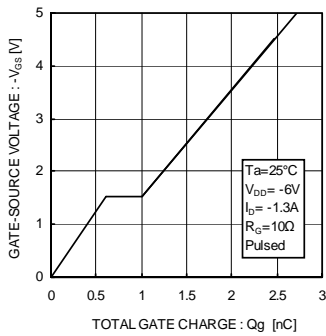


Fig.13 Dynamic Input Characteristics

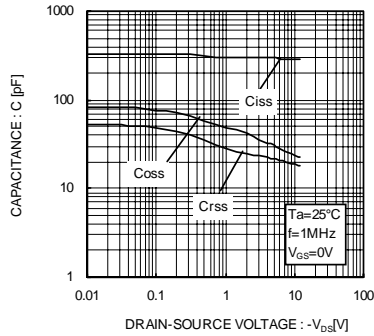


Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuit

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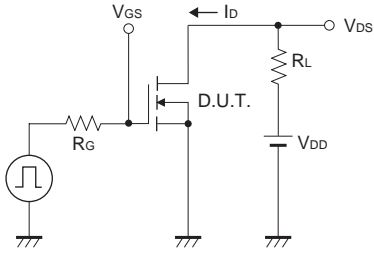


Fig.1-1 Switching Time Measurement Circuit

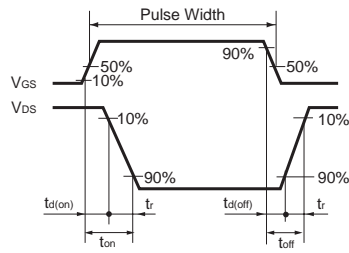


Fig.1-2 Switching Waveforms

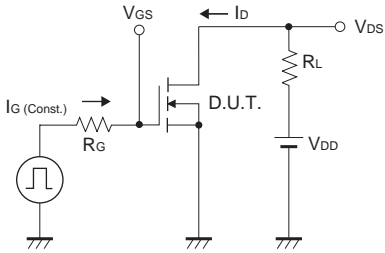


Fig.2-1 Gate Charge Measurement Circuit

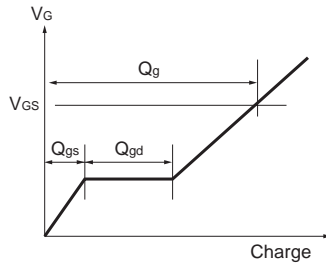


Fig.2-2 Gate Charge Waveform

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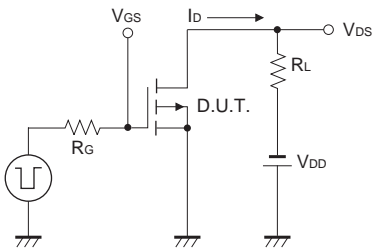


Fig.3-1 Switching Time Measurement Circuit

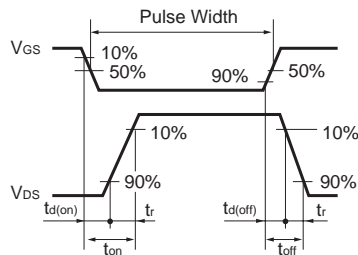


Fig.3-2 Switching Waveforms

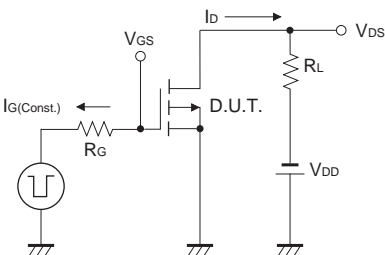


Fig.4-1 Gate Charge Measurement Circuit

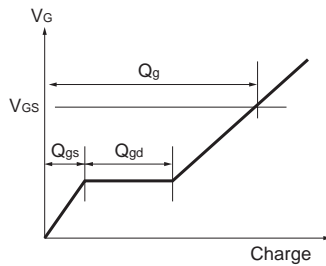


Fig.4-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
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