

MOSFETs Silicon N-channel MOS (U-MOSVII-H)

# TPH5R906NH

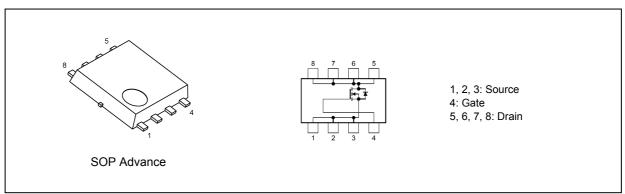
#### 1. Applications

- Switching Voltage Regulators
- · Motor Drivers
- · DC-DC Converters

#### 2. Features

- (1) Small footprint due to a small and thin package
- (2) High-speed switching
- (3) Small gate charge:  $Q_{SW} = 18 \text{ nC (typ.)}$
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 4.8 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (5) Low leakage current:  $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 60 \text{ V)}$
- (6) Enhancement mode:  $V_{th} = 2.0 \text{ to } 4.0 \text{ V } (V_{DS} = 10 \text{ V}, I_D = 0.3 \text{ mA})$

#### 3. Packaging and Internal Circuit



### 4. Absolute Maximum Ratings (Note) (T<sub>a</sub> = 25°C unless otherwise specified)

Characteris	tics		Symbol	Rating	Unit
Drain-source voltage			$V_{DSS}$	60	V
Gate-source voltage			$V_{GSS}$	±20	]
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I <sub>D</sub>	71	Α
Drain current (DC)		(Note 1)	I <sub>D</sub>	28	]
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I <sub>DP</sub>	84	]
Power dissipation	(T <sub>c</sub> = 25°C)		P <sub>D</sub>	57	W
Power dissipation	(t = 10 s)	(Note 3)	P <sub>D</sub>	2.8	W
Power dissipation	(t = 10 s)	(Note 4)	$P_{D}$	1.6	W
Single-pulse avalanche energy		(Note 5)	E <sub>AS</sub>	124	mJ
Avalanche current			I <sub>AR</sub>	28	Α
Channel temperature			T <sub>ch</sub>	150	°C
Storage temperature			T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production



#### 5. Thermal Characteristics

Characterist	Symbol	Max	Unit		
Channel-to-case thermal resistance	$(T_c = 25^{\circ}C)$		R <sub>th(ch-c)</sub>	2.19	°C/W
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 3)	R <sub>th(ch-a)</sub>	44.6	°C/W
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 4)	R <sub>th(ch-a)</sub>	78.1	°C/W

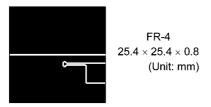
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon capability. Package limit is 60 A.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5:  $V_{DD}$  = 24 V,  $T_{ch}$  = 25°C (initial), L = 0.22 mH,  $R_G$  = 1  $\Omega$ ,  $I_{AR}$  = 28 A



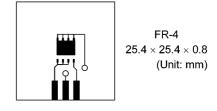


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



#### 6. Electrical Characteristics

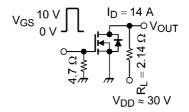
### 6.1. Static Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I <sub>GSS</sub>	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_		±0.1	μΑ
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	_	_	10	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	60			V
Drain-source breakdown voltage (Note 6)	V <sub>(BR)DSX</sub>	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	45			
Gate threshold voltage	$V_{th}$	$V_{DS} = 10 \text{ V}, I_D = 0.3 \text{ mA}$	2.0	_	4.0	
Drain-source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 6.5 V, I <sub>D</sub> = 14 A	_	6.4	14	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A		4.8	5.9	

Note 6: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

### 6.2. Dynamic Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	2340	3100	pF
Reverse transfer capacitance	C <sub>rss</sub>		_	50	95	
Output capacitance	C <sub>oss</sub>		_	745	_	
Gate resistance	r <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	1.0	1.5	Ω
Switching time (rise time)	t <sub>r</sub>	See Figure 6.2.1.	_	9.9	_	ns
Switching time (turn-on time)	t <sub>on</sub>		_	22	_	
Switching time (fall time)	t <sub>f</sub>		_	9.0	_	
Switching time (turn-off time)	t <sub>off</sub>		_	27	_	



Duty  $\leq$  1%,  $t_{\text{W}}=$  10  $\mu s$ 

Fig. 6.2.1 Switching Time Test Circuit

### 6.3. Gate Charge Characteristics ( $T_a = 25^{\circ}$ C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 48 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 28 \text{ A}$		38		nC
Gate-source charge 1	Q <sub>gs1</sub>			12		
Gate-drain charge	$Q_{gd}$			12		
Gate switch charge	$Q_{SW}$			18	_	

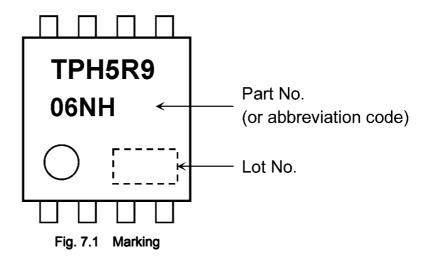
### 6.4. Source-Drain Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (pulsed)	(Note 7)	I <sub>DRP</sub>	_	_	_	84	Α
Diode forward voltage		$V_{DSF}$	I <sub>DR</sub> = 28 A, V <sub>GS</sub> = 0 V	_	_	-1.2	V

Note 7: Ensure that the channel temperature does not exceed 150°C.



## 7. Marking



Rev.4.0

## 8. Characteristics Curves (Note)

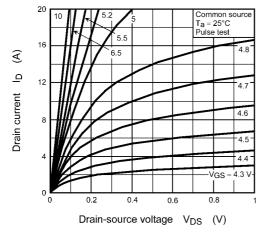


Fig. 8.1 I<sub>D</sub> - V<sub>DS</sub>

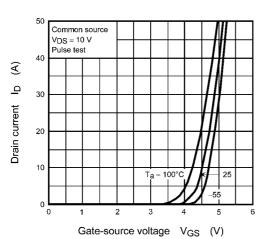


Fig. 8.3  $I_D - V_{GS}$ 

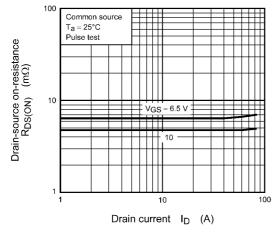


Fig. 8.5 R<sub>DS(ON)</sub> - I<sub>D</sub>

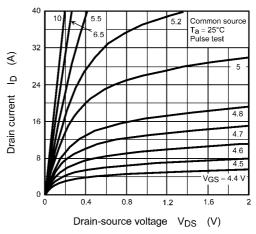


Fig. 8.2 I<sub>D</sub> - V<sub>DS</sub>

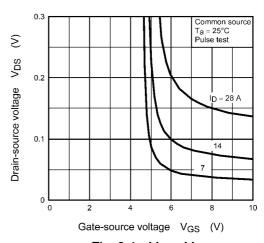


Fig. 8.4 V<sub>DS</sub> - V<sub>GS</sub>

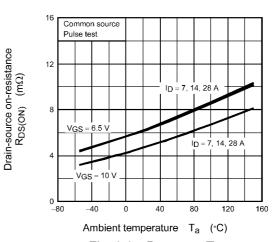


Fig. 8.6 R<sub>DS(ON)</sub> - T<sub>a</sub>

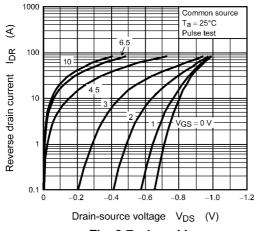


Fig. 8.7 IDR - VDS

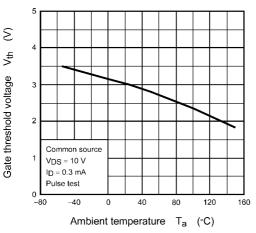


Fig. 8.9 V<sub>th</sub> - T<sub>a</sub>

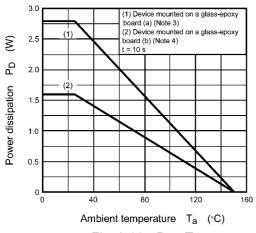


Fig. 8.11 P<sub>D</sub> - T<sub>a</sub> (Guaranteed Maximum)

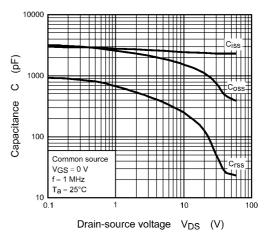


Fig. 8.8 Capacitance - V<sub>DS</sub>

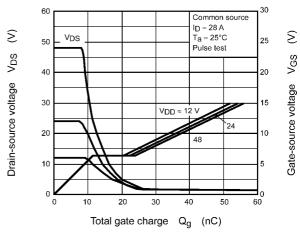


Fig. 8.10 Dynamic Input/Output Characteristics

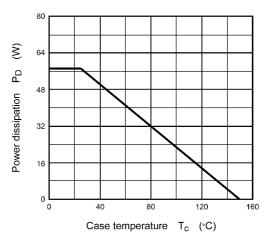


Fig. 8.12 P<sub>D</sub> - T<sub>c</sub> (Guaranteed Maximum)

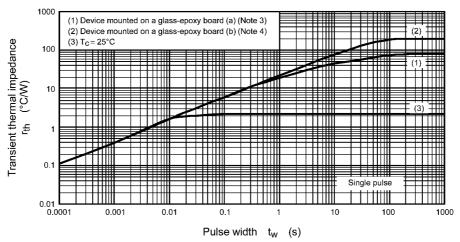


Fig. 8.13 r<sub>th</sub> - t<sub>w</sub> (Guaranteed Maximum)

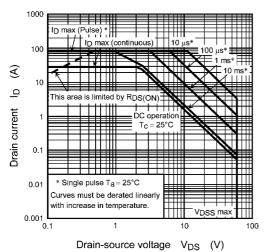


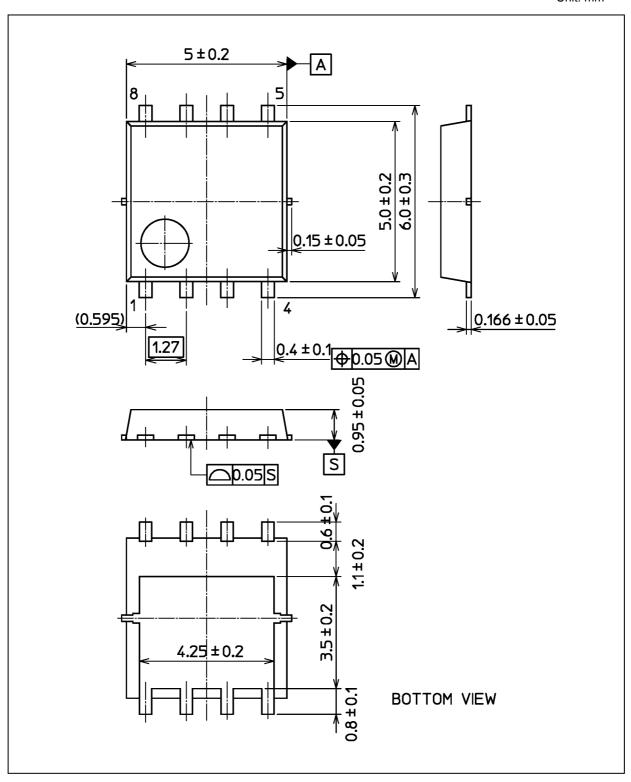
Fig. 8.14 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



### **Package Dimensions**

Unit: mm



Weight: 0.069 g (typ.)

Package Name(s)	
TOSHIBA: 2-5Q1S	
Nickname: SOP Advance	



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