

Four Output Differential Buffer for PCIe Gen 1 and Gen 2

ICS9DB403D

Description

The ICS9DB403 is compatible with the Intel DB400v2 Differential Buffer Specification. This buffer provides 4 PCI-Express Gen2 clocks. The ICS9DB403 is driven by a differential output pair from a CK410B+, CK505 or CK509B main clock generator.

Output Features

- 4 - 0.7V current-mode differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available
- 50-100 MHz operation in PLL mode
- 50-400 MHz operation in Bypass mode

Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread.
- Supports undriven differential outputs in PD# and SRC_STOP# modes for power management.

Key Specifications

- Outputs cycle-cycle jitter < 50ps
- Outputs skew: 50ps
- Phase jitter: PCIe Gen1 < 86ps peak to peak
- Phase jitter: PCIe Gen2 < 3.0/3.1ps rms
- 28-pin SSOP/TSSOP package
- Available in RoHS compliant packaging
- Supports Commercial (0 to +70°C) and Industrial (-40 to +85°C) temperature ranges

Functional Block Diagram



Note: Polarities shown for OE_INV = 0.

Pin Configuration

| | | | | |
|-------------|----|---|----|-----------|
| VDDR | 1 | ICS9DB403D (same as ICS9DB104) | 28 | VDDA |
| SRC_IN | 2 | | 27 | GNDA |
| SRC_IN# | 3 | | 26 | IREF |
| GND | 4 | | 25 | OE_INV |
| VDD | 5 | | 24 | VDD |
| DIF_1 | 6 | | 23 | DIF_6 |
| DIF_1# | 7 | | 22 | DIF_6# |
| OE_1 | 8 | | 21 | OE_6 |
| DIF_2 | 9 | | 20 | DIF_5 |
| DIF_2# | 10 | | 19 | DIF_5# |
| VDD | 11 | | 18 | VDD |
| BYPASS#/PLL | 12 | | 17 | HIGH_BW# |
| SCLK | 13 | | 16 | DIF_STOP# |
| SDATA | 14 | | 15 | PD# |

OE_INV = 0

| | | | | |
|-------------|----|---|----|-----------------|
| VDDR | 1 | ICS9DB403D (same as ICS9DB401) | 28 | VDDA |
| SRC_IN | 2 | | 27 | GNDA |
| SRC_IN# | 3 | | 26 | IREF |
| GND | 4 | | 25 | OE_INV |
| VDD | 5 | | 24 | VDD |
| DIF_1 | 6 | | 23 | DIF_6 |
| DIF_1# | 7 | | 22 | DIF_6# |
| OE1# | 8 | | 21 | OE6# |
| DIF_2 | 9 | | 20 | DIF_5 |
| DIF_2# | 10 | | 19 | DIF_5# |
| VDD | 11 | | 18 | VDD |
| BYPASS#/PLL | 12 | | 17 | HIGH_BW# |
| SCLK | 13 | | 16 | DIF_STOP |
| SDATA | 14 | | 15 | PD |

OE_INV = 1

28-pin SSOP & TSSOP

Polarity Inversion Pin List Table

| Pins | OE_INV | |
|------|-----------|----------|
| | 0 | 1 |
| 8 | OE_1 | OE1# |
| 15 | PD# | PD |
| 16 | DIF_STOP# | DIF_STOP |
| 21 | OE_6 | OE6# |

Power Groups

| Pin Number | | Description |
|---------------|-----|-------------------------------|
| VDD | GND | |
| 1 | 4 | SRC_IN/SRC_IN# |
| 5, 11, 18, 24 | 4 | DIF(1,2,5,6) |
| N/A | 27 | IREF |
| 28 | 27 | Analog VDD & GND for PLL core |

Pin Description When OE_INV = 0

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|-------------|----------|---|
| 1 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 4 | GND | PWR | Ground pin. |
| 5 | VDD | PWR | Power supply, nominal 3.3V |
| 6 | DIF_1 | OUT | 0.7V differential true clock output |
| 7 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 8 | OE_1 | IN | Active high input for enabling output 1. 0 =disable outputs, 1= enable outputs |
| 9 | DIF_2 | OUT | 0.7V differential true clock output |
| 10 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 15 | PD# | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped. |
| 16 | DIF_STOP# | IN | Active low input to stop differential output clocks. |
| 17 | HIGH_BW# | IN | 3.3V input for selecting PLL Band Width 0 = High, 1= Low |
| 18 | VDD | PWR | Power supply, nominal 3.3V |
| 19 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 20 | DIF_5 | OUT | 0.7V differential true clock output |
| 21 | OE_6 | IN | Active high input for enabling output 6. 0 =disable outputs, 1= enable outputs |
| 22 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 23 | DIF_6 | OUT | 0.7V differential true clock output |
| 24 | VDD | PWR | Power supply, nominal 3.3V |
| 25 | OE_INV | IN | This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#) |
| 26 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 27 | GND_A | PWR | Ground pin for the PLL core. |
| 28 | VDD_A | PWR | 3.3V power for the PLL core. |

Pin Description When OE_INV = 1

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|-------------|----------|---|
| 1 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 4 | GND | PWR | Ground pin. |
| 5 | VDD | PWR | Power supply, nominal 3.3V |
| 6 | DIF_1 | OUT | 0.7V differential true clock output |
| 7 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 8 | OE1# | IN | Active low input for enabling DIF pair 1. 1 =disable outputs, 0 = enable outputs |
| 9 | DIF_2 | OUT | 0.7V differential true clock output |
| 10 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 15 | PD | IN | Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped. |
| 16 | DIF_STOP | IN | Active High input to stop differential output clocks. |
| 17 | HIGH_BW# | IN | 3.3V input for selecting PLL Band Width 0 = High, 1= Low |
| 18 | VDD | PWR | Power supply, nominal 3.3V |
| 19 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 20 | DIF_5 | OUT | 0.7V differential true clock output |
| 21 | OE6# | IN | Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs |
| 22 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 23 | DIF_6 | OUT | 0.7V differential true clock output |
| 24 | VDD | PWR | Power supply, nominal 3.3V |
| 25 | OE_INV | IN | This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#) |
| 26 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 27 | GND_A | PWR | Ground pin for the PLL core. |
| 28 | VDD_A | PWR | 3.3V power for the PLL core. |

Absolute Max

| Symbol | Parameter | Min | Max | Units |
|----------------------|--|---------|-----------------------|-------|
| VDDA/R | 3.3V Core Supply Voltage | | 4.6 | V |
| VDD | 3.3V Logic Supply Voltage | | 4.6 | V |
| V _{IL} | Input Low Voltage | GND-0.5 | | V |
| V _{IH} | Input High Voltage | | V _{DD} +0.5V | V |
| T _s | Storage Temperature | -65 | 150 | °C |
| T _{ambient} | Commerical Operating Range | 0 | 70 | °C |
| | Industrial Operating Range | -40 | 85 | °C |
| T _{case} | Case Temperature | | 115 | °C |
| ESD prot | Input ESD protection human body model | 2000 | | V |

Electrical Characteristics - Clock Input Parameters

T_A = T_{ambient} for the desired operating range, Supply Voltage V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | V _{IHDIF} | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 300 | | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | V _{SWING} | Peak to Peak value (single-ended measurement) | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFin} | Differential Measurement | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through V_{swing} min centered around differential zero

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = Tambient for the desired operating range, Supply Voltage V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Input High Voltage | V _{IHSE} | Single Ended Inputs, 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{ILSE} | | GND - 0.3 | | 0.8 | V | 1 |
| Input High Current | I _{IHSE} | V _{IN} = V _{DD} | -5 | | 5 | uA | 1 |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| 9DB803 Supply Current | I _{DD3.3OPC} | Full Active, C _L = Full load; Commerical Temp Range | | 175 | 200 | mA | 1 |
| | I _{DD3.3OPI} | Full Active, C _L = Full load; Industrial Temp Range | | 190 | 225 | mA | 1 |
| 9DB803 Powerdown Current | I _{DD3.3PDC} | all diff pairs driven, C-Temp | | 50 | 60 | mA | 1 |
| | | all differential pairs tri-stated, C-Temp | | 4 | 6 | mA | 1 |
| | I _{DD3.3PDI} | all diff pairs driven, I-temp | | 55 | 65 | mA | 1 |
| | | all differential pairs tri-stated, I-temp | | 6 | 8 | mA | 1 |
| 9DB403 Supply Current | I _{DD3.3OPC} | Full Active, C _L = Full load; Commerical Temp Range | | 105 | 125 | mA | 1 |
| | I _{DD3.3OPI} | Full Active, C _L = Full load; Industrial Temp Range | | 115 | 150 | mA | 1 |
| 9DB403 Powerdown Current | I _{DD3.3PDC} | all diff pairs driven, C-Temp | | 25 | 30 | mA | 1 |
| | | all differential pairs tri-stated, C-Temp | | 2 | 3 | mA | 1 |
| | I _{DD3.3PDI} | all diff pairs driven, I-Temp | | 30 | 35 | mA | 1 |
| | | all differential pairs tri-stated, I-Temp | | 3 | 4 | mA | 1 |
| Input Frequency | F _{IPLL} | PCle Mode (Bypass#/PLL= 1) | 50 | 100.00 | 110 | MHz | 1 |
| | F _{I BYPASS} | Bypass Mode ((Bypass#/PLL= 0) | 33 | | 400 | MHz | 1 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except SRC_IN | 1.5 | | 5 | pF | 1 |
| | C _{INSRC_IN} | SRC_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| PLL Bandwidth | BW | -3dB point in High BW Mode | 2 | 3 | 4 | MHz | 1 |
| | | -3dB point in Low BW Mode | 0.7 | 1 | 1.4 | MHz | 1 |
| PLL Jitter Peaking | t _{JPEAK} | Peak Pass band Gain | | 1.5 | 2 | dB | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | cycles | 1,3 |
| Tdrive_SRC_STOP# | t _{DRVSTP} | DIF output enable after SRC_Stop# de-assertion | | | 10 | ns | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of PD# and SRC_STOP# | | | 5 | ns | 1 |
| Trise | t _R | Rise time of PD# and SRC_STOP# | | | 5 | ns | 2 |
| SMBus Voltage | V _{MAX} | Maximum input voltage | | | 5.5 | V | 1 |
| Low-level Output Voltage | V _{OL} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| Current sinking at V _{OL} | I _{PULLUP} | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.²See timing diagrams for timing requirements.³Time from deassertion until outputs are >200 mV⁴SRC_IN input⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair
 $T_A = T_{\text{ambient}}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 2\text{pF}$, $R_S = 33\Omega$, $R_P = 49.9\Omega$, $R_{REF} = 475\Omega$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------|------------------------|--|------|-------------|------|------------|---------|
| Current Source Output Impedance | Z_{o1} | | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,2 |
| Voltage Low | VLow | | -150 | | 150 | | 1,2 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 |
| Rise Time | t_r | $V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$ | 175 | | 700 | ps | 1 |
| Fall Time | t_f | $V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$ | 175 | | 700 | ps | 1 |
| Rise Time Variation | d- t_r | | | | 125 | ps | 1 |
| Fall Time Variation | d- t_f | | | | 125 | ps | 1 |
| Duty Cycle | d_{t3} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Skew, Input to Output | t_{pdBYP} | Bypass Mode, $V_T = 50\%$ | 2500 | | 5000 | ps | 1 |
| | t_{pdPLL} | PLL Mode $V_T = 50\%$ | -250 | | 250 | ps | 1 |
| Skew, Output to Output | t_{sk3} | $V_T = 50\%$ | | | 50 | ps | 1 |
| | | PLL mode | | | 50 | ps | 1,3 |
| Jitter, Cycle to cycle | $t_{j\text{cyc-cyc}}$ | Additive Jitter in Bypass Mode | | | 50 | ps | 1,3 |
| | | | | | | | |
| Jitter, Phase | $t_{j\text{phaseBYP}}$ | PCIe Gen1 phase jitter (Additive in Bypass Mode) | | 7 | 10 | ps (pk2pk) | 1,4,5 |
| | | PCIe Gen 2 Low Band phase jitter (Additive in Bypass Mode) | | 0 | 0.1 | ps (rms) | 1,4,5 |
| | | PCIe Gen 2 High Band phase jitter (Additive in Bypass Mode) | | 0.3 | 0.5 | ps (rms) | 1,4,5 |
| | $t_{j\text{phasePLL}}$ | PCIe Gen 1 phase jitter | | 40 | 86 | ps (pk2pk) | 1,4,5 |
| | | PCIe Gen 2 Low Band phase jitter | | 1.5 | 3 | ps (rms) | 1,4,5 |
| | | PCIe Gen 2 High Band phase jitter | | 2.7/ 2.2 | 3.1 | ps (rms) | 1,4,5,6 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V}$ @ $Z_O = 50\Omega$.

³ Measured from differential waveform

⁴ See <http://www.pcisig.com> for complete specs

⁵ Device driven by 932S421C or equivalent.

⁶ First number is High Bandwidth Mode, second number is Low Bandwidth Mode

Clock Periods Differential Outputs with Spread Spectrum Enabled

| Measurement Window | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | Units | Notes |
|--------------------|---------|-------------------------|-------------------------|-------------------------|----------|-------------------|--------------------|----------|-------|-------|
| Symbol | | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | | |
| Signal Name | DIF 100 | 9.87400 | 9.99900 | 9.99900 | 10.00000 | 10.00100 | 10.05130 | 10.17630 | ns | 1,2,3 |
| | DIF 133 | 7.41425 | 7.49925 | 7.49925 | 7.50000 | 7.50075 | 7.53845 | 7.62345 | ns | 1,2,4 |
| | DIF 166 | 5.91440 | 5.99940 | 5.99940 | 6.00000 | 6.00060 | 6.03076 | 6.11576 | ns | 1,2,4 |
| | DIF 200 | 4.91450 | 4.99950 | 4.99950 | 5.00000 | 5.00050 | 5.02563 | 5.11063 | ns | 1,2,4 |
| | DIF 266 | 3.66463 | 3.74963 | 3.74963 | 3.75000 | 3.75038 | 3.76922 | 3.85422 | ns | 1,2,4 |
| | DIF 333 | 2.91470 | 2.99970 | 2.99970 | 3.00000 | 3.00030 | 3.01538 | 3.10038 | ns | 1,2,4 |
| | DIF 400 | 2.41475 | 2.49975 | 2.49975 | 2.50000 | 2.50025 | 2.51282 | 2.59782 | ns | 1,2,4 |

Clock Periods Differential Outputs with Spread Spectrum Disabled

| Measurement Window | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | Units | Notes |
|--------------------|---------|-------------------------|-------------------------|-------------------------|----------|-------------------|--------------------|----------|-------|-------|
| Symbol | | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | | |
| Signal Name | DIF 100 | 9.87400 | | 9.99900 | 10.00000 | 10.00100 | | 10.17630 | ns | 1,2,3 |
| | DIF 133 | 7.41425 | | 7.49925 | 7.50000 | 7.50075 | | 7.62345 | ns | 1,2,4 |
| | DIF 166 | 5.91440 | | 5.99940 | 6.00000 | 6.00060 | | 6.11576 | ns | 1,2,4 |
| | DIF 200 | 4.91450 | | 4.99950 | 5.00000 | 5.00050 | | 5.11063 | ns | 1,2,4 |
| | DIF 266 | 3.66463 | | 3.74963 | 3.75000 | 3.75038 | | 3.85422 | ns | 1,2,4 |
| | DIF 333 | 2.91470 | | 2.99970 | 3.00000 | 3.00030 | | 3.10038 | ns | 1,2,4 |
| | DIF 400 | 2.41475 | | 2.49975 | 2.50000 | 2.50025 | | 2.59782 | ns | 1,2,4 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.

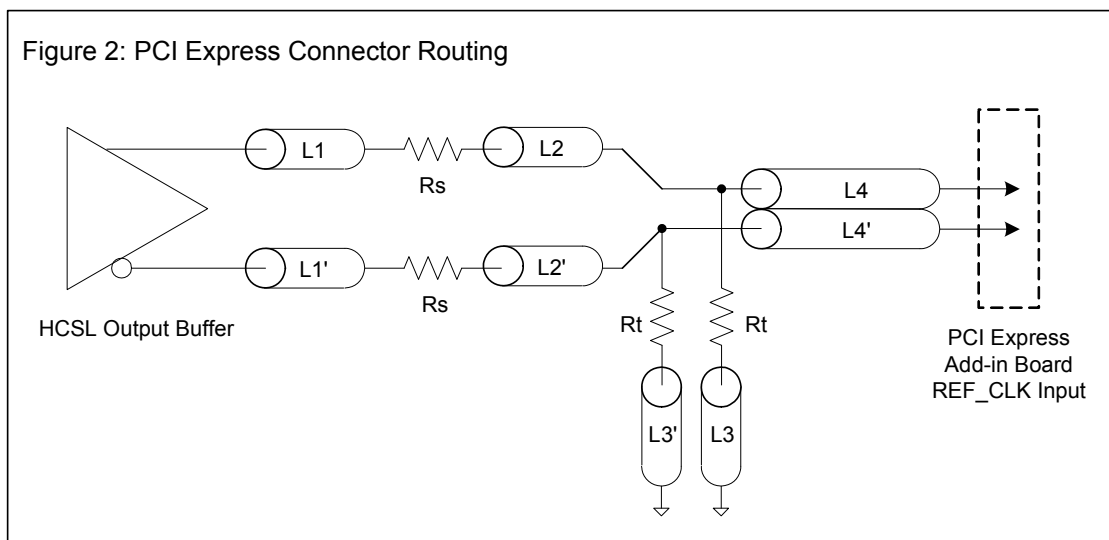
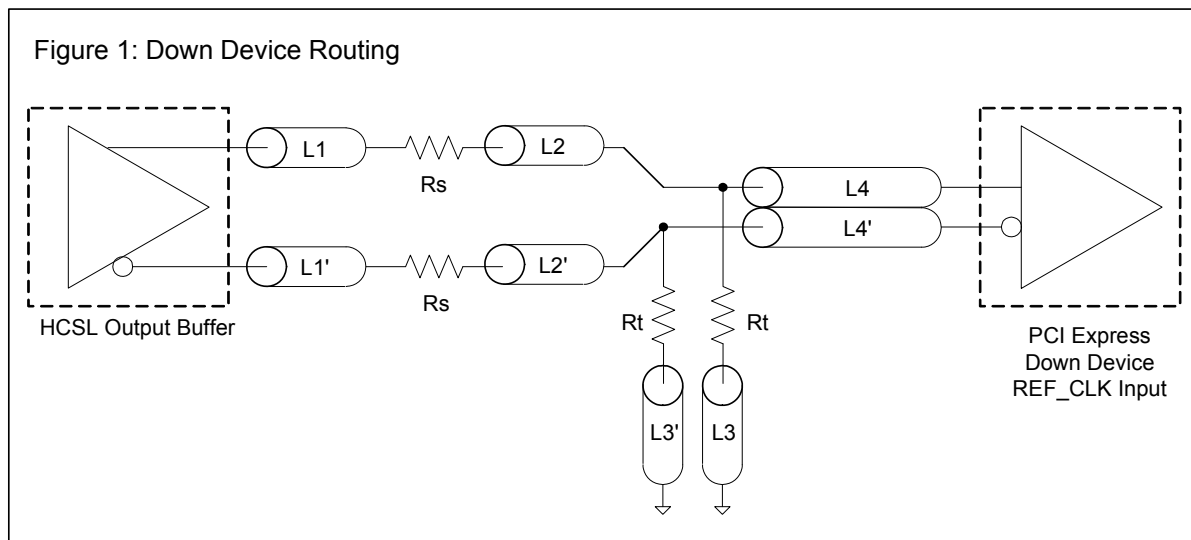
³ Driven by SRC output of main clock, PLL or Bypass mode

⁴ Driven by CPU output of CK410/CK505 main clock, **Bypass mode only**

| SRC Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| R_s | 33 | ohm | 1 |
| R_t | 49.9 | ohm | 1 |

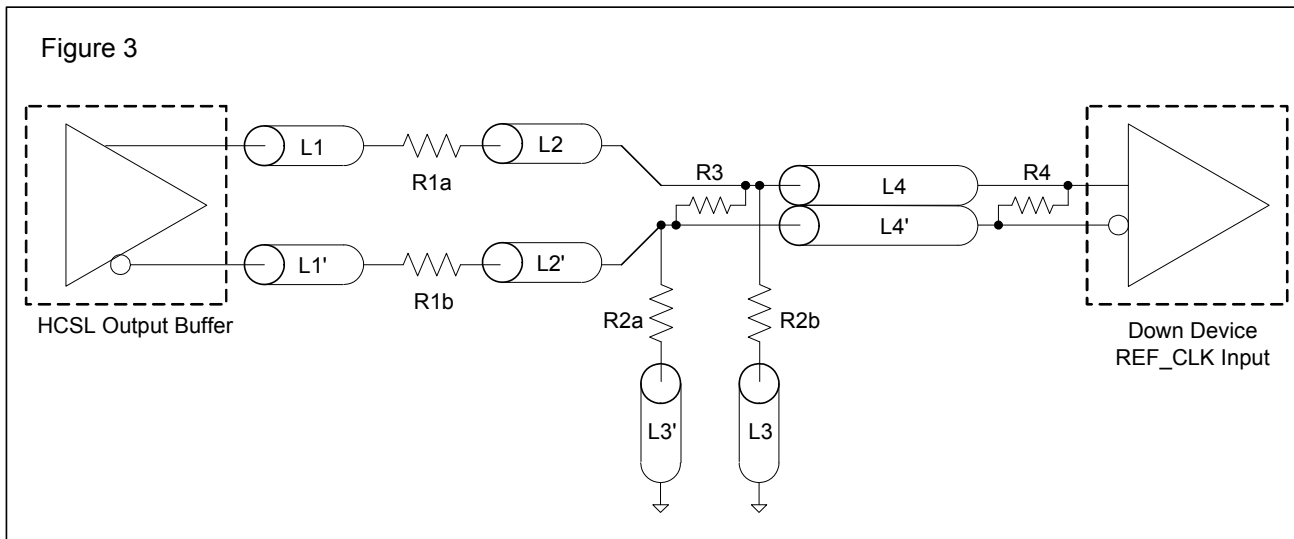
| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

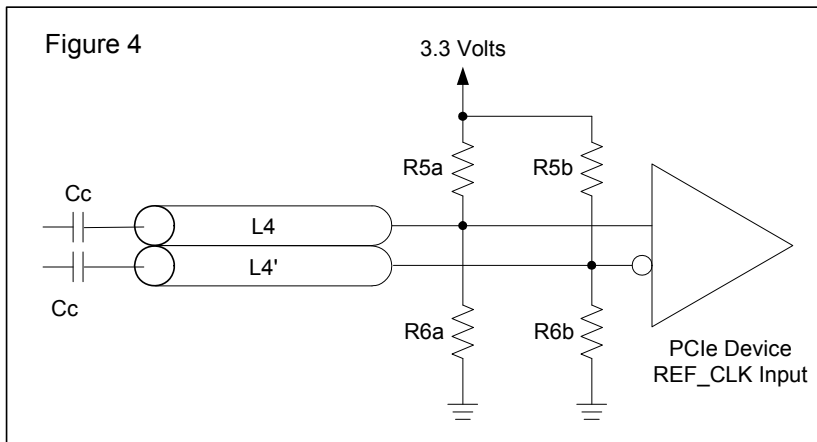


| V _{diff} | V _{p-p} | V _{cm} | R1 | R2 | R3 | R4 | Note |
|-------------------|------------------|-----------------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1
R2a = R2b = R2



| Component | Value | Note |
|-----------------|-------------|------|
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| V _{cm} | 0.350 volts | |



General SMBus serial interface information for the ICS9DB403D

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC_(h)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC_(h)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD_(h)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(h) was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|---------------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address DC _(h) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | X Byte |
| ◊ | | |
| ◊ | | |
| ◊ | | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | |
|---------------------------------|-----------------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address DC _(h) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address DD _(h) | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | |
| | | X Byte |
| ACK | | |
| ◊ | | |
| ◊ | | |
| ◊ | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------|------------------------|------|----------|--------|---------|
| Bit 7 | - | PD_Mode | PD# drive mode | RW | driven | Hi-Z | 0 |
| Bit 6 | - | STOP_Mode | DIF_Stop# drive mode | RW | driven | Hi-Z | 0 |
| Bit 5 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 2 | - | PLL_BW# | Select PLL BW | RW | High BW | Low BW | 1 |
| Bit 1 | - | BYPASS# | BYPASS#/PLL | RW | fan-out | ZDB | 1 |
| Bit 0 | - | SRC_DIV# | SRC Divide by 2 Select | RW | x/2 | 1x | 1 |

SMBus Table: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|----------|--------|---------|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | | 1 |
| Bit 6 | 22,23 | DIF_6 | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | 19,20 | DIF_5 | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | 1 |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | 1 |
| Bit 2 | 9,10 | DIF_2 | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | 6,7 | DIF_1 | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | | 1 |

NOTE: The SMBus Output Enable Bit must be '1' AND the respective OE pin must be active for the output to run!

SMBus Table: OE Pin Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------------------|------|----------|-----------|---------|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 6 | 22,23 | DIF_6 | DIF_6 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 5 | 19,20 | DIF_5 | DIF_5 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 2 | 9,1 | DIF_2 | DIF_2 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 1 | 6,7 | DIF_1 | DIF_1 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | | 0 |

SMBus Table: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | X |
| Bit 6 | | | Reserved | | | | X |
| Bit 5 | | | Reserved | | | | X |
| Bit 4 | | | Reserved | | | | X |
| Bit 3 | | | Reserved | | | | X |
| Bit 2 | | | Reserved | | | | X |
| Bit 1 | | | Reserved | | | | X |
| Bit 0 | | | Reserved | | | | X |

SMBus Table: Vendor & Revision ID Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | 0 |
| Bit 6 | - | RID2 | | R | - | - | 0 |
| Bit 5 | - | RID1 | | R | - | - | 1 |
| Bit 4 | - | RID0 | | R | - | - | 1 |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBus Table: DEVICE ID

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-------------------|------|--|---|---------|
| Bit 7 | - | | Device ID 7 (MSB) | RW | Device ID is 83 Hex for 9DB803 and 43 Hex for 9DB403 | | 0 |
| Bit 6 | - | | Device ID 6 | RW | | | X |
| Bit 5 | - | | Device ID 5 | RW | | | X |
| Bit 4 | - | | Device ID 4 | RW | | | 0 |
| Bit 3 | - | | Device ID 3 | RW | | | 0 |
| Bit 2 | - | | Device ID 2 | RW | | | 0 |
| Bit 1 | - | | Device ID 1 | RW | | | 1 |
| Bit 0 | - | | Device ID 0 | RW | | | 1 |

SMBus Table: Byte Count Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | - | BC7 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |

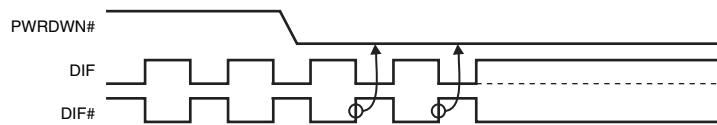
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

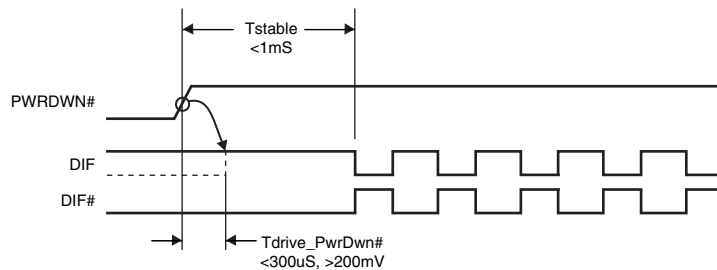
PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with $2 \times I_{REF}$ and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.



PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.



SRC_STOP#

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

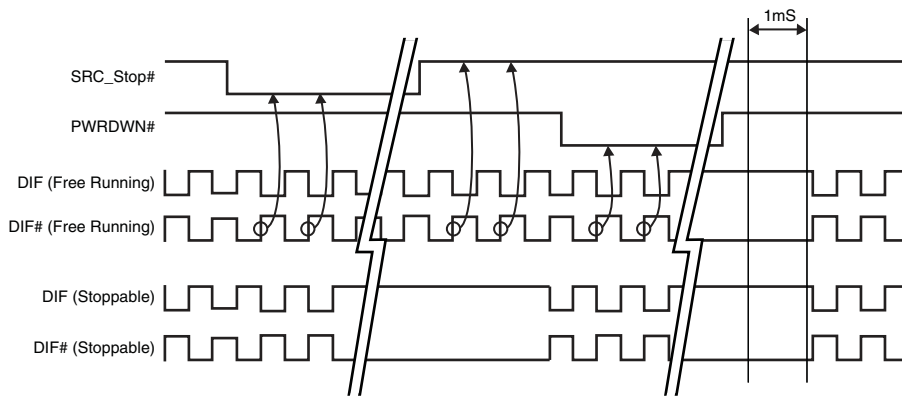
SRC_STOP# - Assertion

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with 6xI_{REF}. DIF# is not driven, but pulled low by the termination. When the SRC_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

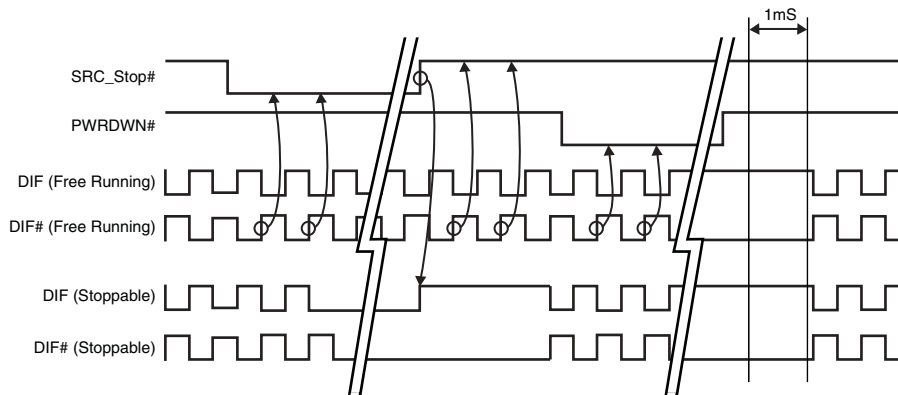
SRC_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)



SRC_STOP_2 (SRC_Stop = Tristate, PD = Driven)



SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)



SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)



28-pin SSOP Package Dimensions



209 mil SSOP

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 2.00 | -- | .079 |
| A1 | 0.05 | -- | .002 | -- |
| A2 | 1.65 | 1.85 | .065 | .073 |
| b | 0.22 | 0.38 | .009 | .015 |
| c | 0.09 | 0.25 | .0035 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 7.40 | 8.20 | .291 | .323 |
| E1 | 5.00 | 5.60 | .197 | .220 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.55 | 0.95 | .022 | .037 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.90 | 10.50 | .390 | .413 |

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

28-pin TSSOP Package Dimensions



4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.60 | 9.80 | .378 | .386 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|--------------|---------------|
| 9DB403DGLF | 9DB403DGLF | Tubes | 28-pin TSSOP | 0 to +70° C |
| 9DB403DGLFT | 9DB403DGLF | Tape and Reel | 28-pin TSSOP | 0 to +70° C |
| 9DB403DGILF | 9DB403DGILF | Tubes | 28-pin TSSOP | -40 to +85° C |
| 9DB403DGILFT | 9DB403DGILF | Tape and Reel | 28-pin TSSOP | -40 to +85° C |
| 9DB403DFLF | 9DB403DFLF | Tubes | 28-pin SSOP | 0 to +70° C |
| 9DB403DFLFT | 9DB403DFLF | Tape and Reel | 28-pin SSOP | 0 to +70° C |
| 9DB403DFILF | 9DB403DFILF | Tubes | 28-pin SSOP | -40 to +85° C |
| 9DB403DFILFT | 9DB403DFILF | Tape and Reel | 28-pin SSOP | -40 to +85° C |

"LF" denotes Pb-free package, RoHS compliant

"D" is the revision designator (will not correlate to datasheet revision)

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|--|---------|
| I | 11/26/2008 | Updated SMBus table - Byte0:Byte3. | 11 |
| J | 2/6/2009 | Added Industrial temp. specs and ordering information. | Various |
| K | 7/13/2009 | Updated general description and block diagram | 1 |
| L | 10/7/2009 | 1. Clarified that Vih and Vil values were for Single ended inputs 2. Added separate Idd values for the 9DB403 3. Added Differential Clock input parameters. | Various |
| M | 1/27/2011 | Updated Termination Figure 4 | 10 |
| N | 5/6/2011 | 1. Update pin 1 pin-name and pin description from VDD to VDDR. This highlights that optimal performance is obtained by treating VDDR as in analog pin. This is a document update only, there is no silicon change. | Various |
| P | 8/27/2012 | Updated Vswing conditions to include "single-ended measurement" | 5 |
| Q | 9/18/2012 | Updated Byte 2, bits 1, 2, 5 and 6 per char review. Outputs can be programmed with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE pins. | 12 |
| R | 11/1/2012 | Updated Input-to-Output Skew max value (Bypass Mode condition only) from 4500ps to 5000ps per latest characterization data. | 7 |

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