19-4204; Rev 2; 2/11

EVALUATION KIT AVAILABLE

Octal, 12-Bit, 50Msps, 1.8V ADC with Serial LVDS Outputs

General Description

The MAX1437B octal, 12-bit analog-to-digital converter (ADC) features fully differential inputs, a pipelined architecture, and digital error correction incorporating a fully differential signal path. This ADC is optimized for low-power and high-dynamic performance in medical imaging instrumentation and digital communications applications. The MAX1437B operates from a 1.8V single supply and consumes only 768mW (96mW per channel) while delivering a 70.2dB (typ) signal-to-noise ratio (SNR) at a 5.3MHz input frequency. In addition to low operating power, the MAX1437B features a low-power standby mode for idle periods.

An internal 1.24V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure allows the use of an external reference for applications requiring increased accuracy or a different input voltage range. The reference architecture is optimized for low noise.

A single-ended clock controls the data-conversion process. An internal duty-cycle equalizer compensates for wide variations in clock duty cycle. An on-chip phase-locked loop (PLL) generates the high-speed serial low-voltage differential signal (LVDS) clock.

The MAX1437B has self-aligned serial LVDS outputs for data, clock, and frame-alignment signals. The output data is presented in two's complement format.

The MAX1437B offers a maximum sample rate of 50Msps. This device is available in a small, 10mm x 10mm x 0.8mm, 68-pin TQFN package with exposed pad and is specified for the extended industrial (-40°C to +85°C) temperature range.

Applications

Ultrasound and Medical Imaging

Instrumentation

Multichannel Communications

Features

- **Excellent Dynamic Performance**
  - **70.2dB SNR at 5.3MHz**
  - **98dBc SFDR at 5.3MHz**
  - **82dB Channel Isolation at 5.3MHz**
- **Ultra-Low Power**
  - **96mW per Channel (Normal Operation)**
- **Serial LVDS Outputs**
- **Pin-Selectable LVDS/SLVS (Scalable Low-Voltage Signal) Mode**
- **LVDS Outputs Support Up to 30in FR-4 Backplane Connections**
- **Test Mode for Digital Signal Integrity**
- **Fully Differential Analog Inputs**
- **Wide Differential Input Voltage Range (1.4V_{P-P})**
- **On-Chip 1.24V Precision Bandgap Reference**
- **Clock Duty-Cycle Equalizer**
- **Compact, 68-Pin TQFN Package with Exposed Pad**
- **Evaluation Kit Available (Order MAX1437BEVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1437BETK+	-40°C to +85°C	68 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
AVDD....................-0.3V to +2.0V
CVDD....................-0.3V to +3.6V
OVDD....................-0.3V to +2.0V
IN_P, IN_N....................-0.3V to (V_{AVDD} + 0.3V)
CLK....................-0.3V to (V_{CVDD} + 0.3V)
OUT_P, $\overline{\text{OUT\_N}}$, FRAME_, CLKOUT_......-0.3V to (V_{OVDD} + 0.3V)
DT, SLVS/$\overline{\text{LVDS}}$, LVDSTEST, PLL_,
REFIO, REFADJ, CMOUT....................-0.3V to (V_{AVDD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 70mW/°C above +70°C)....................4000mW
Operating Temperature Range....................-40°C to +85°C
Maximum Junction Temperature....................+150°C
Storage Temperature Range....................-65°C to +150°C
Lead Temperature (soldering, 10s)....................+300°C
Soldering Temperature (reflow)....................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})...........20°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..............0.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF || 1.0µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)						
Resolution	N		12			Bits
Integral Nonlinearity	INL			±0.3	±2.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature		±0.25	±1	LSB
Offset Error					±0.5	%FS
Gain Error			-3	±0.5	+2	%FS
ANALOG INPUTS (IN_P, IN_N)						
Input Differential Range	V_{ID}	Differential input		1.4		V_{P-P}
Common-Mode Voltage Range	V_{CMO}			0.76		V
Common-Mode Voltage Range Tolerance		(Note 4)		±50		mV
Differential Input Impedance	R_{IN}	Switched capacitor load		2		kΩ
Differential Input Capacitance	C_{IN}			12.5		pF
CONVERSION RATE						
Maximum Conversion Rate	f_{SMAX}		50			MHz
Minimum Conversion Rate	f_{SMIN}			4.0		MHz
Data Latency				6.5		Cycles
DYNAMIC CHARACTERISTICS (differential inputs, 4096-point FFT) (Note 5)						
Signal-to-Noise Ratio	SNR	f_{IN} = 5.3MHz at -0.5dBFS		70.2		dB
		f_{IN} = 20MHz at -0.5dBFS	67	70.2		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 5.3MHz at -0.5dBFS		70.2		dB
		f_{IN} = 20MHz at -0.5dBFS	67	70.1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF ll 1.0µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Effective Number of Bits	ENOB	f_{IN} = 5.3MHz at -0.5dBFS		11.4		Bits
		f_{IN} = 20MHz at -0.5dBFS	10.8	11.4		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 5.3MHz at –0.5dBFS		98		dBc
		f_{IN} = 20MHz at -0.5dBFS	79	93		
Total Harmonic Distortion	THD	f_{IN} = 5.3MHz at -0.5dBFS		-96		dBc
		f_{IN} = 20MHz at -0.5dBFS		-93	-78	
Intermodulation Distortion	IMD	f_1 = 5.3MHz at -6.5dBFS f_2 = 6.3MHz at -6.5dBFS		90.7		dBc
Third-Order Intermodulation	IM3	f_1 = 5.3MHz at -6.5dBFS f_2 = 6.3MHz at -6.5dBFS		98.7		dBc
Aperture Jitter	t_{AJ}	Figure 10		< 0.4		ps_{RMS}
Aperture Delay	t_{AD}	Figure 10		1		ns
Small-Signal Bandwidth	SSBW	Input at -20dBFS		100		MHz
Full-Power Bandwidth	LSBW	Input at -0.5dBFS		100		MHz
Output Noise		IN_P = IN_N		0.44		LSB_{RMS}
Overrange Recovery Time	t_{OR}	R_S = 25Ω, C_S = 50pF		1		Clock cycle
INTERNAL REFERENCE						
REFADJ Internal Reference-Mode Enable Voltage		(Note 6)			0.1	V
REFADJ Low-Leakage Current				1.5		mA
REFIO Output Voltage	V_{REFIO}		1.18	1.24	1.30	V
Reference Temperature Coefficient	TC_{REFIO}			120		ppm/°C
EXTERNAL REFERENCE						
REFADJ External Reference-Mode Enable Voltage		(Note 6)	V_{AVDD} - 0.1			V
REFADJ High-Leakage Current				200		µA
REFIO Input Voltage				1.24		V
REFIO Input Voltage Tolerance				±5		%
REFIO Input Current	I_{REFIO}			< 1		µA
COMMON-MODE OUTPUT (CMOUT)						
CMOUT Output Voltage	V_{CMOUT}			0.76		V
CLOCK INPUT (CLK)						
Input High Voltage	V_{CLKH}		0.8 x V_{AVDD}			V
Input Low Voltage	V_{CLKL}				0.2 x V_{AVDD}	V
Clock Duty Cycle				50		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF ll 1.0µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Duty-Cycle Tolerance					±30		%
Input Leakage Current	DI_{IN}	Input at GND				5	µA
		Input at V_{AVDD}				80	
Input Capacitance	DC_{IN}				5		pF
DIGITAL INPUTS (PLL_, LVDSTEST, DT, SLVS, STBY)							
Input Logic-High Voltage	V_{IH}			0.8 x V_{AVDD}			V
Input Logic-Low Voltage	V_{IL}					0.2 x V_{AVDD}	V
Input Leakage Current	DI_{IN}	Input at GND				5	µA
		Input at V_{AVDD}				80	
Input Capacitance	DC_{IN}				5		pF
LVDS OUTPUTS (OUT_P, OUT_N), SLVS/$\overline{LVDS}$ = LOW							
Differential Output Voltage	V_{OHDIFF}	R_{TERM} = 100Ω		250		450	mV
Output Common-Mode Voltage	V_{OCM}	R_{TERM} = 100Ω		1.125		1.375	V
Rise Time (20% to 80%)	t_{RL}	R_{TERM} = 100Ω, C_{LOAD} = 5pF			350		ps
Fall Time (80% to 20%)	t_{FL}	R_{TERM} = 100Ω, C_{LOAD} = 5pF			350		ps
SLVS OUTPUTS (OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, FRAMEN), SLVS/$\overline{LVDS}$ = HIGH, DT = HIGH							
Differential Output Voltage	V_{OHDIFF}	R_{TERM} = 100Ω			205		mV
Output Common-Mode Voltage	V_{OCM}	R_{TERM} = 100Ω			220		mV
Rise Time (20% to 80%)	t_{RS}	R_{TERM} = 100Ω, C_{LOAD} = 5pF			320		ps
Fall Time (80% to 20%)	t_{FS}	R_{TERM} = 100Ω, C_{LOAD} = 5pF			320		ps
STANDBY MODE (STBY)							
STBY Fall to Output Enable	t_{ENABLE}				200		µs
STBY Rise to Output Disable	$t_{DISABLE}$				60		ns
POWER REQUIREMENTS							
AVDD Supply Voltage Range	V_{AVDD}			1.7	1.8	1.9	V
OVDD Supply Voltage Range	V_{OVDD}			1.7	1.8	1.9	V
CVDD Supply Voltage Range	V_{CVDD}			1.7	1.8	3.5	V
AVDD Supply Current	I_{AVDD}	f_{IN} = 20MHz at -0.5dBFS	STBY = low, DT = low		348	390	mA
			STBY = low, DT = high		348		
			STBY = high, no clock		37		mA
OVDD Supply Current	I_{OVDD}	f_{IN} = 20MHz at -0.5dBFS	STBY = low		74	100	mA
			STBY = low, DT = high		103		
			STBY = high, no clock input		16		µA
CVDD Supply Current	I_{CVDD}	CVDD is used only to bias ESD-protection diodes on CLK input, Figure 2			0		mA
Power Dissipation	P_{DISS}	f_{IN} = 20MHz at -0.5dBFS			759	882	mW

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, external V_{REFIO} = 1.24V, C_{REFIO} = 0.1µF ll 1.0µF, C_{REFP} = 10µF, C_{REFN} = 10µF, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Note 7)						
Data Valid to CLKOUT Rise/Fall	t_{OD}	Figure 5 (Note 8)	$(t_{SAMPLE}/24) - 0.15$		$(t_{SAMPLE}/24) + 0.15$	ns
CLKOUT Output-Width High	t_{CH}	Figure 5		$t_{SAMPLE}/12$		ns
CLKOUT Output-Width Low	t_{CL}	Figure 5		$t_{SAMPLE}/12$		ns
FRAME Rise to CLKOUT Rise	t_{CF}	Figure 4 (Note 8)	$(t_{SAMPLE}/24) - 0.15$		$(t_{SAMPLE}/24) + 0.15$	ns
Sample CLK Rise to FRAME Rise	t_{SF}	Figure 4 (Note 8)	$(t_{SAMPLE}/2) + 1.1$		$(t_{SAMPLE}/2) + 2.6$	ns
Crosstalk		(Note 5)		-75		dB
Gain Matching	C_{GM}	f_{IN} = 5.3MHz (Note 5)		±0.1		dB
Phase Matching	C_{PM}	f_{IN} = 5.3MHz (Note 5)		±0.25		Degrees

Note 2: Specifications at $T_A \geq$ +25°C are guaranteed by production testing. Specifications at $T_A <$ +25°C are guaranteed by design and characterization and not subject to production testing.

Note 3: All capacitances are between the indicated pin and GND, unless otherwise noted.

Note 4: See the *Common-Mode Output (CMOUT)* section.

Note 5: See definition in the *Parameter Definitions* section at the end of this data sheet.

Note 6: Connect REFADJ to GND directly to enable internal reference mode. Connect REFADJ to AVDD directly to disable the internal bandgap reference and enable external reference mode.

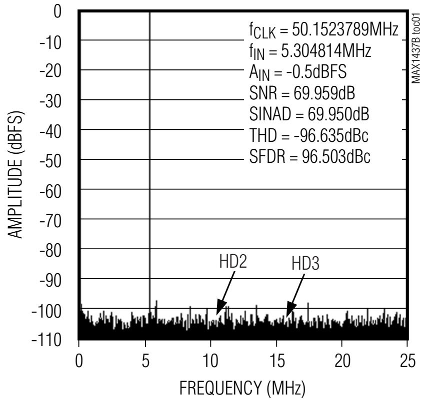
Note 7: Data valid to CLKOUT rise/fall timing is measured from 50% of data output level to 50% of clock output level.

Note 8: Guaranteed by design and characterization. Not subject to production testing.

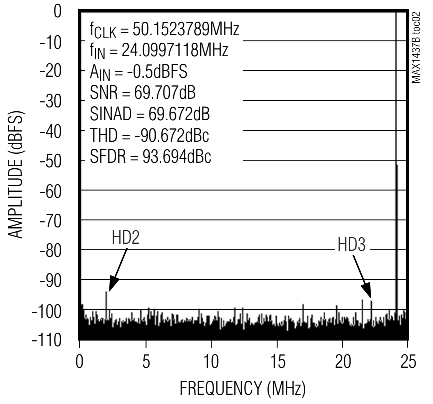
Typical Operating Characteristics

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

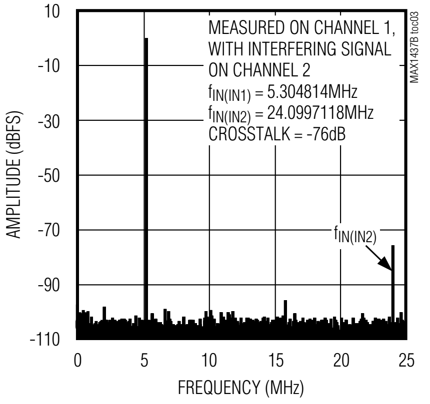
FFT PLOT
(16,384-POINT DATA RECORD)



FFT PLOT
(16,384-POINT DATA RECORD)

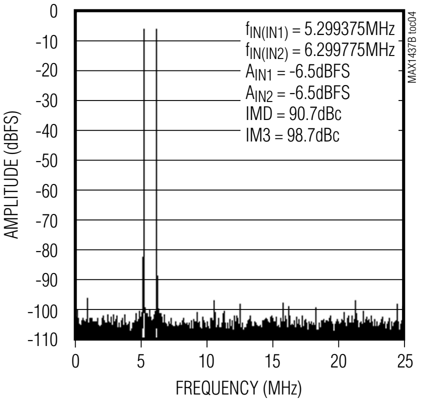


CROSSTALK
(16,384-POINT DATA RECORD)

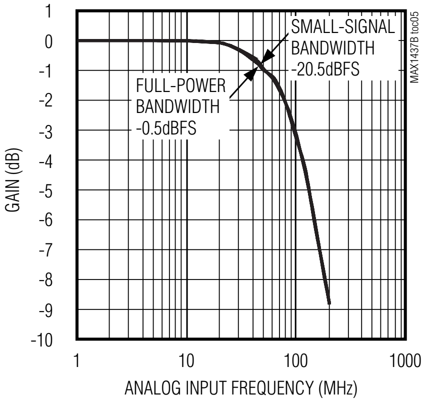


Typical Operating Characteristics (continued)

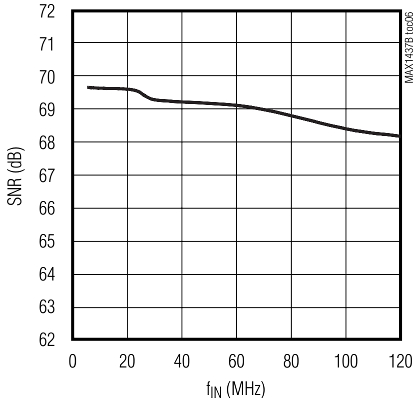
(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)



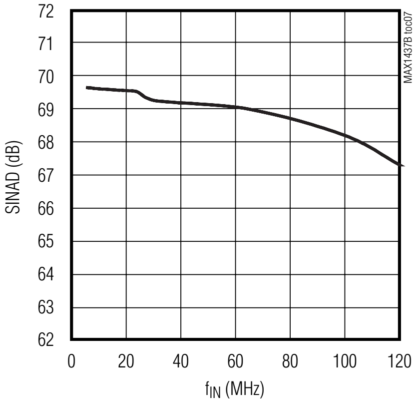
**TWO-TONE INTERMODULATION DISTORTION
(16,384-POINT DATA RECORD)**



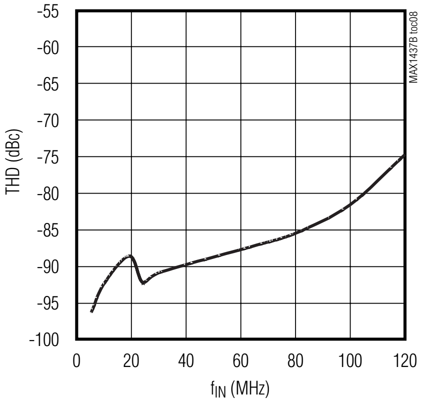
**BANDWIDTH
vs. ANALOG INPUT FREQUENCY**



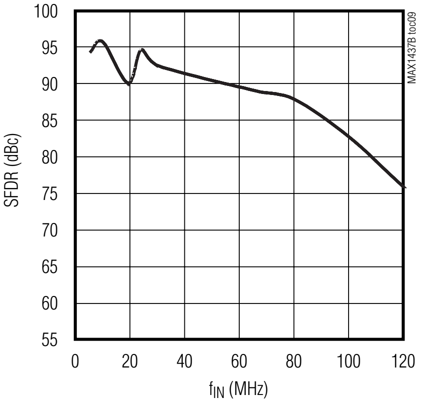
**SIGNAL-TO-NOISE RATIO
vs. ANALOG INPUT FREQUENCY**



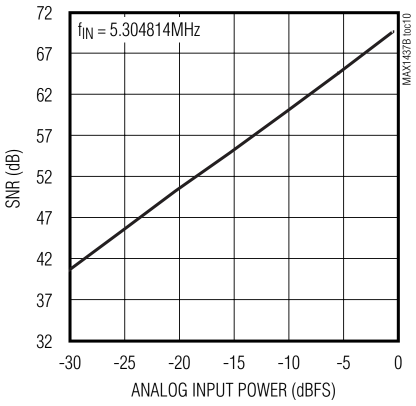
**SIGNAL-TO-NOISE PLUS DISTORTION
vs. ANALOG INPUT FREQUENCY**



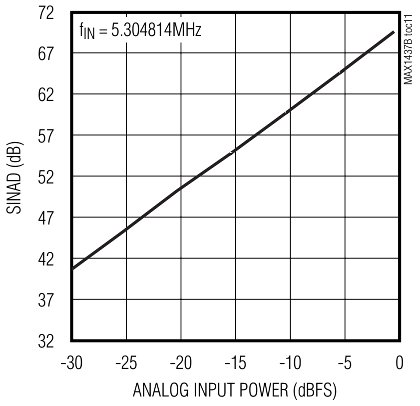
**TOTAL HARMONIC DISTORTION
vs. ANALOG INPUT FREQUENCY**



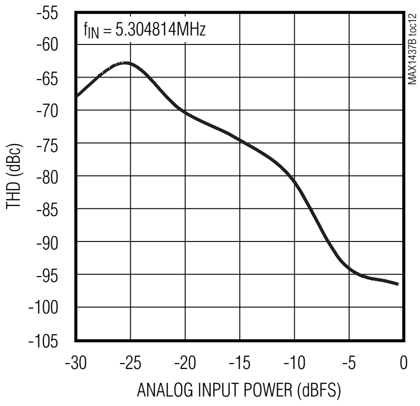
**SPURIOUS-FREE DYNAMIC RANGE
vs. ANALOG INPUT FREQUENCY**



**SIGNAL-TO-NOISE RATIO
vs. ANALOG INPUT POWER**



**SIGNAL-TO-NOISE PLUS DISTORTION
vs. ANALOG INPUT POWER**

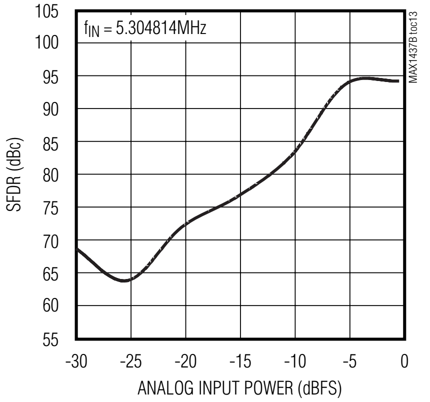


**TOTAL HARMONIC DISTORTION
vs. ANALOG INPUT POWER**

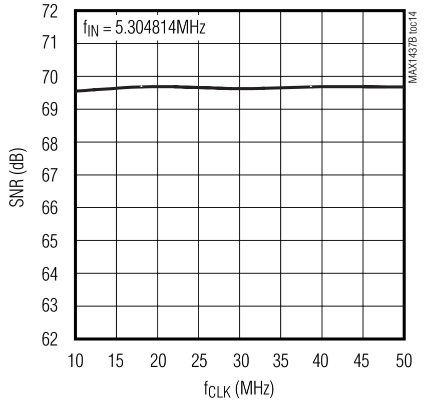
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

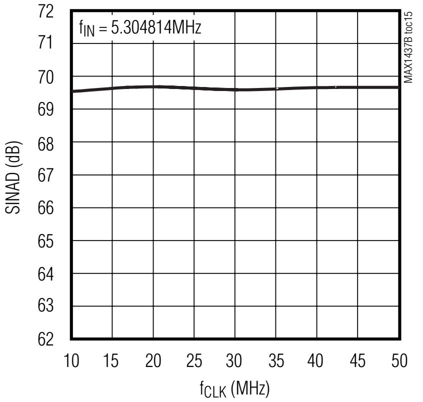
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT POWER



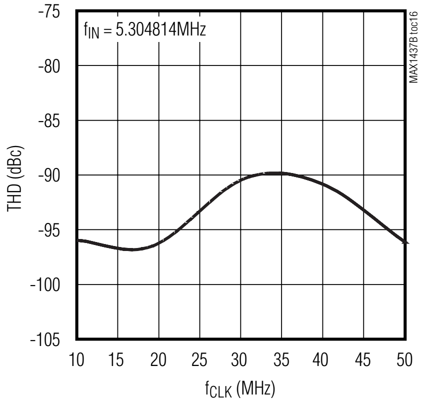
SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



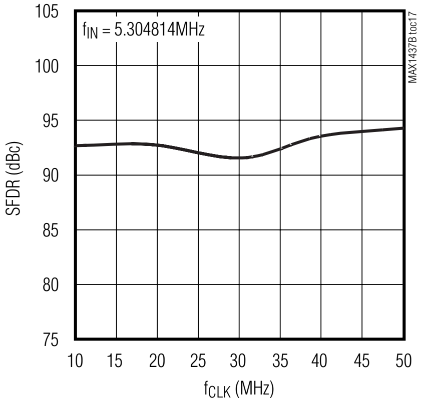
SIGNAL-TO-NOISE PLUS DISTORTION vs. SAMPLING RATE



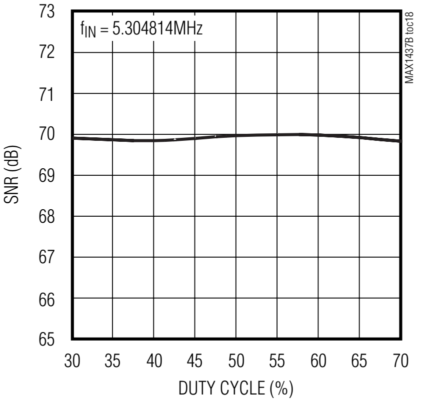
TOTAL HARMONIC DISTORTION vs. SAMPLING RATE



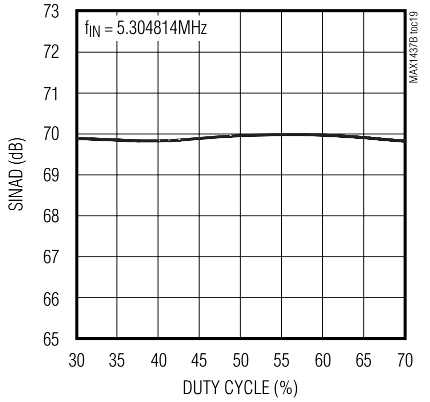
SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



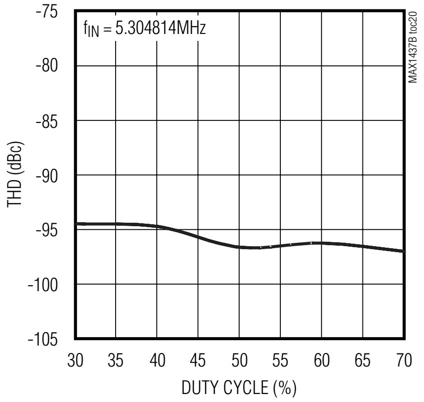
SIGNAL-TO-NOISE RATIO vs. DUTY CYCLE



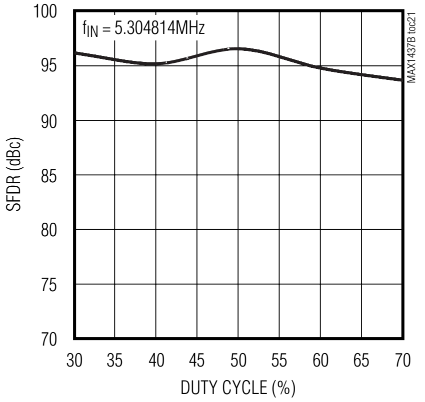
SIGNAL-TO-NOISE PLUS DISTORTION vs. DUTY CYCLE



TOTAL HARMONIC DISTORTION vs. DUTY CYCLE



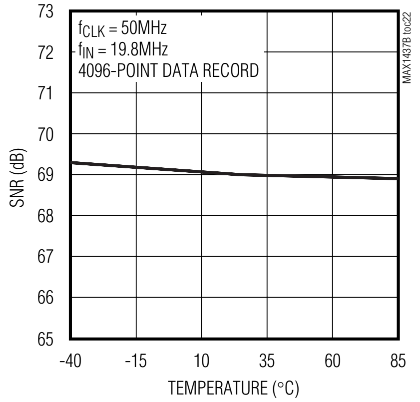
SPURIOUS-FREE DYNAMIC RANGE vs. DUTY CYCLE



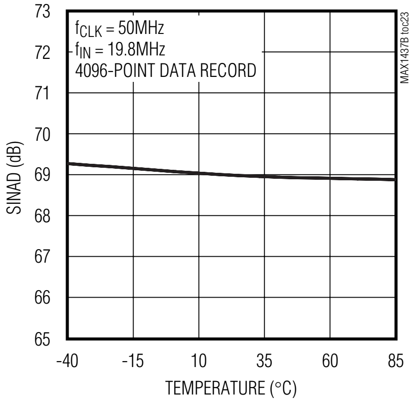
Typical Operating Characteristics (continued)

(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)

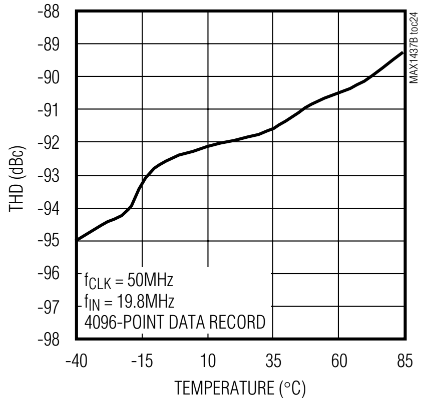
SIGNAL-TO-NOISE RATIO vs. TEMPERATURE



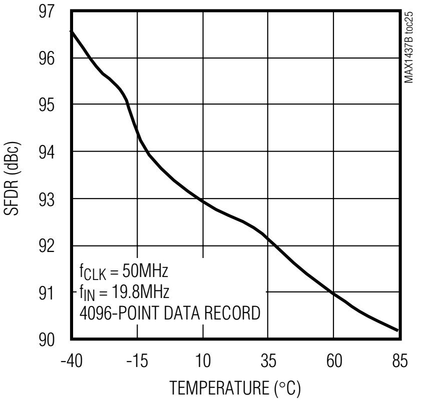
SIGNAL-TO-NOISE PLUS DISTORTION vs. TEMPERATURE



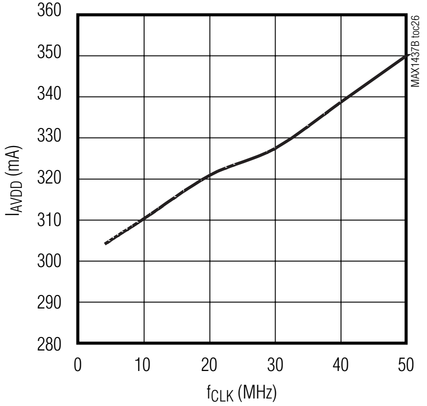
TOTAL HARMONIC DISTORTION vs. TEMPERATURE



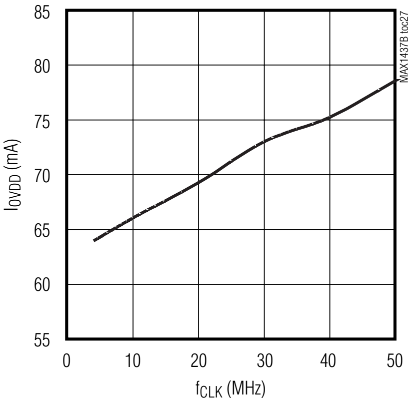
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE



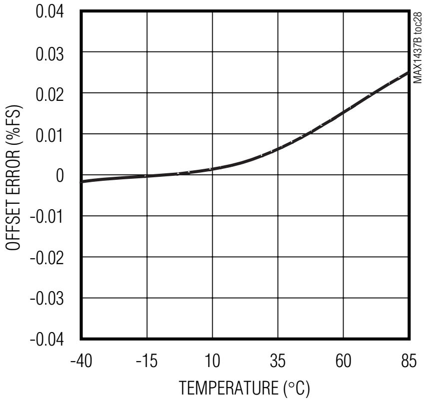
SUPPLY CURRENT vs. SAMPLING RATE (AVDD)



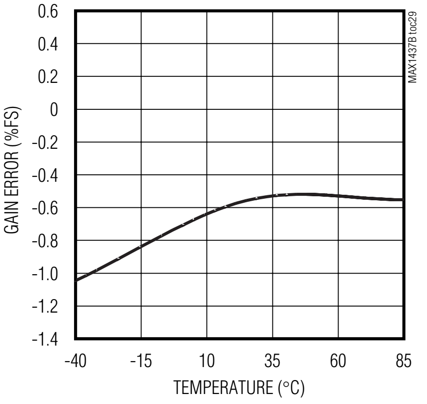
SUPPLY CURRENT vs. SAMPLING RATE (OVDD)



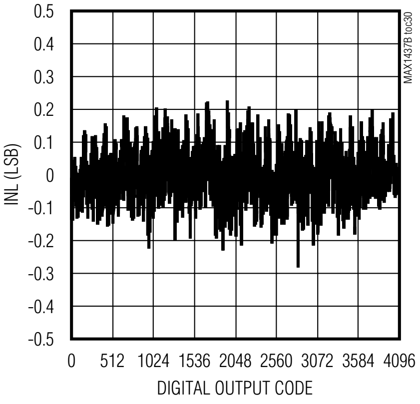
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. TEMPERATURE

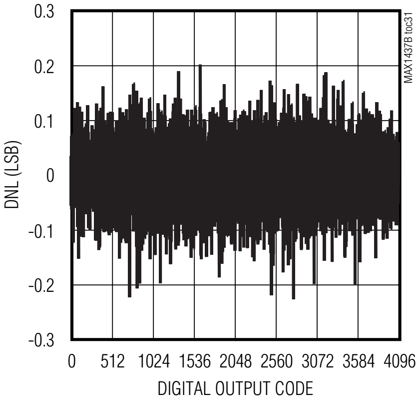


INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE

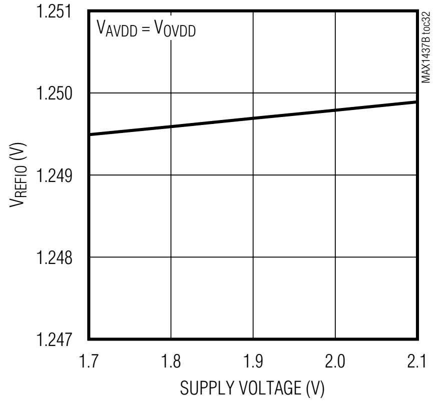


Typical Operating Characteristics (continued)

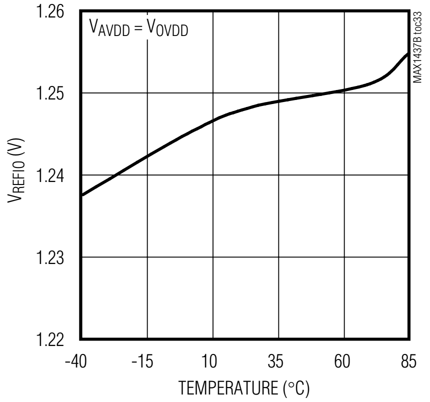
(V_{AVDD} = 1.8V, V_{OVDD} = 1.8V, V_{CVDD} = 3.3V, V_{GND} = 0V, internal reference, differential input at -0.5dBFS, f_{IN} = 5.3MHz, f_{CLK} = 50MHz (50% duty cycle), V_{DT} = 0V, C_{LOAD} = 10pF, T_A = +25°C, unless otherwise noted.)



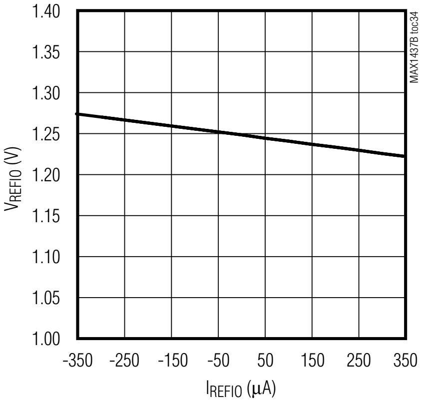
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



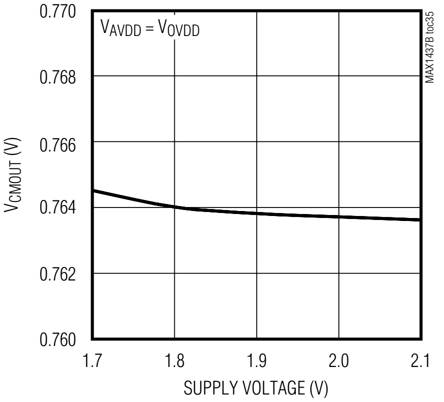
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



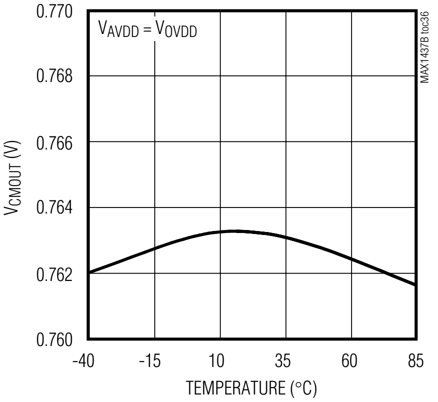
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



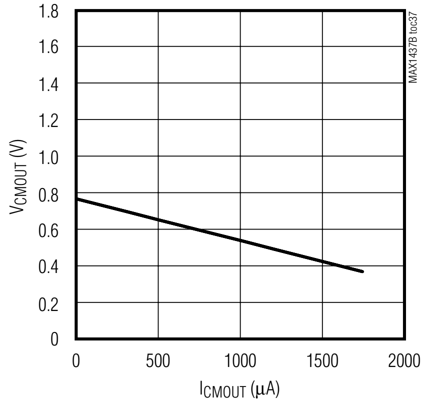
INTERNAL REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



CMOUT VOLTAGE vs. SUPPLY VOLTAGE



CMOUT VOLTAGE vs. TEMPERATURE



CMOUT VOLTAGE vs. LOAD CURRENT

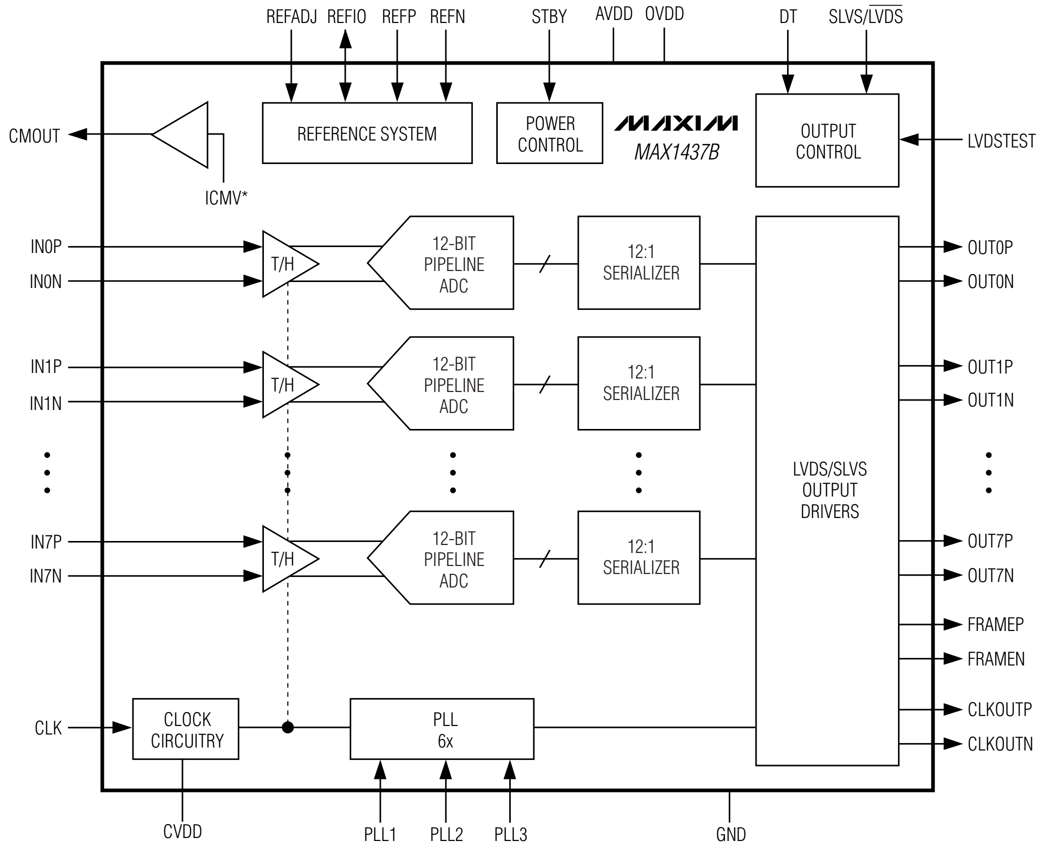
Pin Description

PIN	NAME	FUNCTION
1	IN1P	Channel 1 Positive Input
2	IN1N	Channel 1 Negative Input
3	IN2P	Channel 2 Positive Input
4	IN2N	Channel 2 Negative Input
5	IN3P	Channel 3 Positive Input
6	IN3N	Channel 3 Negative Input
7, 8, 10, 11, 25, 26, 27, 60	AVDD	Analog Power Input. Connect AVDD to a 1.7V to 1.9V power supply. Bypass AVDD to GND with a 0.1µF capacitor as close as possible to the device. Bypass the AVDD power plane to the GND plane with a bulk capacitor of at least 2.2µF. Connect all AVDD pins to the same potential.
9, 18, 68	GND	Ground. Connect all GND pins to the same potential.
12	IN4P	Channel 4 Positive Input
13	IN4N	Channel 4 Negative Input
14	IN5P	Channel 5 Positive Input
15	IN5N	Channel 5 Negative Input
16	IN6P	Channel 6 Positive Input
17	IN6N	Channel 6 Negative Input
19	IN7P	Channel 7 Positive Input
20	IN7N	Channel 7 Negative Input
21	DT	Double Termination Select. Force DT high to select the internal 100Ω termination between the differential output pairs. Force DT low to select no internal output termination.
22	SLVS/$\overline{\text{LVDS}}$	Differential Output Signal Format Select Input. Force SLVS/$\overline{\text{LVDS}}$ high to select SLVS outputs. Force SLVS/$\overline{\text{LVDS}}$ low to select LVDS outputs.
23	CVDD	Clock Power Input. Connect CVDD to a 1.7V to 3.5V power supply. Bypass CVDD to GND with a 0.1µF capacitor in parallel with a capacitor of at least 2.2µF. Install the bypass capacitors as close as possible to the device.
24	CLK	Single-Ended CMOS Clock Input
28, 31, 34, 39, 44, 49, 52	OVDD	Output Driver Power Input. Connect OVDD to a 1.7V to 1.9V power supply. Bypass OVDD to GND with a 0.1µF capacitor as close as possible to the device. Bypass the OVDD power plane to the GND plane with a bulk capacitor of at least 2.2µF. Connect all OVDD pins to the same potential.
29	OUT7N	Channel 7 Negative LVDS/SLVS Output
30	OUT7P	Channel 7 Positive LVDS/SLVS Output
32	OUT6N	Channel 6 Negative LVDS/SLVS Output
33	OUT6P	Channel 6 Positive LVDS/SLVS Output
35	OUT5N	Channel 5 Negative LVDS/SLVS Output
36	OUT5P	Channel 5 Positive LVDS/SLVS Output
37	OUT4N	Channel 4 Negative LVDS/SLVS Output
38	OUT4P	Channel 4 Positive LVDS/SLVS Output
40	FRAMEN	Negative Frame-Alignment LVDS/SLVS Output. A rising edge on the differential FRAME output aligns to a valid D0 in the output data stream.
41	FRAMEP	Positive Frame-Alignment LVDS/SLVS Output. A rising edge on the differential FRAME output aligns to a valid D0 in the output data stream.
42	CLKOUTN	Negative LVDS/SLVS Serial Clock Output

Pin Description (continued)

PIN	NAME	FUNCTION
43	CLKOUTP	Positive LVDS/SLVS Serial Clock Output
45	OUT3N	Channel 3 Negative LVDS/SLVS Output
46	OUT3P	Channel 3 Positive LVDS/SLVS Output
47	OUT2N	Channel 2 Negative LVDS/SLVS Output
48	OUT2P	Channel 2 Positive LVDS/SLVS Output
50	OUT1N	Channel 1 Negative LVDS/SLVS Output
51	OUT1P	Channel 1 Positive LVDS/SLVS Output
53	OUT0N	Channel 0 Negative LVDS/SLVS Output
54	OUT0P	Channel 0 Positive LVDS/SLVS Output
55	LVDSTEST	LVDS Test Pattern Enable. Force LVDSTEST high to enable the output test pattern, 0000 1011 1101. As with the analog conversion results, the test pattern data are output LSB first. Force LVDSTEST low for normal operation.
56	STBY	Standby Input. Force STBY high to put the MAX1437B into standby mode. In standby, the reference circuitry remains active. Force STBY low for normal operation.
57	PLL3	PLL Control Input 3. See Table 1 for details.
58	PLL2	PLL Control Input 2. See Table 1 for details.
59	PLL1	PLL Control Input 1. See Table 1 for details.
61	REFN	Negative Reference Bypass Output. Connect a capacitor of at least 1µF (10µF typ) between REFP and REFN, and connect a capacitor of at least 1µF (10µF typ) between REFN and GND. Place the capacitors as close as possible to the device on the same side of the PCB as the MAX1437B.
62	REFP	Positive Reference Bypass Output. Connect a capacitor of at least 1µF (10µF typ) between REFP and REFN, and connect a capacitor of at least 1µF (10µF typical) between REFN and GND. Place the capacitors as close as possible to the device on the same side of the PCB as the MAX1437B.
63	REFIO	Reference Input/Output. For internal reference operation (REFADJ = GND), the reference output voltage is 1.24V. For external reference operation (REFADJ = AVDD), apply a stable reference voltage at REFIO. Bypass to GND with a capacitor of at least 0.1µF.
64	REFADJ	Internal/External Reference Mode Select and Reference Adjust Input. For internal reference, connect REFADJ to GND. For external reference, connect REFADJ to AVDD. For adjusting the reference, see the *Full-Scale Range Adjustments Using the Internal Reference* section.
65	CMOUT	Common-Mode Reference Voltage Output. CMOUT outputs the input common-mode voltage for DC-coupled applications. Bypass CMOUT to GND with a capacitor of at least 0.1µF.
66	IN0P	Channel 0 Positive Input
67	IN0N	Channel 0 Negative Input
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane for maximum thermal performance. Must be connected to GND.

Functional Diagram



*ICMV = INPUT COMMON-MODE VOLTAGE (INTERNALLY GENERATED).

Detailed Description

The MAX1437B ADC features fully differential inputs, a pipelined architecture, and digital error correction for high-speed signal conversion. The ADC pipeline architecture moves the samples taken at the inputs through the pipeline stages every half clock cycle. The converted digital results are serialized and sent through the LVDS/SLVS output drivers. The total clock-cycle latency from input to output is 6.5 clock cycles.

The MAX1437B offers 8 separate fully differential channels with synchronized inputs and outputs. Global standby minimizes power consumption.

Input Circuit

Figure 1 displays a simplified diagram of the input T/H circuits. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the operational transconductance amplifier (OTA), and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are

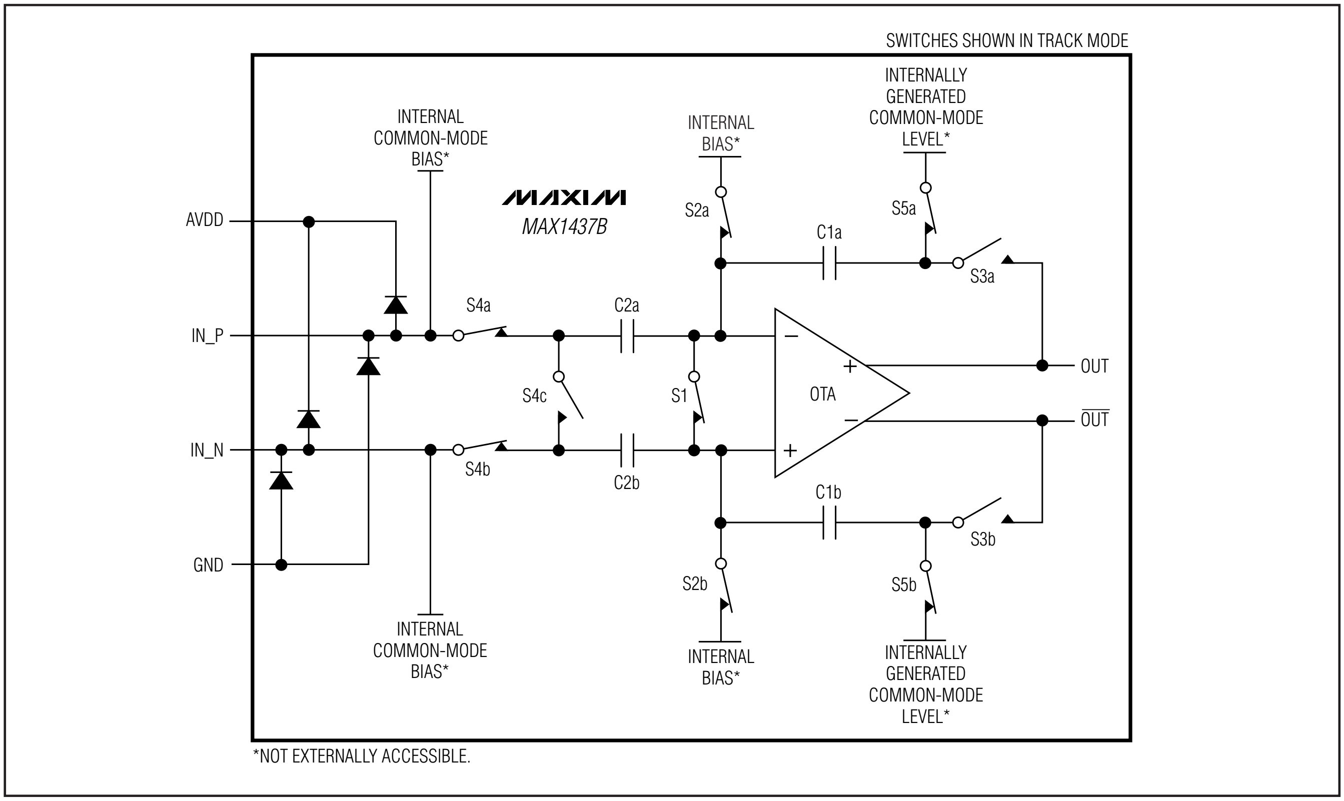


Figure 1. Internal Input Circuit

then presented to the first-stage quantizers and isolate the pipelines from the fast-changing inputs. Analog inputs, IN_P to IN_N, are driven differentially. For differential inputs, balance the input impedance of IN_P and IN_N for optimum performance.

Reference Configurations (REFIO, REFADJ, REFP, and REFN)

The MAX1437B provides an internal 1.24V bandgap reference or can be driven with an external reference voltage. The full-scale analog differential input range is ±FSR. FSR (full-scale range) is given by the following equation:

$$FSR = \frac{(0.700 \times V_{REFIO})}{1.24V}$$

where V_{REFIO} is the voltage at REFIO, generated internally or externally. For a V_{REFIO} = 1.24V, the full-scale input range is ±700mV ($1.4V_{P-P}$).

Internal Reference Mode

Connect REFADJ to GND to use the internal bandgap reference directly. The internal bandgap reference generates V_{REFIO} to be 1.24V with a 120ppm/°C temperature coefficient in internal reference mode. Connect an external ≥ 0.1µF bypass capacitor from REFIO to GND for stability. REFIO sources up to 200µA and sinks up to 200µA for external circuits, and REFIO has a 75mV/mA load regulation. Putting the MAX1437B into standby mode turns off all circuitry except the reference circuit, allowing the converter to power up faster when the ADC exits standby with a high-to-low transitional signal on STBY. The internal circuits of the MAX1437B require 200µs to power up and settle when the converter exits standby mode.

To compensate for gain errors or to decrease or increase the ADC's FSR, add an external resistor between REFADJ and GND or REFADJ and REFIO. This adjusts the internal reference value of the MAX1437B by up to ±5% of its nominal value. See the *Full-Scale Range Adjustments Using the Internal Reference* section.

Connect ≥1µF (10µF typ) capacitors to GND from REFP and REFN and a ≥1µF (10µF typ) capacitor between REFP and REFN as close to the device as possible on the same side of the PCB.

External Reference Mode

The external reference mode allows for more control over the MAX1437B reference voltage and allows multiple converters to use a common reference. Connect REFADJ to AVDD to disable the internal reference. Apply a stable 1.18V to 1.30V source at REFIO. Bypass REFIO to GND with a ≥ 0.1µF capacitor. The REFIO input impedance is >1MΩ.

Clock Input (CLK)

The MAX1437B accepts a CMOS-compatible clock signal with a wide 20% to 80% input clock duty cycle. Drive CLK with an external single-ended clock signal. Figure 2 shows the simplified clock input diagram.

Low clock jitter is required for the specified SNR performance of the MAX1437B. Analog input sampling occurs on the rising edge of CLK, requiring this edge to provide the lowest possible jitter. Jitter limits the maximum SNR performance of any ADC according to the following relationship:

$$\mathrm{SNR} = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_J}\right)$$

where f_{IN} represents the analog input frequency and t_J is the total system clock jitter.

PLL Inputs (PLL1, PLL2, PLL3)

The MAX1437B features a PLL that generates an output clock signal with six times the frequency of the input clock. The output clock signal is used to clock data out of the MAX1437B (see the *System Timing Requirements* section). Set the PLL1, PLL2, and PLL3 pins according to the input clock range provided in Table 1.

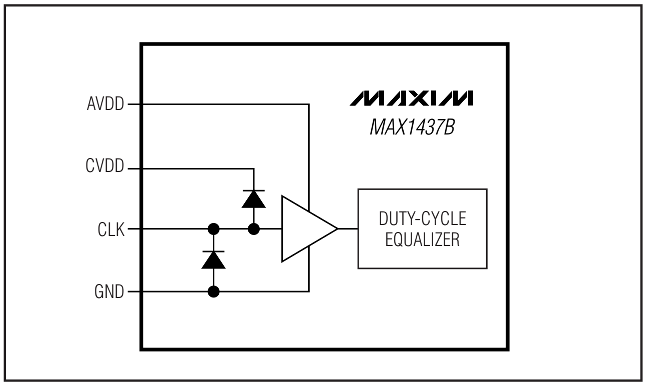


Figure 2. Clock Input Circuitry

Table 1. PLL1, PLL2, and PLL3 Configuration Table

PLL1	PLL2	PLL3	INPUT CLOCK RANGE (MHz)	
			MIN	MAX
0	0	0	45.0	50.0
0	0	1	32.5	45.0
0	1	0	22.5	32.5
0	1	1	16.3	22.5
1	0	0	11.3	16.3
1	0	1	8.1	11.3
1	1	0	5.6	8.1
1	1	1	4.0	5.6

System Timing Requirements

Figure 3 shows the relationship between the analog inputs, input clock, frame-alignment output, serial-clock output, and serial-data output. The differential analog input (IN_P and IN_N) is sampled on the rising edge of the CLK signal and the resulting data appears at the digital outputs 6.5 clock cycles later. Figure 4 provides a detailed, two-conversion timing diagram of the relationship between the inputs and the outputs.

Clock Output (CLKOUTP, CLKOUTN)

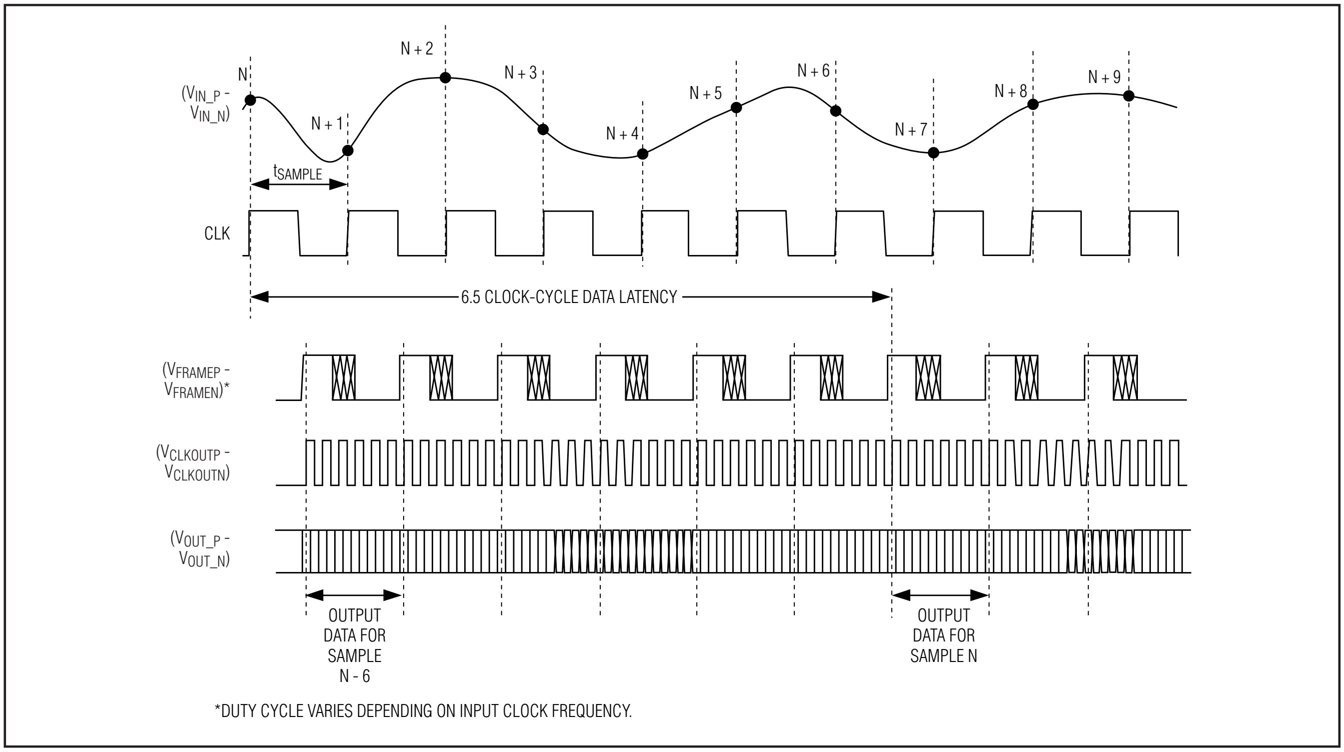
The MAX1437B provides a differential clock output that consists of CLKOUTP and CLKOUTN. As shown in Figure 4, the serial output data is clocked out of the MAX1437B on both edges of the clock output. The frequency of the output clock is six times the frequency of CLK.

Frame-Alignment Output (FRAMEP, FRAMEN)

The MAX1437B provides a differential frame-alignment signal that consists of FRAMEP and FRAMEN. As shown in Figure 4, the rising edge of the frame-alignment signal corresponds to the first bit (D0) of the 12-bit serial data stream. The frequency of the frame-alignment signal is identical to the frequency of the input clock.

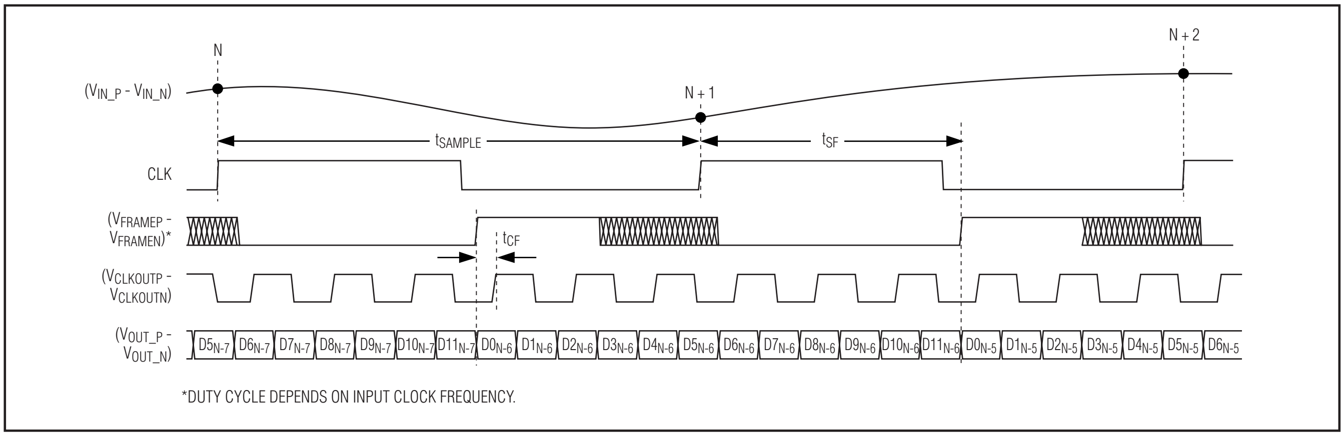
Serial Output Data (OUT_P, OUT_N)

The MAX1437B provides its conversion results through individual differential outputs consisting of OUT_P and OUT_N. The results are valid 6.5 input clock cycles after the sample is taken. As shown in Figure 3, the output data is clocked out on both edges of the output clock, LSB (D0) first. Figure 5 provides the detailed serial-output timing diagram.



*DUTY CYCLE VARIES DEPENDING ON INPUT CLOCK FREQUENCY.

Figure 3. Global Timing Diagram



*DUTY CYCLE DEPENDS ON INPUT CLOCK FREQUENCY.

Figure 4. Detailed Two-Conversion Timing Diagram

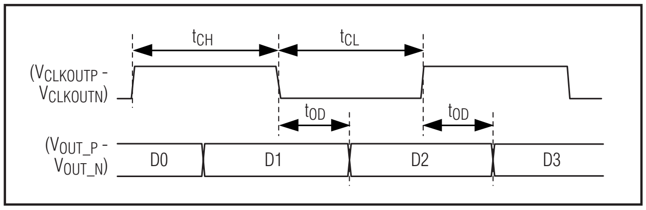


Figure 5. Serialized-Output Detailed Timing Diagram

Table 2. Output Code Table (V_{REFIO} = 1.24V)

TWO'S-COMPLEMENT DIGITAL OUTPUT CODE			V_{IN_P} - V_{IN_N} (mV) (V_{REFIO} = 1.24V)
BINARY D11 → D0	**HEXADECIMAL EQUIVALENT OF D11 → D0**	**DECIMAL EQUIVALENT OF D11 → D0**	
0111 1111 1111	0x7FF	+2047	+699.66
0111 1111 1110	0x7FE	+2046	+699.32
0000 0000 0001	0x001	+1	+0.34
0000 0000 0000	0x000	0	0
1111 1111 1111	0xFFF	-1	-0.34
1000 0000 0001	0x801	-2047	-699.66
1000 0000 0000	0x800	-2048	-700.00

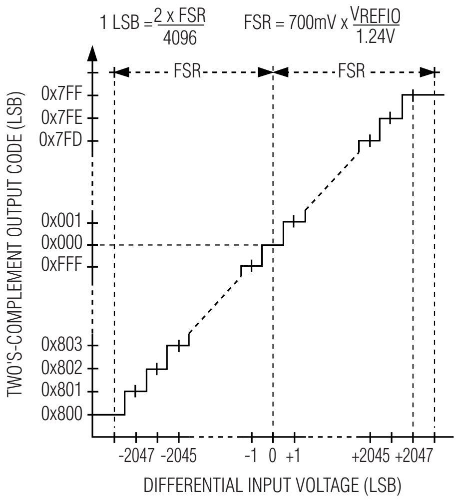


Figure 6. Two's-Complement Transfer Function

Output Data Transfer Function

The MAX1437B output data format is two's complement. The following equation, Table 2, and Figure 6 define the relationship between the digital output and the analog input:

$$V_{IN\_P} - V_{IN\_N} = FSR \times 2 \times \frac{CODE_{10}}{4096}$$

where $CODE_{10}$ is the decimal equivalent of the digital output code as shown in Table 2.

Keep the capacitive load on the MAX1437B digital outputs as low as possible.

LVDS and SLVS Selection (SLVS/$\overline{\text{LVDS}}$)

Drive SLVS/$\overline{\text{LVDS}}$ low for LVDS or drive SLVS/$\overline{\text{LVDS}}$ high for SLVS levels at the MAX1437B outputs (OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, and FRAMEN). For SLVS levels, enable double-termination by driving DT high. See the *Electrical Characteristics* table for LVDS and SLVS output voltage levels.

LVDS Test Pattern (LVDSTEST)

Drive LVDSTEST high to enable the output test pattern on all LVDS or SLVS output channels. The output test pattern is 0000 1011 1101. Drive LVDSTEST low for normal operation (test pattern disabled).

Common-Mode Output (CMOUT)

CMOUT provides a common-mode reference for DC-coupled analog inputs. If the input is DC-coupled, match the output common-mode voltage of the circuit driving the MAX1437B to the output voltage at V_{CMOUT} to within ±50mV. It is recommended that the output common-mode voltage of the driving circuit be derived from CMOUT.

Double Termination (DT)

The MAX1437B offers an optional, internal 100Ω termination between the differential output pairs (OUT_P and OUT_N, CLKOUTP and CLKOUTN, FRAMEP and FRAMEN). In addition to the termination at the end of the line, a second termination directly at the outputs helps eliminate unwanted reflections down the line. This feature is useful in applications where trace lengths are long (> 5in) or with mismatched impedance. Drive DT high to select double-termination, or drive DT low to disconnect the internal termination resistor (single-termination). Selecting double-termination increases the OVDD supply current (see Figure 7).

Standby Mode

The MAX1437B offers a standby mode to efficiently use power by transitioning to a low-power state when conversions are not required. STBY controls the standby mode of all channels and the internal reference circuitry. The reference does not power down in standby mode. Drive STBY high to enable standby. In standby mode, the output impedance of all of the LVDS/SLVS outputs is approximately 342Ω, if DT is low. The output impedance of the differential LVDS/SLVS outputs is 100Ω when DT is high. See the *Electrical Characteristics* table for typical supply currents during standby. The following list shows the state of the analog inputs and digital outputs in standby mode:

- IN_P, IN_N analog inputs are disconnected from the internal input amplifier
- Reference circuit remains active
- OUT_P, OUT_N, CLKOUTP, CLKOUTN, FRAMEP, and FRAMEN have approximately 342Ω between the output pairs when DT is low. When DT is high, the differential output pairs have 100Ω between each pair.

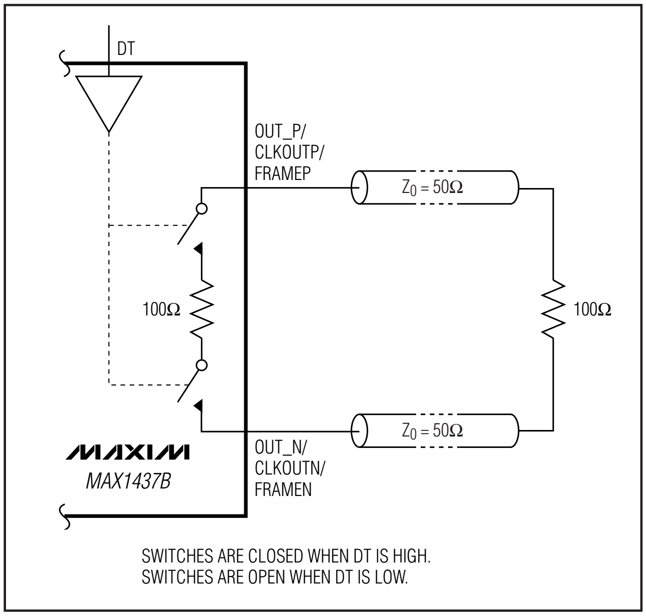


Figure 7. Double Termination

When operating in internal reference mode, the MAX1437B requires 200µs to power up and settle when the converter exits standby mode. To exit standby mode, STBY, the applied control signal must transition from high to low. When using an external reference, the wake-up time is dependent on the external reference drivers.

Applications Information

Full-Scale Range Adjustments Using the Internal Reference

The MAX1437B supports a full-scale adjustment range of 10% (±5%). To decrease the full-scale range, add a 25kΩ to 250kΩ external resistor or potentiometer (R_{ADJ}) between REFADJ and GND. To increase the full-scale range, add a 25kΩ to 250kΩ resistor between REFADJ and REFIO. Figure 8 shows the two possible configurations.

The following equations provide the relationship between R_{ADJ} and the change in the analog full-scale range:

$$FSR = 0.7V\left(1 + \frac{1.25k\Omega}{R_{ADJ}}\right)$$

for R_{ADJ} connected between REFADJ and REFIO, and:

$$FSR = 0.7V\left(1 - \frac{1.25k\Omega}{R_{ADJ}}\right)$$

for R_{ADJ} connected between REFADJ and GND.

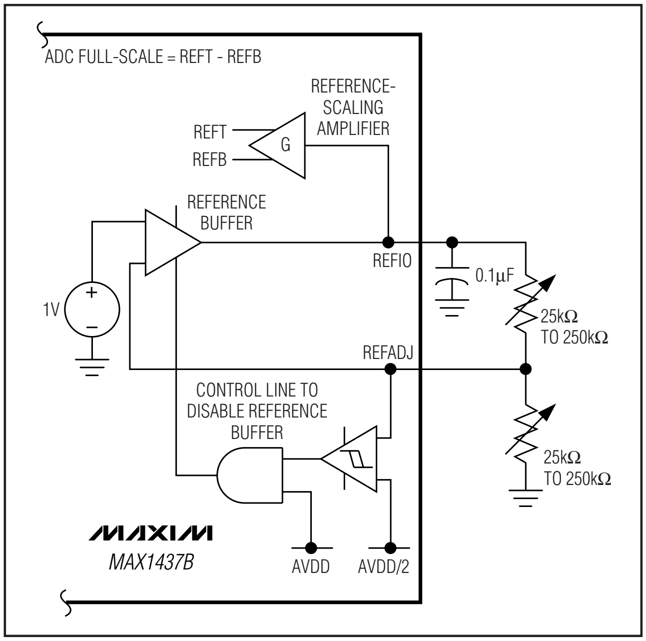


Figure 8. Circuit Suggestions to Adjust the ADC's Full-Scale Range

Using Transformer Coupling

An RF transformer (Figure 9) provides an excellent solution to convert a single-ended input source signal to a fully differential signal. The MAX1437B input common-mode voltage is internally biased to 0.76V (typ) with f_{CLK} = 50MHz. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion.

Grounding, Bypassing, and Board Layout

The MAX1437B requires high-speed board layout design techniques. Refer to the MAX1437B EV kit data sheet for a board layout reference. Locate all bypass capacitors as close as possible to the device, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass AVDD to GND with a 0.1μF ceramic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass OVDD to GND with a 0.1μF ceramic capacitor in parallel with a ≥ 2.2μF ceramic capacitor. Bypass CVDD to GND with a 0.1μF ceramic capacitor in parallel with a ≥ 2.2μF ceramic capacitor.

Multilayer boards with ample ground and power planes produce the highest level of signal integrity. Connect the MAX1437B ground pins and the exposed backside pad to the same ground plane. The MAX1437B relies on the exposed-backside-pad connection for a low-inductance ground connection. Isolate the ground plane from any noisy digital system ground planes.

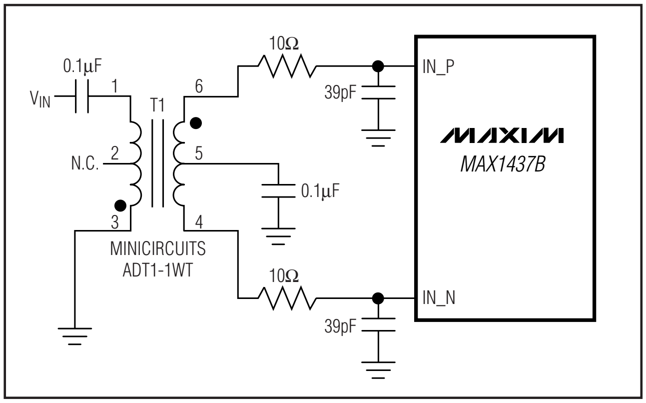


Figure 9. Transformer-Coupled Input Drive

Route high-speed digital signal traces away from the sensitive analog traces. Keep all signal lines short and free of 90° turns.

Ensure that the differential analog input network layout is symmetric and that all parasitics are balanced equally. Refer to the MAX1437B EV kit data sheet for an example of symmetric input layout.

Parameter Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For the MAX1437B, this straight line is between the end points of the transfer function, once offset and gain errors have been nullified. INL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* table.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. For the MAX1437B, DNL deviations are measured at every step and the worst-case deviation is reported in the *Electrical Characteristics* table.

Offset Error

Offset error is a figure of merit that indicates how well the actual transfer function matches the ideal transfer function at a single point. For the MAX1437B, the ideal midscale digital output transition occurs when there is -1/2 LSBs across the analog inputs (Figure 6). Bipolar offset error is the amount of deviation between the measured midscale transition point and the ideal midscale transition point.

Gain Error

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. For the MAX1437B, the gain error is the difference of the measured full-scale and zero-scale transition points minus the difference of the ideal full-scale and zero-scale transition points.

For the bipolar device (MAX1437B), the full-scale transition point is from 0x7FE to 0x7FF and the zero-scale transition point is from 0x800 to 0x801.

Crosstalk

Crosstalk indicates how well each analog input is isolated from the others. For the MAX1437B, a 5.3MHz, -0.5dBFS analog signal is applied to 1 channel while a 24.1MHz, -0.5dBFS analog signal is applied to another channel. An FFT is taken on the channel with the 5.3MHz analog signal. From this FFT, the crosstalk is measured as the difference in the 5.3MHz and 24.1MHz amplitudes.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken. See Figure 10.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the aperture delay. See Figure 10.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc.

For the MAX1437B, SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first six harmonics (HD2–HD7), and the DC offset.

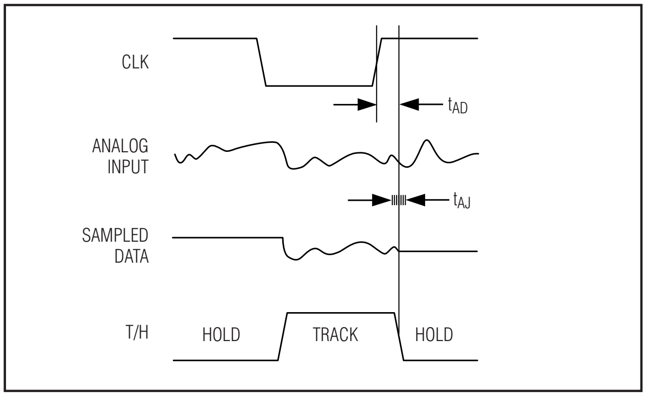


Figure 10. Aperture Jitter/Delay Specifications

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency, excluding the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \left(\frac{SINAD - 1.76}{6.02} \right)$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first six harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{{V_2}^2 + {V_3}^2 + {V_4}^2 + {V_5}^2 + {V_6}^2 + {V_7}^2}}{V_1} \right)$$

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Intermodulation Distortion (IMD)

IMD is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones f_1 and f_2. The individual input tone levels are at -6.5dBFS. The intermodulation products are as follows:

- 2nd-order intermodulation products (IM2): $f_1 + f_2$, $f_2 - f_1$
- 3rd-order intermodulation products (IM3): $2 \times f_1 - f_2$, $2 \times f_2 - f_1$, $2 \times f_1 + f_2$, $2 \times f_2 + f_1$
- 4th-order intermodulation products (IM4): $3 \times f_1 - f_2$, $3 \times f_2 - f_1$, $3 \times f_1 + f_2$, $3 \times f_2 + f_1$
- 5th-order intermodulation products (IM5): $3 \times f_1 - 2 \times f_2$, $3 \times f_2 - 2 \times f_1$, $3 \times f_1 + 2 \times f_2$, $3 \times f_2 + 2 \times f_1$

Third-Order Intermodulation (IM3)

IM3 is the total power of the 3rd-order intermodulation product to the Nyquist frequency relative to the total input power of the two input tones f_1 and f_2. The individual input tone levels are at -6.5dBFS. The 3rd-order intermodulation products are $2 \times f_1 - f_2$, $2 \times f_2 - f_1$, $2 \times f_1 + f_2$, $2 \times f_2 + f_1$.

Small-Signal Bandwidth

A small -20.5dBFS analog input signal is applied to an ADC so that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

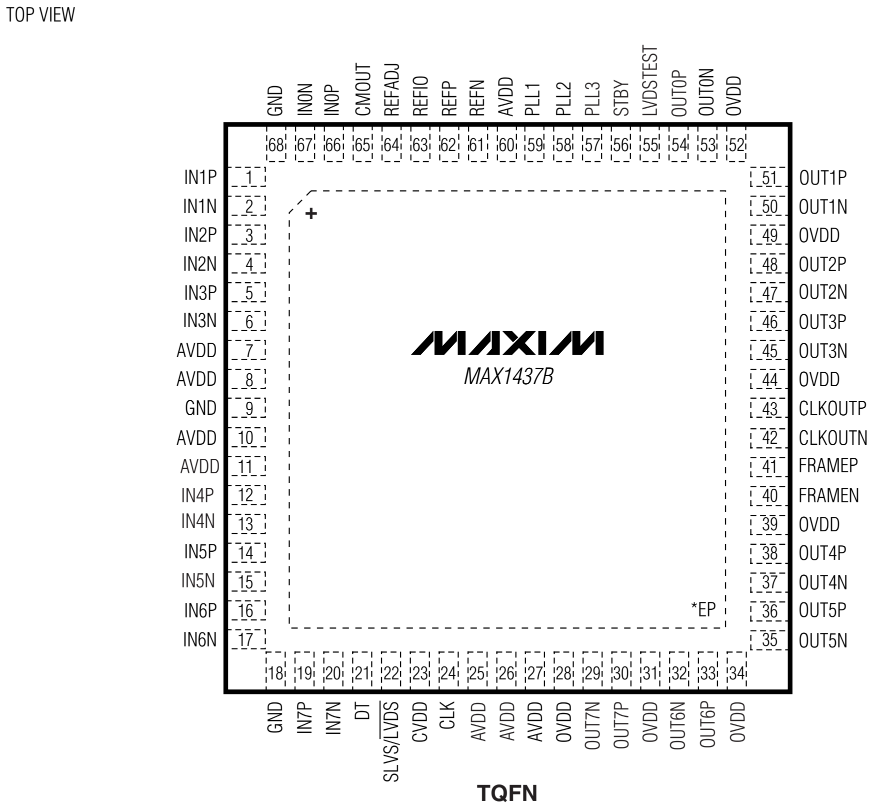
Gain Matching

Gain matching is a figure of merit that indicates how well the gain of all 8 ADC channels is matched to each other. For the MAX1437B, gain matching is measured by applying the same 5.3MHz, -0.5dBFS analog signal to all analog input channels. These analog inputs are sampled at 50Msps and the maximum deviation in amplitude is reported in dB as gain matching in the *Electrical Characteristics* table.

Phase Matching

Phase matching is a figure of merit that indicates how well the phases of all 8 ADC channels are matched to each other. For the MAX1437B, phase matching is measured by applying the same 5.3MHz, -0.5dBFS analog signal to all analog input channels. These analog inputs are sampled at 50Msps and the maximum deviation in phase is reported in degrees as phase matching in the *Electrical Characteristics* table.

Pin Configuration



TQFN
10mm x 10mm x 0.8mm

*CONNECT EP TO GND.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
68 TQFN	T6800+4	**21-0142**	**90-0101**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	12/08	Corrected errors in the *Internal Reference Mode* and *Gain Error* sections.	13, 19
2	2/11	Added new *Package Thermal Characteristics* section and fixed errors in EC table	2–5

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