

## 74AC191

### Up/Down Counter with Preset and Ripple Clock

#### General Description

The AC191 is a reversible modulo 16 binary counter. It features synchronous counting and asynchronous presetting. The preset feature allows the AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

#### Features

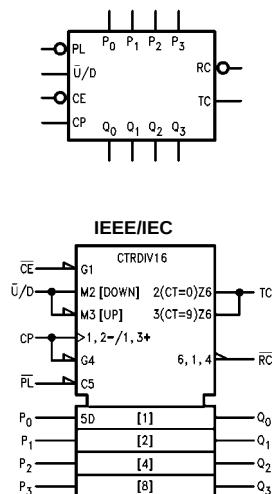
- $I_{CC}$  reduced by 50%
- High speed—133 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable
- Outputs source/sink 24 mA

#### Ordering Code:

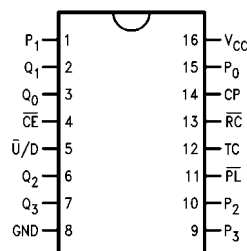
| Order Number | Package Number | Package Description                                                               |
|--------------|----------------|-----------------------------------------------------------------------------------|
| 74AC191SC    | M16A           | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74AC191SJ    | M16D           | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide                     |
| 74AC191MTC   | MTC16          | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide       |
| 74AC191PC    | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide            |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



#### Pin Descriptions

| Pin Names        | Description                      |
|------------------|----------------------------------|
| $\overline{CE}$  | Count Enable Input               |
| CP               | Clock Pulse Input                |
| $P_0$ – $P_3$    | Parallel Data Inputs             |
| $\overline{PL}$  | Asynchronous Parallel Load Input |
| $\overline{U/D}$ | Up/Down Count Control Input      |
| $Q_0$ – $Q_3$    | Flip-Flop Outputs                |
| RC               | Ripple Clock Output              |
| TC               | Terminal Count Output            |

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## RC Truth Table

| Inputs |    |                |                                                                                   | Outputs                                                                           |
|--------|----|----------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| PL     | CE | TC<br>(Note 1) | CP                                                                                | RC                                                                                |
| H      | L  | H              |  |  |
| H      | H  | X              | X                                                                                 | H                                                                                 |
| H      | X  | L              | X                                                                                 | H                                                                                 |
| L      | X  | X              | X                                                                                 | H                                                                                 |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 = LOW-to-HIGH Transition  
 = Clock Pulse

**Note 1:** TC is generated internally

## Functional Description

The AC191 is a synchronous up/down counter. The AC191 is organized as a 4-bit binary counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Load inputs (P<sub>0</sub>–P<sub>3</sub>) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the CE input inhibits counting. When CE is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the U/D input signal, as indicated in the Mode Select Table. CE and U/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 15 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until U/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, RC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figure 1 and Figure 2. In Figure 1, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure 2. All clock inputs are driven in parallel and the RC outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to

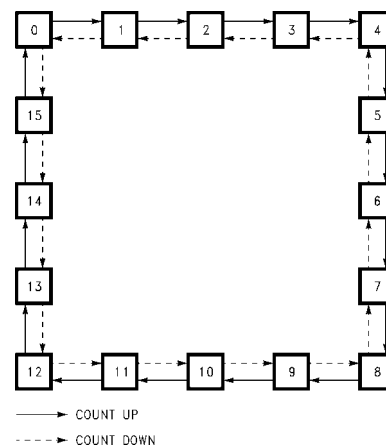
ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the RC output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure 3 avoids ripple delays and their associated restrictions. The CE input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figure 1 and Figure 2 doesn't apply, because the TC output of a given stage is not affected by its own CE.

## Mode Select Table

| Inputs |    |     |                                                                                     | Mode             |
|--------|----|-----|-------------------------------------------------------------------------------------|------------------|
| PL     | CE | U/D | CP                                                                                  |                  |
| H      | L  | L   |  | Count Up         |
| H      | L  | H   |  | Count Down       |
| L      | X  | X   | X                                                                                   | Preset (Asyn.)   |
| H      | H  | X   | X                                                                                   | No Change (Hold) |

## State Diagram



## Functional Description (continued)

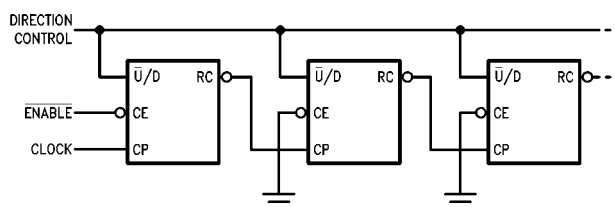


FIGURE 1. N-Stage Counter Using Ripple Clock

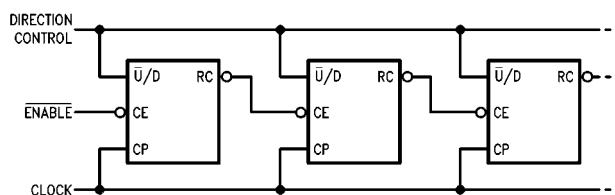


FIGURE 2. Synchronous N-Stage Counter Using Ripple Carry/Borrow

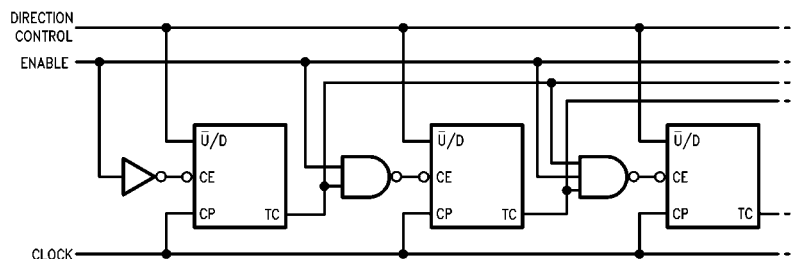
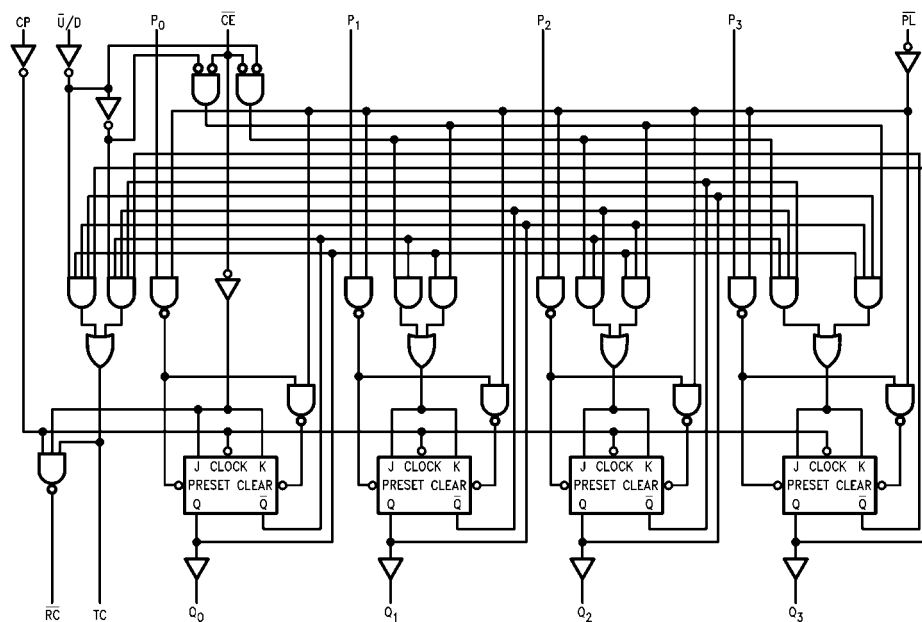


FIGURE 3. Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 2)

|                                                                           |                          |
|---------------------------------------------------------------------------|--------------------------|
| Supply Voltage ( $V_{CC}$ )                                               | -0.5V to +7.0V           |
| DC Input Diode Current ( $I_{IK}$ )                                       |                          |
| $V_I = -0.5V$                                                             | -20 mA                   |
| $V_I = V_{CC} + 0.5V$                                                     | +20 mA                   |
| DC Input Voltage ( $V_I$ )                                                | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current ( $I_{OK}$ )                                      |                          |
| $V_O = -0.5V$                                                             | -20 mA                   |
| $V_O = V_{CC} + 0.5V$                                                     | +20 mA                   |
| DC Output Voltage ( $V_O$ )                                               | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source<br>or Sink Current ( $I_O$ )                             | ±50 mA                   |
| DC $V_{CC}$ or Ground Current<br>per Output Pin ( $I_{CC}$ or $I_{GND}$ ) | ±50 mA                   |
| Storage Temperature ( $T_{STG}$ )                                         | -65°C to +150°C          |
| Junction Temperature ( $T_J$ )                                            |                          |
| PDIP                                                                      | 140°C                    |

**Recommended Operating Conditions**

|                                                 |                |
|-------------------------------------------------|----------------|
| Supply Voltage ( $V_{CC}$ )                     | 2.0V to 6.0V   |
| Input Voltage ( $V_I$ )                         | 0V to $V_{CC}$ |
| Output Voltage ( $V_O$ )                        | 0V to $V_{CC}$ |
| Operating Temperature ( $T_A$ )                 | -40°C to +85°C |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                |
| $V_{IN}$ from 30% to 70% of $V_{CC}$            |                |
| $V_{CC}$ @ 3.3V 4.5V, 5.5V                      | 125 mV/ns      |

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

| Symbol                      | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |                   | T <sub>A</sub> = −40°C to +85°C | Units | Conditions                                                                                                                                        |
|-----------------------------|--------------------------------------|------------------------|------------------------|-------------------|---------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|                             |                                      |                        | Typ                    | Guaranteed Limits |                                 |       |                                                                                                                                                   |
| V <sub>IH</sub>             | Minimum HIGH Level<br>Input Voltage  | 3.0                    | 1.5                    | 2.1               | 2.1                             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> − 0.1V                                                                                              |
|                             |                                      | 4.5                    | 2.25                   | 3.15              | 3.15                            |       |                                                                                                                                                   |
|                             |                                      | 5.5                    | 2.75                   | 3.85              | 3.85                            |       |                                                                                                                                                   |
| V <sub>IL</sub>             | Maximum LOW Level<br>Input Voltage   | 3.0                    | 1.5                    | 0.9               | 0.9                             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> − 0.1V                                                                                              |
|                             |                                      | 4.5                    | 2.25                   | 1.35              | 1.35                            |       |                                                                                                                                                   |
|                             |                                      | 5.5                    | 2.75                   | 1.65              | 1.65                            |       |                                                                                                                                                   |
| V <sub>OH</sub>             | Minimum HIGH Level<br>Output Voltage | 3.0                    | 2.99                   | 2.9               | 2.9                             | V     | I <sub>OUT</sub> = −50 μA                                                                                                                         |
|                             |                                      | 4.5                    | 4.49                   | 4.4               | 4.4                             |       |                                                                                                                                                   |
|                             |                                      | 5.5                    | 5.49                   | 5.4               | 5.4                             |       |                                                                                                                                                   |
|                             |                                      | 3.0                    |                        | 2.56              | 2.46                            | V     | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OH</sub> = −12 mA<br>I <sub>OH</sub> = −24 mA<br>I <sub>OH</sub> = −24 mA (Note 3) |
|                             |                                      | 4.5                    |                        | 3.86              | 3.76                            |       |                                                                                                                                                   |
|                             |                                      | 5.5                    |                        | 4.86              | 4.76                            |       |                                                                                                                                                   |
| V <sub>OL</sub>             | Maximum LOW Level<br>Output Voltage  | 3.0                    | 0.002                  | 0.1               | 0.1                             | V     | I <sub>OUT</sub> = 50 μA                                                                                                                          |
|                             |                                      | 4.5                    | 0.001                  | 0.1               | 0.1                             |       |                                                                                                                                                   |
|                             |                                      | 5.5                    | 0.001                  | 0.1               | 0.1                             |       |                                                                                                                                                   |
|                             |                                      | 3.0                    |                        | 0.36              | 0.44                            | V     | V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OL</sub> = 12 mA<br>I <sub>OL</sub> = 24 mA<br>I <sub>OL</sub> = 24 mA (Note 3)    |
|                             |                                      | 4.5                    |                        | 0.36              | 0.44                            |       |                                                                                                                                                   |
|                             |                                      | 5.5                    |                        | 0.36              | 0.44                            |       |                                                                                                                                                   |
| I <sub>IN</sub><br>(Note 5) | Maximum Input<br>Leakage Current     | 5.5                    |                        | ±0.1              | ±1.0                            | μA    | V <sub>I</sub> = V <sub>CC</sub> , GND                                                                                                            |
| I <sub>OLD</sub>            | Minimum Dynamic                      | 5.5                    |                        |                   | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max                                                                                                                      |
| I <sub>OHD</sub>            | Output Current (Note 4)              | 5.5                    |                        |                   | −75                             | mA    | V <sub>OHD</sub> = 3.85V Min                                                                                                                      |
| I <sub>CC</sub><br>(Note 5) | Maximum Quiescent<br>Supply Current  | 5.5                    |                        | 4.0               | 40.0                            | μA    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND                                                                                                       |

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

| AC Electrical Characteristics                                                       |                                                          |                                    |                                                  |             |              |                                                           |              |       |
|-------------------------------------------------------------------------------------|----------------------------------------------------------|------------------------------------|--------------------------------------------------|-------------|--------------|-----------------------------------------------------------|--------------|-------|
| Symbol                                                                              | Parameter                                                | V <sub>CC</sub><br>(V)<br>(Note 6) | C <sub>L</sub> = 50 pF<br>T <sub>A</sub> = +25°C |             |              | T <sub>A</sub> = −40°C to +85°C<br>C <sub>L</sub> = 50 pF |              | Units |
|                                                                                     |                                                          |                                    | Min                                              | Typ         | Max          | Min                                                       | Max          |       |
| f <sub>MAX</sub>                                                                    | Maximum Count Frequency                                  | 3.3<br>5.0                         | 70<br>90                                         | 105<br>133  |              | 65<br>85                                                  |              | MHz   |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>CP to Q <sub>n</sub>                | 3.3<br>5.0                         | 2.0<br>1.5                                       | 8.5<br>6.0  | 15.0<br>11.0 | 1.5<br>1.5                                                | 16.0<br>12.0 | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>CP to Q <sub>n</sub>                | 3.3<br>5.0                         | 2.5<br>1.5                                       | 8.5<br>6.0  | 14.5<br>10.5 | 2.0<br>1.5                                                | 16.0<br>11.5 | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>CP to TC                            | 3.3<br>5.0                         | 3.5<br>2.5                                       | 10.5<br>7.5 | 18.0<br>12.0 | 2.5<br>1.5                                                | 20.0<br>14.0 | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>CP to TC                            | 3.3<br>5.0                         | 4.0<br>2.5                                       | 10.5<br>7.5 | 17.5<br>12.5 | 3.0<br>2.0                                                | 19.0<br>13.5 | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>CP to $\overline{RC}$               | 3.3<br>5.0                         | 2.5<br>2.0                                       | 7.5<br>5.5  | 12.0<br>9.5  | 2.0<br>1.0                                                | 13.5<br>10.5 | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>CP to $\overline{RC}$               | 3.3<br>5.0                         | 2.5<br>1.5                                       | 7.0<br>5.0  | 11.5<br>8.5  | 2.0<br>1.0                                                | 12.5<br>9.5  | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>CE to $\overline{RC}$               | 3.3<br>5.0                         | 2.5<br>1.5                                       | 7.0<br>5.0  | 12.0<br>8.5  | 1.5<br>1.0                                                | 13.5<br>9.5  | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>$\overline{CE}$ to $\overline{RC}$  | 3.3<br>5.0                         | 2.0<br>1.5                                       | 6.5<br>5.0  | 11.0<br>8.0  | 1.5<br>1.0                                                | 12.5<br>9.0  | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>$\overline{U}/D$ to $\overline{RC}$ | 3.3<br>5.0                         | 2.5<br>1.5                                       | 6.5<br>5.0  | 12.5<br>9.0  | 2.0<br>1.0                                                | 14.5<br>10.0 | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>$\overline{U}/D$ to $\overline{RC}$ | 3.3<br>5.0                         | 2.5<br>1.5                                       | 7.0<br>5.0  | 12.0<br>8.5  | 2.0<br>1.0                                                | 13.5<br>10.0 | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>$\overline{U}/D$ to TC              | 3.3<br>5.0                         | 2.0<br>1.5                                       | 7.0<br>5.0  | 11.5<br>8.5  | 1.5<br>1.0                                                | 13.5<br>9.5  | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>$\overline{U}/D$ to TC              | 3.3<br>5.0                         | 2.0<br>1.5                                       | 6.5<br>5.0  | 11.0<br>8.5  | 1.5<br>1.0                                                | 12.5<br>9.5  | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>P <sub>n</sub> to Q <sub>n</sub>    | 3.3<br>5.0                         | 2.5<br>2.0                                       | 8.0<br>5.5  | 13.5<br>9.5  | 2.0<br>1.0                                                | 15.5<br>10.5 | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>P <sub>n</sub> to Q <sub>n</sub>    | 3.3<br>5.0                         | 2.5<br>1.5                                       | 7.5<br>5.5  | 13.0<br>9.5  | 1.5<br>1.0                                                | 14.5<br>10.5 | ns    |
| t <sub>PLH</sub>                                                                    | Propagation Delay<br>$\overline{PL}$ to Q <sub>n</sub>   | 3.3<br>5.0                         | 3.5<br>2.0                                       | 9.5<br>5.5  | 14.5<br>9.5  | 2.5<br>1.0                                                | 17.5<br>10.5 | ns    |
| t <sub>PHL</sub>                                                                    | Propagation Delay<br>$\overline{PL}$ to Q <sub>n</sub>   | 3.3<br>5.0                         | 3.0<br>2.0                                       | 8.0<br>6.0  | 13.5<br>10.0 | 2.0<br>1.5                                                | 15.5<br>11.0 | ns    |
| <b>Note 6:</b> Voltage Range 3.3 is 3.3V ± 0.3V<br>Voltage Range 5.0 is 5.0V ± 0.5V |                                                          |                                    |                                                  |             |              |                                                           |              |       |

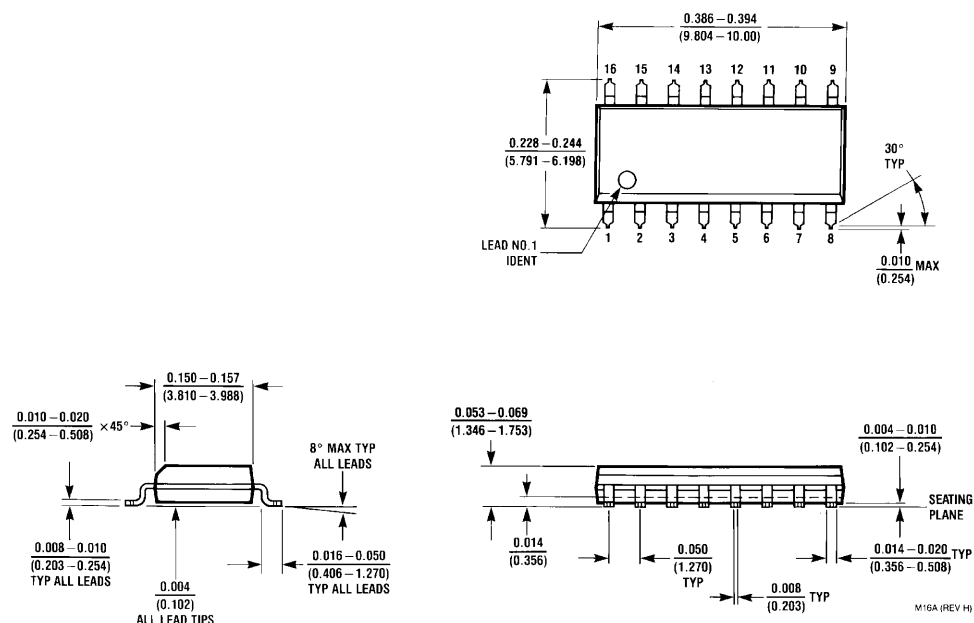
## AC Operating Requirements

| Symbol           | Parameter                                                           | V <sub>CC</sub><br>(V)<br>(Note 7) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |                    | T <sub>A</sub> = -40°C to +85°C<br>C <sub>L</sub> = 50 pF | Units |
|------------------|---------------------------------------------------------------------|------------------------------------|--------------------------------------------------|--------------------|-----------------------------------------------------------|-------|
|                  |                                                                     |                                    | Typ                                              | Guaranteed Minimum |                                                           |       |
| t <sub>S</sub>   | Setup Time, HIGH or LOW<br>P <sub>n</sub> to $\overline{\text{PL}}$ | 3.3                                | 1.0                                              | 3.0                | 3.0                                                       | ns    |
|                  |                                                                     | 5.0                                | 0.5                                              | 2.0                | 2.5                                                       |       |
| t <sub>H</sub>   | Hold Time, HIGH or LOW<br>P <sub>n</sub> to $\overline{\text{PL}}$  | 3.3                                | -1.5                                             | 0.5                | 1.0                                                       | ns    |
|                  |                                                                     | 5.0                                | -0.5                                             | 1.0                | 1.0                                                       |       |
| t <sub>S</sub>   | Setup Time, LOW<br>$\overline{\text{CE}}$ to CP                     | 3.3                                | 3.0                                              | 6.0                | 7.0                                                       | ns    |
|                  |                                                                     | 5.0                                | 1.5                                              | 4.0                | 4.5                                                       |       |
| t <sub>H</sub>   | Hold Time, LOW<br>$\overline{\text{CE}}$ to CP                      | 3.3                                | -4.0                                             | -0.5               | -0.5                                                      | ns    |
|                  |                                                                     | 5.0                                | -2.5                                             | 0                  | 0                                                         |       |
| t <sub>S</sub>   | Setup Time, HIGH or LOW<br>$\overline{\text{U/D}}$ to CP            | 3.3                                | 4.0                                              | 8.0                | 9.0                                                       | ns    |
|                  |                                                                     | 5.0                                | 2.5                                              | 5.5                | 6.5                                                       |       |
| t <sub>H</sub>   | Hold Time, HIGH or LOW<br>$\overline{\text{U/D}}$ to CP             | 3.3                                | -5.0                                             | 0                  | 0                                                         | ns    |
|                  |                                                                     | 5.0                                | -3.0                                             | 0.5                | 0.5                                                       |       |
| t <sub>W</sub>   | $\overline{\text{PL}}$ Pulse Width, LOW                             | 3.3                                | 2.0                                              | 3.5                | 4.0                                                       | ns    |
|                  |                                                                     | 5.0                                | 1.0                                              | 1.0                | 1.0                                                       |       |
| t <sub>W</sub>   | CP Pulse Width, LOW                                                 | 3.3                                | 2.0                                              | 3.5                | 4.0                                                       | ns    |
|                  |                                                                     | 5.0                                | 2.0                                              | 3.0                | 4.0                                                       |       |
| t <sub>rec</sub> | Recovery Time<br>$\overline{\text{PL}}$ to CP                       | 3.3                                | -0.5                                             | 0                  | 0                                                         | ns    |
|                  |                                                                     | 5.0                                | -1.0                                             | 0                  | 0                                                         |       |

**Note 7:** Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

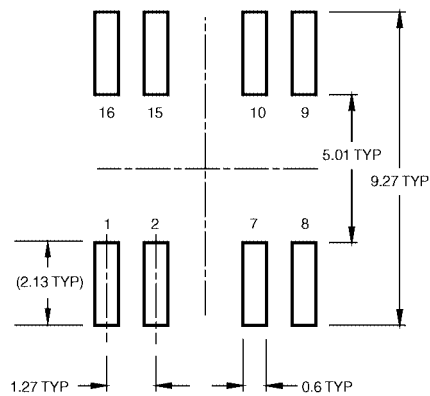
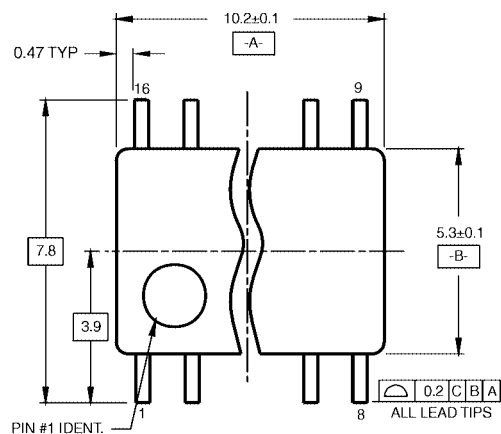
## Capacitance

| Symbol          | Parameter                     | Typ  | Units | Conditions             |
|-----------------|-------------------------------|------|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance             | 4.5  | pF    | V <sub>CC</sub> = OPEN |
| C <sub>PD</sub> | Power Dissipation Capacitance | 75.0 | pF    | V <sub>CC</sub> = 5.0V |

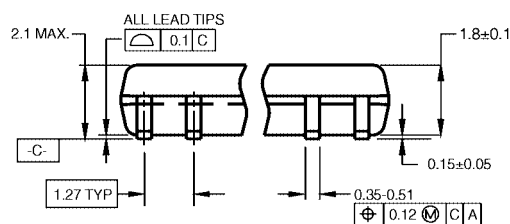
**Physical Dimensions** inches (millimeters) unless otherwise noted


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body  
Package Number M16A**

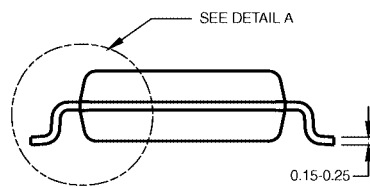
# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



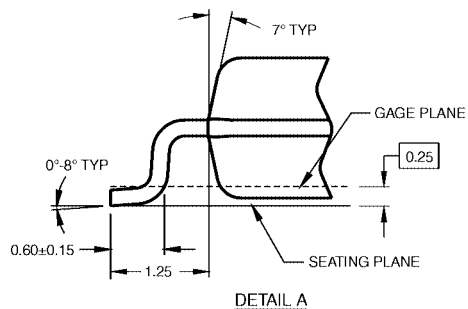
DIMENSIONS ARE IN MILLIMETERS



## NOTES:

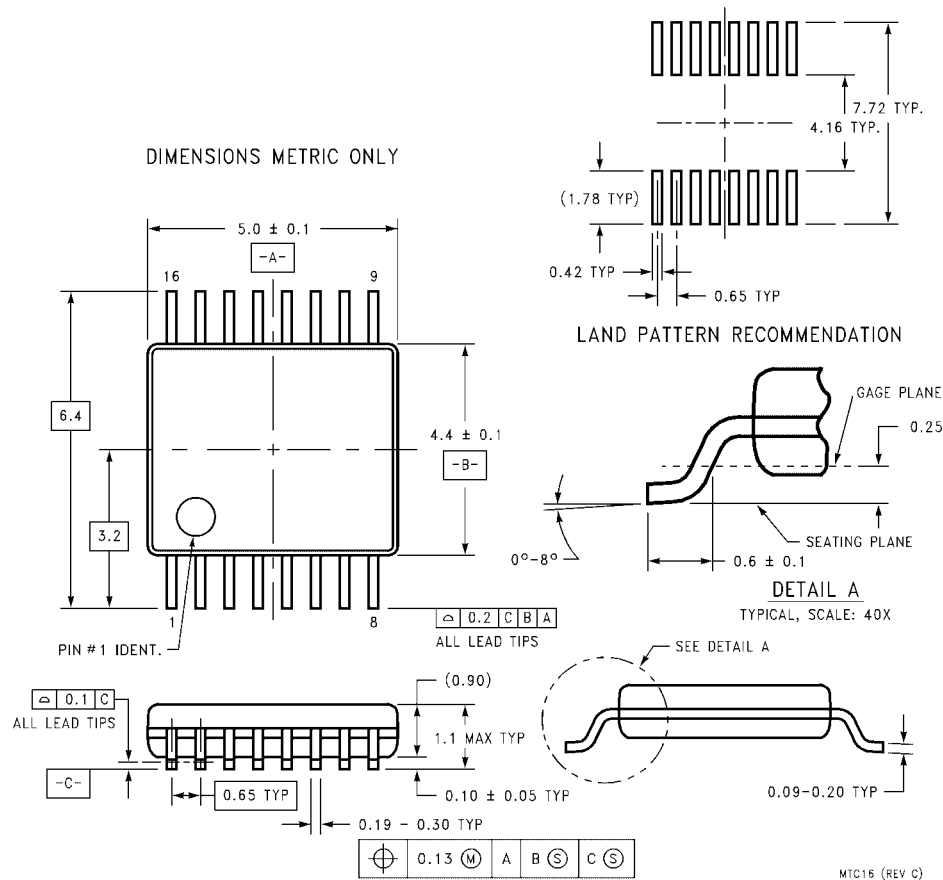
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

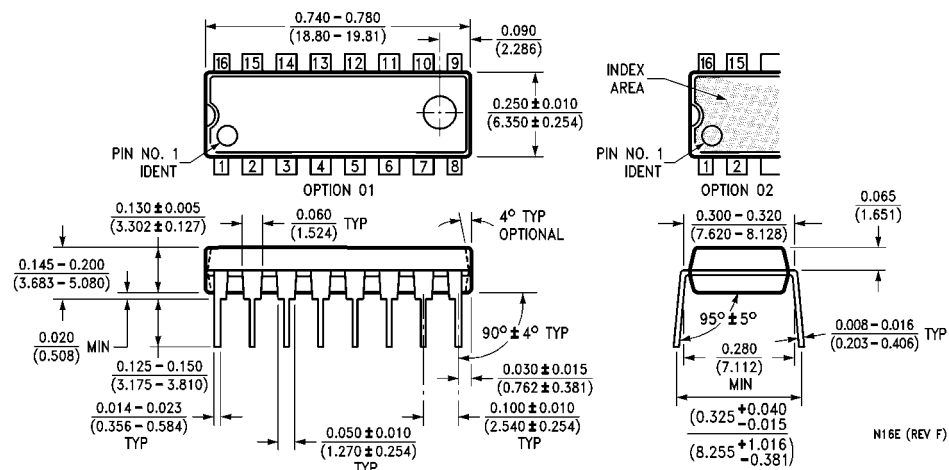


DETAIL A

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)


**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
  2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
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Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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