# Battery Charging IC, 98% Efficient, Safe 6 A Direct with Regulation and Protection

The FAN54161UCX is a low loss direct charger which charges the battery safely at 6 A and provides active protection, regulation and monitoring features.

Integrated Protection and Regulation features control a pair of MOSFETs to ensure that the FAN54161UCX output voltage and current stay within a safe programmed operating range. Configurable hardware based safety features turn off the MOSFET in the event of a fault and notify the system.

An integrated 10-bit Analog-to-Digital Converter (ADC) provides real-time monitoring of input, output voltage, currents and temperature so that the system host or microcontroller can effectively use this information to optimize adapter and charger configuration.

#### Features

- Integrated Back-to-Back Common Source N-channel MOSFETs with Combined  $R_{ON} = 11 \text{ m}\Omega$
- Maximum Input Voltage Tolerance of +22 V
- Reverse Input Voltage Tolerance of -2 V
- External N-channel MOSFET Drive Capability with Tolerance up to +32 V
- Regulation Modes
  - Charge Current
  - Input Current
  - Output Voltage
  - Battery Cell Voltage
- Hardware-based Safety Protections
  - Input Over–Voltage
  - Input Under-Voltage
  - Output Over–Voltage
  - Input Over-Current
  - Die Over-Temperature
  - Internal Switch Short
- 10-bit High-accuracy ADC

### **Typical Applications**

- Mobile Devices
- Tablets



## **ON Semiconductor®**

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WLCSP42 CASE 567TY

### MARKING DIAGRAM



12 = Specific Device Code

KK = Lot Run Code

X = Year Code

- Y = 2-Weeks Date Code
- Z = Assembly Plant Code

### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

### **Block Diagram and Application Schematic**



Figure 1. FAN54161, External FET, Switching Charger, Battery Pack with Exposed Cell, and External Fuel Gauge

### **RECOMMENDED COMPONENTS**

Component	Manufacturer	Part Number	Value	Case Size	Rating
C <sub>BUS</sub>	Murata	GRM188R61E105K	1.0 μF	0603 (1608 metric)	25 V
C <sub>BUS</sub> (alternative)	TDK	C1608X5R1E105K	1.0 μF	0603 (1608 metric)	25 V
C <sub>OUT</sub>	TDK	C1608X5R0J226M	22 μF	0603 (1608 metric)	6.3 V
R <sub>SENSE</sub>	Ohmite	MCS1632R010FER	0.01 (±1%) Ohm	1206 (3216 metric)	1 W
R <sub>SENSE</sub> (alternative)	Ohmite	MCS1632R005FER	0.005 (±1%) Ohm	1206 (3216 metric)	1 W

#### **ORDERING INFORMATION**

Part Number	Temperature Range	Package	Packing Method
FAN54161UCX	–40°C to +85°C	2.78 x 3.06 mm, 42-Bump WLCSP	Tape and Reel

# Pin Connections and Functional Description



Figure 2. WLCSP-42 Pin Assignments

### Table 1. PIN DESCRIPTIONS

Name	Position	Туре	Description
ADR	E2	Digital Input	I <sup>2</sup> C Slave Device Address Selection Pin Refer to I2C Interface section for details ADR logic level must be set before releasing RESET_N high. Recommend connecting this pin to the appropriate logic level before power is applied (VBUS or VOUT).
GND	F2	Ground	Device Ground Connect to the ground node in the PCB.
INT_N	C2	Open–Drain Digital Output	Interrupt Output (Active Low) Pull-up with 100 k $\Omega$ resistor to logic supply voltage. When an un-masked interrupt bit is set this pin will assert low. Connect to GND if not used.
RESET_N	D2	Digital Input	Reset Input (Active Low) 0 (Logic Low) – IC held in reset condition (lowest power state), switch is open, ADC is disabled, and I <sup>2</sup> C communication is not available. 1 (Logic High) – IC logic allowed to operate, switch closed if SW_EN = 1; ADC enabled if ADC_EN = 1. If not used, it is recommended to pull-up to VOUT.
SCL	B1	Digital Input	I <sup>2</sup> C Serial Clock Input Pull-up with a resistor to logic supply voltage.
SDA	C1	Open-drain Digital I/O	I <sup>2</sup> C Serial Data Pull-up with a resistor to logic supply voltage.
VBUS	A6, B6, C6, D6, E6, F6, G6	Power Input	Switch Input, Device Supply and Input Voltage Sense Connect to the input power source of system. If an external N-channel MOSFET is used for protection, connect VBUS to the source of this MOSFET. VBUS has an internal 100 $\Omega$ pulldown resistor that is active when VBUSPD_EN = 1.
PMID	A5, B5, C5, D5, E5, F5, G5		Switch Common Source Point Leave floating. Connect to a floating copper plane to provide an additional thermal relief path to the PCB.

#### Table 1. PIN DESCRIPTIONS

Name	Position	Туре	Description
VOUT	A3, A4, B3, B4, C3, C4, D3, D4, E3, E4, F3, F4, G3, G4	Power Output	Switch Output, Device Supply, and Output Voltage Sense Connect to the battery pack. VOUT will be regulated to a maximum level, relative to GND, as set by the VOREG(TH) register value.
SNSN	G1	Analog Input	Battery Cell Voltage Sense Negative
			Connect to the negative side of the cell inside the battery pack through a 1 k $\Omega$ resistor in series. If the battery pack does not provide access to the negative side of the cell, connect SNSN physically as close as possible to the negative terminal of the pack.
			If the voltage sensed across SNSP and SNSN tries to exceed the threshold $V_{BATREG(TH)}$ , the voltage across SNSP and SNSN is regulated to the threshold.
SNSP	G2	Analog Input	Battery Cell Voltage Sense Positive
			Connect to the positive side of the cell inside the battery pack through a 1 $k\Omega$ resistor in series.
			If the voltage sensed across SNSP and SNSN tries to exceed the threshold
			If the battery pack does not provide access to the positive side of the cell, connect SNSP
			to VOUT.
SRN	E1	Analog Input	Battery Current Sense Negative
			Connect to the negative side of the sense resistor in series with the cell.
			If the current through $R_{\mbox{SENSE}}$ tries to exceed the threshold $I_{\mbox{BATREG(TH)}}$ , the voltage across SRN and SRP is regulated to the threshold.
SRP	F1	Analog Input	Battery Current Sense Positive
			Connect to the positive side of the sense resistor in series with the cell.
			If the current through $R_{\mbox{SENSE}}$ tries to exceed the threshold $I_{\mbox{BATREG(TH)}}$ , the voltage across SRN and SRP is regulated to the threshold.
TS_BUS	B2	Analog Input	Thermistor Input for input connector temperature sense
			Connect an NTC thermistor from TS_BUS to GND. Connect a pull–up resistor from TS_BUS to an external 2.4 V supply.
			Connect to GND if not used.
TS_BAT	D1	Analog Input	Thermistor Input for battery temperature sense
			Connect an NTC thermistor from TS_BAT to GND. Connect a pull-up resistor from
			IS_BAT to an external 2.4 V supply.
VUOD		Dowerland	
VUSB	AI	Power input	Connect this nin to the drain of external N=channel MOSEET (which is also the USB sup-
			ply voltage) with a 500 $\Omega$ series resistor, R <sub>LIMIT</sub> . The source of the external N–channel MOSFET must be connected to the VBUS pin. If an external MOSFET is not used, the VUSB pin must be left floating. Do not connect this pin to GND.
OVP_C	A2	Analog Output	Gate Control Output for external VBUS OVP blocking FET
		-	Connect to the gate of external N-channel MOSFET. If an external MOSFET is not used, the OVP_C pin should be tied to VBUS or float. Do not connect this pin to GND.

Symbol	Parameter	Min	Тур	Max	Units
V <sub>BUS</sub>	Protected Input Supply Voltage, VBUS to GND	-2.0		+22.0	V
V <sub>OUT</sub>	Battery Voltage, VOUT to GND	-0.3		+7.0	V
V <sub>USB</sub>	Input connector sense pin, $R_{LIMIT}$ = 500 $\Omega$	-2.0		+32.0	V
V <sub>OVP_C</sub>	OVP Gate Control Output, OVP_C = VBUS	-2.0		+29.0	V
V <sub>SNSP</sub> , V <sub>SRP</sub> , V <sub>SRN</sub>	Battery Positive Voltage and Current Sense, SNSP to GND, SRP to GND, SRN to GND	-0.3		+6.0	V
V <sub>SNSN</sub>	Battery Negative Voltage Sense, SNSN to GND	-4.6		+6.0	V
V <sub>TS_BUS</sub> , V <sub>TS_BAT</sub>	Thermistor Voltage Sense Inputs, TS_BUS to GND, TS_BAT to GND	-0.3		+6.0	V
V <sub>IOD</sub>	Digital Input and Open Drain Output Pins (SCL, SDA, ADR, RESET_N, INT_N)	-0.3		+6.0	V
IPASS	Maximum Continuous Switch Current			7.50	А
T <sub>A</sub>	Operating Free-air Temperature	-40		+85	°C
T <sub>J(MAX)</sub>	Maximum Junction Temperature	-40		+150	°C
T <sub>STG</sub>	Storage Temperature Range	-65		+150	°C
ΤL	Lead Soldering Temperature, 10 secs			260	°C
ESD	Human-Body Model (HBM-JESD22-A114), VBUS and VUSB	3000			V
	Human-Body Model (HBM-JESD22-A114), All Other Pins	2000			V
	Charged Device Model (CDM-JESD22-C101), All Pins	500			V

#### Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltages are referenced to ground, GND, unless otherwise noted.

2. Pins should be protected with external TVS devices when tested for IEC compliance.

#### **Table 3. THERMAL CHARACTERISTICS**

Symbol	Parameter	Conditions	Min	Тур	Max	Units
ThetaJA	Junction -to-Ambient Thermal Resistance	JEDEC, 2S2P, No Vias		50		°C/W

NOTES: Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with two-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T<sub>J(max)</sub> at a given ambient temperature T<sub>A</sub>.

#### Table 4. RECOMMENDED OPERATING RANGES (Note 3)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings. The recommended operating conditions assume the following:  $V_{OUT} = 2.7$  V to 4.5 V,  $V_{PU} = 1.8$  V to 4.5 V,  $T_A = -40^{\circ}$ C to 85°C, unless otherwise noted.

Symbol	Parameter	Min	Тур	Max	Units
V <sub>BUS</sub>	Input Voltage	2.66		6.4	V
V <sub>USB</sub>	Input Connector Voltage Sense	2.5		15	V
V <sub>OUT</sub>	Battery Voltage	2.66		5.2	V
V <sub>SNSP</sub>	Battery Positive Voltage Sense	2.66		5.2	V
V <sub>SNSN</sub>	Battery Negative Voltage Sense	-0.2		+0.2	V
V <sub>SRP</sub> , V <sub>SRN</sub>	Battery Current Sense	-0.2		+0.2	V
V <sub>PU</sub>	I <sup>2</sup> C External Pull-up Supply Voltage	1.62		3.63	V
V <sub>TS_BUS</sub> , V <sub>TS_BAT</sub>	Thermistor Input Voltage Sense	0.1		2.3	V
T <sub>A</sub>	Operating Free-air temperature	-40		+85	°C
TJ	Operating Junction Temperature	-30		+120	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. All voltages are measured relative to GND.

Table 5. ELECTRICAL CHARACTERISTICS (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1; recommended operating range for  $T_J$  and  $T_A$ ; The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{OUT} = 2.7 \text{ V}$  to 4.5 V and  $T_A = -40^{\circ}\text{C}$  to 85°C, unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{OUT} = 3.8 \text{ V}$ ,  $V_{PU} = 1.8 \text{ V}$ .

Symbol	Parameter	Conditions	Min	Тур	Мах	Units
SUPPLY CURREN	Т					
IACTIVE	Active Mode Current	Switch Closed, RESET_N=HIGH, I <sub>PASS</sub> =6A, V <sub>USB</sub> =0V, [ADC_EN]=0		5	9	mA
ISTANDBY_ADCOFF	VOUT Standby Mode Current	RESET_N=HIGH, [ADC_EN]=0, V <sub>BUS</sub> =Open		5.5	10	μA
		RESET_N=HIGH, [ADC_EN]=0, V <sub>BUS</sub> =5V		1.5	3.0	μA
ISHUTDOWN	VOUT Shutdown Mode Current	RESET_N=LOW, V <sub>BUS</sub> =5V		1.5	3.0	μΑ
		RESET_N=LOW, V <sub>BUS</sub> =Open		1.5	3.0	μΑ
ISTANDBY_ADCOFF	VBUS Standby Mode Current	RESET_N=HIGH, [ADC_EN]=0, V <sub>BUS</sub> =5V, V <sub>OUT</sub> =3.8V		10	25	μΑ
		RESET_N=HIGH, [ADC_EN]=0, V <sub>BUS</sub> =5V, V <sub>OUT</sub> =Open		10	25	μΑ
ISHUTDOWN	VBUS Shutdown Mode Current	RESET_N=LOW, V <sub>BUS</sub> =5V, V <sub>OUT</sub> =3.8V		3	18	μΑ
		RESET_N=LOW, V <sub>BUS</sub> =5V, V <sub>OUT</sub> =Open		3	18	μΑ
I <sub>VUSB</sub>	VUSB Quiescent Current	V <sub>USB</sub> =5V		63	100	μA

#### SWITCH CHARACTERISTICS

R <sub>ON</sub>	On-Resistance from VBUS to VOUT	$3.0 \le V_{OUT} \le 4.5 V$ , $I_{PASS} = 1A$ , $T_A = 25^{\circ}C$		11		mΩ
R <sub>VBUS_PD</sub>	VBUS Pulldown Resistance	[VBUSPD_EN] = 1	80	100	120	Ω

#### SWITCH DYNAMIC CHARACTERISTICS

<sup>t</sup> ENABLE	Switch Turn_On Time	V <sub>BUS</sub> =5V, V <sub>OUT</sub> =3.8V, [SW_EN]=0 to 1, [ADC_EN]=0, RESET_N=HIGH, [IBUS- REG]=3.5A		1.7	ms
		V <sub>BUS</sub> =5V, V <sub>OUT</sub> =3.8V, [SW_EN]=0 to 1, [ADC_EN]=1, RESET_N=HIGH, [IBUS- REG]=3.5A		1.6	ms
t <sub>DISABLE</sub>	Switch Turn_Off Time	[SW_EN] = 1 to 0		0.4	ms
toff_busovp	Time to Isolate VBUS from VOUT for VBUS OVP	V <sub>BUS</sub> Overdrive = 100 mV above VBUSOVP(th)		5.7	μs
<sup>t</sup> OFF_BUSUVLO	Time to Isolate VBUS from VOUT for VBUS UVLO	VBUS Underdrive = 100 mV below VBUSUVLO(th)		5.7	μs
toff_vdropovp	Time to Isolate VBUS from VOUT for VDROP OVP	(V <sub>BUS</sub> -V <sub>OUT</sub> ) Overdrive = 10 mV above VDROPOVP(TH)		5.7	μs
<sup>t</sup> OFF_IBUSOCP	Time to Isolate VBUS from VOUT for IBUS Over Current Fault	I <sub>PASS</sub> Overdrive = 200 mA above I <sub>BU</sub> - <sub>SOCP(TH)</sub> , no Regulation Mode control (Note 9)		425	μS
<sup>t</sup> OFF_TSHDN	Time to Isolate VBUS from VOUT for Die Over Temperature Fault	$T_{J} > T_{SDN(TH)}$		1.2	ms
<sup>t</sup> OFF_RCB	Time to Isolate VBUS from VOUT for Reverse Current Fault	(V <sub>OUT</sub> – V <sub>BUS</sub> ) Overdrive = 10 mV above VRCB(TH)		10	μs
twl_reset	RESET_N Input Pulse Width Low		1200		μs

4. V<sub>IH(max)</sub> = V<sub>PU</sub> + 0.5 V or V<sub>BAT</sub> whichever is lower
5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply V<sub>PU</sub>.
6. V<sub>IH</sub> and V<sub>IL</sub> have been chosen to be fully compliant to I<sup>2</sup>C specification at V<sub>PU</sub> = 1.8 V± 10%. At 2.25V ≤ V<sub>PU</sub> ≤ 3.63 V the V<sub>IL(max)</sub> provides > 200 mV on noise margin to the required V<sub>OL(max)</sub> of the transmitter.
7. I<sup>2</sup>C standard specifies V<sub>OL(max)</sub> for V<sub>PU</sub> ≤ 2.0 V to be 0.2 x V<sub>PU</sub>.
8. Guaranteed by design. Not tested in production.

9. Regulation Mode control will reduce tOFF\_IBUSOCP

Table 5. ELECTRICAL CHARACTERISTICS (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1; recommended operating range for T<sub>J</sub> and T<sub>A</sub>; The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{OUT} = 2.7 \text{ V}$  to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C,  $V_{OUT} = 3.8 \text{ V}$ ,  $V_{PU} = 1.8 \text{ V}$ .

Symbol	Parameter	Conditions	Min	Тур	Max	Units
SWITCH DYNAMI	C CHARACTERISTICS	•		-		
t <sub>RL_RESETI2C</sub>	RESET_N Release to I <sup>2</sup> C Delay Time	Duration required between rising edge of RESET_N and first I2C START (Note 8)	120			μs
HARDWARE PRO	TECTION (Bypass Switch)	•		-		
V <sub>BUSOVP(TH)</sub>	VBUS OVP Threshold Range		4.2		6.5	V
	VBUS OVP Threshold Stepsize			25		mV
	VBUS OVP Threshold Accuracy	[VBUSOVP_TH] = 6.5 V	6.4	6.5	6.6	V
t <sub>BUSOVPGLTCH</sub>	VBUS OVP Deglitch Time	[OVP_DLY]=0		4		μs
		[OVP_DLY]=1		20		μs
V <sub>BUSUVLO(TH)</sub>	VBUS UVLO Threshold	$V_{BUS}$ > $V_{BUSUVLO(TH)}$ allows the switch to close	2.84	2.9	2.96	V
V <sub>BUSUVLO(HYS)</sub>	VBUS UVLO Hysteresis	Falling		300		mV
t <sub>BUSUVLOGLTCH</sub>	VBUS UVLO Deglitch Time			4		μs
V <sub>DROPOVP(TH)</sub>	VDROP OVP Threshold Range	V <sub>BUS</sub> – V <sub>OUT</sub>	0		1000	mV
	VDROP OVP Threshold Stepsize	V <sub>BUS</sub> – V <sub>OUT</sub>		5		mV
	VDROP OVP Threshold Accuracy	V <sub>BUS</sub> – V <sub>OUT</sub> , 2.66V < V <sub>OUT</sub> < 4.5 V, [VDROPOVP_TH]=300mV	295	300	305	mV
t <sub>VDROPGLTCH</sub>	VDROP OVP Deglitch Time	[OVP_DLY]=0		4		μs
		[OVP_DLY]=1		20		μs
V <sub>DROPALM(TH)</sub>	VDROP Alarm Threshold Range	V <sub>BUS</sub> – V <sub>OUT</sub>	0		1000	mV
	VDROP Alarm Threshold Stepsize	V <sub>BUS</sub> – V <sub>OUT</sub>		5		mV
	VDROP Alarm Threshold Accuracy	V <sub>BUS</sub> – V <sub>OUT</sub> , 2.66 V < V <sub>OUT</sub> < 4.5 V, [VDROPOVP_TH]=100mV	80	100	115	mV
t <sub>VDROPALMGLTCH</sub>	VDROP Alarm Deglitch Time	[OVP_DLY]=0		4		μs
		[OVP_DLY]=1		20		μs
IBUSOCP(TH)	IBUS OCP Threshold Range		0.5		7.5	А
	IBUS OCP Threshold Stepsize			500		mA
	IBUS OCP Threshold Accuracy	2.66V < V <sub>OUT</sub> < 4.5V, [IBUSOCP_TH]=5A	4.75	5.00	5.25	А
t <sub>IBUSOCPGLTCH</sub>	IBUS OCP Deglitch Time	[IBUSOCP_MODE]=0		50		μs
		[IBUSOCP_MODE]=1; Deglitch time before entering Hiccup Mode		8		μs
<sup>t</sup> HICCUP	IBUS OCP Hiccup Mode Retry Time	[IBUSOCP_MODE]=1	80	100	125	ms
I <sub>RCB(TH)</sub>	RCB Threshold	[IRCB]=0, Current from V <sub>OUT</sub> to V <sub>BUS</sub> , V <sub>BUS</sub> $\geq$ 3 V	-100	100	+300	mA
		[IRCB]=1, Current from V <sub>OUT</sub> to V <sub>BUS</sub> , V <sub>BUS</sub> $\geq$ 3 V	2.6	3	3.3	A
t <sub>RCBGLTCH</sub>	RCB Deglitch Time			8		μs

4.  $V_{IH(max)} = V_{PU} + 0.5 \text{ V or } V_{BAT}$  whichever is lower 5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply  $V_{PU}$ . 6.  $V_{IH}$  and  $V_{IL}$  have been chosen to be fully compliant to I<sup>2</sup>C specification at  $V_{PU} = 1.8 \text{ V} \pm 10\%$ . At 2.25V  $\leq V_{PU} \leq 3.63 \text{ V the } V_{IL(max)}$  provides > 200 mV on noise margin to the required  $V_{OL(max)}$  of the transmitter. 7. I<sup>2</sup>C standard specifies  $V_{OL(max)}$  for  $V_{PU} \le 2.0$  V to be 0.2 x  $V_{PU}$ . 8. Guaranteed by design. Not tested in production.

9. Regulation Mode control will reduce tOFF\_IBUSOCP

**Table 5. ELECTRICAL CHARACTERISTICS** (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1;recommended operating range for T<sub>J</sub> and T<sub>A</sub>; The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{OUT} =$ 2.7 V to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C,  $V_{OUT} =$ 8.8 V,  $P_{PU} =$ 9.8 V,  $P_{PU} =$ 9.9 C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
HARDWARE PRO	TECTION (Bypass Switch)					
T <sub>SDN(TH)</sub>	Thermal Shutdown Threshold Range		115		145	°C
	Thermal Shutdown Threshold Stepsize			10		°C
	Thermal Shutdown Threshold	3.0V < V <sub>BUS</sub> < 5.9V, [TJSHDN]=125°C		125		°C
t <sub>TSDGLTCH</sub>	Thermal Shutdown Deglitch Time			800		μs
V <sub>FAIL</sub>	VFAIL Short Detect Threshold	Active only when SW_EN=0, ADC_EN=1	1.9	2	2.2	V
R <sub>VFAIL</sub>	VFAIL Pulldown Resistor (PMID to GND)	Active only when SW_EN=0		23		kΩ
<sup>t</sup> VFAIL_GLTCH	VFAIL Deglitch Time			4		μs
VBATINSERT(TH)	VBAT Insert Voltage	V <sub>BUS</sub> > V <sub>BUSUVLO(TH)</sub> ; V <sub>SNSP</sub> rising above V <sub>BATINSERT(TH)</sub> indicates a con- nected battery.	1.9	2.0	2.2	V
V <sub>BATINSERT(HYS)</sub>	VBAT Insert Hysteresis	Falling		100		mV
V <sub>OUTOVP(TH)</sub>	VOUT OVP Threshold Range		4.5		5.3	V
	VOUT OVP Threshold	[VOUTOVP_TH]=4.7V	4.55	4.7	4.85	
V <sub>OUTOVP(HYS)</sub>	VOUT OVP Hysteresis	Falling		100		mV
tvoutovpgltch	VOUT OVP Deglitch Time	[VOUTOVP_DLY]=0		4		μs
		[VOUTOVP_DLY]=1		20		μs

#### VOUT VOLTAGE REGULATION

Voreg(TH)	VOREG Regulation Threshold Range		4.2		5	V
	VOREG Regulation Threshold Stepsize			10		mV
	VOREG Regulation Threshold Accuracy	[VOREG]=4.4V, T <sub>J</sub> = 25°C	-10		+10	mV

#### **VBAT VOLTAGE REGULATION**

V <sub>BATREG(TH)</sub>	VBATREG Regulation Threshold Range	V <sub>SNSP</sub> – V <sub>SNSN</sub>	4.2		5	V
	VBATREG Regulation Threshold Stepsize	V <sub>SNSP</sub> – V <sub>SNSN</sub>		10		mV
	VBATREG Regulation Threshold Accuracy	[VBATREG]=4.3V, T <sub>J</sub> = 25°C	-10		+10	mV

4.  $V_{IH(max)} = V_{PU} + 0.5 V \text{ or } V_{BAT}$  whichever is lower 5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply  $V_{PU}$ . 6.  $V_{IH}$  and  $V_{IL}$  have been chosen to be fully compliant to  $I^2C$  specification at  $V_{PU} = 1.8 V \pm 10\%$ . At 2.25V  $\leq V_{PU} \leq 3.63 V$  the  $V_{IL(max)}$  provides > 200 mV on noise margin to the required  $V_{OL(max)}$  of the transmitter. 7. I<sup>2</sup>C standard specifies  $V_{OL(max)}$  for  $V_{PU} \le 2.0$  V to be 0.2 x  $V_{PU}$ . 8. Guaranteed by design. Not tested in production.

9. Regulation Mode control will reduce tOFF IBUSOCP.

**Table 5. ELECTRICAL CHARACTERISTICS** (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1;recommended operating range for T<sub>J</sub> and T<sub>A</sub>; The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{OUT} = 2.7$  V to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C,  $V_{OUT} = 3.8$  V,  $V_{PU} = 1.8$  V.

Symbol	Parameter	Conditions	Min	Тур	Max	Units			
IBAT CURRENT REGULATION									
IBATREG(TH)	IBATREG Regulation Threshold Range	$V_{SRP}$ – $V_{SRN}$ sensed across $R_{SENSE}$ .	0.1		6.35	A			
	IBATREG Regulation Threshold Stepsize			50		mA			
	IBATREG Regulation Threshold Accuracy	2.5V < V <sub>OUT</sub> < 4.5V, R <sub>SENSE</sub> =10mΩ, [IBATREG]=2A	-5		+5	%			
		2.5V < V <sub>OUT</sub> < 4.5V, R <sub>SENSE</sub> =5mΩ, [IBATREG]=4A	-5		+5	%			

#### **IBUS CURRENT REGULATION**

I <sub>BUSREG(TH)</sub>	IBUSREG Regulation Threshold Range		0.1		6.5	A
	IBUSREG Regulation Threshold Stepsize			50		mA
	IBUSREG Regulation Threshold Accuracy	2.66 < V <sub>OUT</sub> < 4.5; [IBUSREG] = 3.5 A	-5		+5	%

#### BATTERY CELL VOLTAGE SENSE INPUTS (VSNSP, VSNSN)

I <sub>SNSP</sub>	SNSP Input Current	2.66 V < V <sub>SNSP</sub> < 4.5 V		5	μA
I <sub>SNSN</sub>	SNSN Input Current	0.0 V < V <sub>SNSN</sub> < 0.2 V		1	μA

#### LOGIC LEVELS (SCL, SDA, ADR, INT N, RESET N)

V <sub>IH</sub>	Input High Voltage Level		1.05		V
V <sub>IL</sub>	Input Low Voltage Level			0.4	V
V <sub>OL</sub>	Output Low Voltage, INT_N, SDA	I <sub>OL</sub> = 3 mA		0.4	V
I <sub>IN</sub>	Input current each I/O pin	V <sub>PIN</sub> = 0 V or 5 V	-10	+10	μΑ

#### BATTERY CURRENT SENSE INPUTS (VSRP, VSRN)

I <sub>SRP</sub>	V <sub>SRP</sub> Input Current	0 < V <sub>SRP</sub> < 0.2		1	μA
I <sub>SRN</sub>	V <sub>SRN</sub> Input Current	–0.2 < V <sub>SRN</sub> < 0	-1		μΑ

### WATCH DOG TIMER

t <sub>WDT</sub>	Watchdog Timer Range		0.5	2	s
	Watchdog Timer Accuracy	All [WDT] Settings	-10	+10	%

#### ANALOG TO DIGITAL CONVERTER

RES	Resolution	(Note 8)	10			Bits
INL	Integral Non-Linearity			±1		LSB
DNL	Differential Non-Linearity			±1		LSB
OE	Offset Error			±1		LSB
GE	Gain Error (Full Scale Error)			±1		LSB
f <sub>CONV</sub>	Conversion Clock		2.7	3.0	3.3	MHz

4.  $V_{IH(max)} = V_{PU} + 0.5 V$  or  $V_{BAT}$  whichever is lower 5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply  $V_{PU}$ .

N is assumed that the SCL and SDA pins are open dram with external pun-ups resistors tied to an external supply vpg.
V<sub>IH</sub> and V<sub>IL</sub> have been chosen to be fully compliant to l<sup>2</sup>C specification at V<sub>PU</sub> = 1.8 V± 10%. At 2.25V ≤ V<sub>PU</sub> ≤ 3.63 V the V<sub>IL(max)</sub> provides > 200 mV on noise margin to the required V<sub>OL(max)</sub> of the transmitter.
I<sup>2</sup>C standard specifies V<sub>OL(max)</sub> for V<sub>PU</sub> ≤ 2.0 V to be 0.2 x V<sub>PU</sub>.
Guaranteed by design. Not tested in production.

9. Regulation Mode control will reduce tOFF IBUSOCP

Table 5. ELECTRICAL CHARACTERISTICS (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1; recommended operating range for  $T_J$  and  $T_A$ ; The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{OUT} = 2.7 \text{ V}$  to 4.5 V and  $T_A = -40^{\circ}\text{C}$  to 85°C, unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{OUT} = 3.8 \text{ V}$ ,  $V_{PU} = 1.8 \text{ V}$ .

Symbol	Parameter	Conditions	Min	Тур	Max	Units
ANALOG TO DIGI	TAL CONVERTER				-	
t <sub>THR_ONE</sub>	Throughput time (Single-shot conversion)	No Averaging, 1 channel, One-shot con- version (ADC_RATE = 0, ADC_EN written from 0 to 1)		47		μs
		8-sample Averaging (AVG_EN=1, SAM- PLES=0), 1 channel, One-shot conver- sion (ADC_RATE = 0, ADC_EN written from 0 to 1)		84		μs
		16-sample Averaging (AVG_EN=1, SAM- PLES=1), 1 channel, One-shot conver- sion (ADC_RATE = 0, ADC_EN written from 0 to 1)		127		μs
		16-sample Averaging (AVG_EN=1, SAM- PLES=1), 9 channels, One-shot conver- sion (ADC_RATE = 0, ADC_EN written from 0 to 1)		1031		μs
<sup>t</sup> THR_CONT	Throughput time (Continuous Conversion)	No Averaging, 1 channel, Continuous conversion (ADC_RATE = 1, ADC_EN=1)		33		μs
		8-sample Averaging (AVG_EN=1, SAM- PLES=0), 1 channel, Continuous conver- sion (ADC_RATE = 1, ADC_EN=1)		70		μs
		16-sample Averaging (AVG_EN=1, SAM- PLES=1), 1 channel, Continuous conver- sion (ADC_RATE = 1, ADC_EN=1)		113		μs
		16-sample Averaging (AVG_EN=1, SAM- PLES=1), 9 channels, Continuous con- version (ADC_RATE = 1, ADC_EN=1)		1018		μs
GAIN <sub>IBAT</sub>	Battery Current ADC Gain Range	RSENSE = 0		40		V/V
		RSENSE = 1		20		V/V
VBUS <sub>ADC</sub>	VBUS Channel Full Scale Range	Signal sensed at VBUS pin, 7.3 mV per LSB	0		6.1	V
VBAT <sub>ADC</sub>	VBAT Channel Full Scale Range	Signal sensed across and SNSP and SNSN pins, 5.3 mV per LSB	2.5		5.0	V
VOUT <sub>ADC</sub>	VOUT Channel Full Scale Range	Signal sensed at VOUT, 5.3 mV per LSB	0		5.0	V
VDROP <sub>ADC</sub>	VDROP Channel Full Scale Range	Signal sensed between VBUS and VOUT pins, 2.9 mV per LSB	0		1.0	V
IBUS <sub>ADC</sub>	IBUS Channel Full Scale Range	Signal sensed across internal switch, 14.6 mA per LSB	0		7.0	А
IBAT <sub>ADC</sub>	IBAT Channel Full Scale Range	Signal sensed across SRP and SRN pins, 14.6 mA per LSB	-7.0		+7.0	A
TBUS_BAT <sub>ADC</sub>	TBUS and TBAT Channel Full Scale Range	Signal sensed at TS_BUS and TS_BAT pins, 2.9 mV per LSB respectively	0		2.4	V
<sup>t</sup> TBUS_TBAT_GLTCH	TBUS and TBAT Temperature Fault Deglitch Time	Deglitch time to open switch when V <sub>TBUS</sub> falls below TBUS_TH or V <sub>TBAT</sub> falls below TBAT_TH	0.9	1	1.1	S
TDIEADC	TDIE Channel Full Scale Range	Signal sensed by internal temperature sensor, 1°C per LSB	25		150	°C

4.  $V_{IH(max)} = V_{PU} + 0.5 V$  or  $V_{BAT}$  whichever is lower 5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply  $V_{PU}$ .

6. V<sub>IH</sub> and V<sub>IL</sub> have been chosen to be fully compliant to I<sup>2</sup>C specification at V<sub>PU</sub> = 1.8 V  $\pm$  10%. At 2.25V  $\leq$  V<sub>PU</sub>  $\leq$  3.63 V the V<sub>IL(max)</sub> provides > 200 mV on noise margin to the required  $V_{OL(max)}$  of the transmitter. > 1<sup>2</sup>C standard specifies  $V_{OL(max)}$  for  $V_{PU} \le 2.0$  V to be 0.2 x  $V_{PU}$ . 8. Guaranteed by design. Not tested in production. 9. Regulation Mode control will reduce  $t_{OFF\_IBUSOCP}$ .

**Table 5. ELECTRICAL CHARACTERISTICS** (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1;recommended operating range for T<sub>J</sub> and T<sub>A</sub>; The Recommended Operating Conditions for DC Electrical Characteristics assume  $V_{OUT} =$ 2.7 V to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C,  $V_{OUT} =$ 8.8 V,  $V_{PU} =$ 9.8 V,  $V_{PU} =$ 9.9 V to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C,  $V_{OUT} =$ 9.9 V to 4.5 V and T<sub>A</sub> = -40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
OVP_C CONTROL	. (External OVP FET Control)					
V <sub>USBOVP(TH)</sub>	VUSB OVP Threshold	$V_{USB} > V_{USBOVP(TH)}$ drives OVP_C low	15	16.5	18	V
V <sub>USBOVP(HYS)</sub>	VUSB OVP Hysteresis	V <sub>USB</sub> Falling		1		V
V <sub>USBUVLO(TH)</sub>	VUSB UVLO Threshold	V <sub>USBOVP(TH)</sub> >V <sub>USB</sub> > V <sub>USBUVLO(TH)</sub> will drive OVP_C high	2.5	2.6	2.7	V
V <sub>USBUVLO(HYS)</sub>	VUSB UVLO Hysteresis	Falling, V <sub>USB</sub> < V <sub>USBUVLO(TH)</sub> - V <sub>USBUVLO(HYS)</sub> will drive OVP_C low		200		mV
OVP_C(HI)	OVP_C Gate Drive Voltage	V <sub>USBUVLO(TH)</sub> < V <sub>USB</sub> < V <sub>USBOVP(TH)</sub> ; measured from OVP_C to VBUS	4.5	4.8	5.1	V
<sup>t</sup> off_usbovp	OVP_C Gate Turn-Off Time	Gate Capacitance =5.2nF; 2V/us $V_{USB}$ ramp rate; Time from $V_{USB}$ rising above $V_{USBOVP(TH)}$ to external FET open (where VBUS stops increasing); $V_{USB}$ compara- tor delay included; FDMC8321L N–Chan- nel FET		0.7		μs

I<sup>2</sup>C TIMING SPECIFICATIONS

f <sub>SCL</sub>	SCL Clock Frequency	Standard Mode		100	kHz
		Fast Mode		400	kHz
		Fast Mode Plus		1000	kHz
t <sub>BUF</sub>	Bus-Free Time Between STOP	Standard Mode	4.7		μs
	and START Conditions	Fast Mode	1.3		μs
		Fast Mode Plus	0.5		μs
t <sub>HD;STA</sub>	START or Repeated START Hold	Standard Mode	4		μs
	lime	Fast Mode	600		ns
		Fast Mode Plus	260		ns
t <sub>LOW</sub>	SCL LOW Period	Standard Mode	4.7		μs
		Fast Mode	1.3		μs
		Fast Mode Plus	0.5		μs
<sup>t</sup> ніgн	SCL HIGH Period	Standard Mode	4		μs
		Fast Mode	600		ns
		Fast Mode-Plus	260		ns
t <sub>SU;STA</sub>	Repeated START Setup Time	Standard Mode	4.7		μs
		Fast Mode	600		ns
		Fast Mode-Plus	260		ns
t <sub>SU;DAT</sub>	Data Setup Time	Standard Mode	250		ns
		Fast Mode	100		ns
		Fast Mode Plus	50		ns

4. V<sub>IH(max)</sub> = V<sub>PU</sub> + 0.5 V or V<sub>BAT</sub> whichever is lower
5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply V<sub>PU</sub>.
6. V<sub>IH</sub> and V<sub>IL</sub> have been chosen to be fully compliant to I<sup>2</sup>C specification at V<sub>PU</sub> = 1.8 V ± 10%. At 2.25V ≤ V<sub>PU</sub> ≤ 3.63 V the V<sub>IL(max)</sub> provides > 200 mV on noise margin to the required V<sub>OL(max)</sub> of the transmitter.
7. I<sup>2</sup>C standard specifies V<sub>OL(max)</sub> for V<sub>PU</sub> ≤ 2.0 V to be 0.2 x V<sub>PU</sub>.
8. Guaranteed by design. Not tested in production.
9. Regulation Mode control will reduce t<sub>OFF\_IBUSOCP</sub>.

<b>Table 5. ELECTRICAL CHARACTERISTICS</b> (Notes 4, 5, 6, 7) Unless otherwise specified: according to the circuit in Figure 1;
recommended operating range for T <sub>J</sub> and T <sub>A</sub> ; The Recommended Operating Conditions for DC Electrical Characteristics assume V <sub>OUT</sub> =
2.7 V to 4.5 V and $T_A = -40^{\circ}$ C to 85°C, unless otherwise noted. Typical values are at $T_A = 25^{\circ}$ C, $V_{OUT} = 3.8$ V, $V_{PU} = 1.8$ V.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
I <sup>2</sup> C TIMING SPEC	CIFICATIONS					
t <sub>HD;DAT</sub>	Data Hold Time	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
		Fast Mode Plus	0		450	ns
t <sub>RCL</sub>	SCL Rise Time	Standard Mode	20 + 0.1Cb		1000	ns
		Fast Mode	20 + 0.1Cb		300	ns
		Fast Mode Plus	20 + 0.1Cb		120	ns
t <sub>RDA</sub>	SDA Rise Time	Standard Mode	20 + 0.1Cb		1000	ns
		Fast Mode	20 + 0.1Cb		300	ns
		Fast Mode Plus	20 + 0.1Cb		120	ns
t <sub>FDA</sub>	SDA Fall Time	Standard Mode	20 + 0.1Cb		300	ns
		Fast Mode	20 + 0.1Cb		300	ns
		Fast Mode Plus	20 + 0.1Cb		120	ns
t <sub>SU;STO</sub>	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns
C <sub>b</sub>	Capacitive Load for SDA and SCL				400	pF
t <sub>SP</sub>	Pulse width of spikes which must be suppressed by input filter	SCL, SDA only	0		50	ns

4. V<sub>IH(max)</sub> = V<sub>PU</sub> + 0.5 V or V<sub>BAT</sub> whichever is lower
5. It is assumed that the SCL and SDA pins are open drain with external pull-ups resistors tied to an external supply V<sub>PU</sub>.
6. V<sub>IH</sub> and V<sub>IL</sub> have been chosen to be fully compliant to I<sup>2</sup>C specification at V<sub>PU</sub> = 1.8 V± 10%. At 2.25V ≤ V<sub>PU</sub> ≤ 3.63 V the V<sub>IL(max)</sub> provides > 200 mV on noise margin to the required V<sub>OL(max)</sub> of the transmitter.
7. I<sup>2</sup>C standard specifies V<sub>OL(max)</sub> for V<sub>PU</sub> ≤ 2.0 V to be 0.2 x V<sub>PU</sub>.
8. Guaranteed by design. Not tested in production.
9. Regulation Mode control will reduce t<sub>OFF\_IBUSOCP</sub>.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### **Typical Characteristics**

Unless otherwise specified: Default register settings,  $T_A = 25^{\circ}C$ , VOUT = 3.8 V, VPU = 1.8 V.







VBUS=Open, RESET\_N=LOW



Figure 5. On Resistance from VBUS to VOUT, Normalized to 1.0 A/25°C









# **Typical Characteristics**

Unless otherwise specified: Default register settings,  $T_A$  = 25°C, VOUT = 3.8 V, VPU = 1.8 V.



Figure 8. Switch Opening IBUS OCP Fault, [IBUSOCP]=4A, [IBUSREG]=[IBATREG]=max, TA Current Limit Raised from 3 A to 5 A



Figure 9. Load Transient Response, [IBATREG]=2A, [IBUSREG]=3.5A, TA Configured for 5 V/5 A

### **Functional Specifications**

### **Charging Bypass Switch with Regulation Mode**

#### Overview

The FAN54161 is designed to be placed in a system that requires high current charging for a large battery. It is essentially a high current bypass switch with protection that provides a path from a charging source (adapter) to the battery directly through a low resistance path. In order to ensure safety of the battery as well as the system, the FAN54161 features multiple hardware protection mechanisms. Most of these result in the path from the charging source to the battery being opened. Examples of these are input over–voltage, over–current through the switch and reverse current.

Some of the parameters are monitored and regulated such that they are at or below a programmed threshold. This is achieved by controlling the gate of the power switch. However, this mode of operation is only meant to be used temporarily while the system controller/host reacts to this and corrects the system configuration to allow the switch to return to a bypass mode (fully–on state).

Many of the hardware protection mechanisms have  $I^2C$  programmable thresholds, enable/disable controls, interrupts with masks and status bits. The product block diagram (Figure 1) provides an illustrative overview of the functionality within the FAN54161.

The FAN54161 also utilizes a fully independent charge pump based gate drive circuit to control an optional external N-channel MOSFET for an additional level of input protection from over voltage faults up to 32 V applied at the USB port.

#### **Bypass Switch Modes of Operation**

Broadly speaking, the FAN54161 has four modes of bypass switch operation.

- 1. **OFF:** This represents a lack of power to the FAN54161.
- 2. **SHUTDOWN:** Valid power is applied to one of VBUS or VOUT but the RESET\_N input is asserted low. In this state, no communication with the FAN54161 is possible and the switch is forced open.
- 3. **STANDBY:** Valid power is applied to one of VBUS or VOUT and the RESET\_N input is de-asserted high. I2C communication is enabled, but, the switch is not programmed to close.
- 4. **SWITCH ENABLED:** As evidenced by the name, the FAN54161 bypass switch is closed in this state. From the STANDBY state, when the SW\_EN bit is written with a 1, the FAN54161 enters the SWITCH ENABLED state. In this state, the switch's gate is controlled by the control circuit of the FAN54161 to be either fully on (bypass mode) or partially on (regulation mode) based on the parameters being monitored.

#### Power-up and Reset (VBUS and VOUT)

When power is first applied to either VBUS or VOUT, an internal power-on reset (POR) circuit ensures the default state of all registers and circuits and keeps the switch in the OPEN state. Power for all internal logic circuits comes from the higher of VBUS and VOUT. This allows the FAN54161 to be I<sup>2</sup>C programmable even with just one of the supplies present (VBUS or VOUT).

The RESET\_N pin is an active-low reset input. When the RESET\_N pin is asserted low externally, the FAN54161 remains in a reset state and does not support I<sup>2</sup>C communication. The switch is forced OPEN. This corresponds to the SHUTDOWN state. The RESET\_N pin being low also forces the ADC in the FAN54161 to its SHUTDOWN state.

In order to properly control and operate the FAN54161, a valid supply must be present at VBUS or VOUT and the RESET\_N pin must be de-asserted (logic high state).

#### VUSB Power

The VUSB pin does not affect POR behavior of the FAN54161 and should be considered a completely independent power domain with respect to VBUS and VOUT.

#### **Hardware Fault Protection**

The FAN54161 features hardware safety protection monitors, some of which can cause the switch to OPEN if enabled. Other than VBUS UVLO and IC Thermal Shutdown, each hardware safety protection monitor has an independently programmable enable bit.

The high current switch is closed by setting  $SW_EN = 1$ . Before the switch closes, though, the IC is checked against the following safety protection thresholds:

- VBUS UVLO
- VBUS OVP
- VOUT OVP
- VDROP OVP
- Thermal Shutdown

If any of these safety protection monitors are enabled and the associated fault is triggered, the switch is not allowed to close and the appropriate interrupt bit is set to report the fault to the system controller/host. If no faults are triggered when SW EN bit is set, the switch is closed.

When the switch is closed, all enabled safety protection monitors are armed. With the exception of VOREG, VBATREG, IBATREG, and IBUSREG, if any enabled fault is triggered, the switch is opened and its appropriate interrupt bit is set to 1. Refer to Figure 10 for details.

When the switch is closed, if a VOREG, VBATREG, IBATREG, or IBATREG fault is triggered, the internal logic drives the gate of the bypass switch such that the current or voltage does not exceed its regulation threshold. Additionally, its appropriate interrupt bit is set to 1. It is expected that the host will take action to correct the system configuration such that the FAN54161's regulation control loop can drive the gate of the power switch to make it fully on again. Refer to Figure 11 for details.

The hardware protections for the VBUS connector and battery (T\_BUS and T\_BAT) are implemented through digital comparisons of a digital threshold (programmed in the TBUSOTP and TBATOTP registers) to the ADC's converted results of these channels. Therefore, if these fault protections are enabled, it must be ensured that the ADC is enabled and programmed to convert this channel.

For additional details on Hardware Fault Protection, refer to Table 6 and Table 7.



Figure 10. Hardware Protection Logic Diagram

### Table 6. HARDWARE FAULT PROTECTION ENTRY SUMMARY

Safety Feature	Safety Mode Entry	Safety Mode Deglitch Time	Safety Mode Hardware Action	Safety Mode Register Action
VBUS OVP	V <sub>BUS</sub> > V <sub>BUSOVP(TH)</sub>	4us (OVP_DLY=0) 20us (OVP_DLY=1)	Open Bypass Switch Pull INT_N low	SW_EN=0 VBUSOVP_INT=1
VBUS UVLO Falling	$V_{BUS} < (V_{BUSUVLO(H)} - V_{BUSUVLO(HYS)})$ 4us		Open Bypass Switch Pull INT_N low	VBUSINSERT_INT=1
VDROP Alarm	$V_{DROP} > V_{DROPALM(TH)}$	4us (OVP_DLY=0) 20us (OVP_DLY=1)	Pull INT_N low	VDROPALM_INT=1
VDROP OVP	$V_{DROP} > V_{DROPOVP(TH)}$	4us (OVP_DLY=0) 20us (OVP_DLY=1)	Open Bypass Switch Pull INT_N low	SW_EN=0 VDROPOVP_INT=1
TS_BUS Overtemp	V <sub>TS_BUS</sub> < T <sub>BUS_TH</sub> (digital comparator)	1s	Open Bypass Switch Pull INT_N low	SW_EN=0 TBUSOTP_INT=1
TS_BAT Overtemp	V <sub>TS_BAT</sub> < T <sub>BAT_TH</sub> (digital comparator)	1s	Open Bypass Switch Pull INT_N low	SW_EN=0 TBATOTP_INT=1
Thermal Shutdown	$T_J > T_{SDN(TH)}$	800us	Open Bypass Switch Disable ADC Pull INT_N Iow	SW_EN=0 ADC_EN bit does not change state TSDN_INT=1
Watchdog Timer	Watchdog Timer Expired	N/A	Open Bypass Switch Pull INT_N low	SW_EN=0 Reset registers to default (except TIMER_INT) TIMER_INT=1
		50us (IBUSOCP_MODE=0)	Open Bypass Switch Pull INT_N low	SW_EN=0 IBUSOCP_INT=1
IBUS OCP	$I_{BUS} > I_{BUSOCP(TH)}$	4us (IBUSOCP_MODE=1)	1- Open Bypass Switch and enter Hiccup Mode 2- Wait 100ms then close switch 3- If $I_{UUS} < I_{BUSOCP(TH)}$ continue charging 4- If $I_{UUS} > I_{BUSOCP(TH)}$ return to top (up to 6 attempts) 5- If still OCP leave Bypass Switch open 6- Pull INT_N low	Set SW_EN=0 IBUSOCP_INT=1 (Only after 6 failed Hiccup attempts)
IBUSREG	I <sub>BUS</sub> > I <sub>BUSREG(TH)</sub>	N/A	Enter Regulation Mode Limit I <sub>BUS</sub> to I <sub>BUSREG(TH)</sub> Pull INT_N low	IBUSREG_INT=1
IBATREG	$((V_{SRP} - V_{SRN}) / R_{SENSE}) > I_{BATREG(TH)}$	N/A	Enter Regulation Mode Limit I <sub>ват</sub> to I <sub>ватвед(тн)</sub> Pull INT_N Iow	IBATREG_INT=1
VOREG	$V_{OUT} > V_{OREG(TH)}$	N/A	Enter Regulation Mode Limit V <sub>OUT</sub> to V <sub>OREG(TH)</sub> Pull INT_N low	VOREG_INT=1
VBATREG	$(V_{SNSP} - V_{SNSN}) > V_{BATREG(TH)}$	N/A	Enter Regulation Mode Limit V <sub>SNSP</sub> – V <sub>SNSN</sub> to V <sub>BATREG(TH)</sub> Pull INT_N Iow	VBATREG_INT=1
VUSB OVP	$V_{USB} > V_{USBOVP(TH)}$	No Deglitch	Pull OVP_C low Pull INT_N low	VUSBOVP_INT=1 (if SW_EN=1 or ADC_EN=1)
VUSB UVLO Falling	V <sub>USB</sub> < (V <sub>USBUVLO(TH)</sub> - V <sub>USBUVLO(HYS)</sub> )	No Deglitch	Pull OVP_C low Pull INT_N low	VUSBINSERT_INT=1
VOUT OVP	$V_{OUT} > V_{OUTOVP(TH)}$	4us (VOUTOVP_DLY=0) 20us (VOUTOVP_DLY=1)	Open Bypass Switch Pull INT_N low	SW_EN=0 VOUTOVP_INT =1
IBUS RCB	Reverse I <sub>BUS</sub> > I <sub>RCB(TH)</sub>	10us	Open Bypass Switch Pull INT_N low	SW_EN=0 IBUSRCB_INT=1

Safety Feature	Safety Mode Exit (Recovery)	Recovery Hardware Action	Recovery Register Action
VBUS OVP	V <sub>BUS</sub> < V <sub>BUSOVP(TH)</sub>	Wait for host command	
VBUS UVLO Rising	$V_{BUS} > V_{BUSUVLO(TH)}$	switch autorecovers Pull INT_N low	VBUSINSERT_INT=1
VDROP Alarm	N/A	No Action	
VDROP OVP	$V_{DROP} < V_{DROPOVP(TH)}$	Wait for host command	
TS_BUS Overtemp	V <sub>TS_BUS</sub> > T <sub>BUS_TH</sub> (digital comparator)	Wait for host command	
TS_BAT Overtemp	V <sub>TS_BAT</sub> > T <sub>BAT_TH</sub> (digital comparator)	Wait for host command	
Thermal Shutdown	$T_{\rm J} < T_{\rm SDN(TH)}$	Wait for host command to close Bypass Switch; ADC auto recovery if ADC_EN=1	
Watchdog Timer	SW_EN= 1 starts watchdog	Wait for host command	
	I <sub>BUS</sub> < I <sub>BUSOCP(TH)</sub>	Wait for host command	
IBUS OCP	I <sub>вus</sub> < I <sub>визоср(тн)</sub> During Hiccup Mode retry	Auto recovery after successful Hiccup Mode retry. OR Wait for host command if all 6 Hiccup retries fail.	Keep SW_EN=1 after successful Hiccup Mode retry. OR Set SW_EN=0 only after 6 failed Hiccup attempts.
IBUSREG	I <sub>BUS</sub> < I <sub>BUSREG(TH)</sub>	Exit Regulation Mode Bypass Switch remains closed	
IBATREG	$((V_{SRP} - V_{SRN}) / R_{SENSE}) < I_{BATREG(TH)}$	Exit Regulation Mode Bypass Switch remains closed	
VOREG	$V_{OUT} < V_{OREG(TH)}$	Exit Regulation Mode Bypass Switch remains closed	
VBATREG	$(V_{SNSP} - V_{SNSN}) < V_{BATREG(TH)}$	Exit Regulation Mode Bypass Switch remains closed	
VUSB OVP	$V_{\text{USB}} < (V_{\text{USBOVP(TH)}} - V_{\text{USBOVP(HYS)}})$	Drive OVP_C High Pull INT_N low	VBUSOVP_INT=1
VUSB UVLO Rising	$V_{USB} > V_{USBUVLO(TH)}$	Drive OVP_C High Pull INT_N low	VUSBINSERT_INT=1
VOUT OVP	VOUT < V OUTOVP(TH) - VOUTOVP(HYS)	Wait for host command	
IBUS RCB	Reverse $I_{BUS} > I_{RCB(TH)}$	Wait for host command	

#### Table 7. HARDWARE FAULT PROTECTION EXIT (RECOVERY) SUMMARY

#### VBUS Input Over–Voltage Protection

When the voltage at the VBUS pin exceeds the programmed  $V_{BUSOVP(TH)}$  threshold for more than  $t_{BUSOVPGLTCH}$ , the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW\_EN to 0
- 3. Set the VBUSOVP\_INT bit to 1 and pull the INT\_N pin low

A VBUS OVP fault recovery is not automatic and requires the host processor to re-enable the switch by programming SW\_EN to 1. The switch will not close again until after VBUS has fallen below  $V_{BUSOVP(TH)} - V_{BUSOVP(HYS)}$ . Any attempts to write SW\_EN to 1 during a VBUS OVP condition will result in a SW EN self clear.

The ADC is not affected by this fault and operates according to the ADC EN setting.

#### VBUS Input Under-Voltage Lockout

If the voltage applied to VBUS fails to exceed the  $V_{BUSUVLO(TH)}$  threshold after an input plug-in event, the bypass switch will remain open. Setting SW\_EN to 1 while  $V_{BUS} < V_{BUSUVLO(TH)}$  will keep the bypass switch open. Once the VBUS voltage exceeds the  $V_{BUSUVLO(TH)}$  threshold, the switch is allowed to close if SW\_EN is set to 1.

From a closed position, the bypass switch will be forced open if VBUS falls below  $V_{BUSUVLO(TH)} - V_{BUSUVLO(HYS)}$ . In addition, the  $V_{BUSINSERT\_INT}$  interrupt bit will be set, the INT\_N pin is pulled low, and the SW\_EN bit will remain set.

If VOUT is available to support ADC operation during a VBUS UVLO fault, ADC will operate according to the ADC\_EN setting.

#### **VDROP Alarm Reporting**

While the bypass switch is closed, if the voltage measured across the switch ( $V_{BUS} - V_{OUT}$ ) exceeds the  $V_{DROPALM(TH)}$  threshold for more than  $t_{VDROPALMGLTCH}$ , the FAN54161 sets the VDROPALM\_INT bit to 1 and pulls the INT\_N pin low. This alerts the host processor that the FAN54161 is operating in a condition that may soon trigger a VDROP OVP fault which would force the switch to open. This alert feature warns the host processor to reprogram the Travel Adapter or the FAN54161's charge parameter settings to prevent a VDROP OVP fault from triggering.

#### **VDROP Over-Voltage Protection**

While the bypass switch is closed, if the voltage measured across the switch ( $V_{BUS} - V_{OUT}$ ) exceeds the  $V_{DROPOVP(TH)}$  threshold for more than  $t_{VDROPGLTCH}$ , the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW EN to 0
- 3. Set the VBUSOVP\_INT bit to 1 and pull the INT\_N pin low

If a VDROP OVP fault occurs, the host processor should reprogram the FAN54161's charging parameter settings to prevent a VDROP OVP fault from reoccurring the next time the bypass switch is closed. Once the VDROP OVP fault is removed, the host processor must set SW\_EN to 1 in order to close the bypass switch again. The VDROP OVP protection is disabled by default to allow the switch to close even if the difference between VBUS and VOUT is greater than the VDROP OVP threshold. If VDROP OVP protection is enabled before the switch is closed, care should be taken to ensure that VBUS–VOUT is less than the VDROP OVP threshold, otherwise the VDROP OVP protection will prevent the switch from closing when writing SW\_EN to 1.

The ADC is not affected by this fault and operates according to the ADC EN setting.

#### Input Connector Over-Temperature Fault

The FAN54161 can monitor the temperature of the input connector with an external NTC thermistor tied from the TS\_BUS pin to ground. This protection prevents bypass charging from continuing if the input connector temperature rises to a dangerous level. A TS\_BUS pullup resistor tied to an externally supplied reference voltage (recommended  $V_{EXTREF} = 2.4 \text{ V}$ ) along with the NTC thermistor generate a temperature dependent voltage on the TS\_BUS pin. The FAN54161's ADC must be enabled to measure and digitally compare the voltage at TS\_BUS to a programmed TBUS\_TH threshold. The ADC's measurement of the TS\_BUS voltage is monitored by the TBUSADC register. A digital comparison is made between the TBUSADC register contents and the TBUS\_TH threshold.

If the TBUSADC value falls below the TBUS\_TH threshold for more than  $t_{TBUS}_{TBAT}_{GLTCH}$ , the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW\_EN to 0
- 3. Set the TBUSOTP\_INT bit to 1 and pull the INT N pin low

There is no automatic recovery from this fault, and the host must program SW\_EN to 1 to close the switch again. The ADC is not affected by this fault and operates according to the ADC\_EN setting.

This digital comparison scheme does not restrict the use of NTC thermistor type or pullup resistor value. The desired TBUS\_TH threshold can be programmed based on the external components selected by the system designer.

#### **Battery Over-Temperature Fault**

The FAN54161 can monitor the temperature of the battery by measuring the battery pack's thermistor output pin. This protection prevents bypass charging from continuing if the battery temperature rises to a dangerous level. A TS\_BAT pull-up resistor tied to an externally supplied reference voltage (recommended V<sub>EXTREF</sub> = 2.4 V) along with the battery pack's NTC thermistor generate a temperature dependent voltage on the TS\_BAT pin. The FAN54161's ADC must be enabled to measure and digitally compare the voltage at TS\_BAT to a programmed TBAT\_TH threshold. The ADC's measurement of the TS\_BAT voltage can be monitored by the TBATADC register. A digital comparison is made between the TBATADC register contents and the TBAT\_TH threshold.

If the TBATADC value falls below the TBAT\_TH threshold for more than  $t_{TBUS\_TBAT\_GLTCH}$ , the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW\_EN to 0
- 3. Set the TBATOTP\_INT bit to 1 and pull the INT\_N pin low

There is no automatic recovery from this fault, and the host must program SW\_EN to 1 to close the switch. The ADC is not affected by this fault and operates according to the ADC EN setting.

This digital comparison scheme does not restrict the use of NTC thermistor type or pullup resistor value. The desired TBAT\_TH threshold can be programmed based on the external components selected by the system designer.

#### **Thermal Shutdown Protection**

When the FAN54161's junction temperature exceeds the thermal shutdown threshold ( $T_{SDN(TH)}$ ), the IC will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW EN to 0
- 3. Set the TSDN\_INT bit to 1 and pull the INT\_N pin low

4. Disable ADC conversion and ADC reference.

ADC enters standby state, maintains ADC\_EN=1

There is no automatic recovery from this fault, and the host must program SW\_EN to 1 to close the switch again.

### **IBUS Over Current Protection**

If the input current through the bypass switch exceeds the programmed  $I_{BUSOCP(TH)}$  threshold, the bypass switch will be forced open to protect the IC, battery, and system from an over-current fault condition. The IBUSOCP\_MODE control bit determines the manner in which the bypass switch will react to an IBUS over-current fault event. The IC internally monitors the IBUS current through the bypass switch.

When IBUSOCP\_MODE=0 and  $I_{BUS} > I_{BUSOCP(TH)}$  for more than  $t_{IBUSOCPGLTCH}$ , the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW\_EN to 0
- 3. Set the IBUSOCP\_INT bit to 1 and pulls the INT\_N pin low
- 4. Rely on the host processor to send a SW\_EN=1 command to close the switch again

When IBUSOCP\_MODE=1 and  $I_{BUS} > I_{BUSOCP(TH)}$  for more than  $t_{IBUSOCPGLTCH}$ , the FAN54161 will:

- 1. Enter the Hiccup Mode cycle and isolate VBUS and VOUT by opening the bypass switch
- 2. Maintain SW\_EN =1 during hiccup mode retry
- 3. Wait 100 ms, close the bypass switch to check if the IBUS over-current condition is removed
- If the IBUS over-current condition is removed, the bypass switch will remain closed, keep SW\_EN=1, and exit the Hiccup Mode cycle
- If the IBUS over-current condition remains, the Hiccup Mode cycle (starting from step 1) is repeated up to 6 more times
- If the IBUS over-current condition remains after 6 attempts, the IBUSOCP\_INT interrupt bit is set to 1 and the INT\_N pin is pulled low. The bypass switch is forced open and SW\_EN is reset to 0 and the host processor must set SW\_EN=1 to close the switch again

The ADC is not affected by this fault and operates according to the ADC\_EN setting.

### Watchdog Timer

To prevent unattended charging that may potentially damage the battery and/or system while the bypass switch is closed, the FAN54161 uses a watchdog timer as an additional layer of protection. The WDT control bits set the watchdog timer period and whether the watchdog timer protection will be enabled. If enabled, the watchdog timer starts when SW\_EN is programmed to 1. To clear the watchdog timer, the host processor must execute an I<sup>2</sup>C read or write command to any of the FAN54161's I<sup>2</sup>C registers. When changing the setting of the watchdog timer

in REG 0x06h[3:2], the new watchdog setting will not take effect until the next I<sup>2</sup>C read/write transaction.

If the host processor fails to clear the watchdog timer and allows the watchdog timer to expire, the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset all registers to their default values
- 3. Set the TIMER\_INT bit to 1 and pull the INT\_N pin low

### **VOUT Over-Voltage Protection**

If the voltage applied to the VOUT pin exceeds the programmed  $V_{OUTOVP(TH)}$  threshold for more than t<sub>VOUTOVPGLTCH</sub>, the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW\_EN to 0
- 3. Set the VOUTOVP\_INT bit to 1 and pull the INT\_N pin low

If a VOUT OVP fault occurs, the host processor should reprogram the FAN54161's charge parameter settings to prevent a VOUT OVP fault from reoccurring the next time the bypass switch is closed. Once the VOUT OVP fault is removed, the host processor must set SW\_EN to 1 in order to close the bypass switch again. The switch will not close again until after VOUT has fallen below  $V_{OUTOVP(TH)} - V_{OUTOVP(HYS)}$ .

The VOUT over-voltage protection feature serves as an additional layer of protection in case the VOREG CV regulation loop is not fast enough to respond to a VOUT over-voltage fault, or if VOREG regulation is disabled.

The ADC is not affected by this fault and operates according to the ADC\_EN setting.

### **IBUS Reverse Current Protection**

If the reverse current through the bypass switch (from VOUT to VBUS) rises above the programmed  $I_{RCB(TH)}$  threshold, the bypass switch will be forced open to prevent excessive reverse current flow from the battery back to the input source. The IRCB control bit sets the  $I_{RCB(TH)}$  reverse current threshold (0 = 100 mA, 1 = 3 A). The direction of  $I_{RCB(TH)}$  is defined as current flow from VOUT to VBUS. The IC internally monitors the IBUS current through the bypass switch.

When the current from VOUT to VBUS rises above  $I_{RCB(TH)}$  for more than the  $t_{RCBGLTCH}$  deglitch time, the FAN54161 will:

- 1. Isolate VBUS from VOUT by opening the bypass switch
- 2. Reset SW\_EN to 0
- 3. Set the IBUSRCB\_INT bit to 1 and pull the INT\_N pin low
- 4. Rely on the host processor to send a SW\_EN=1 command to close the switch again

The ADC is not affected by this fault and operates according to the ADC\_EN setting.

#### VFAIL Detection

In bypass charging applications, a failure of the bypass charging switch (however, this is rare) could result in the travel adapter output being directly connected to the battery pack which can cause a potentially dangerous system fault. A V<sub>FAIL</sub> comparator monitors the voltage at PMID while the bypass switch is open to detect the presence of a leakage path from VBUS to PMID (when TA is attached) or VOUT to PMID (when battery is connected) which would indicate a failure in the bypass charging FET. During VFAIL detection, a R<sub>FAIL</sub> pulldown resistor is connected to PMID and a comparator checks if the PMID voltage exceeds the VFAIL threshold. R<sub>FAIL</sub> will be disconnected from PMID anytime the bypass switch is enabled to avoid power consumption during bypass charging.

If the detection determines that  $V_{PMID} > V_{FAIL}$  for more than  $t_{VFAIL}$  GLTCH, the FAN54161 will:

1. Set the VFAIL\_INT bit to 1 and pull the INT\_N pin low

A VFAIL interrupt alerts the host that damage to the bypass charging FET has occurred. The host can then alert the system bypass charging controller to clamp the travel adapter's output voltage to the battery pack's float voltage to prevent an overcharge of the battery. Additionally, the host can alert the end user that the portable device is damaged and should be returned for repair.

If VFAIL\_EN=1, VFAIL detection is momentarily activated when:

- 1. SW\_EN is set from 0 to 1, while ADC\_EN=0 and RESET\_N=1. VFAIL detection occurs before the charge pump gate drive turns on the bypass charging FET but after the main bandgap reference is enabled
- 2. ADC\_EN is set from 0 to 1, while SW\_EN=0 and RESET\_N=1

#### **Regulation Loops**

Figure 11 illustrates the logic that causes the FAN54161 to enter regulation mode.

Either of the following four fault protections being triggered can cause the switch to operate in regulation mode as follows:

- 1. If the voltage at VOUT exceeds V<sub>OREG(TH)</sub>, and VOREG\_EN=1, the bypass switch will be regulated such that V<sub>OUT</sub> is limited to V<sub>OREG(TH)</sub>.
- 2. If the voltage across SNSP and SNSN exceeds  $V_{BATREG(TH)}$ , and VBATREG\_EN=1, the bypass switch will be regulated such  $V_{BAT}$  is limited to  $V_{BATREG(TH)}$ .
- 3. If  $I_{BAT}$  (sensed as a voltage across SRP and SRN) exceeds  $I_{BATREG(TH)}$ , and IBATREG\_EN=1, the bypass switch will be regulated such that  $I_{BAT}$  is limited to  $I_{BATREG(TH)}$ .
- 4. If I<sub>BUS</sub> (from VBUS to VOUT) exceeds I<sub>BUSREG(TH)</sub>, and IBUSREG\_EN=1, the bypass switch will be regulated such that I<sub>BUS</sub> is limited to I<sub>BUSREG(TH)</sub>.

It must be noted that the switch essentially becomes more resistive during regulation mode. This will cause more power dissipation in the switch and a greater likelihood of the junction temperature reaching or exceeding the shutdown threshold  $T_{\text{SDN(TH)}}$ . Therefore it is imperative for the system host controller to update the system configuration such that none of the above four monitors are triggered. This can be done by increasing the thresholds in the FAN54161 or changing other external system parameters (ex: adapter voltage or current limit).



Figure 11. Switch Regulation Mode Entry Diagram

### External N-Channel MOSFET Gate Control (OVP\_C)

The FAN54161 utilizes an additional protection scheme to protect the bypass switch from over voltage faults up to 32 V. Integrating a charge pump based gate control circuit, the FAN54161 can sense an over voltage fault applied to the VUSB input pin while controlling an external N-channel MOSFET to isolate the over voltage fault condition from the bypass switch's VBUS input pin. The VUSB pin serves as the power supply input for the charge pump gate control and also as the sense pin for an VUSB over voltage fault. Connect an at least 32 V rated N-channel MOSFET with its source to VBUS, drain to VUSB, and gate to OVP\_C.

The OVP\_C gate control pin will enable the external N-channel MOSFET when  $V_{USBUVLO(TH)} < V_{USB} < V_{USBOVP(TH)}$ . If  $V_{USB} < V_{USBUVLO(TH)}$  or  $V_{USB} > V_{USBOVP(TH)}$ , the OVP\_C gate control will disable the external N-channel MOSFET and set the appropriate VUSB fault interrupt.

The OVP\_C gate control and VUSB OVP detection circuits operate completely independent of the bypass switch and are solely powered by the VUSB input. If an external N-channel MOSFET is not used, the VUSB pin must be left floating and the OVP\_C pin must be connected to VBUS (preferred) or can be left floating. This will not affect bypass switch operation.

#### Interrupt Mechanism

Figures 10 and 11 illustrate the interrupt and mask architecture that drives the INT N pin.

The FAN54161 features interrupt flag and interrupt mask registers that contain interrupt bits for all the fault protection monitors, in addition to interrupt flags for other events. All interrupt bits are clear–on–read. When an interrupt flag bit

is set in the INT1, INT2 or INT3 register and its corresponding mask bit is a 0 (unmasked), the INT\_N pin is asserted low. For proper interrupt reporting, the ADC must be enabled or the switch closed.

### Analog to Digital Converter

#### **Feature Summary**

The integrated 10-bit Analog-to-Digital Converter in the FAN54161 comprises the following features:

- 1. Fully Differential Input high-accuracy SAR ADC
- 2. Up to 9 channels that can be independently configured for conversion

(i) Hardware protection based on digitized result of connector (VBUS) temperature and Battery temperature

- 3. Single-shot or Continuous conversion
- 4. Fast throughput

(i) 54  $\mu$ s conversion time for a single channel without averaging

(ii) 1166µs conversion time for all 9 channels with 16 samples per channel

5. Configurable averaging

(i) Enable/Disable for all channels

(ii) Programmable options of 8- or 16-sample average per channel

6. Post-processed Output Format

(i) ADC output format removes the need for host post-processing

7. Fully configurable through digital I<sup>2</sup>C interface
(i) Interrupt based indication of conversion completion

### ADC Power Supply

The ADC operation is primarily focused during charging when a valid input is present at VBUS. However, the ADC can operate with a valid supply on VOUT (possibly from the battery) even without a valid VBUS input. For reliable operation, the voltage at VBUS or VOUT should be no less than 3.1 V.

The ADC does not restrict the conversion of the VBUS or IBUS channels when a valid VBUS is not present. If the channel is enabled and conversion is started, the ADC will report the result of whatever the voltage and currents are for VBUS and IBUS which would typically be zero.

### ADC Channel Summary

Table 8 demonstrates all the possible channels that the ADC in the FAN54161 can be configured to convert.

- 1. Every signal is processed through an analog
  - pre-scalar circuit that converts the incoming signal range in volts, amps or °C to the ADC input range.

- 2. IBAT has special considerations since it measures current through a sense resistor that is part of the external application circuit. Depending on the  $R_{sense}$  value used, RSENSE should be programmed for the correct ADC reading on IBAT.
- 3. T\_BUS and T\_BAT are meant for measuring external NTC voltages pulled up externally to 2.4V. However, they can also be used as general purpose inputs that conform to the same signal range shown in the table.
- 4. The accuracy referred to the input is based on error analysis of the entire signal chain comprising the pre-scalars and the ADC. Refer to the Electrical Characteristics table of the ADC for the referenced parameters.

Channel #	Name	Signal Range (V, A, °C)	LSB Step (mV, mA, °C)	Input Referred Accuracy (mV, mA, °C) at room temp
0	VBUS	0.3 to 6.1	7.3	11
1	VOUT	0 to 5.0	5.3	14
VBAT (charging)		2.5 to 5.0	5.3	14
2	VBAT (discharging)	2.5 to 5.0	5.3	11
3	VDROP	0 to 1.0	2.9	6
4	IBUS	0 to 7.0	14.6	34
5	IBAT	-7.0 to +7.0	14.6	73
6	T_BUS	0 to 2.4	2.9	12
7	T_BAT	0 to 2.4	2.9	12
8	T_DIE	25 to 150	0.067	1

### Table 8. ADC CHANNEL SUMMARY

#### **ADC Configuration**

There are two registers, ADC\_CHANNEL and ADC\_CONTROL, which are used to configure and control the ADC. All 9 channels have independent enable bits which reside in these registers.

The ADC\_CONTROL register and ADC\_CHANNEL register values should not be reprogrammed when the ADC is performing a conversion.

#### ADC Control

The ADC can be configured to perform a one-shot conversion or perform continuous conversion by setting the ADC RATE bit to 1.

An ADC conversion is initiated by setting the ADC\_EN bit to 1. Once initiated, the ADC will convert the channels enabled for conversion according to the average mode selected (programmed by AVG\_EN and SAMPLES). The enabled ADC channels are converted in order (LSB to MSB of ADC\_CHANNEL register), followed by the ICTEMP bit in the ADC CONTROL register.

- If the ADC\_RATE bit is 0 (one-shot conversion), the ADC stores the results in the appropriate registers and sets the ADC\_DONE interrupt bit. The ADC\_EN bit is cleared to 0 after the conversion of all channels is complete.
- If the ADC\_RATE bit is 1 (continuous conversion), the ADC stores the results in the appropriate registers and immediately begins a new conversion. In order to stop conversions, it is recommended to set the ADC\_RATE bit to 0. This will ensure a complete conversion where the ADC\_DONE interrupt bit is set and the ADC\_EN bit is cleared to 0 similar to a normal one-shot conversion.
  - Writing a 0 to the ADC\_EN bit during continuous conversion is not recommended. This will immediately stop conversion without completing even the currently scheduled channel's conversion. The ADC DONE interrupt bit will not be set.

#### **ADC Output Format**

Each channel of the ADC has a dedicated pair of registers (an MSB register and an LSB register) where the input referred results are stored after a conversion is completed. Each pair is used to report the ADC's converted result and polarity in binary format.

**Example 1:** if the IBAT current is 5 A, the ADC's output in 10-bit format is converted back to represent 5 A = 5000 mA = 0b0000100111000100. This value is stored in the registers IBAT MSB and IBAT LSB.

If IBAT is -5 A instead, the final result stored in 0b1000100111000100.

#### **ADC Result Access**

The required sequence for reading the results of any ADC channel is to first read its MSB register followed by its LSB register.

If the ADC is in one-shot conversion mode (ADC\_RATE = 0), the host should issue  $I^2C$  read commands to any of the results registers (REG 0x13 to 0x23) after the ADC\_DONE interrupt is issued.

If the ADC is in continuous conversion mode  $(ADC\_RATE = 1)$ , the host can issue I<sup>2</sup>C read commands to any of the results registers (REG 0x13 to 0x23) even while the ADC is performing conversions and storing results in these registers.

#### **ADC Based Over-temperature Protection**

The two pins TS\_BUS and TS\_BAT are used to measure temperature of the VBUS connector and the battery respectively, by measuring voltage of an external NTC thermistor. This thermistor has an external pull–up to a 2.4 V supply. The ADC also converts the signal on these two pins to 10–bit results and stores them in the registers TBUS\_MSB, TBUS\_LSB, TBAT\_MSB and TBAT\_LSB respectively. These results are used in the following manner described to provide hardware protection for over-temperature of the VBUS connector or battery. The logic to explain this is illustrated in Figure 12.

- There are two registers to configure a digital over-temperature threshold called TBUSOTP and TBATOTP respectively.
- When the voltage measured by the ADC on TS\_BUS or TS\_BAT drops below the value in the registers TBUSOTP or TBATOTP respectively, the over-temperature hardware protection is triggered.
- If TBUSOTP\_EN or TBATOTP\_EN bits in the PROTECT\_EN register are set to 1, and in addition, the corresponding TBUSADC\_EN or TBATADC\_EN bits are enabled, then the TBUSOTP or TBATOTP fault being triggered will result in the switch of the FAN54161 to be opened.
- This also causes the interrupt bit TBUSOTP\_INT or TBATOTP\_INT to be set accordingly, and if unmasked, will assert the INT\_N pin low.

**Example 1:** TBUSOTP\_EN = 1 and TBUSADC\_EN = 1 If the output of the ADC for the TBUS channel (TBUS\_MSB, TBUS\_LSB) drops below the value programmed in TBUSOTP, the switch will open and TBUSOTP\_INT will be set.

**Example 2:** TBATOTP\_EN = 1 and TBATADC\_EN = 0 If the output of the ADC for the TBAT channel (TBAT\_MSB, TBAT\_LSB) drops below the value programmed in TBATOTP, the switch will not open and the TBATOTP\_INT will not be set.

Although the value in the ADC result registers exceeds that in the threshold register, since the ADC is not enabled to convert that channel, the result cannot be trusted and hence is not allowed to control the switch.



Figure 12. ADC Monitored Hardware Protection Diagram

### I<sup>2</sup>C Interface

### Introduction

The FAN54161 I<sup>2</sup>C specification is compatible with the Standard, Fast Mode, Fast Mode+ and High Speed Mode specifications.

- The FAN54161's SCL pin is an input and the SDA pin is an open-drain bi-directional output.
- The SDA pin pulls the the SDA bus low only when data is being read out from the FAN54161 or during the "acknowledge" bit duration of a valid I<sup>2</sup>C transaction.
- All data is shifted in MSB first (Bit 7).
- The FAN54161 supports single register read and write transactions as well as multiple register read transactions.

### Selectable I<sup>2</sup>C Slave Address

The ADR pin sets the 7-bit  $I^2C$  slave address of the device. The FAN54161 can be set for three unique slave addresses. To set the 7-bit slave address to 0x65h, tie the ADR pin to a valid supply with a 10 kOhm pullup. To set the slave address to 0x66h, float the ADR pin. To set the slave address to 0x67h, connect the ADR pin to ground.

Note that the ADR pin logic state is checked in order to set the corresponding  $I^2C$  address during power-up from previous state of no power supply or when the RESET\_N pin is toggled from LOW to HIGH.

Table 9. I <sup>2</sup> C Slave Add	Iress when ADR =	High (0x65h, 7 bit
-------------------------------------	------------------	--------------------

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	0	1	Х

Table 10. I<sup>2</sup>C Slave Address when ADR = Float (0x66h, 7 bit)

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	1	0	Х

 Table 11. I<sup>2</sup>C Slave Address when ADR = Low (0x67h, 7 bit)

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	1	1	Х

### **Bus Timing**

Data is transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically data transitions at or after the subsequent falling edge of SCL in order to provide ample setup time for the next data bit to be ready before the subsequent rising edge of SCL.



Figure 13. Data Transfer Timing

The idle state of the  $I^2C$  bus is SDA and SCL both in the high state. A valid transaction begins with a START condition which occurs when SDA transitions from HIGH to LOW when SCL remains HIGH.



Figure 14. I<sup>2</sup>C Start Condition

A valid transaction ends with a STOP condition which occurs when SDA transitions from LOW to HIGH when SCL remains HIGH.



Figure 15. I<sup>2</sup>C Stop Condition

A REPEATED START condition is functionally equivalent to a STOP condition followed immediately by a START condition.

### **Read and Write Transactions**

### **Single Register Write Transaction**

The FAN54161 supports the following protocol to write to a single register at a time.



Figure 16. Single Register Write Transaction

### Single Register Read Transaction

The FAN54161 supports the following protocol to read from a single register at a time.



#### Figure 17. Single Register Read Transaction

#### **Multiple Register Read Transaction**

The FAN54161 supports the following protocol to read from multiple registers at a time.



### PCB Layout and Component Placement

Proper PCB layout and component placement will provide an optimal thermal relief path for the FAN54161 IC as well as a low impedance charging path. The VBUS (A6 through G6) and VOUT (A3/A4 through G3/G4) balls, and the associated charging path, carry the majority of the charging current when the FAN54161 switch is closed.

Layout recommendations:

- Increase copper weight to greater than 1 oz, if possible.
- Use large as possible copper area for both VBUS and VOUT planes and ensure that copper floods the landing pads of all the VBUS and VOUT balls.
- Place via-in-pad on all VBUS and VOUT landing pads and mirror the top layer copper to the bottom layer for an additional thermal relief path.
  - Follow the recommended placement for CBUS and COUT shown in Figure 19.
- Place a floating copper plane on PMID (A5 through G5) to provide an additional thermal relief path.
  - Place via-in-pad on all PMID landing pads and mirror the top layer copper to the bottom layer for an additional thermal relief path.



Figure 19. VBUS and VOUT Copper Top Layer Routing

# I<sup>2</sup>C Registers and Bit Descriptions

### **Register Map**

Register			Bit Name						
Name	Adr	7	6	5	4	3	2	1	0
IC INFO	00h	Reserved	Reserved		REV			PN	
INT1 MASK	01h	VBUSOVP_M	IBUSREG_M	VBATREG_M	IBATREG_M	VOREG_M	TBUSOTP_M	TBATOTP_M	IBUSRCB_M
INT2 MASK	02h	Reserved	ADCDONE_M	VDROPALM_M	VDROPOVP_M	VBUSINSERT_M	VBATINSERT_M	TSDN_M	IBUSOCP_M
INT1	03h	VBUSOVP_INT	IBUSREG_INT	VBATREG_INT	IBATREG_INT	VOREG_INT	TBUSOTP_INT	TBATOTP_INT	IBUSRCB_INT
INT2	04h	Reserved	ADCDONE_INT	VDROPALM_INT	VDROPOVP_INT	VBUSINSERT_INT	VBATINSERT_INT	TSDN_INT	IBUSOCP_INT
PROTECT_EN	05h	VBUSOVP_EN	IBUSREG_EN	VBATREG_EN	IBATREG_EN	VOREG_EN	TBUSOTP_EN	TBATOTP_EN	VBUSPD_EN
SW_CONTROL	06h	VDROPOVP_EN	VDROPALM_EN	RSENSE	SW_EN	W	т	IRCB	REG_RST
ADC_CONTROL	07h	ICTEMPADC_EN	Reserved	Reserved	Reserved	ADC_EN	ADC_RATE	AVG_EN	SAMPLES
ADC_CHANNEL	08h	VBUSADC_EN	IBUSADC_EN	VOUTADC_EN	VDROPADC_EN	VBATADC_EN	IBATADC_EN	TBUSADC_EN	TBATADC_EN
PROT_DELAY	09h		IBUSC	CP_TH		Reserved	Reserved	IBUSOCP_MODE	OVP_DLY
VBUSOVP	0Ah	Reserved				VBUSOVP_TH			
VOREG	0Bh	Reserved				VOREG			
VDROPOVP	0Ch				VDR	OPOVP_TH			
VDROP_ALM	0Dh				VD	ROP_ALM			
VBATREG	0Eh	Reserved				VBATREG			
IBATREG	0Fh	Reserved				IBATREG			
IBUSREG	10h				I	BUSREG			
TBUSOTP	11h	Reserved				TBUS_TH			
TBATOTP	12h	Reserved				TBAT_TH			
VBUS_MSB	13h	Reserved	Reserved	Reserved			VBUSADC_MSB		
VBUS_LSB	14h				VBU	SADC_LSB			
IBUS_MSB	15h	Reserved	Reserved	Reserved			IBUSADC_MSB		
IBUS_LSB	17h				IBU	SADC_LSB			
VOUT_MSB	17h	Reserved	Reserved	Reserved			VOUTADC_MSB		
VOUT_LSB	18h				VOU	JTADC_LSB			
VDROP_MSB	19h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VDROP	ADC_MSB
VDROP_LSB	1Ah				VDR	OPADC_LSB			
VBAT_MSB	1Bh	Reserved	Reserved	Reserved			VBATADC_MSB		
VBAT_LSB	1Ch				VBA	TADC_LSB			
IBAT_MSB	1Dh	IBATADC_POL	Reserved	Reserved			IBATADC_MSB		
IBAT_LSB	1Eh				IBA	TADC_LSB			
TBUS_MSB	1Fh	Reserved	Reserved	Reserved	Reserved		TBUSA	DC_MSB	
TBUS_LSB	20h				TBU	ISADC_LSB			
TBAT_MSB	21h	Reserved	Reserved Reserved TBATADC_MSB						
TBAT_LSB	22h		TBATADC_LSB						
ICTEMP_ADC	23h		ICTEMPADC						
CONTROL1	50h	TJSI	HDN	Reserved VOUTOVP_DLY VOUTOVP_EN VFAIL_EN IBUSRCB_EN IBUSOCP_E					IBUSOCP_EN
CONTROL2	51h	Reserved				VOUTOVP_TH			
INT3 MASK	52h	Reserved	Reserved	Reserved	Reserved	VOUTOVP_M	VFAIL_M	VUSBOVP_M	VUSBINSERT_M
INT3	53h	Reserved	Reserved	Reserved	TIMER_INT	VOUTOVP_INT	VFAIL_INT	VUSBOVP_INT	VUSBINSERT_INT
STATUS1	54h	VOREG_ST	VBATREG_ST	IBATREG_ST	IBUSREG_ST	VBUSINSERT_ST	VBATINSERT_ST	Reserved	VUSBINSERT_ST

### **Bit Descriptions**

Default values are in bold text. Default values are with  $V_{BAT} = 3.8$  V and  $V_{BUS} = open$ .

IC INFO				Register Address = 00h Default = 0000 1010			
Bit	Name	Default	Туре	Description			
7	Reserved	0	Read	Reserved. Always reads 0.			
6	Reserved	0	Read	Reserved. Always reads 0.			
5:3	REV	001	Read	This indicates the revision number of the IC.			
2:0	PN	010	Read	This indicates the part number of the IC.			

	INT1 M	ASK		Register Address = 01h Default = 0000 0000			
Bit	Name	Default	Туре	D	escription		
7	VBUSOVP_M	0	R/W	This is the interrupt mask for a VBUS over voltage fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
6	IBUSREG_M	0	R/W	This is the interrupt mask for an IBUS over current regulation event where the switch operates in regulation mode to limit the input current to the IBUSREG setting. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
5	VBATREG_M	0	R/W	This is the interrupt mask for the VBAT CV regulation loop. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
4	IBATREG_M	0	R/W	This is the interrupt mask for the IBAT CC regulation loop. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
3	VOREG_M	0	R/W	This is the interrupt mask for the VOUT Reset condition: RESET_N falling; RE	ΓCV regulation loop. G_RST=1; Watchdog Timer Expiry		
2	TBUSOTP_M	0	R/W	This is the interrupt mask for a T_BUS over temperature fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
1	TBATOTP_M	0	R/W	This is the interrupt mask for a T_BAT over temperature fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
0	IBUSRCB_M	0	R/W	This is the interrupt mask for an IBUS Reset condition: RESET_N falling; RE	reverse current fault. G_RST=1; Watchdog Timer Expiry		

	INT2 MA	ASK		Register Address = 02h	Default = 0000 0000		
Bit	Name	Default	Туре	D	Description		
7	Reserved	0	Read	Reserved. Always reads 0.			
6	ADCDONE_M	0	R/W	This is the interrupt mask for a comple Reset condition: RESET_N falling; RE	This is the interrupt mask for a completed ADC conversion. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
5	VDROPALM_M	0	R/W	This is the interrupt mask for when VDROP rises above its alarm threshold. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
4	VDROPOVP_M	0	R/W	This is the interrupt mask for when VDROP rises above its OVP threshold. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
3	VBUSINSERT_M	0	R/W	This is the interrupt mask for when VB VBUSUVLO(TH) – VBUSUVLO(HYS). Reset condition: RESET_N falling; RE	US rises above V <sub>BUSUVLO(TH)</sub> or falls below :G_RST=1; Watchdog Timer Expiry		
2	VBATINSERT_M	0	R/W	This is the interrupt mask for when V <sub>S</sub> V <sub>BATINSERT(TH)</sub> – V <sub>BATINSERT(HYS)</sub> . Reset condition: RESET_N falling; RE	<sub>NSP</sub> rises above V <sub>BATINSERT(TH)</sub> or falls below G_RST=1; Watchdog Timer Expiry		
1	TSDN_M	0	R/W	This is the interrupt mask for an IC thermal shutdown fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
0	IBUSOCP_M	0	R/W	This is the interrupt mask for an IBUS old is exceeded. Reset condition: RESET_N falling; RE	over current event where the IBUSOCP thresh- G_RST=1; Watchdog Timer Expiry		

	INT	1		Register Address = 03h	Default = 0000 0000
Bit	Name	Default	Туре	D	escription
7	VBUSOVP_INT	0	R/CLR	This interrupt bit is set when the VBUS Reset condition: RESET_N falling; RE	i voltage exceeds V <sub>BUSOVP(TH)</sub> . G_RST=1; Watchdog Timer Expiry
6	IBUSREG_INT	0	R/CLR	This interrupt bit is set when IBUS CC limit $I_{BUS}$ to $I_{BUSREG(TH)}$ . Reset condition: RESET_N falling; RE	loop operates the switch in regulation mode to G_RST=1; Watchdog Timer Expiry
5	VBATREG_INT	0	R/CLR	This interrupt bit is set when the VBAT CV loop is operating the switch in regulation mode to limit ( $V_{SNSP}-V_{SNSN}$ ) to $V_{BATREG(TH)}$ . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
4	IBATREG_INT	0	R/CLR	This interrupt bit is set when the IBAT CC loop is operating the switch in regulation mode to limit $I_{BAT}$ to $I_{BATREG(TH)}$ . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
3	VOREG_INT	0	R/CLR	This interrupt bit is set when the VOUT mode to limit V <sub>OUT</sub> to V <sub>OREG(TH)</sub> . Reset condition: RESET_N falling; RE	CV loop is operating the switch in regulation G_RST=1; Watchdog Timer Expiry
2	TBUSOTP_INT	0	R/CLR	This interrupt bit is set when the temperature of the T_BUS NTC thermistor has exceeded the T_BUS over temperature threshold. The ADC must have the TBUSOTP channel active to trigger this interrupt. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
1	TBATOTP_INT	0	R/CLR	This interrupt bit is set when the temperature of the T_BAT NTC thermistor has exceeded the T_BAT over temperature threshold. The ADC must have the TBATOTP channel active to trigger this interrupt. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
0	IBUSRCB_INT	0	R/CLR	This interrupt bit is set when the currer Reset condition: RESET_N falling; RE	nt from VOUT to VBUS exceeds I <sub>RCB(TH)</sub> . G_RST=1; Watchdog Timer Expiry

	INT2			Register Address = 04h	Default = 0000 0000	
Bit	Name	Default	Туре	De	escription	
7	Reserved	0	Read	Reserved. Always reads 0.		
6	ADCDONE_INT	0	R/CLR	This interrupt bit is set when ADC conve Reset condition: RESET_N falling; REC	ersion is complete in one-shot mode only a_RST=1; Watchdog Timer Expiry	
5	VDROPALM_INT	0	R/CLR	This interrupt bit is set when the VDROP voltages exceeds V <sub>DROPALM(TH)</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
4	VDROPOVP_INT	0	R/CLR	This interrupt bit is set when the VDROP voltages exceeds V <sub>DROPOVP(TH)</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
3	VBUSINSERT_INT	0	R/CLR	This interrupt bit is set when the ADC is $V_{BUSUVLO(TH)}$ or falls below $V_{BUSUVLO(TH)}$ triggered. Reset condition: RESET_N falling; REC	e enabled and VBUS voltage rises above <sub>TH)</sub> – V <sub>BUSUVLO(HYS)</sub> . This interrupt is edge a_RST=1; Watchdog Timer Expiry	
2	VBATINSERT_INT	0	R/CLR	This interrupt bit is set when the ADC is enabled and V <sub>SNSP</sub> rises above V <sub>BATIN</sub> - SERT(TH) or falls below V <sub>BATINSERT(TH)</sub> – V <sub>BATINSERT(HYS)</sub> . This interrupt is edge trig- gered. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
1	TSDN_INT	0	R/CLR	This interrupt bit is set when the die temperature exceeds T <sub>SDN(TH)</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
0	IBUSOCP_INT	0	R/CLR	This interrupt bit is set when the IBUS of Reset condition: RESET_N falling; REG	eurrent exceeds I <sub>BUSOCP(TH)</sub> . à_RST=1; Watchdog Timer Expiry	

	PROTE	CT_EN		Register Address = 05h	Default = 1111 1110	
Bit	Name	Default	Туре	[	Description	
7	VBUSOVP_EN	1	R/W	A 1 enables VBUS OVP protection. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
6	IBUSREG_EN	1	R/W	A 1 enables IBUS constant current regulation capability. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
5	VBATREG_EN	1	R/W	A 1 enables VBAT constant voltage regulation capability. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
4	IBATREG_EN	1	R/W	A 1 enables IBAT constant current regulation capability. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
3	VOREG_EN	1	R/W	A 1 enables VOUT constant voltage Reset condition: RESET_N falling; R	regulation capability. EG_RST=1; Watchdog Timer Expiry	
2	TBUSOTP_EN	1	R/W	A 1 enables T_BUS over temperature protection. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
1	TBATOTP_EN	1	R/W	A 1 enables T_BAT over temperature protection. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
0	VBUSPD_EN	0	R/W	A 1 enables an internal 100 Ohm pull Reset condition: RESET_N falling; R	down resistor on VBUS. EG_RST=1; Watchdog Timer Expiry	

	SW_CON	TROL		Register Address = 06h	Default = 0010 1000		
Bit	Name	Default	Туре		Description		
7	VDROPOVP_EN	0	R/W	A 1 enables the VDROP pro open whenever V <sub>BUS</sub> -V <sub>OU</sub> - Reset condition: RESET_N	ptection circuit. If this protection is enabled, the switch will $_{\Gamma} > V_{DROPOVP(TH)}$ for more than t <sub>VDROPGLTCH</sub> . falling; REG_RST=1; Watchdog Timer Expiry		
6	VDROPALM_EN	0	R/W	A 1 enables the VDROP alarm circuit. If this alarm is enabled, the IC will flag the host that $V_{BUS}-V_{OUT}$ has exceeded the $V_{DROPALM(TH)}$ . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
5	RSENSE	1	R/W	Program this bit according to the value of the external sense resistor across RSP and RSN.			
				Code RSENSE Value			
				0	5 mΩ		
				1	10 mΩ		
				Reset condition: RESET_N	falling; REG_RST=1; Watchdog Timer Expiry		
4	SW_EN	0	R/W	A 1 enables the switch and when the switch is opened	A 1 enables the switch and hardware protection. This bit will automatically reset to 0 when the switch is opened due to a fault condition other than VBUS UVLO.		
				Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
3:2	WDT	10	R/W	This enables and sets the duration of the watch dog timer. When enabled, the watchdog timer is reset by an $I^2C$ read or write command to any register of the FAN54161. A watchdog timer expiry opens the switch and generates an interrupt.			
				Code WDT Setting			
				00	Disabled		
				01	0.5 sec		
				10	1.0 sec		
				11	2.0 sec		
				Reset condition: RESET_N	falling; REG_RST=1; Watchdog Timer Expiry		
1	IRCB	0	R/W	This bit sets the reverse curverse current flow through t	rrent blocking protection threshold. The direction of re- he switch is from VOUT to VBUS.		
				Code	IRCB Threshold (mA)		
				0	100		
				1	3000		
				Reset condition: RESET_N	falling; REG_RST=1; Watchdog Timer Expiry		
0	REG_RST	0	W1CLR	Setting this bit will reset all I <sup>2</sup> C control and interrupt register bits (except status) to their default value. This bit is self-clear.			
				Code	Action		
				0	No Effect		
				1	Reset I <sup>2</sup> C control and interrupt bits to default values		
				Reset condition: RESET_N	falling; REG_RST=1; Watchdog Timer Expiry		

	ADC_CON	TROL		Register Address = 07h	Default = 1000 0111			
Bit	Name	Default	Туре	Description				
7	ICTEMPADC_EN	1	R/W	A 1 enables the ADC measurement of the IC temperature. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry				
6	Reserved	0	Read	Reserved. Always reads 0.				
5	Reserved	0	Read	Reserved. Always reads 0.				
4	Reserved	0	Read	Reserved. Always reads 0.				
3	ADC_EN	0	R/W	A 1 enables the ADC. Reset condition: RESET_N falling; RE	A 1 enables the ADC. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
2	ADC_RATE	1	R/W	This bit controls the conversion mode of the ADC.				
				Code ADC Mode				
				0	Single Conversion			
				1	Continuous Conversion			
				Reset condition: RESET_N falling; RE	G_RST=1; Watchdog Timer Expiry			
1	AVG_EN	1	R/W	A 1 enables ADC measurement avera Reset condition: RESET_N falling; RE	ging. G_RST=1; Watchdog Timer Expiry			
0	SAMPLES	1	R/W	This bit sets the number of samples us abled.	sed for an ADC conversion if averaging is en-			
				Code	# of ADC Averaging Samples			
				0	8			
				1 16				
				Reset condition: RESET_N falling; RE	G_RST=1; Watchdog Timer Expiry			

	ADC_CHAN	NEL		Register Address = 08h	Default = 1111 1111		
Bit	Name	Default	Туре	D	escription		
7	VBUSADC_EN	1	R/W	A 1 enables ADC measurement of V <sub>BUS</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
6	IBUSADC_EN	1	R/W	A 1 enables ADC measurement of I <sub>BL</sub> Reset condition: RESET_N falling; RE	A 1 enables ADC measurement of I <sub>BUS</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
5	VOUTADC_EN	1	R/W	A 1 enables ADC measurement of V <sub>OUT</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
4	VDROPADC_EN	1	R/W	A 1 enables ADC measurement of V <sub>DROP</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
3	VBATADC_EN	1	R/W	A 1 enables ADC measurement of V <sub>B</sub> Reset condition: RESET_N falling; RE	<sub>AT</sub> via V <sub>SNSP</sub> and V <sub>SNSN</sub> . :G_RST=1; Watchdog Timer Expiry		
2	IBATADC_EN	1	R/W	A 1 enables ADC measurement of I <sub>BAT</sub> through the sense resistor across SRP and SRN. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
1	TBUSADC_EN	1	R/W	A 1 enables ADC measurement of T_BUS. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
0	TBATADC_EN	1	R/W	A 1 enables ADC measurement of T_ Reset condition: RESET_N falling; RE	BAT. EG_RST=1; Watchdog Timer Expiry		

	PROT_DELAY			Register Address = 09h			De	fault = 1010 00	00	
Bit	Name	Default	Туре	Descri			iption	ption		
7:4	IBUSOCP_TH	1010	R/W	This sets the over protection	IBUS over current on threshold, the	ent protection the switch will ope	reshold. When and an interr	IBUS rises abo upt will be gene	ve the IBUS rated.	
				Code	IBUS OCP T	hreshold (A)				
				0000	0	.5				
				0001	0	.5				
				0010	1	.0				
				0011	1	.5				
				0100	2	.0				
				0101	2	.5				
				0110	3	.0				
				0111	3	.5				
				1000	4	.0				
				1001	4	.5				
				1010	5	.0				
				1011	5	.5				
				1100	6	.0				
				1101	6	.5				
				1110	7	.0				
				1111	7	.5				
				Reset conditi	on: RESET_N f	alling; REG_RS	T=1; Watchdog	g Timer Expiry		
3	Reserved	0	Read	Reserved. Al	ways reads 0.					
2	Reserved	0	Read	Reserved. Al	ways reads 0.					
1	IBUSOCP_MODE	0	R/W	This bit cont	rols the IBUS ov	ver current prote	ection mode of	operation.		
				Code	IBUS ( Ov	OCP Response ver Current Fau	e After ult	IBUS OCP Deglitch Time		
				0	Open swit	ch and reset S	W_EN = 0	50 µs		
				1	Hiccup Mode tempt to close 7 times before current fault s	(open switch ar e switch every 1 e latching switch till exists)	nd then at- 00 ms up to n open if over	8 µs		
				Reset conditi	on: RESET_N f	alling; REG_RS	T=1; Watchdog	g Timer Expiry		
0	OVP_DLY	0	R/W	This bit sets the deglitch time of the VBUS and VDROP over voltage protection circuits.						
				Code	VBUS OVP Deglitch Time (μs)	VDROP OVP Deglitch Time (μs)	VDROP Alarm Deglitch Time (μs)			
				0	4	4	4			
				1	20	20	20			
				Reset conditi	on: RESET_N f	alling; REG_RS	T=1; Watchdo	g Timer Expiry		

	VBUSC	OVP		Register Address = 0Ah		Default = 0011 0100	
Bit	Name	Default	Туре	Description			
7	Reserved	0	Read	Reserved. Always reads 0.			
6:0	VBUSOVP_TH	0110100	R/W	This sets the VBUS over voltage protection threshold. When VBUS rises above the VBUS over protection threshold, the switch will open and an interrupt will be generated.			
				Code	VBUSOVP Threshold (V)		
				0000000	4.200		
				0000001	4.225		
				0000010	4.250		
				-	-		
				0110100	5.500		
				-	-		
				1011100 to 1111111 6.500			
				Reset condition: RESET	N falling; REG_RST=1; Watch	dog Timer Expiry	

	VOR	EG		Register Address = 0Bh Default = 00		Default = 0001 0100
Bit	Name	Default	Туре		Description	
7	Reserved	0	Read	Reserved. Always reads 0.		
6:0	VOREG	0010100	R/W	This sets the VOREG regulation threshold of the VOUT CV loop. When VOUT rises to the VOREG threshold, the switch will operate in regulation mode and limit VOUT to the VOREG threshold.		
				Code		
				0000000	4.20	
				0000001	4.21	
				0000010	4.22	
				-	-	
				0010100	4.40	
				-		
				1001111		
				1010000 to 1111111	5.00	
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry

	VDROP	OVP		Register Address = 0Ch Default = 0011 1100			
Bit	Name	Default	Туре		Description		
7:0	VDROPOVP_TH	00111100	R/W	This sets the VDROP over voltage protection threshold. When VDROP voltage rises above the VDROP over voltage protection threshold, the switch will open and an interrupt will be generated.			
				Code	VDROP OVP Threshold (V)		
				0000 0000	0		
				0000 0001	5		
				0000 0010	10		
				0000 0011	15		
				-	-		
				0011 1100	300		
				-	-		
				11000111	995		
				1100 1000 to 1111 1111	1000		
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry	

	VDROP	ALM		Register Address = 0Dh		Default = 0001 0100	
Bit	Name	Default	Туре	Description			
7:0	VDROP_ALM	00010100	R/W	This sets the VDROP alarm threshold. When VDROP voltage rises above the VDROP alarm threshold, an interrupt will be generated.			
				Code			
				0000 0000	0		
				0000 0001	5		
				0000 0010	10		
				-	-		
				0001 0100	100		
				-	-		
				1100 0111	995		
				1100 0000 to 1111 1111	1000		
				Reset condition: RESET	N falling; REG RST=1; Watch	dog Timer Expiry	

	VBAT	REG		Register Address = 0Eh		Default = 0000 1011	
Bit	Name	Default	Туре	Description			
7	Reserved	0	Read	Reserved. Always reads 0.			
6:0	VBATREG	0001010	R/W	This sets the VBATREG regulation threshold of the VBAT CV loop. When V <sub>SNSP</sub> -V <sub>SNSN</sub> rises to the VBATREG threshold, the switch will operate in regulation mode and limit V <sub>SNSP</sub> -V <sub>SNSN</sub> to the VBATREG threshold.			
				Code	VBATREG Threshold (V)		
				0000000	4.20		
				0000001	4.21		
				0000010	4.22		
				-	-		
				0001010	4.3		
				-	-		
				1001111	4.99		
				1010000 to 1111111 5.00			
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry	

	IBATR	EG		Register Address = 0Fh Default = 0010 1000			
Bit	Name	Default	Туре		Description		
7	Reserved	0	Read	Reserved. Always reads	s 0.		
6:0	IBATREG	0101000	R/W	This sets the IBATREG regulation threshold of the IBAT CC loop. When the measured IBAT current rises above the IBATREG threshold, the switch will operate in regulation mode to limit the IBAT current to IBATREG. The IBAT current is sensed using the SRP and SRN pins with an external R <sub>SENSE</sub> resistor.			
				Code	IBATREG Threshold (V)		
				0000000	0.10		
				0000001	0.10		
				0000010	0.10		
				0000011	0.15		
				-	-		
				0101000	2.00		
				-	-		
				1111101	6.25		
				1111110	6.30		
				1111111	6.35		
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry	

	IBUSE	REG		Register Address = 10h Default = 0100 01		Default = 0100 0110		
Bit	Name	Default	Туре	Description				
7:0	IBUSREG	01000110	R/W	This sets the IBUSREG regulation threshold of the IBUS CC loop. When the measured IBUS current rises above the IBUSREG threshold, the switch will operate in regula- tion mode to limit the IBUS current to IBUSREG. The IBUS current is sensed internally through the switch.				
				Code	IBUSREG Threshold (A)			
				0000 0000	0.10			
				0000 0001	0.10			
				0000 0010	0.10			
				0000 0011	0.15			
				-	-			
				0100 0110	3.50			
				-	-			
				1000 0000	6.40			
				1000 0001	6.45			
				1000 0010 to 1111 1111	6.50			
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry		

	TBUS	OTP		Register	Address = 11h	Default = 0001 1110			
Bit	Name	Default	Туре		Description				
7	Reserved	0	Read	Reserved. Always reads	i 0.				
6:0	TBUS_TH	0011110	R/W	This sets the T_BUS over temperature threshold. When the ADC measurement of the T_BUS voltage falls below the T_BUS over temperature voltage threshold, the switch will open and a VBUS connector over-temperature interrupt will be generated. An external NTC thermistor is used to measure the temperature of the VBUS connector.					
				Code T_BUS Over Temperature Threshold (V)					
				0000 0000	0.0				
				0000 0001	0.02				
				0000 0010	0.04				
				-	-				
				0011110	0.60				
				-	-				
				1110111	2.38				
				1111000 to 1111 1111 2.40					
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry			

	TBATO	ОТР		Register	Default = 0010 0011				
Bit	Name	Default	Туре		Description				
7	Reserved	0	Read	Reserved. Always reads	; 0.				
6:0	TBAT_TH	0100011	R/W	This sets the T_BAT over temperature threshold. When the ADC measurement of the T_BAT voltage falls below the T_BAT over temperature voltage threshold, the switch will open and a battery over-temperature interrupt will be generated. An external NTC thermistor can be used to measure the temperature of the battery.					
				Code T_BAT Over Temperature Threshold (V)					
				0000 0000	0.0				
				0000 0001	0.02				
				0000 0010	0.04				
				-	-				
				0100011	0.70				
				-	-				
				1110111	2.38				
				1111000 to 1111 1111	2.40				
				Reset condition: RESET	_N falling; REG_RST=1; Watch	dog Timer Expiry			

	VBUS_I	NSB		Register Ad	Register Address = 13h Default = 0000 0000		0000 0000
Bit	Name	Default	Туре		Descr	iption	
7	Reserved	0	Read	Reserved. Always re	ads 0.		
6	Reserved	0	Read	Reserved. Always reads 0.			
5	Reserved	0	Read	Reserved. Always reads 0.			
4:0	VBUSADC_MSB	00000	Read	VBUSADC_MSB along with VBUSADC_LSB form the 13 bit result of the VBUS voltage. When $V_{BUS}$ < 300mV, VBUSADC will report 0V.			
VBUSADC (b) V			VBUSADC (h)	VBUS (mV)			
				0000000000000	0000	0 to 299	
				0000100101100	012C	300	
				0000100101101	012D	301	
				-	-	-	
				1011111010011	17D3	6099	
				1011111010100	17D4	6100	
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry

	VBUS_	LSB		Register Address = 14h Default = 0000 0000		
Bit	Name	Default	Туре	Description		
7:0	VBUSADC_LSB	0000000	Read	VBUSADC_LSB along with VBUSADC_MSB ( the VBUS voltage. When V <sub>BUS</sub> < 300mV, VBU Reset condition: RESET_N falling; REG_RST=	REG 13h[4:0]) form the 13 bit result of JSADC will report 0V. -1; Watchdog Timer Expiry	

	IBUS_N	ISB		Register Address = 15h		Default = 0000 0000		
Bit	Name	Default	Туре		Descr	iption		
7	Reserved	0	Read	Reserved. Always rea	ads 0.			
6	Reserved	0	Read	Reserved. Always reads 0.				
5	Reserved	0	Read	Reserved. Always reads 0.				
4:0	IBUSADC_MSB	00000	Read	IBUSADC_MSB along with IBUSADC_LSB form the 13 bit result of the IBUS current.				
				IBUSADC (b)	IBUSADC (h)	IBUS (mA)		
				00000000000000	0000	0		
				000000000001	0001	1		
				000000000010	0002	2		
				-	-	-		
				1101101010111	1B57	6999		
				1101101011000	1B58	7000		
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry	

	IBUS_	LSB		Register Address = 16h Default = 0000 0000			
Bit	Name	Default	Туре	Description			
7:0	IBUSADC_LSB	00000000	Read	IBUSADC_MSB along with IBUSADC_LSB (R IBUS current.	EG15h[4:0]) form the 13 bit result of the		
				Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			

	VOUT_I	MSB		Register Ad	Register Address = 17h Default = 0000 0000		
Bit	Name	Default	Туре		Descr	iption	
7	Reserved	0	Read	Reserved. Always re	ads 0.		
6	Reserved	0	Read	Reserved. Always reads 0.			
5	Reserved	0	Read	Reserved. Always reads 0.			
4:0	VOUTADC_MSB	00000	Read	VOUTADC_MSB along with VOUTADC_LSB form the 13 bit result of the VOUT volt- age.			
			VOUTADC (b) VOUTADC (h) VOUT (mV)				
				00000000000000	0000	0	
				000000000001	0001	1	
				000000000010	0002	2	
				-	-	-	
				1001110000111	1387	4999	
				1001110001000	1388	5000	
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry

	VOUT_	LSB		Register Address = 18h Default = 0000 0000			
Bit	Name	Default	Туре	Description			
7:0	VOUTADC_LSB	00000000	Read	VOUTADC_LSB along with VOUTADC_MSB ( the VOUT voltage. Reset condition: RESET_N falling; REG_RST=	REG17h[4:0]) form the 13 bit result of =1; Watchdog Timer Expiry		

	VDROP_	MSB		Register Address = 19h Default = 0000 0000			0000 0000	
Bit	Name	Default	Туре		Descr	iption		
7	Reserved	0	Read	Reserved. Always re	ads 0.			
6	Reserved	0	Read	Reserved. Always re	ads 0.			
5	Reserved	0	Read	Reserved. Always re	Reserved. Always reads 0.			
4	Reserved	0	Read	Reserved. Always reads 0.				
3	Reserved	0	Read	Reserved. Always re	Reserved. Always reads 0.			
2	Reserved	0	Read	Reserved. Always re	Reserved. Always reads 0.			
1:0	VDROPADC_MSB	00	Read	VDROPADC_LSB all voltage = V <sub>BUS</sub> - V <sub>O</sub>	ong with VDROPADC_	MSB form the 10 bit re	esult of the VDROP	
				VDROPADC (b)	VDROPADC (h)	VDROP (mV)		
				000000000	0000	0		
				000000001	0001	1		
				000000010	0002	2		
				-	-	-		
				1111100111	3E7	999		
				1111101000	3E8	1000		
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry	

	VDROP	LSB		Register Address = 1Ah	Default = 0000 0000	
Bit	Name	Default	Туре	Description		
7:0	VDROPADC_LSB	00000000	Read	VDROPADC_LSB along with VDROPADC_MS of the VDROP voltage = V <sub>BUS</sub> – V <sub>OUT</sub> . Reset condition: RESET_N falling; REG_RST=	B (REG19h[1:0]) form the 10 bit result =1; Watchdog Timer Expiry	

	VBAT_N	MSB		Register Address = 1Bh Default = 0000 0000		0000 0000	
Bit	Name	Default	Туре	Description			
7	Reserved	0	Read	Reserved. Always reads 0.			
6	Reserved	0	Read	Reserved. Always reads 0.			
5	Reserved	0	Read	Reserved. Always re	Reserved. Always reads 0.		
4:0	VBATADC_MSB	00000	Read	VBATADC_LSB along with VBATADC_MSB form the 13 bit result of the $V_{BAT}$ = $V_{SNSP}$ – $V_{SNSN}.$			
				VBATADC (b)	VBATADC (h)	VBAT (mV)	
				0000000000000	0000	0	
				0000000000001	0001	1	
				000000000010	0002	2	
				-	-	-	
				1001110000111	1387	4999	
				1001110001000	1388	5000	1
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry

	VBAT_	LSB		Register Address = 1Ch Default = 0000 0000		
Bit	Name	Default	Туре	Description		
7:0	VBATADC_LSB	0000000	Read	$\label{eq:VBATADC_LSB} B along with VBATADC_MSB (R V_{BAT} = V_{SNSP} - V_{SNSN}.$ Reset condition: RESET_N falling; REG_RST=	EG1B[4:0]) form the 13 bit result of the 1; Watchdog Timer Expiry	

	IBAT_N	ISB		Register Address = 1Dh Default = 0000 0000			0000 0000
Bit	Name	Default	Туре		Descr	iption	
7	IBATADC_POL	0	Read	Polarity of IBAT_ADC result. 0 – positive (+) 1 – negative (–)			
6	Reserved	0	Read	Reserved. Always reads 0.			
5	Reserved	0	Read	Reserved. Always reads 0.			
4:0	IBATADC_MSB	00000	Read	<code>IBATADC_MSB</code> along with <code>IBATADC_LSB</code> form the 13 bit ADC measurement of the <code>IBAT</code> current measured through $R_{SENSE}$ across SRP and SRN pins.			
				IBUSADC (b)	IBUSADC (h)	IBUS (mA)	
				000000000000	0000	0	
				000000000001	0001	1	
				000000000010	0002	2	
				-	-	-	
				1101101010111	1387	6999	
				1101101011000	1388	7000	
				Reset condition: RESET	Γ_N falling; REG_R	ST=1; Watchdog Time	r Expiry

IBAT_LSB				Register Address = 1Eh Default = 0000 0000		
Bit	Name	Default	Туре	Description		
7:0	IBATADC_LSB	0000000	Read	IBATADC_LSB along with IBATADC_MSB (RE surement of the IBAT current measured throug Reset condition: RESET_N falling; REG_RST=	G1Dh[4:0]) form the 13 bit ADC mea- h R <sub>SENSE</sub> across SRP and SRN pins. =1; Watchdog Timer Expiry	

	TBUS_N	MSB		Register Add	Register Address = 1Fh Default = 0000 0000			
Bit	Name	Default	Туре	Description				
7	Reserved	0	Read	Reserved. Always reads 0.				
6	Reserved	0	Read	Reserved. Always reads 0.				
5	Reserved	0	Read	Reserved. Always reads 0.				
4	Reserved	0	Read	Reserved. Always reads 0.				
3:0	TBUSADC_MSB	0000	Read	TBUSADC_MSB along with TBUSADC_LSB form the raw bit ADC measurement of the TS_BUS voltage formed by the external NTC thermistor network used to sense the temperature of the input connector. A 2.4V external reference is recommended.				
				TBUSADC (b)	TBUSADC (h)	TBUS (mV)		
				0000000000000	0000	0		
				000000000001	0001	1		
				000000000010	0002	2		
				-	-	-		
				100101011111	95F	2399		
				100101100000	960	2400		
				Reset condition: RES	ET_N falling; REG_R	ST=1; Watchdog Time	r Expiry	

TBUS_LSB				Register Address = 20h Default = 0000 0000		
Bit	Name	Default	Туре	Description		
7:0	TBUSADC_LSB	0000000	Read	TBUSADC_LSB along with TBUSADC_MSB ( the TS_BUS voltage formed by the external N the temperature of the input connector. A 2.4V Reset condition: RESET_N falling; REG_RST=	REG1Fh[3:0]) form the 12 bit result of IC thermistor network used to sense external reference is recommended. =1; Watchdog Timer Expiry	

	TBAT_M	MSB		Register Address = 21h Default = 0000 0000			0000 0000	
Bit	Name	Default	Туре	Description				
7	Reserved	0	Read	Reserved. Always reads 0.				
6	Reserved	0	Read	Reserved. Always reads 0.				
5	Reserved	0	Read	Reserved. Always rea	Reserved. Always reads 0.			
4	Reserved	0	Read	Reserved. Always reads 0.				
3:0	TBATADC_MSB	0000	Read	TBATADC_MSB along with TBATADC_LSB form the 12 bit result of the TS_BAT volt- age formed by the external NTC thermistor network used to sense the temperature of the battery. A 2.4V external reference is recommended.				
				TBATADC (b)	TBATADC (h)	TBAT (mV)		
				00000000000000	0000	0		
				0000000000001	0001	1		
				000000000010	0002	2		
				-	-	-		
				100101011111	95F	2399		
				100101100000	960	2400		
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry	

	TBAT_	LSB		Register Address = 22h Default = 0000 0000			
Bit	Name	Default	Туре	Description			
7:0	TBATADC_LSB	0000000	Read	TBATADC_LSB along with TBATADC_MSB (re TS_BAT voltage formed by the external NTC th temperature of the battery. A 2.4V external refe Reset condition: RESET_N falling; REG_RST=	<ul> <li>3g21h[3:0]) form the 12 bit result of the nermistor network used to sense the prence is recommended.</li> <li>=1; Watchdog Timer Expiry</li> </ul>		

	ICTEMP_LSB			Register Address = 23h		Default = 0000 0000	
Bit	Name	Default	Туре	Description			
7:0	ICTEMPADC	00000000	Read	ICTEMPADC forms t	ICTEMPADC forms the 8 bit result of the IC's internal die temperature sensor.		
				ICTEMPADC (b)	ICTEMPADC (h)	ICTEMP (°C)	
				0000000	0	0	
				-	-	-	
				00011001	19	25	
				00011010	1A	26	
				00011011	1B	27	
				-	-	-	
				10010101	95	149	
				10010110	96	150	
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Time	r Expiry

	CONTROL1			Register Address = 50h		Default = 0100 0011	
Bit	Name	Default	Туре		Descr	iption	
7:6	TJSHDN	01	R/W	TJSHDN programs t	he thermal shutdown tl	nreshold.	
				Code	Junction Temperature Threshold (°C)		
				00	115		
				01	125		
				10	135		
				11	145		
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Timer Expiry	
5	Reserved	0	Read	Reserved			
4	VOUTOVP_DLY	0	R/W	This bit sets the deglitch time of the VOUT over voltage protection circuit.			
			VOUT OVP Code Deglitch Time (μS)				
				00	4		
				01	20		
				Reset condition: RES	SET_N falling; REG_R	ST=1; Watchdog Timer Expiry	
3	VOUTOVP_EN	0	R/W	A 1 enables the VOL switch is forced oper Reset condition: RES	JT OVP protection circ n. SET_N falling; REG_R	uit. If enabled and VOUT > VOUTOVP, the ST=1; Watchdog Timer Expiry	
2	VFAIL_EN	0	R/W	A 1 enables a detection mechanism that senses if the bypass switch is permanently shorted. RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
1	IBUSRCB_EN	1	R/W	A 1 (default setting) enables IBUS reverse current blocking protection. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry			
0	IBUSOCP_EN	1	R/W	A 1 (default setting) programmable IBUS Reset condition: RES	enables the IBUS over OCP threshold. SET_N falling; REG_R	current protection circuit that is set by a ST=1; Watchdog Timer Expiry	

	CONTR	OL2		Register Address = 51h Default = 0001 0100			
Bit	Name	Default	Туре	Description			
7	Reserved	0	Read	Reserved. Always rea	Reserved. Always reads 0.		
6:0	VOUTOVP_TH	0010100	R/W	This sets the VOUT OVP threshold. When VOUT rises above its OVP threshold, the switch will open.			
				Code	VOUT OVP Threshold (V)		
				0000000	4.50		
				0000001	4.51		
				0000010	4.52		
				-	-		
				0010100	4.70		
				-	-		
				1001111	5.29		
				1010000 to 1111111	5.30		
				Reset condition: RES	ET_N falling; REG_R	ST=1; Watchdog Timer Expiry	

INT3 MASK				Register Address = 52h	Default = 0000 0001	
Bit	Name	Default	Туре	Description		
7	Reserved	0	Read	Reserved. Always reads 0.		
6	Reserved	0	Read	Reserved. Always reads 0.		
5	Reserved	0	Read	Reserved. Always reads 0.		
4	Reserved	0	Read	Reserved. Always reads 0.		
3	VOUTOVP_M	0	R/W	A 1 sets the interrupt mask for a VOUT OVP fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
2	VFAIL_M	0	R/W	A 1 sets the interrupt mask for a VFAIL fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
1	VUSBOVP_M	0	R/W	A 1 sets the interrupt mask for a VUSBOVP fault. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
0	VUSBINSERT_M	1	R/W	A 1 (default setting) sets the interrupt mask for a VUSB insertion or removal event. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		

INT3				Register Address = 53h	Default = 0000 0000	
Bit Name Default Type			Туре	Description		
7	Reserved	0	Read	Reserved. Always reads 0.		
6	Reserved	0	Read	Reserved. Always reads 0.		
5	Reserved	0	Read	Reserved. Always reads 0.		
4	TIMER_INT	0	R/CLR	This interrupt is set when the watchdog timer has expired. Reset condition: RESET_N falling; REG_RST=1		
3	VOUTOVP_INT	0	R/CLR	This interrupt is set when VOUT exceeds V <sub>OUTOVP(TH)</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
2	VFAIL_INT	0	R/CLR	This interrupt is set when the common source voltage of the bypass switch is above the V <sub>FAIL</sub> threshold when the switch is open (SW_EN=0). A "1" would indicate that the bypass switch has failed and the host processor should flag the user to service the device. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
1	VUSBOVP_INT	0	R/CLR	This interrupt is set when V <sub>USB</sub> exceeds the V <sub>USBOVP</sub> threshold. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry		
0	VUSBINSERT_INT	0	R/CLR	This interrupt is set when $V_{USB}$ rises above $V_{LO(TH)} - V_{USBUVLO(HYS)}$ . When an extern floating VUSB pin can still exceed the $V_{US}$ event causing a false VUSBINSERT interview when no external FET is used to prevent to OVP event. Masking this bit does not preignored when an external OVP blocking F Reset condition: RESET_N falling; REG_I	<sup>re</sup> V <sub>USBUVLO(TH)</sub> or falls below V <sub>USBU</sub> - rnal OVP blocking FET is not used, the <sub>SBUVLO(TH)</sub> threshold during a VBUS OVP rupt. It is recommended to mask this bit the INT pin from pulling low due to a VBUS vent it from being set, so this bit should be 'ET is not used. RST=1; Watchdog Timer Expiry	

STATUS1				Register Address = 54h	Default = 0000 0100
Bit	Name	Default	Туре	Description	
7	VOREG_ST	0	Read	A 1 indicates that the VOREG CV regulation loop is active. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
6	VBATREG_ST	0	Read	A 1 indicates that the VBATREG CV regulation loop is active Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
5	IBATREG_ST	0	Read	A 1 indicates that the IBATREG CC regulation loop is active. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
4	IBUSREG_ST	0	Read	A 1 indicates that the IBUSREG CC regulation loop is active. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
3	VBUSINSERT_ST	0	Read	A 1 indicates that V <sub>BUS</sub> is above V <sub>BUSUVLO(TH)</sub> . When the switch is open (SW_EN=0) and the ADC is disabled (ADC_EN=0), this bit is latched to 0 regardless if there is a valid source on VBUS. Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
2	VBATINSERT_ST	1	Read	A 1 indicates that V <sub>SNSP</sub> is above V <sub>BATINSERT(TH)</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	
1	Reserved	0	Read	Reserved. Always reads 0.	
0	VUSBINSERT_ST	0	Read	A 1 indicates that V <sub>USB</sub> is above V <sub>USBUVLO(TH)</sub> . Reset condition: RESET_N falling; REG_RST=1; Watchdog Timer Expiry	

### PRODUCT SPECIFIC DIMENSIONS

Product	D (mm)	E (mm)	X (mm)	Y (mm)
FAN54161UCX	2.78 +/-0.03	3.06 +/-0.03	0.370	0.310

### PACKAGE DIMENSIONS





- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE
- PER ASMEY14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS
  - ∧ 612 ± 38 MICRONS (574-650 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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#### ООО "ЛайфЭлектроникс"

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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