NCP370

Positive and Negative Overvoltage Protection with Internal Low R_{ON} N-MOSFETs and Reverse Charge Control Pin

The NCP370 is an overvoltage, overcurrent and reverse control device. Two main modes are available by setting logic pins. First mode is Direct Mode from Wall−Adapter to the system. In this mode the system is both positive and negative over−voltage protected up to +28 V and down to −28 V. The wall adapter (or AC/DC charger) is disconnected from the system if the input voltage exceeds the overvoltage (OVLO) or undervoltage (UVLO) thresholds. At power up, the V_{out} turns on 30 ms after the V_{in} exceeds the undervoltage threshold.

The second mode (see Tables 1 & 2), called the Reverse Mode, allows an external accessory to be powered by the system battery or boost converter. Here the external accessory would be connected to the device input (bottom connector of system) and the device battery would be at the device output. In this case overcurrent protection is activated to prevent accessory faults and battery discharge. Thanks to the NCP370 using an internal NMOS, the system cost and the PCB area of the application board are minimized.

The NCP370 provides a negative going flag ($\overline{FLAG}$) output which alerts the system that a fault has occurred.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1 μF or larger capacitor.

Features

- Overvoltage Protection Up to 28 V
- Negative Voltage Protection Down to −28 V
- Reverse Charge Control: $\overline{REV}$
- Direct Charge Control: $\overline{DIR}$
- Overcurrent Protection
- Thermal Shutdown
- On−chip Low $R_{DS(on)}$ NMOS Transistors: Typical 130 mΩ
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Soft−Start
- Alert $\overline{FLAG}$ Output
- Compliance to IEC61000−4−2 (Level 4)
  - 8 kV (Contact)
  - 15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 2
- 12 Lead TLLGA 3x3 mm Package
- This is a Pb−Free Device

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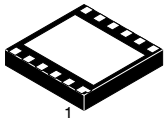
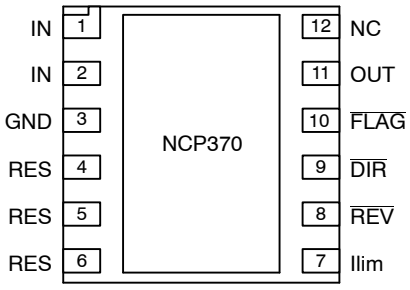


12 PIN LLGA
MU SUFFIX
CASE 513AK

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP370MUAITXG	LLGA12 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Applications

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications
- MP3 Players

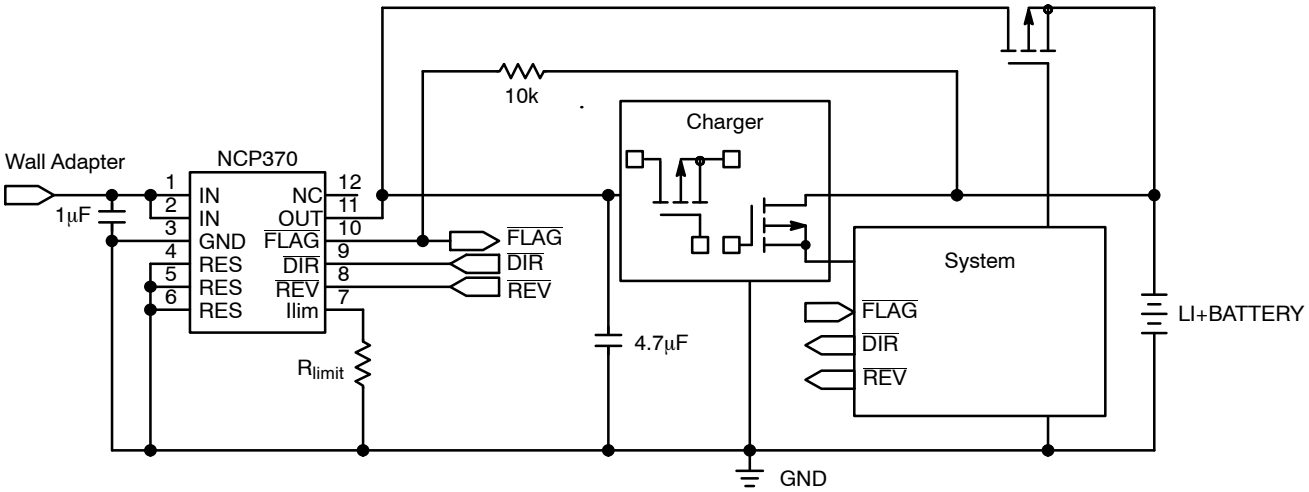


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

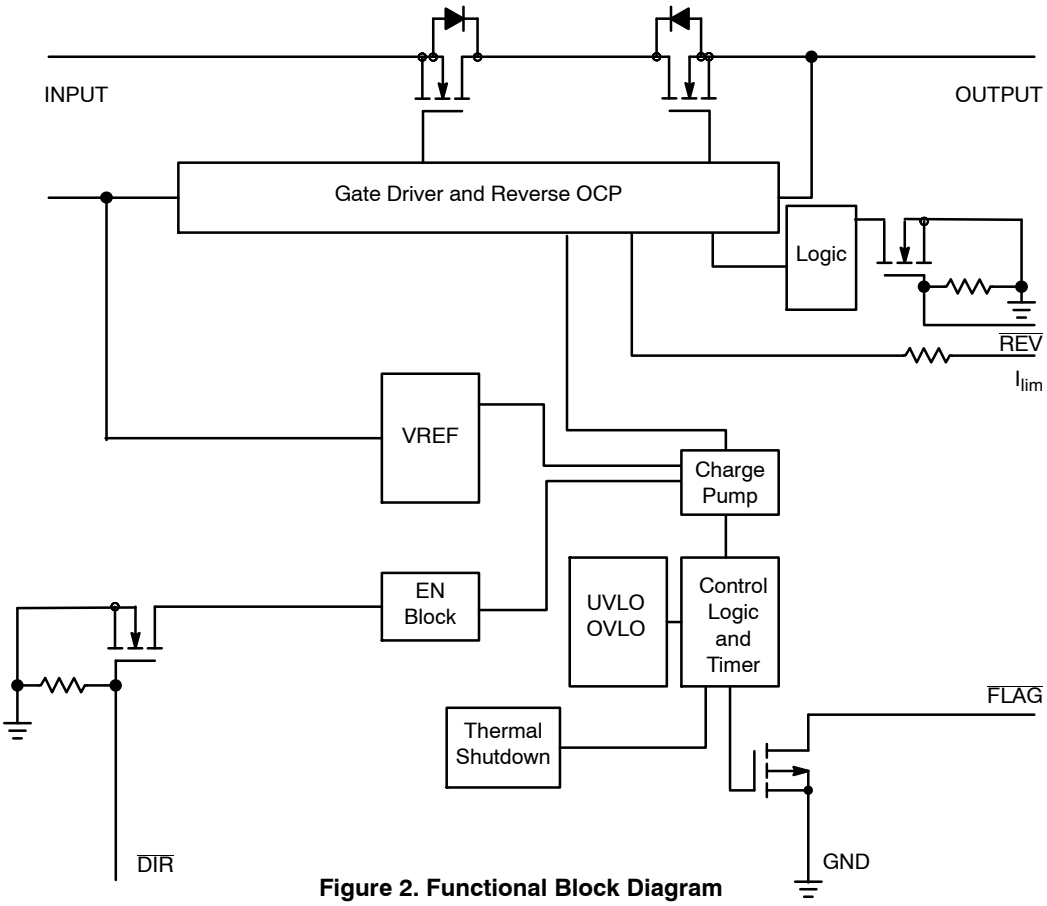


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
1, 2	IN	POWER	Input voltage pins. These pins are connected to the power supply. A 1 μF low ESR ceramic capacitor, or larger, must be connected between these pins and GND. The two IN pins must be hardwired to common supply.
3	GND	POWER	Main Ground
4	RES	INPUT	Reserved pin. This pin must be connected to GND.
5	RES	INPUT	Reserved pin. This pin must be connected to GND.
6	RES	INPUT	Reserved pin. This pin must be connected to GND.
7	Ilim	OUTPUT	Current Limit Pin. This pin provides the reference, based on the internal band−gap voltage reference, to limit the over current, across internal N−MOSFETs, from battery to external accessory. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the overcurrent limit.
8	$\overline{\text{REV}}$	INPUT	Reverse Charge Control Pin. In combination with $\overline{\text{DIR}}$, the internal N−MOSFETs are turned on if Battery is applied on the OUT pin (See Tables 1 & 2). In reverse mode, the internal overcurrent protection is activated. When reverse mode is disabled, the NCP370 current consumption, into OUT pin, is drastically decreased to limit battery discharge.
9	$\overline{\text{DIR}}$	INPUT	Direct Mode Pin. In combination with $\overline{\text{REV}}$, the internal N−MOSFETs are turned on if a wall adapter AC−DC is applied on the IN pins (See Tables 1 & 2). The device enters in shutdown mode when this pin is tied to a high level and the $\overline{\text{REV}}$ pin is tied to high. In this case the output is disconnected from input. The state of this pin does not have an impact on the fault detect of the $\overline{\text{FLAG}}$ pin.
10	$\overline{\text{FLAG}}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect fault condition. The pin goes low when input voltage exceeds OVLO threshold or drops below UVLO threshold, charge current from battery to accessory exceeds current limit or internal temperature exceeds thermal shutdown limit. Since the pin is open drain functionality, an external pull up resistor to VBat must be added (10 kΩ minimum value).
11	OUT	OUTPUT	Output Voltage Pin. This pin follows IN pins when “no input fault” is detected. The output is disconnected from the V_{IN} power supply when the input voltage is under the UVLO threshold or above OVLO threshold or thermal shutdown limit is exceeded.In Reverse Mode, the device is supplied across OUT pin.
12	NC	NC	Not Connected
13	PAD1	POWER	The PAD1 is used to dissipate the internal MOSFET thermal energy and must be soldered to an isolated PCB area. The area mustn’t be connected to any other potential than complete isolated one. See PCB recommendations on page 9.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	$Vmin_{in}$	−30	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{in}$	30	V
Maximum Voltage (OUT to GND)	$Vmax_{out}$	10	V
Maximum Voltage (All others to GND)	Vmax	7	V
Thermal Resistance, Junction−to−Air, (Note 1)	$R_{\theta JA}$	200	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Junction Operating Temperature	T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), Model = 2, (Note 2) Machine Model (MM) Model = B, (Note 3)	Vesd	15kV air, 8kV contact 2000V 200V	kV V V
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to PAD1). See PCB recommendation paragraph.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS (V_{in} = 5 V, Minimum/Maximum limits at −40°C < T_A < +85°C unless otherwise noted. Typical values are at T_A = +25°C)

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}	Disable, Direct and Enhance Modes, V_{out} = 0 V	−28		28	V
Input Voltage	Vin_{min}	Disable, Direct and Enhance Modes, V_{out} = 4.25V	−24			V
Output Voltage Range	V_{out}	Reverse Mode	2.5		5.5	V
Undervoltage Lockout Threshold	UVLO	Vin falls below UVLO Threshold (Disable, Direct and Enhance Modes)	2.6	2.7	2.8	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$	V_{in} rises above UVLO Threshold + $UVLO_{hyst}$	45	60	75	mV
Over voltage Lockout Threshold NCP370MUAITXG	OVLO	V_{in} rises above OVLO threshold (Disable and Direct Modes)	6.3	6.6	6.9	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$	V_{in} falls below to OVLO − $OVLO_{hyst}$	60	80	100	mV
Over System Voltage Lockout	$OVLO_{00}$	V_{in} rises above $OVLO_{00}$ Threshold Enhanced Mode @ 25°C	7.9	8.27	8.6	V
Overvoltage Lockout Hysteresis	$OVLO_{00hyst}$	V_{in} falls below to $OVLO_{00}$ − $OVLO_{00hyst}$ @ 25°C	80	100	145	mV
V_{in} to V_{out} Resistance	$R_{DS(on)}$	V_{in} = 5 V, Direct Mode, Load Connected to V_{out} V_{in} = 5 V, Direct Mode, Load Connected to V_{out} @ 25°C		130 130	220 200	mΩ
V_{out} to V_{in} Resistance	$R_{DS(on)}$	V_{out} = 5 V, Reverse Mode, Accessory Connected to V_{in} V_{out} = 5 V, Reverse Mode, Accessory Connected to V_{in} @ 25°C		130 130	220 200	mΩ
Input Standby Current	Idd_{STD}	No Load. Disable Mode, V_{in} connected		140	200	μA
Input Supply Quiescent Current	Idd_{IN}	No Load. Direct Mode		200	280	μA
Output Standby Current	Idd_{STDOUT}	Rin = 10 kΩ, V_{out} = 5.5 V, Disable Mode		0.02	1.0	μA
Reverse Mode current	Idd_{REV}	No Accessory, V_{out} = 4.2 V, Reverse Mode		200	315	μA
Minimum DC Current	I_{CHG}	Output Load, V_{in} = 5.5 V, Direct	1.3			A
	I_{REV}	Accessory, V_{out} = 5.5 V, Reverse Modes	1.3			
Overcurrent Threshold	I_{OCP}	V_{out} = 4.2 V, Load on V_{in}, Reverse Mode, R_{ILIM} = 0 Ω, 1 A/1 μs	1.35	1.75	2.10	A
Overcurrent Response	I_{acc}	Direct Accessory Short, Reverse Mode, V_{out} = 4.2 V, I_{lim} = 1.6 A		7.0		%
$\overline{FLAG}$ Output Low Voltage	Vol_{flag}	1.2 V < V_{in} < UVLO Sink 50 μA on $\overline{FLAG}$ Pin		30	400	mV
		V_{in} > OVLO, Sink 1 mA on FLAG Pin			400	
		$I_{reverse}$ > I_{lim}, Sink 1 mA on FLAG Pin			400	
$\overline{FLAG}$ Leakage Current	$\overline{FLAG}_{leak}$	$\overline{FLAG}$ Level = 5.5 V		1.0		nA
$\overline{DIR}$ Voltage High	V_{ihDIR}		1.2			V
$\overline{DIR}$ Voltage Low	V_{ilDIR}				0.55	V
$\overline{DIR}$ Leakage Current	$\overline{DIR}_{leak}$	V_{in} or V_{out} connected V_{in} and V_{out} disconnected		200 1.0		nA
$\overline{REV}$ Voltage High	V_{ihREV}		1.2			V
$\overline{REV}$ Voltage Low	V_{ilREV}				0.55	V
$\overline{REV}$ Leakage Current	$\overline{REV}_{leak}$	V_{in} or V_{out} connected V_{in} and V_{out} disconnected		200 1.0		nA
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SDHYST}			30		°C

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
TIMINGS						
DIRECT MODE						
Start Up Delay	t_{on}	From V_{in} > UVLO to $V_{out} \geq$ 0.3 V	20	30	40	ms
$\overline{FLAG}$ Going Up Delay	t_{start}	From V_{out} > 0.3 V to $\overline{FLAG}$ = 1.2 V	20	30	40	ms
Turn Off Delay	t_{off}	From V_{in} > OVLO to $V_{out} \leq$ 0.3 V V_{in} Increasing from 5 V to 8 V at 3 V/μs		1.5	5.0	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to $\overline{FLAG} \leq$ 0.4 V See Figure 3 and 9 V_{in} Increasing from 5 V to 8 V at 3 V/μs		1.5		μs
Disable Time	t_{dis}	$\overline{REV}$ = 1.2 V, From $\overline{DIR}$ = 0.4 V to 1.2 V to $V_{out} \leq$ 0.3 V		2.5		μs
REVERSE MODE						
Reverse Start Up Delay	ton_{REV}	$V_{out} \geq$ 2.5 V, From $\overline{REV}$ = 1.2 to 0.55 to $V_{in} \geq$ 0.3 V, Reverse Mode	0.6	1.2	1.8	ms
Reverse $\overline{FLAG}$ Going Up Delay	$tstart_{REV}$	From $V_{in} \geq$ 0.3 V $\overline{FLAG}$ = 1.2 V, Reverse Mode	0.6	1.2	1.8	ms
Rearming Reverse Delay	t_{RRD}	V_{out} > 2.5 V, R_{in} = 1 Ω, Reverse Mode	20	30	40	ms
Over Current Regulation Time	t_{REG}	V_{out} > 2.6, V_{in} > 0.3 V, Reverse Mode	0.5	1.2	1.8	ms
OCP Delay Time	t_{OCP}	From $I_{reverse} > I_{lim}$, 1 A/1 μs		5		μs
Reverse Disable Time	t_{REVDIS}	From $\overline{REV}$ = 0.55 V to 1.2 V, to V_{in} < 0.3 V. V_{out} = 5 V		200		μs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

TYPICAL OPERATING CHARACTERISTICS

Operation

The NCP370 provides overvoltage protection for positive and negative voltages, up to 28 V or down to −28 V on IN pins. At powerup, with $\overline{DIR}$ pin = low, $\overline{REV}$ = high, the output rises 30 ms after the input rises above the UVLO. The NCP370 provides a $\overline{FLAG}$ output, which alerts the system that a fault has occurred. The $\overline{FLAG}$ signal rises 30 ms after the output signal rises.

A Reverse Mode is available when an accessory is connected on IN pins and the internal battery is applied on the OUT pin, allowing the accessory to be powered. In this mode, no supply must be connected on IN pins and $\overline{REV}$ pin must be tied to low level. The NCP370 provides overcurrent protection for the battery from current faults in the accessory.

Undervoltage Lockout (UVLO)

To ensure proper turn−on operation from AC/DC (or Wall adapter charging) under any conditions, the device has a built−in undervoltage lock out (UVLO) circuit. During positive going slope on V_{in}, the output remains disconnected from input until V_{in} voltage is above UVLO. The $\overline{FLAG}$ output will be low as long as V_{in} has not reached UVLO threshold. This circuit has a 60 mV hysteresis to provide noise immunity to transient conditions.

In Reverse Mode ($\overline{REV}$ pin $\leq$ 0.55 V, $\overline{DIR} \geq$ 1.2 V), UVLO and OVLO comparators are inactivated.

Overvoltage Lockout (OVLO)

To protect connected systems on Vout pin from overvoltage, the device has a built−in overvoltage lock out (OVLO) circuit. During overvoltage condition, the output is disabled as long as the input voltage exceeds OVLO.

Additional OVLO thresholds can be manufactured (Please contact your ON Semiconductor representative for availability).

$\overline{FLAG}$ output will be low since V_{in} is higher than OVLO. This circuit has a 80 mV hysteresis to provide noise immunity to transient conditions.

Oversystem Voltage Lockout ($OVLO_{00}$)

A second overvoltage comparator is available for supplying the sytem (output) by the Wall Adaptor (input) by setting $\overline{DIR}$ = low and $\overline{REV}$ = low. The $R_{DS(on)}$ will be higher during this mode allowing to handle few 10 mA.

This additional comparator allows to put higher input voltage (OVLO = 8.27 V typical) on the NCP370 during test production sequence (I.E: One Time Programming of the cell phone, PDA). This parameter is 25°C guaranteed only.

$\overline{FLAG}$ Output

The NCP370 provides a $\overline{FLAG}$ output which alerts that a fault has occurred. As soon as a fault state is detected by the NCP370 (see Figure 3), the $\overline{FLAG}$ pin output goes low, alerting the micro−controller to take appropriate action.

The $\overline{\text{FLAG}}$ pin goes low as soon the input voltage exceeds the OVLO threshold or falls below the UVLO threshold. When the V_{in} level recovers normal condition, $\overline{\text{FLAG}}$ goes high after a time delay, t_{start} (see Figure 3), following the V_{out} response. The $\overline{\text{FLAG}}$ pin is an open drain output and therefore a pull up resistor (typically 1 MΩ, minimum 10 kΩ) must be connected to Battery. The $\overline{\text{FLAG}}$ level will always reflect V_{in} status, even if the device is turned off ($\overline{\text{DIR}}$ = 1 and $\overline{\text{REV}}$ = 1).

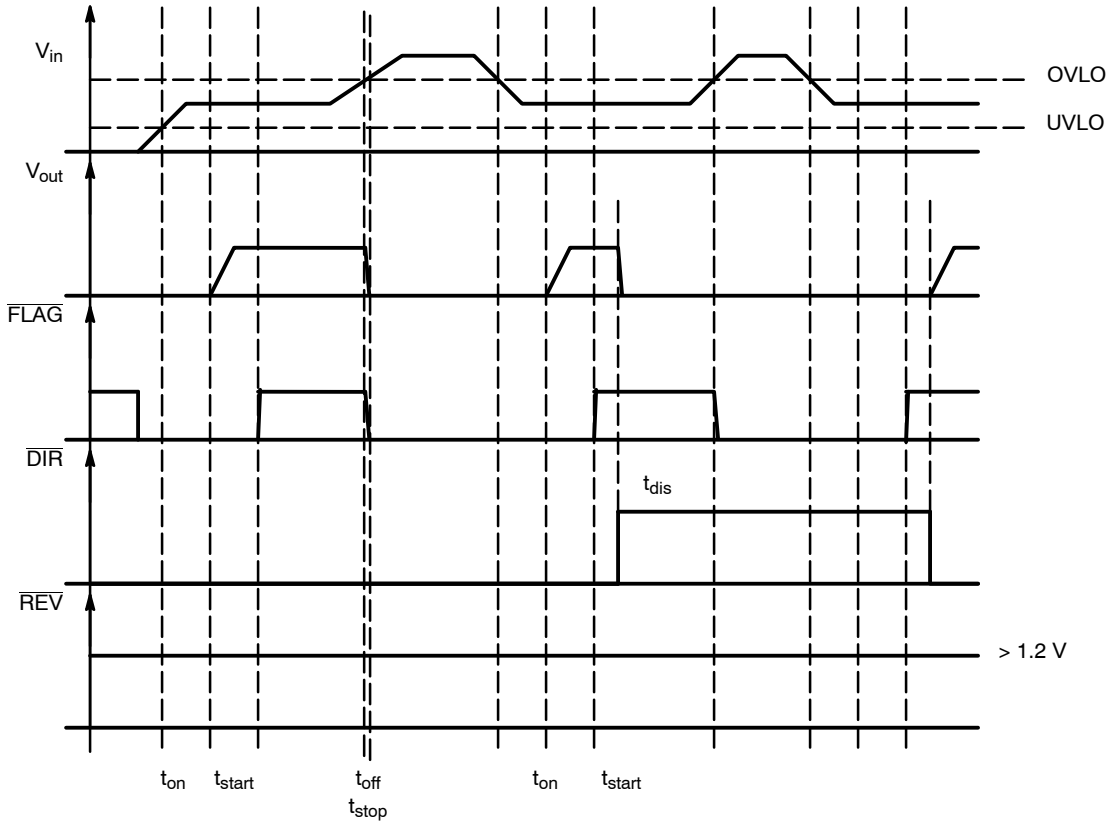


Figure 3. $\overline{\text{FLAG}}$ Pin in AC/DC Charging Mode

During over thermal condition ($T°_J > T°_{SD}$), output is disconnected from input, and $\overline{\text{FLAG}}$ pin goes low.

In Reverse Mode, $\overline{\text{FLAG}}$ pin remains available, allowing the micro−controller to appropriately process the overvoltage condition, overcurrent condition or thermal shutdown condition.

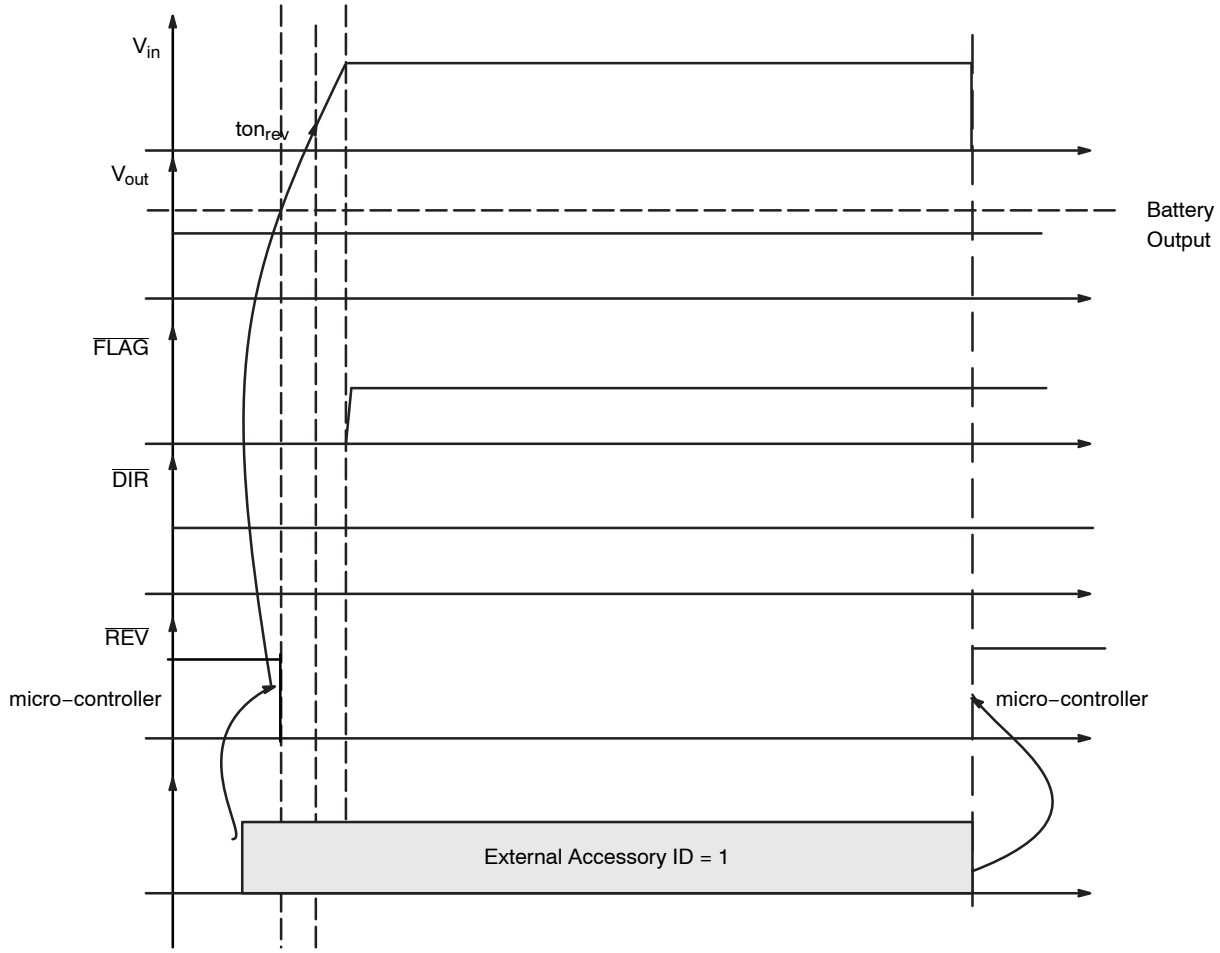


Figure 4. $\overline{FLAG}$ status in Reverse Mode

Table 1. $\overline{FLAG}$ TABLE

$\overline{DIR}$	$\overline{REV}$	IN	OUT	$\overline{FLAG}$ Status	Pass Element (Dual NMOS FET)
0	0	1.5 < V_{in} < UVLO or V_{in} > $OVLO_{oo}$	Hiz	Low	Open
0	0	UVLO < V_{in} < $OVLO_{oo}$	= V_{in}−DROPOUT	High	Close
0	1	1.5 < V_{in} < UVLO or V_{in} > OVLO	Hiz	Low	Open
0	1	UVLO < V_{in} < OVLO	= V_{in}−DROPOUT	High	Close
1	0	= V_{out}−DROPOUT	V_{out} > 2.5 V	High	Close
1	1	1.5 < V_{in} < UVLO or V_{in} > OVLO	Hiz	Low	Open
1	1	UVLO < V_{in} < OVLO	Hiz	High	Open

$\overline{DIR}$ Input

To enable Direct Charge operation (Direct Mode), the $\overline{DIR}$ pin shall be forced to low and $\overline{REV}$ to high. A high level on the $\overline{DIR}$ pin disconnects OUT pin from IN pin. $\overline{DIR}$ does not over−ride an OVLO or UVLO fault ($\overline{FLAG}$ status is still available).

Table 2. TABLE SELECTION OF CHARGE MODES

$\overline{DIR}$	$\overline{REV}$	Mode
0	0	Enhance Mode
0	1	Direct Mode
1	0	Reverse Mode
1	1	Disable Mode

Negative Voltage and Reverse Current.

The device protects the downstream side from negative voltage occurring on the IN pin, down to −28 V. When a negative voltage occurs, the output is disconnected from the IN pins.

Reverse Mode

In Reverse Mode, an external accessory plugged into the bottom connector can be powered by the internal battery of the system.

To access to the reverse mode, $\overline{\text{DIR}}$ pin must be tied high (> 1.2) and $\overline{\text{REV}}$ must be tied high to low (< 0.55 V).

In this case, the core of the NCP370 will be supplied by the battery, with a 2.5 V minimum voltage and 5.5 V maximum voltage.

In this reverse state, both OCP and thermal modes are available.

Overcurrent Protection (OCP)

This device integrates the reverse over current protection function, from battery to external accessory.

That means the current across the internal NMOS is limited when the value, set by the external R_{limit} resistor, exceeds I_{OCP}.

An internal resistor is placed in series with the I_{lim} pin allowing a maximum OCP value when I_{lim} pin is directly connected to GND.

By adding external resistors in series from I_{lim} to GND, the OCP value is lowered. The typical overcurrent threshold can be calculated with the following formula;

R_{ilim} (kΩ) = (60 / I_{OCP}) − 36

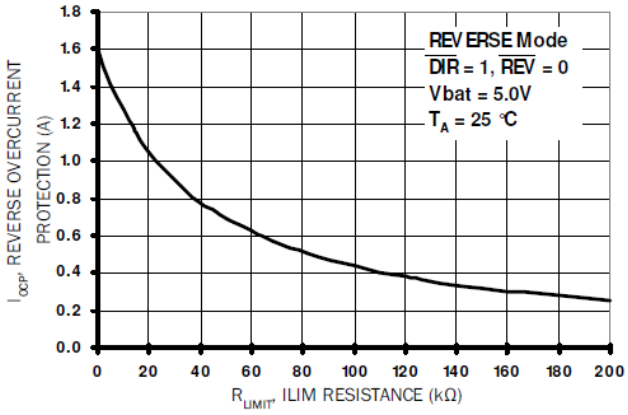


Figure 5. Reverse Mode Overcurrent Protection vs. ILIM Resistance, R_{LIMIT}

During an overcurrent event, the N−MOSFETs turn off and $\overline{\text{FLAG}}$ output goes low, allowing the micro−controller to process the fault event and then disable reverse charge path.

At power up (accessory is plugged on input pins), the current is limited up to I_{lim} for 1.2 ms (typical), to allow capacitor charge and limit inrush current. If the I_{lim} threshold is exceeded over 1.2 ms, the device enters OCP burst mode until the overcurrent event disappears.

After 1 ms following the plug in of the accessory, the OCP mode is engaged. See Figure 6.

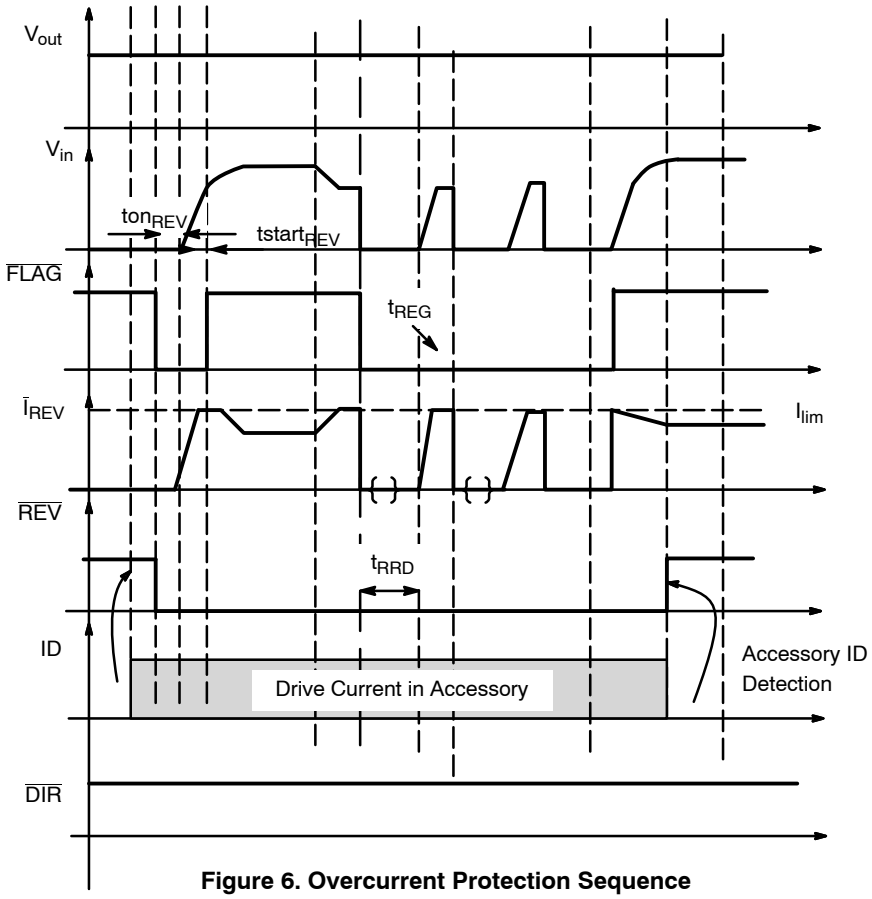


Figure 6. Overcurrent Protection Sequence

Thermal Shutdown Protection

In case of internal overheating, the integrated thermal shutdown protection turns off the internal MOSFETs in order to instantaneously decrease the device temperature. The thermal threshold has been set at 150°C $\overline{FLAG}$ then goes low to inform the MCU.

As the thermal hysteresis is 30°C, the MOSFETs will turn on as soon the device temperature falls below 120°C.

If the fault event is still present, the temperature increase engages the thermal shutdown again until the fault event disappears.

PCB Recommendations

Since the NCP370 integrates the 1. 3A N−MOSFETs, PCB rules must be respected to properly evacuate the heat out of the silicon.

From an applications standpoint, PAD1 of the NCP370 package should be connected to an isolated PCB area to increase the heat transfer if necessary.

In any case, PAD1 should be not connected to any other potential or GND other than the isolated extra copper surface.

To assist in the design of the transfer plane connected to PAD1, Figure 7 shows the copper area required with respect to $R_{\theta JA}$.

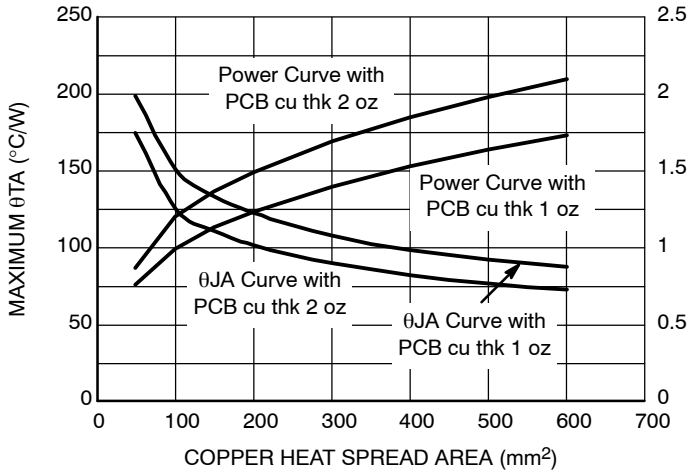


Figure 7. Copper heat Spread Area

ESD Tests

The NCP370 conforms to the IEC61000−4−2, level 4 on the Input pin. A 1 μF (I.E Murata GRM188R61E105KA12D) must be placed close to the IN pins. If the IEC61000−4−2 is not a requirement, a 100 nF/25 V must be placed between IN and GND.

The above configuration supports 15 kV (Air) and 8 kV (Contact) at the input per IEC61000−4−2 (level 4).

Please refer to Figure 8 for the IEC61000−4−2 electrostatic discharge waveform.

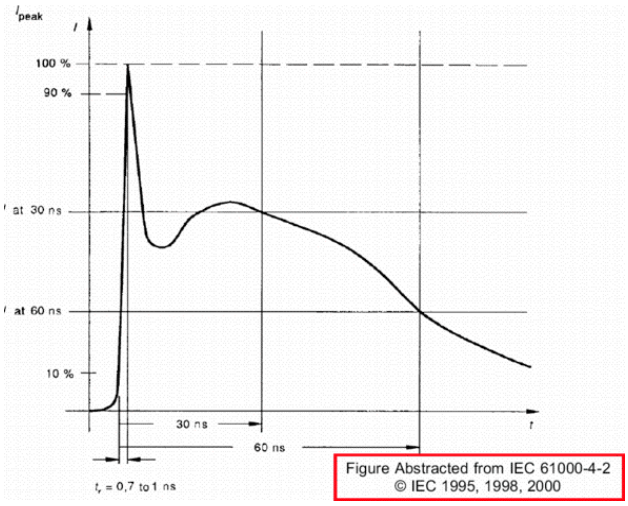


Figure 8. I_{peak} = f(t)/IEC61000−4−2

$R_{DS(on)}$ and Dropout

The NCP370 includes two internal low $R_{DS(on)}$ N−MOSFETs to protect the system, connected on OUT pin, from overvoltage, negative voltage and reverse current protection. During normal operation, the $R_{DS(on)}$ characteristics of the N−MOSFETs give rise to low losses on V_{out} pin.

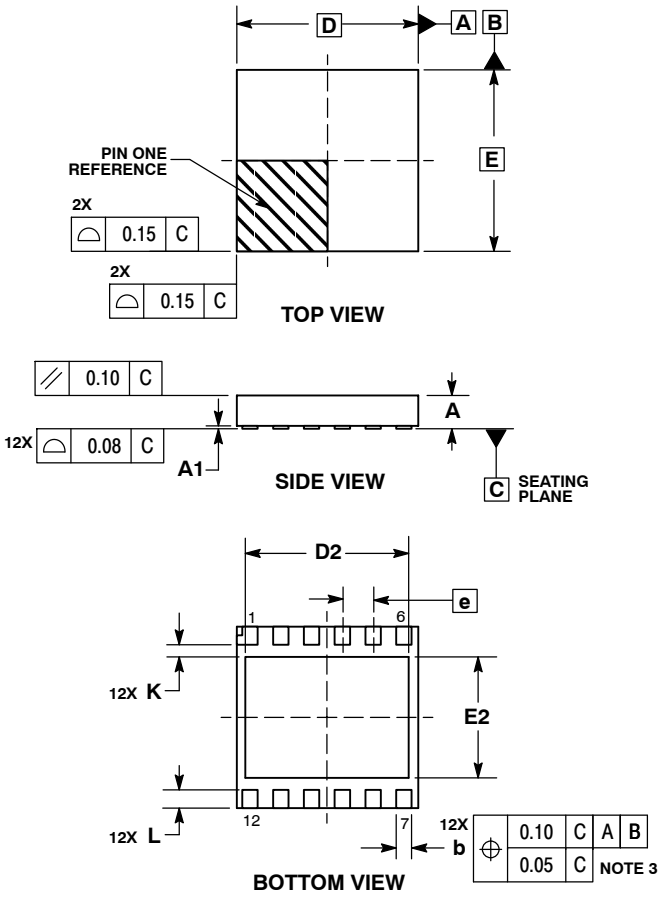
As example: R_{load} = 8 Ω, Vin= 5 V. $R_{DS(on)}$ = 155 mΩ. I_{out} = 800 mA.

V_{out} = 4.905 V

NMOS Losses = $R_{DS(on)}$ x I_{out}^2 = 0.155 x 0.8^2 = 0.0992 W

PACKAGE DIMENSIONS

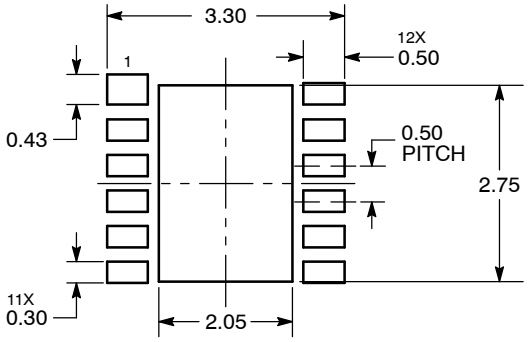
LLGA12 3x3, 0.5P
CASE 513AK−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	2.60	2.80
E	3.00 BSC	
E2	1.90	2.10
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Тел: +7 (812) 336 43 04 (многоканальный)
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