MAX77826

Power Management IC

General Description

The MAX77826 is a subpower management IC for the latest 3G/4G smartphones and tablets. The MAX77826 contains a high-efficiency BUCK regulator, a BUCK BOOST regulator and 15 LDOs to power up peripherals. The MAX77826 also provides power on/off control logic and an I²C serial interface to program individual regulator output voltages and on/off control for complete flexibility.

The linear regulators support a remote cap feature and provide greater than 70dB PSRR and less than 45μV_{RMS} noise.

The MAX77826 features I²C-compatible, 2-wire serial interface that comprises a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77826 supports SCL clock rates up to 3.4MHz.

Applications

- GSM, GPRS, EDGE, CDMA WCDMA, and LTE Smartphones and Tablets

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Compact Total Solution Size Allows More Peripheral Devices in Smartphones and Tablets
  - 3A High-Efficiency BUCK Regulator
    - DVS (Dynamic Voltage Scaling) Through HS I²C
    - ±1% (typ) Output Voltage DC Accuracy
    - Low Power Mode
  - 2A BUCK BOOST Regulator
  - 15 Linear Regulators with Remote Cap
    - 3 NMOS LDOs (V_{OUT} Range: 0.6V to 2.1875V with 12.5mV Step)
    - 1 x 150mA
    - 1 x 450mA
    - 1 x 600mA
  - 6 PMOSLV LDOs (V_{OUT} Range: 0.8V to 3.975V with 25mV Step)
    - 3 x 150mA
    - 3 x 300mA
  - 6 PMOSLS LDOs (V_{OUT} Range: 0.8V to 3.975V with 25mV Step)
    - 3 x 150mA
    - 3 x 300mA
  - ±1.5% Typical Output Voltage DC Accuracy
  - 70dB PSRR at 1kHz
  - Low Power Mode with 2µA (typ) for all LDOs
- Simple Management of Power-Up/Down Sequence, Output Voltage Setting, and Fault Detection
  - High-Speed (Up to 3.4MHz) I²C Serial Interface

19-6893; Rev 0; 6/15

maxim integrated™

Absolute Maximum Ratings

SYS, V_{IO}, INL1, INL2, INL3, INL4, INL5 to GND ..... -0.3V to +6.0V
INB to PGNDB ..... -0.3V to +6.0V
INBB, OUTBB to PGNDBB ..... -0.3V to +6.0V
PGNDB, PGNDBB to GND ..... -0.3V to +0.3V
IRQB, CE, SDA, SCL to GND ..... -0.3V to (V_{IO} + 0.3V)
FB_B, ENBB, ENB, ENL12, REFBYP to GND ..... -0.3V to (V_{SYS} + 0.3V)
FB_BB to PGNDBB ..... -0.3V to (V_{OUTBB} + 0.3V)
LXB to PGNDB ..... -0.3V to (V_{INB} + 0.3V)
LXBB1 to PGNDBB ..... -0.3V to (V_{INBB} + 0.3V)
LXBB2 to PGNDBB ..... -0.3V to (V_{OUTBB} + 0.3V)
LDO1, LDO2 to GND ..... -0.3V to (V_{INL1} + 0.3V)
LDO3 to GND ..... -0.3V to (V_{INL2} + 0.3V)
LDO4, LDO5, LDO6, LDO7, LDO8, LDO9 to GND ..... -0.3V to (V_{INL3} + 0.3V)
LDO10, LDO11 to GND ..... -0.3V to (V_{INL4} + 0.3V)
LDO12, LDO13, LDO14, LDO15 to GND ..... -0.3V to (V_{INL5} + 0.3V)
LXB Continuous RMS Current (Note 1) 3A
LXBB1/LXBB2 Continuous RMS Current (Note 1) 3.3A
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LX_ node has internal clamp diodes to PGND_ and INB_. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed IC's package power dissipation limits.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

General Electrical Characteristics

(V_{SYS} = $V_{IN_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{SHDN_SYS}	CE = low		2.5	10	µA
Standby Current	I_{Q_SYS}	CE = high and all regulators are off		35		µA
Shutdown V_{IO} Current	I_{SHDN_VIO}	All regulators are off		0		µA
No Load Supply Current 1	I_{NO_LOAD1}	BUCK is on in normal mode (no switching)		60		µA
No Load Supply Current 2	I_{NO_LOAD2}	BUCK and BUCK BOOST are on in normal mode (no switching)		120		µA
No Load Supply Current 3	I_{NO_LOAD3}	All regulators are on in normal mode (no switching)		400	700	µA
V_{SYS} UNDERVOLTAGE LOCKOUT						
V_{SYS} Undervoltage Lockout Threshold	V_{UVLO_R}	V_{SYS} rising	2.375	2.50	2.625	V
	V_{UVLO_F}	V_{SYS} falling (default)		2.05		
REFERENCE						
REFBYP Output Voltage			0.786	0.80	0.814	V
REFBYP Supply Rejection		2.7V ≤ V_{SYS} ≤ 5.5V		0.2		mV/V

General Electrical Characteristics (continued)

(V_{SYS} = $V_{IN_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN							
Thermal Shutdown Threshold	T_{SHDN}	T_J rising, 15°C hysteresis			+165		°C
Thermal Interrupt at +120°C	T_{120}	T_J rising, 15°C hysteresis			+120		°C
Thermal Interrupt at +140°C	T_{140}	T_J rising, 15°C hysteresis			+140		°C
LOGIC AND CONTROL INPUTS							
Input Low Level	V_{IL}	ENB, ENBB, ENL12	V_{SYS} ≤ 4.5V T_A = +25°C			0.4	V
		CE	T_A = +25°C			0.3 x V_{IO}	
Input High Level	V_{IH}	ENB, ENBB, ENL12	V_{SYS} ≤ 4.5V T_A = 25°C	1.2			V
		CE	T_A = +25°C	0.7 x V_{IO}			
Logic Input Leakage Current	I_{LEAK}	CE (0V < V_{IO} < 1.8V)	T_A = +25°C	-1		+1	µA
			T_A = +85°C		0.1		
IRQB Output Low Voltage	V_{OL}	I_{SINK} = 1mA				0.4	V
IRQB Output High Leakage	I_{OZH}	V_{IO} = 5.5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		0.1		
INTERNAL PULLDOWN RESISTANCE							
ENB, ENBB, ENL12	R_{PD}	Pulldown resistor to GND		400	800	1600	kΩ

I²C Electrical Characteristics

(V_{SYS} = $V_{IN_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage	V_{IO}		1.7		3.6	V
SDA AND SCL I/O STAGES						
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Current	I_I	V_{IO} = 3.7V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IO} to 0.3 x V_{IO}	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 3)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Capacitive Load for Each Bus Line	C_B				550	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				50		ns

I²C Electrical Characteristics (continued)

(V_{SYS} = $V_{IN_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF			C_B = 400pF			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I²C-COMPATIBLE INTERFACE TIMING (HS MODE)									
Clock Frequency	f_{SCL}				3.4			1.7	MHz
Set-Up Time REPEATED START Condition	$t_{SU;STA}$		160			160			ns
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		160			160			ns
CLK Low Period	t_{LOW}		160			320			ns
CLK High Period	t_{HIGH}		60			120			ns
DATA Setup time	$t_{SU:DAT}$		10			10			ns
DATA Hold Time	$t_{HD:DAT}$			35			75		ns
SCL Rise Time (Note 3)	t_{RCL}	T_A = +25°C	10		40	20		80	ns
Rise Time of SCL Signal After a REPEATED START Condition and After an Acknowledge Bit (Note 3)	t_{rCL1}	T_A = +25°C	10		80	20		160	ns
SCL Fall Time (Note 3)	t_{fCL}	T_A = +25°C	10		40	20		80	ns
SDA Rise Time (Note 3)	t_{rDA}	T_A = +25°C			80			160	ns
SDA Fall Time (Note 3)	t_{fDA}	T_A = +25°C			80			160	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			160			ns
Capacitive Load for Each Bus Line	C_B				100			400	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				10			10		ns

BUCK Electrical Characteristics

(V_{SYS} = V_{INB} = +3.7V, V_{FB_B} = V_{OUT} = 1.25V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Parametric		2.6		5.5	V
Shutdown Supply Current (Note 3)				0.1		µA
Supply Quiescent Current (Note 3)	No switching, No load	Normal mode		22		µA
		Low power mode		8		
Output Voltage Range	I^2C-programmable 6.25mV step		0.5		1.8	V
Output Voltage Accuracy	V_{INB} = 2.6V to 4.5V, V_{OUT} = 1.25V, no load	PWM mode, T_A = +25°C	-1.0		+1.0	%
		Low power mode	-3.0		+4.0	
Line Regulation	V_{INB} = 2.6V to 4.5V			0.200		%/V
Load Regulation (Note 3)	V_{OUT} = 1.25V			0.125		%/A
Transient Load Response, VDROOP (Note 3)	V_{OUT} = 1.25V, IOUT changes from 0A to 1.5A in 6µs, C_{OUT_ACTUAL} = 22µF, L = 0.47µH			-50		mV
Soft-Start Slew Rate				14		mV/µs
Output Voltage Ramp-Up Slew Rate	RAMP[1:0] = 00b (default)			12.5		mV/µs
	RAMP[1:0] = 01b			25		
	RAMP[1:0] = 10b			50		
	RAMP[1:0] = 11b			100		
Maximum Output Current	Normal mode		3000			mA
	Low power mode			10		
Peak Current Limit			3.30	4.25	5.50	A
Valley Current Limit				3.825		A
Negative Current Limit				1.000		A
N-FET Zero-Crossing Threshold	Skip mode			20		mA
Switching Frequency			1.8	2	2.2	MHz
Turn-On Delay Time	EN signal to LX switching with bias ON			30		µs
HS PMOS RDSON	V_{INB} = 3.7V, INB to LX, I_{LX} = 200mA			60		mΩ
LS NMOS RDSON	V_{INB} = 3.7V, LX to PGNDB, I_{LX} = 200mA			35		mΩ
Output Active Discharge Resistance	Output disabled, resistance from FB_B to PGNDB			100		Ω
LX Leakage	V_{LXB} = 5.5V or 0V	T_A = +25°C	-1	0.1	+1	µA
		T_A = +85°C		1		
POWER-OK COMPARATOR						
Output POK Trip Level	V_{OUT} POK rising threshold			90		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

BUCK BOOST Electrical Characteristics

(V_{INBB} = +3.7V, V_{OUTBB} = +3.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Operating Input Voltage Range	Supplied from V_{SYS}		2.6		5.5	V
Shutdown Supply Current	V_{INBB} = 5.5V, V_{OUTBB} = 0V	T_A = +25°C		0.01		µA
		T_A = +85°C		1		
Input Supply Current	Enabled, no load	HSKIP mode (no switching)		60		µA
		FPWM mode (switching)		9		mA
Active Discharge Resistance				100		Ω
Thermal Shutdown	T_A rising, 20°C hysteresis			+165		°C
H-BRIDGE						
Maximum Output Current (Note 6)	V_{INBB} = 3.0V, V_{OUTBB} = 3.5V		2000			mA
	V_{INBB} = 2.6V, V_{OUTBB} = 3.5V		1500			
Default Output Voltage	No load, BB_VOUT[6:0] = 0x48			3.5		V
Output Voltage Accuracy	BB_VOUT[6:0] = 0x48, no load	PWM mode	-1.0		+1.0	%
		HSKIP mode T_A = +25°C	-1.0		+4.0	
Output Voltage Range	I^2C programmable (12.5mV step)		2.6		4.1875	V
Line Regulation	V_{INBB} = 2.6V to 5.5V			0.200		%/V
Load Regulation (Note 6)	V_{OUTBB} = 3.5V			0.125		%/A
Transient Load Response, V_{DROOP} (Note 6)	V_{INBB} = 3.8V, V_{OUTBB} = 3.5V, I_{OUT} changes from 10mA to 1A in 10µs, C_{OUT_ACTUAL} = 47µF, L = 1µH			-100		mV
Output Overvoltage Threshold	With respect to V_{OUTBB}	BB_OVP_TH[1:0] = 01b		110		%
		BB_OVP_TH[1:0] = 10b		115		
		BB_OVP_TH[1:0] = 11b (default)		120		
Switching Frequency	2-phase BUCK or BOOST mode		1.6	1.8	2.0	MHz
	3-phase mode			0.9		
LXBB1, LXBB2 Leakage Current	$V_{LXBB1/2}$ = 0V or 5.5V, V_{OUTBB} = 5.5V, V_{SYS} = V_{INBB} = 5.5V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.2		
LXBB1/2 Current Limit			3.5	4.5	5.5	A
PMOS On-Resistance	I_{LXBB} = 100mA, per switch			65		mΩ
NMOS On-Resistance	I_{LXBB} = 100mA, per switch			55		mΩ

BUCK BOOST Electrical Characteristics (continued)

(V_{INBB} = +3.7V, V_{OUTBB} = +3.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Effective Output Capacitance	0µA < I_{OUT} < 2000mA		16		µF
Turn-On Delay Time	From ENBB asserting to LXBB Switching with bias on		6		µs
Soft-Start Time	V_{OUTBB} = 3.5V, I_{OUT} = 10mA		40		µs
POWER-OK COMPARATOR					
Output POK Trip Level	$V_{OUTBB\ POK}$ rising threshold		80		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches		5		%

LDO Electrical Characteristics

LDO NO.	TYPE	V_{OUT} RANGE (V)	STEP SIZE (mV)	I_{OUT} (max, mA)	DEFAULT V_{OUT} (V)	DEFAULT ON/OFF	INPUT PIN	C_{OUT} (µF)
1	NMOS	0.6–2.1875	12.5	600	1.0	Off	INL1	4.7
2	NMOS	0.6–2.1875	12.5	150	1.0	Off	INL1	1
3	NMOS	0.6–2.1875	12.5	450	1.0	Off	INL2	4.7
4	PMOSLV	0.8–3.975	25	300	1.5	Off	INL3	4.7
5	PMOSLV	0.8–3.975	25	300	1.8	Off	INL3	4.7
6	PMOSLV	0.8–3.975	25	150	1.8	Off	INL3	2.2
7	PMOSLV	0.8–3.975	25	300	1.8	Off	INL3	4.7
8	PMOSLV	0.8–3.975	25	150	1.8	Off	INL3	2.2
9	PMOSLV	0.8–3.975	25	150	1.8	Off	INL3	2.2
10	PMOSLS	0.8–3.975	25	300	2.8	Off	INL4	2.2
11	PMOSLS	0.8–3.975	25	150	2.8	Off	INL4	2.2
12	PMOSLS	0.8–3.975	25	300	3.3	Off	INL5	2.2
13	PMOSLS	0.8–3.975	25	300	3.3	Off	INL5	2.2
14	PMOSLS	0.8–3.975	25	150	3.3	Off	INL5	2.2
15	PMOSLS	0.8–3.975	25	150	3.3	Off	INL5	2.2

Note: *LDO12 can also be enabled/disabled by external logic inputs, ENL12.*

LDO1 (600mA NMOS)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		V_{OUT}		V_{SYS}	V
	V_{SYS}		2.6		5.5	
	(Note 7)		1.5			
Input Supply Current	Normal mode, no load			2		µA
	Low power mode, no load			2		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			30		µA
	Low power mode, no load			4		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.6		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			2.1875		
	Least significant step size			0.0125		
Output Voltage Accuracy	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		600			mA
	Low power mode		5			
Load Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V)	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{SYS} - V_{OUT} = 2.5V		60	150	mV
		V_{SYS} - V_{OUT} = 1.5V		100		
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		900	1800	mA
		Low power mode		10		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		2.35	4.7		µF

LDO1 (600mA NMOS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = 2.7V, V_{INLx} = 1.2V, V_{OUT} = V_{OUTMIN}		30		μV_{RMS}
		V_{SYS} = 2.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = 3.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 4.7µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.0V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 1.8V to 1.5V to 1.8V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled.			5		µs
Output Overshoot during Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

LDO2 (150mA NMOS)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 1.0µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		V_{OUT}		V_{SYS}	V
	V_{SYS}		2.6		5.5	
	(Note 7)		1.5			
Input Supply Current	Normal mode, no load			2		µA
	Low power mode, no load			2		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			25		µA
	Low power mode, no load			3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.6		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			2.1875		
	Least significant step size			0.0125		
Output Voltage Accuracy	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		150			mA
	Low power mode		5			
Load Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V)	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{SYS} - V_{OUT} = 2.5V		60	150	mV
		V_{SYS} - V_{OUT} = 1.5V		100		
Output Current Limit	V_{OUT} = 90% of V_{OUT} (TARGET)	Normal mode		225	450	mA
		Low power mode		10		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		0.5	1.0		µF

LDO2 (150mA NMOS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 1.0µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = 2.7V, V_{INLx} = 1.2V, V_{OUT} = V_{OUTMIN}		30		μV_{RMS}
		V_{SYS} = 2.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = 3.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 1.0µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.0V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 1.8V to 1.5V to 1.8V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled.			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

LDO3 (450mA NMOS)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		V_{OUT}		V_{SYS}	V
	V_{SYS}		2.6		5.5	
	(Note 7)		1.5			
Input Supply Current	Normal mode, no load			2		µA
	Low power mode, no load			2		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			25		µA
	Low power mode, no load			3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.6		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			2.1875		
	Least significant step size			0.0125		
Output Voltage Accuracy	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		450			mA
	Low power mode		5			
Load Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V)	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal Mode, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{SYS} - V_{OUT} = 2.5V		60	150	mV
		V_{SYS} - V_{OUT} = 1.5V		100		
Output Current Limit	V_{OUT} = 90% of V_{OUT} (TARGET)	Normal mode		675	1350	mA
		Low power mode		10		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		2.35	4.7		µF

LDO3 (450mA NMOS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 1.0µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = 2.7V, V_{INLx} = 1.2V, V_{OUT} = V_{OUTMIN}		30		μV_{RMS}
		V_{SYS} = 2.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power-Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = 3.7V, V_{INLx} = 1.8V, V_{OUT} = 1.2V, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 4.7µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.2V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 1.8V to 1.5V to 1.8V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot during Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

LDO4, LDO5 and LDO7 (300mA PMOSLV)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		1.7		V_{SYS}	V
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			1.5		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3		µA
	Low power mode, no load			0.3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum VOUT, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		300			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{INLx} = 3.7V		60	150	mV
		V_{INLx} = 1.7V		100		
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		600	1120	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		2.35	4.7		µF

LDO4, LDO5 and LDO7 (300mA PMOSLV) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 4.7µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.2V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 2.0V to 1.7V to 2.0V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Over-shoot during Startup Over-shoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			+165		°C
	T_J falling			+150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

LDO6, LDO8, and LDO9 (150mA PMOSLV)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		1.7		V_{SYS}	V
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			1.5		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3		µA
	Low power mode, no load			0.3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA,	-5		+5	
Maximum Output Current (Note 8)	Normal mode		150			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{INLx} = 3.7V		60	150	mV
		V_{INLx} = 1.7V		100		
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		300	560	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		1.1	2.2		µF

LDO6, LDO8, and LDO9 (150mA PMOSLV) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x IMAX to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 2.2µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.2V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 2.0V to 1.7V to 2.0V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			+165		°C
	T_J falling			+150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

LDO11, LDO14 and LDO15 (150mA PMOSLS)

(V_{SYS} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx}		2.6		5.5	V
	V_{SYS}		2.6		5.5	
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			4		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3.25		µA
	Low power mode, no load			0.85		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		150			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = V_{INLx} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}			100	200	mV
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		300	560	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		0.6	2.2		µF

LDO11, LDO14 and LDO15 (150mA PMOSLS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x IMAX to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 2.2µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{INLx} = 3.7V to 3.2V to 3.7V, V_{OUT} = default, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs			5		mV
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

LDO10, LDO12 and LDO13 (300mA PMOSLS)

(V_{SYS} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx}		2.6		5.5	V
	V_{SYS}		2.6		5.5	
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			4		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3.25		µA
	Low power mode, no load			0.85		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		300			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = V_{INLx} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}			100	200	mV
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		600	1120	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		0.6	2.2		µF

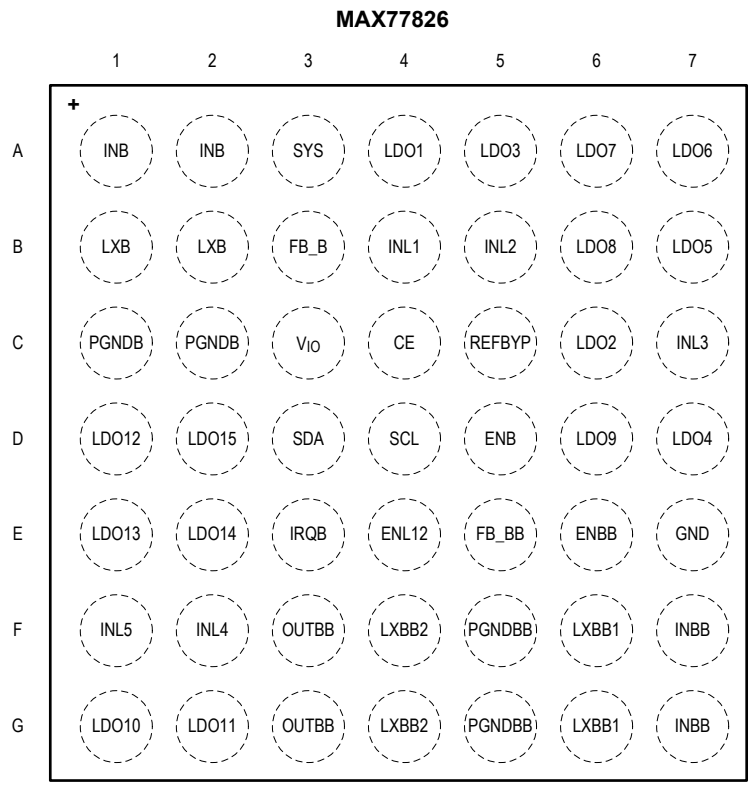
LDO10, LDO12 and LDO13 (300mA PMOSLS) (continued)

(V_{SYS} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 2.2µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{INLx} = 3.7V to 3.2V to 3.7V, V_{OUT} = default, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs			5		mV
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 (or ENL12 = high) to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			+165		°C
	T_J falling			+150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

Note 3: Guaranteed by design. Not production tested.
Note 4: 100% production tested at T_A = +25°C, limits over the operating range are guaranteed by design.
Note 5: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
Note 6: The maximum output current spec is not directly tested. Instead, it is guaranteed by LX NMOS current limit test.
Note 7: For NMOS LDOs, V_{SYS} must be at least 1.5V above V_{OUT} ($V_{SYS} \geq V_{OUT}$ + 1.5V).
Note 8: The maximum output current is guaranteed by the output voltage accuracy tests.
Note 9: For stability, guaranteed by design and not production tested.
Note 10: There is an n-channel MOSFET in series with the output active discharge resistance. This NMOS requires V_{SYS} > 1.2V to be enhanced.

Pin Configurations



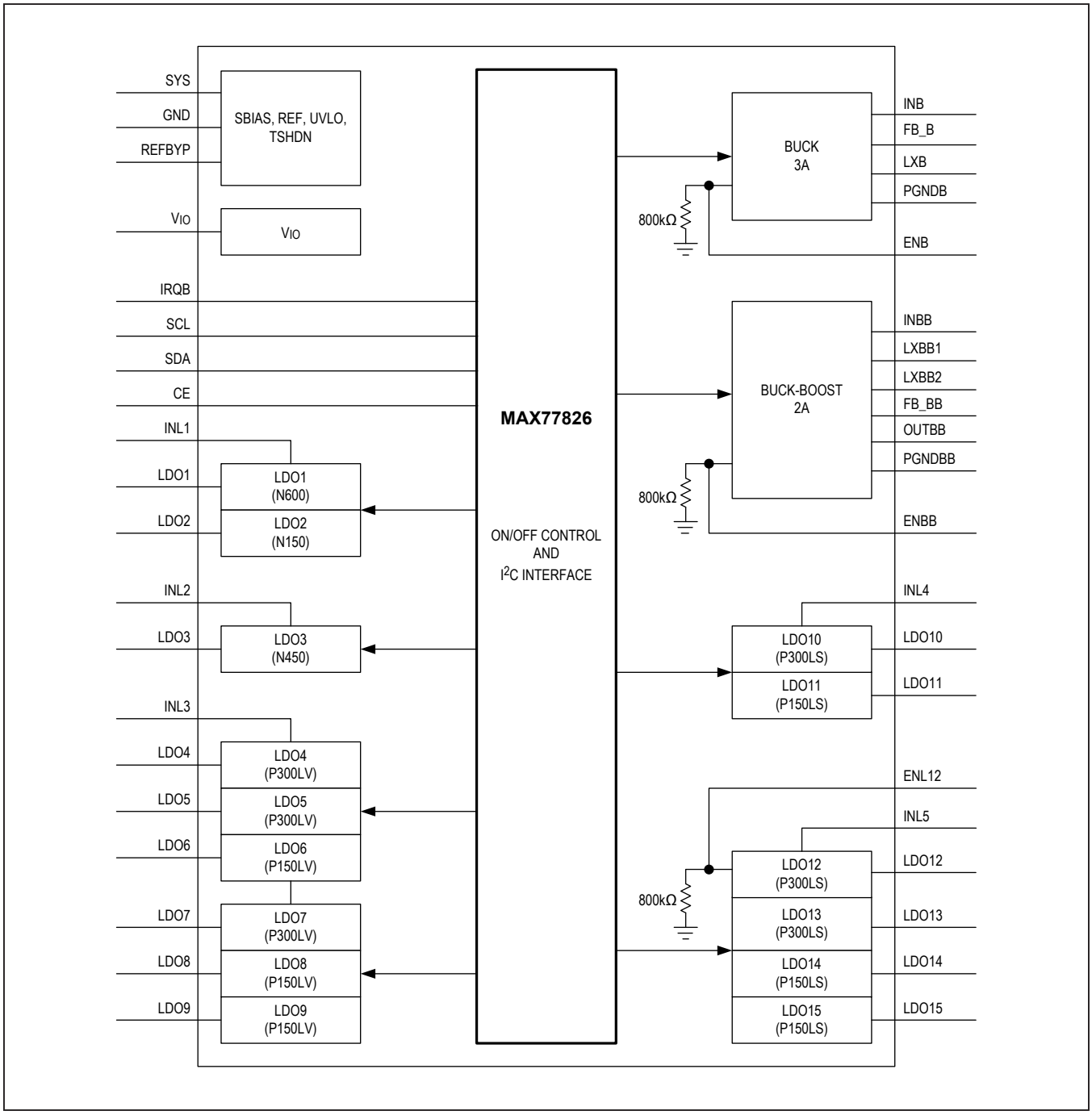
Pin Description

PIN	NAME	FUNCTION
C4	CE	Active-High Chip Enable Input. When CE = high (standby), the I²C interface is enabled and regulators are ready to be turned on. When CE = low (shutdown), all regulators are turned off and all Type-O registers are reset to their POR default values.
D5	ENB	Active-High BUCK External Enable Input. An 800kΩ internal pull-down resistance to the GND. If this pin is not used, leave it floating.
E6	ENBB	Active-High BUCK BOOST External Enable Input. An 800kΩ internal pulldown resistance to the GND. If this pin is not used, leave it unconnected.
E4	ENL12	Active-High LDO12 External Enable Input. An 800kΩ internal pulldown resistance to the GND. If this pin is not used, leave it unconnected.
B3	FB_B	BUCK Output Voltage Feedback
E5	FB_BB	BUCK BOOST Output Voltage Feedback
E7	GND	Ground
A1, A2	INB	BUCK Input. Bypass to PGNDB with a 10µF capacitor.
F7, G7	INBB	BUCK BOOST Input

Pin Description (continued)

PIN	NAME	FUNCTION
B4	INL1	Input for LDO1 and 2. Bypass to GND with a 4.7µF capacitor.
B5	INL2	Input for LDO3. Bypass to GND with a 1µF capacitor.
C7	INL3	Input for LDO4, 5, 6, 7, 8, and 9. Bypass to GND with a 4.7µF capacitor.
F2	INL4	Input for LDO10 and 11. Bypass to GND with a 4.7µF capacitor.
F1	INL5	Input for LDO12, 13, 14, and 15. Bypass to GND with a 4.7µF capacitor.
E3	IRQB	Interrupt Output. A 100kΩ external pullup resistor to V_{IO} is required.
B1, B2	LXB	BUCK Switching Node
F6, G6	LXBB1	BUCK BOOST Switching Node 1
F4, G4	LXBB2	BUCK BOOST Switching Node 2
A4	LDO1	LDO1 (600mA NMOS) Output. Bypass to GND with a 4.7µF capacitor.
C6	LDO2	LDO2 (150mA NMOS) Output. Bypass to GND with a 1µF capacitor.
A5	LDO3	LDO3 (450mA NMOS) Output. Bypass to GND with a 4.7µF capacitor.
D7	LDO4	LDO4 (300mA PMOSLV) Output. Bypass to GND with a 4.7µF capacitor.
B7	LDO5	LDO5 (300mA PMOSLV) Output. Bypass to GND with a 4.7µF capacitor.
A7	LDO6	LDO6 (150mA PMOSLV) Output. Bypass to GND with a 2.2µF capacitor.
A6	LDO7	LDO7 (300mA PMOSLV) Output. Bypass to GND with a 4.7µF capacitor.
B6	LDO8	LDO8 (150mA PMOSLV) Output. Bypass to GND with a 2.2µF capacitor.
D6	LDO9	LDO9 (150mA PMOSLV) Output. Bypass to GND with a 2.2µF capacitor.
G1	LDO10	LDO10 (300mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
G2	LDO11	LDO11 (150mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
D1	LDO12	LDO12 (300mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
E1	LDO13	LDO13 (300mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
E2	LDO14	LDO14 (150mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
D2	LDO15	LDO15 (150mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
F3, G3	OUTBB	BUCK BOOST Output
C1, C2	PGNDB	BUCK Power GND
F5, G5	PGNDBB	BUCK BOOST Power GND
C5	REFBYP	LDO Reference Bypass Node. Connect a 0.1µF Cap to GND.
D4	SCL	I^2C Clock Input. High Impedance in Off State. A 1.5kΩ~2.2kΩ of pullup resistor to VIO is required.
D3	SDA	I^2C Data I/O. High Impedance in Off State. A 1.5kΩ–2.2kΩ of pullup resistor to V_{IO} is required.
A3	SYS	System (Battery) Voltage Input. Bypass to GND with a 1µF capacitor.
C3	V_{IO}	IO Supply Voltage Input. Bypass to GND with a 0.1µF capacitor.

Block Diagram



Detailed Description

Top System Management

System Faults

The MAX77826 monitors the system for the following faults: global thermal, local thermal shutdown, and undervoltage lockout.

Global Thermal Fault

The MAX77826 has a centralized thermal protection circuit which monitors temperature on the die. If the die temperature exceeds +165°C (T_{SHDN}), a thermal shutdown event initiates, and the MAX77826 enters its global shutdown state.

In addition to the +165°C threshold, there are two additional comparators that trip at +120°C and +140°C. Interrupts are generated in the event the die temperature reaches +120°C or +140°C.

There is a 15°C thermal hysteresis. After the thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown bus deasserts.

Local Thermal Shutdown

If any of the BUCK BOOST or LDOs reach the thermal shutdown threshold, the MAX77826 shuts down the corresponding block locally. If the temperature goes below a threshold, that block goes back to normal operation.

Undervoltage Lockout

When V_{SYS} falls below V_{UVLO_F} (typ 2.05V), the MAX77826 enters its undervoltage lockout (UVLO) mode. UVLO forces the MAX77826 to a dormant state until the source voltage is high enough to allow the MAX77826 to be securely functional. I2C does not function and the Type-O register contents are reset to their default values in UVLO mode. UVLO rising threshold is set to 2.5V by an OTP option.

Chip Enable (CE)

A logic-high on CE pin puts the MAX77826 into standby mode (enabled). In standby mode, all user registers are accessible through I2C so that the host processor can overwrite the default output voltages of regulators and each regulator can be enabled by either I2C or the GPIO input if applicable.

When the CE pin goes high, the MAX77826 turns on the top-level bias circuitry, and it takes typically 85µs to settle. As soon as the top-level bias is ready, BUCK BOOST is ready to be turned on. However, BUCK and LDOs require additional 85µs (typ) for REFBYP to settle. Total, it takes 170µs (85µs + 85µs) for REFBYP to settle from CE = high. In the worst-case scenario, it can take up to 230µs. Once REFBYP is ready, all the regulators are allowed to be tuned on through I2C or the ENx pins. In case the regulars are enabled before the bias circuitry is ready, the regulators require longer time to startup.

When CE pin is pulled low, the MAX77826 goes into shutdown mode (disabled) and turns off all the regulators regardless of ENx pins. This event also resets all Type-O registers to their POR default values.

Immediate Shutdown Events

The following events initiate immediate shutdown: thermal protection (T_J > +165°C), V_{SYS} < V_{SYS} UVLO falling threshold (V_{UVLO_F}), V_{IO} < V_{IO} OK threshold ($V_{TH_VIO_OK}$)

The events in this category are associated with potentially hazardous system states. Powering down the host processor and resetting all Type-O registers help mitigate any issues that can occur due to these potentially hazardous conditions. Note that the MAX77826 cannot be enabled until the junction temperature drops below +150°C in case thermal protection caused the immediate shutdown.

Operating Mode (OPMD)

Each regulator (BUCK, BUCK BOOST, and LDO) has independent register bits to control its operating mode. These bits determines on/off operation during initial startup, output enable control, and sleep mode operation based on the enable control logic of each regulator. The POR default values of output enable bits (x_EN) are 0 (output off).

Enable Control Logic1

BUCK, BUCK BOOST, and LDO12 have independent I2C enable bits and dedicated GPIO enable pins (ENB, ENBB, and ENL12). As shown in Table 1, regulators can be turned on/off by ENx or I2C control bits.

Enable Control Logic 2

LDO1–LDO11 and LDO13–LDO15 have independent I2C enable bits. As shown in Table 2, regulators can be turned on/off by the I2C control bits.

Reset Conditions

System Reset

When V_{SYS} voltage drops below its POR threshold (≈1.55V), all Type-S1 registers are reset to their POR default values.

Off Reset

Off reset occurs by any power-off events. This condition resets all Type-O registers to their POR default values.

Table 1. Enable Control Logic 1 Truth Table

CE	ENx	B_EN BB_EN L12_EN	B_LPM L12_LPM	OPERATING MODE
Low	x	x	x	Device off
High	Low	0	x	Output off
High	High	x	1	Output on (low power mode*)
High	High	x	0	Output on
High	x	1	1	Output on (low power mode*)
High	x	1	0	Output on

**The BUCK BOOST regulator does not have a low power mode.*

Table 2. Enable Control Logic 2 Truth Table

CE	Lx_EN	Lx_LPM	OPERATING MODE
Low	x	x	Device off
High	0	x	Output off
High	1	1	Output on (low power mode)
High	1	0	Output on

Interrupt and Mask

IRQB pin is used to indicate to the host processor that the status on the MAX77826 has changed. IRQB signal is asserted whenever one or more interrupts are triggered. The host processor reads the interrupt source register (ADDR 0x00) and the interrupt registers as indicated by the interrupt source register in order to see the cause of interrupt event.

Each interrupt register can be read at a time. IRQB pin goes high (cleared) as soon as the read sequence finishes. If an interrupt is captured during the read sequence, IRQB pin is held low. Note that the interrupt source register is cleared when the corresponding interrupt registers are read by the host processor.

Each interrupt can be masked (disabled) by setting the corresponding interrupt mask register bit. In case an interrupt mask bit is set (masked), the corresponding interrupt bit is not supposed to be set even when the interrupt condition is met. As a result, the IRQB pin stays high for this event. If the mask bit is cleared for an active interrupt, the corresponding interrupt bit is set to pull the IRQB pin low.

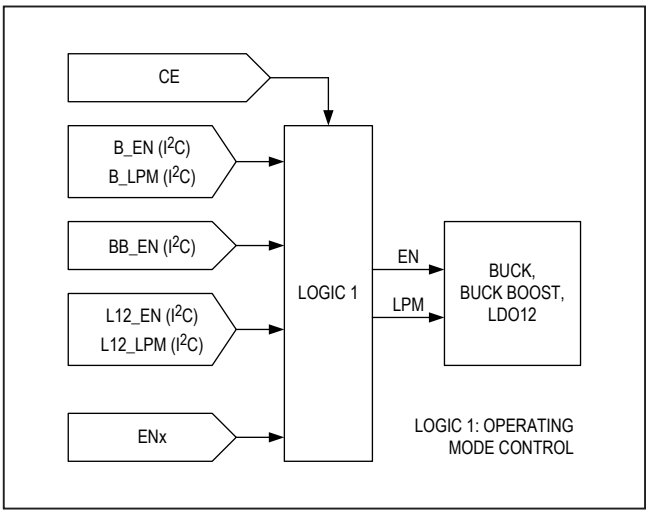


Figure 1. Enable Control Logic 1

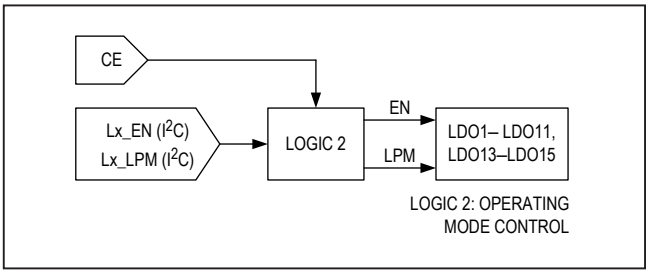


Figure 2. Enable Control Logic 2

BUCK Regulator

The MAX77826 includes a 3A current-mode BUCK regulator. In normal operation, BUCK consumes only 22µA quiescent current. In low power mode, the quiescent current is decreased to 8µA with reduced load capability.

The summary of features is:

- 3A of maximum output current rating
- 2.6V to 5.5V input voltage range
- Output voltage range from 0.50V to 1.80V in 6.25mV steps
- ±1% (typ) output voltage DC accuracy
- 2MHz (typ) switching frequency
- Automatic SKIP/PWM or forced PWM modes
- > 90% peak efficiency
- Programmable slew rate for increasing output voltage settings

Operating Mode Control

The operating mode bit resides in the top level that controls the enable/disable state of BUCK through the B_EN register and also controls the operating mode (low power or normal mode) through the B_LPM register.

SKIP/Forced PWM Operation

In normal operating mode, BUCK automatically transitions from SKIP mode to fixed frequency operation as load current increases. For operating modes where lowest output ripple is required, forced PWM switching behavior can be enabled by writing 1 to B_FPWM bit.

Low Power Mode Operation

In low power mode, the quiescent current is reduced from 22µA to 8µA. The output current is limited to 10mA. It is not recommended to adjust the output voltage in low power mode. The regulator does not automatically enter/exit low power mode. The host processor needs to control low power mode operation in times of known low power states through the I^2C serial interface.

Startup and Soft-Start

When starting up BUCK regulator, the bias circuitry must be enabled and provided with adequate time to settle. The bias circuitry is guaranteed to settle within 250µs, at which time, the BUCK regulators' power-up sequences can commence. Note that attempting to implement a power-up sequence before BIASOK signal is generated results in all enabled regulators starting up at the same time.

The BUCK regulator supports starting into a prebiased output. For example, if the output capacitor has an initial voltage of 0.4V when the regulator is enabled, the regulator gradually increases the capacitor voltage to the required target voltage such as 1.0V. This is unlike other regulators without the start into prebias feature in which they can force the output capacitor voltage to 0V before the soft-start ramp begins.

The BUCK regulator has a soft-start rate of 14mV/µs. The controlled soft-start rate and BUCK regulator current limit (I_{LIMP}) limit the input inrush current to the output capacitor (I_{INRUSH}). I_{INRUSH} = min (I_{LIMP} and C_{OUT} x dv/dt). Note that the input current of BUCK regulator is lower than the inrush current to the output capacitor by the ratio of output to input voltage.

Output Voltage Setting

The output voltage is programmable from 0.50V to 1.80V in 6.25mV steps to allow fine adjustment to the processor supply voltage under light load conditions to minimize power loss within the processor. The default output voltage is set by an OTP option at the factory. The default output voltage can be overwritten by changing the contents in B_VOUT[7:0] register prior to enabling the regulator. The output voltage can also be adjusted during normal operation.

Changing Output Voltage While Operating

In a typical smartphone or tablet application, there are several power domains in which the operating frequency of the processor increases or decreases (DVFS). When the operating frequency needs to be changed, it is expected that BUCK regulator responds to a command to change the output voltages to new target values quickly. The high peak current limit, coupled with low inductance and small output capacitance, allows the BUCK regulator to respond to a positive step change in output voltage and settle to the new target value quickly. The BUCK regulator provides programmable ramp-up slew rates to accommodate different requirements.

For a negative step change in output voltage, the settling time is not critical. In forced PWM mode (either B_FPWM bit or B_FSRAD bit is enabled), the negative inductor current through NMOS discharges energy from the output capacitor to help the output voltage decrease to the new target value faster. In skip mode, negative inductor current is not allowed so that the output voltage settling time is dependent on the load current and the output capacitance.

Output Voltage Slew Rate Control

The BUCK regulator supports programmable slew rate control feature when increasing and decreasing the output voltage. The ramp-up slew rate can be set to 12.5mV/µs, 25mV/µs, 50mV/µs or 100mV/µs independently through the B_RAMP[1:0] bits, while the ramp-down slew rate is fixed to 6.25mV/µs.

Output Active Discharge Resistance

BUCK provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (B_AD = 1), the internal resistor discharges the energy stored in the output capacitor to GND whenever the regulator is disabled.

Either the regulator remains enabled or the active discharge function is disabled (B_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

Inductor Selection

BUCK is optimized for a 0.47µH inductor. The lower the inductor DCR, the higher BUCK efficiency is. Users need to trade off inductor size with DCR value and choose a suitable inductor for BUCK.

Input Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. The recommended minimum output capacitance for BUCK is 22µF.

BUCK BOOST Regulator

The MAX77826 BUCK BOOST regulator utilizes a four-switch H-bridge configuration to realize BUCK, BUCK BOOST, and BOOST operating modes. In this way, this topology maintains output voltage regulation when the input voltage is greater than, equal to, or less than the output voltage. The MAX77826 BUCK BOOST is ideal in Li-ion battery powered applications, providing 2.6V to 4.1875V output voltage and up to 2A output current across the input voltage range. High switching frequency and a unique control algorithm allow the smallest solution size, low output noise, and highest efficiency across a wide input voltage and output current range.

The MAX77826 BUCK BOOST regulator typically generates a 3.50V output voltage. The input current limit is set to 3.5A (typ) to guarantee delivery of 2A at 3.50V from 3.0V input. Internal soft-start limits the inrush current at startup.

Table 3. Suggested Inductors for BUCK

MANUFACTURER	SERIES	NOMINAL INDUCTANCE (µH)	DC RESISTANCE (typ, mΩ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT = +40°C RISE	DIMENSIONS L x W x H (mm)
Semco	CIGT201610G MR47MNE	0.47	35	4.0	2.9	2.0 x 1.6 x 1.0
Toko	DFE201610-H -R47N	0.47	37	3.5	3.5	2.0 x 1.6 x 1.0

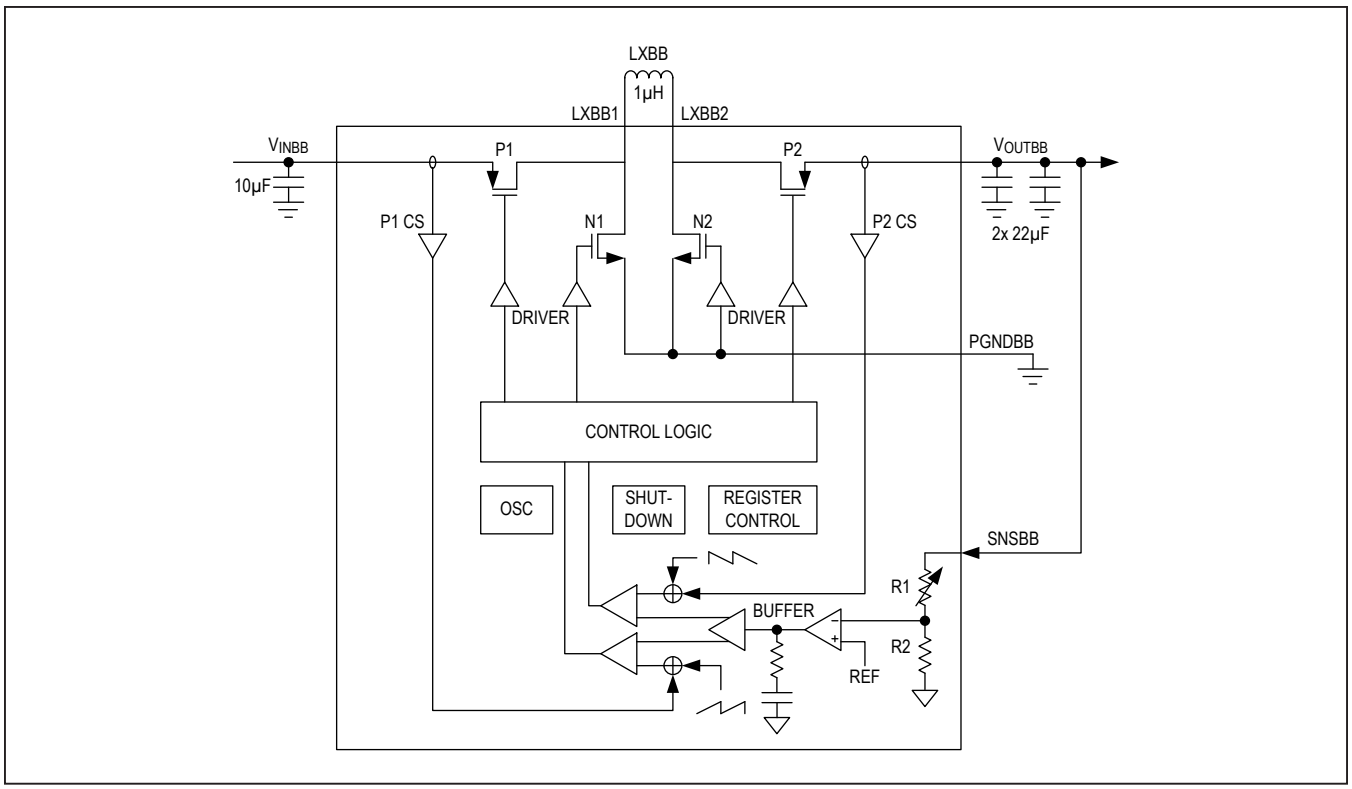


Figure 3. BUCK BOOST Block Diagram

H-Bridge Controller

The H-bridge architecture operates at 3MHz fixed frequency with a pulse width modulated (PWM), current mode control scheme. This topology is in a cascade of a BOOST regulator and a BUCK regulator using a single inductor and output capacitor. BUCK, BUCK BOOST, and BOOST stages are 100% synchronous for highest efficiency in portable applications.

There are three phases implemented with the H-bridge switch topology, as shown in Figure 4:

Φ1 switch period (Phase 1: P1 = on, N2 = on) stores energy in the inductor, ramping up the inductor current at a rate proportional to the input voltage divided by inductance; $V_{INBB/L}$.

Φ2 switch period (Phase 2: P1 = on, N3 = on) ramps the inductor current up or down, depending on the differential voltage across the inductor, divided by inductance; $\pm(V_{INBB} - V_{OUTBB})/L$.

Φ3 switch period (Phase 3: N1 = on, N3 = on) ramps down the inductor current at a rate proportional to the output voltage divided by inductance, $-V_{OUTBB}/L$.

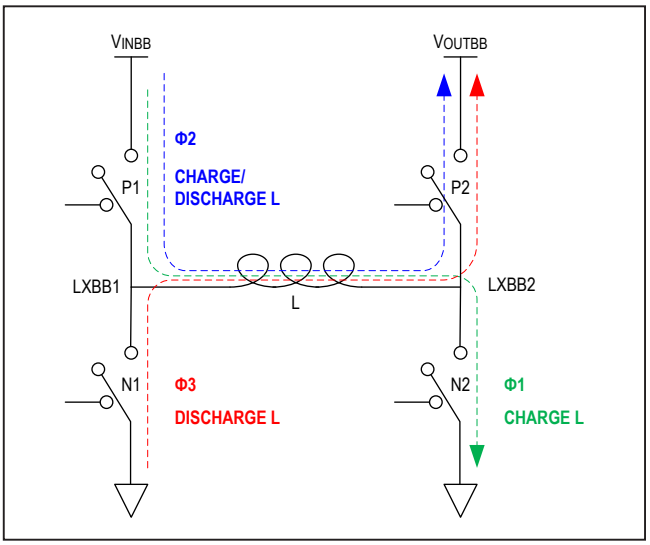


Figure 4. BUCK BOOST Switching Intervals

2-Phase BUCK topology is utilized when $V_{INBB} > V_{OUTBB}$. A switching cycle is completed in one clock periods. Switch period Φ2 is followed by switch period Φ3, resulting in an inductor current waveform similar to Figure 5.

3-Phase BUCK topology is utilized when $V_{INBB} > V_{OUTBB}$ and 2-Phase BUCK cannot support V_O. Switch period is: Φ1 → Φ2 → Φ3. Switch period Φ1 is fixed. This results in an inductor current waveform similar to Figure 6.

2-Phase BOOST topology is utilized when $V_{INBB} < V_{OUTBB}$. A switching cycle is completed in one clock periods. Switch period Φ1 is followed by switch period Φ2, resulting in an inductor current waveform similar to Figure 7.

3-Phase BOOST topology is utilized when $V_{INBB} < V_{OUTBB}$ and 2-Phase BOOST cannot support V_O. Switch period is: Φ1 → Φ2 → Φ3. Switch period Φ3 is fixed. This results in an inductor current waveform similar to Figure 8.

Inductor Selection

BUCK BOOST is optimized for a 1µH inductor. The lower the inductor DCR, the higher BUCK BOOST efficiency is. Users need to trade off inductor size with DCR value and choose a suitable inductor for BUCK BOOST.

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. The recommended minimum output capacitance for BUCK BOOST is 47µF.

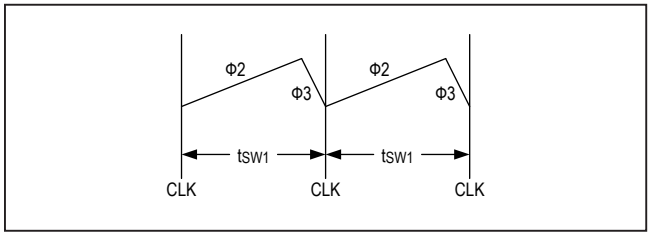


Figure 5. 2-Phase BUCK Switching Current Waveforms

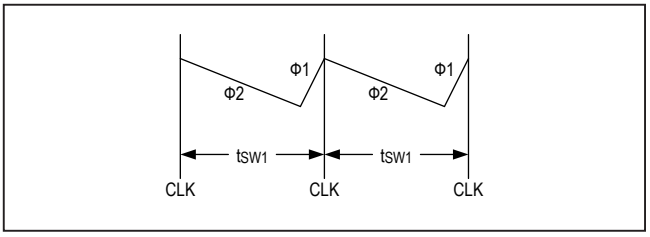


Figure 7. 2-Phase BOOST Mode Switching Current Waveform

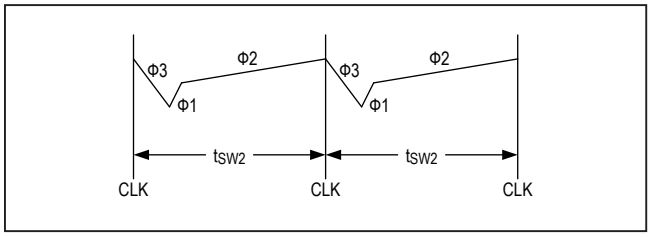


Figure 6. 3-Phase BUCK Switching Current Waveforms When $V_{INBB} > V_{OUTBB}$

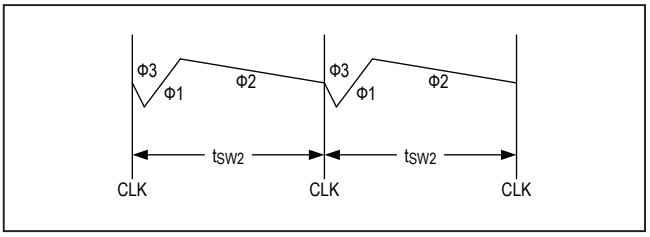


Figure 8. BOOST Mode Switching Current Waveforms When $V_{INBB} < V_{OUTBB}$

Table 4. Suggested Inductors for BUCK BOOST

MANUFACTURER	SERIES	NOMINAL INDUCTANCE (µH)	DC RESISTANCE (typ, mΩ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT = +40°C RISE	DIMENSIONS L x W x H (mm)
TDK	TFM201610GHM -1R0MTAA	1.0	50	3.8	3.0	2.0 x 1.6 x 1.0

Linear Regulators

The MAX77826 provides 15 low dropout linear regulators including 3 NMOS LDOs, 6 PMOSLV LDOs, and 6 PMOSLS LDOs. Each of these regulators draws 27µA/18µA (NMOS/PMOS) of quiescent current in normal operating mode and < 5µA in low power mode. PMOSLV LDOs allow input voltages as low as 1.7V for optimized system efficiency.

All regulators can be operated in low power mode that supports up to 5mA of maximum load current.

The summary of features is:

- 3 NMOS LDOs (V_{OUT} range: 0.6V to 2.1875V with 12.5mV step)
  - 1 x 150mA
  - 1 x 450mA
  - 1 x 600mA
- 6 PMOSLV LDOs (V_{OUT} range: 0.8V to 3.975V with 25mV step)
  - 3 x 150mA
  - 3 x 300mA
- 6 PMOSLS LDOs (V_{OUT} range: 0.8V to 3.975V with 25mV step)
  - 3 x 150mA
  - 3 x 300mA
  - ±1.5% typical Output Voltage DC Accuracy
  - 70dB PSRR at 1kHz

LDO Reference

The MAX77826 has a single LDOREF bias rail. LDOREF is enabled or disabled along with the central bias block (SBIA) so that LDOREF is ready whenever any LDO turns on. It has a very low quiescent current of 2µA typical.

Operating Mode Control

The operation mode bits for each LDO reside in the top level that controls the enable/disable state for each LDO through the Lx_EN signal and also controls the operation modes (low power or normal mode) for each LDO through the Lx_LPM signal.

Low Power Mode

In low power mode, the quiescent current of each LDO is reduced from 27µA/18µA (NMOS/PMOS) to less than 5µA. The output current of each LDO is limited to 5mA if operating in low power mode. Each LDO can be individually enabled to operate in low power mode.

Soft-Start and Dynamic Voltage Change

When a regulator is enabled, the output voltage ramps to the final voltage at the slew rate of 30mV/µs. The 30mV/µs ramp rate results in around 30mA inrush current with a 1.0µF output capacitor under no load condition. For a 1.8V LDO ramping from 0V, the output voltage regulation is achieved within 60µs. The soft-start ramp rate is also the rate of change at the output when switching dynamically between two output voltages without disabling. The soft-start circuitry of LDOs supports starting into a prebiased output.

Output Active Discharge

Each LDO provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (Lx_AD = 1), the internal resistor discharges the energy stored in the output capacitor to GND whenever the regulator is disabled.

Either the regulator remains enabled or the active discharge function is disabled (Lx_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

Thermal Considerations

In most applications, the MAX77826 does not dissipate much heat because of its high efficiency. However, in applications where the MAX77826 runs with heavy loads at high ambient temperature, the junction temperature can exceed the maximum operating temperature. In case the junction temperature reaches approximately +165°C, the thermal overload protection triggers. The maximum power dissipation of the MAX77826 depends on the thermal resistance of the IC package and PCB. The power dissipated in the device is:

$$P_D = P_{OUT} \times (1/\eta - 1)$$

where η is the efficiency of the regulator and P_{OUT} is the output power delivered to the load.

The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

$T_{JMAX} - T_A$ is the temperature difference between the maximum rated junction temperature and the ambient temperature, θ_{JA} is the thermal resistance between the junction and the ambient.

Serial Interface

The I2C-compatible, 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the Register Map for details.

The I2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

I2C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

The figure above shows an example of a typical I2C system. A device on I2C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is addressed by the master is considered a slave. When the MAX77826 I2C-compatible interface is operating in normal mode, it is a slave on I2C bus, and it can be both a transmitter and a receiver.

Bit Transfer

One data bit transfers for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

START and STOP Conditions

When the I2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the MAX77826. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the MAX77826 internally disconnects SCL from the I2C serial interface until the next START condition, minimizing digital noise and feedthrough.

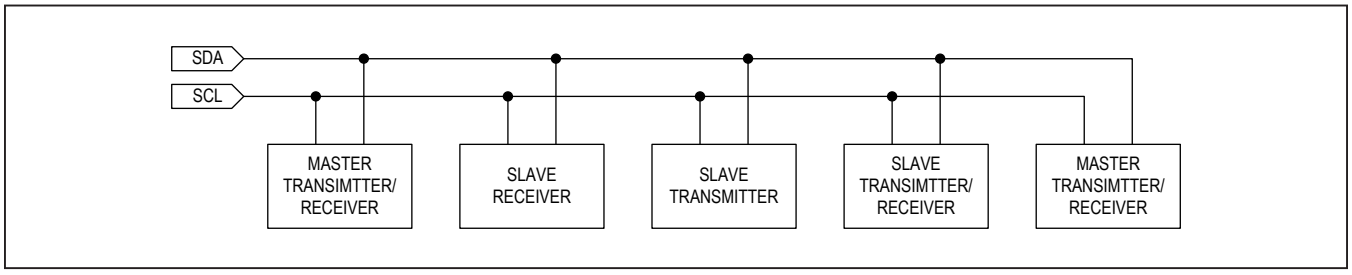


Figure 9. Functional Logic Diagram for Communications Controller

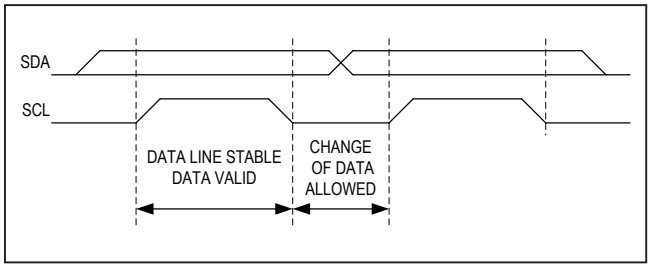


Figure 10. I2C Bit Transfer

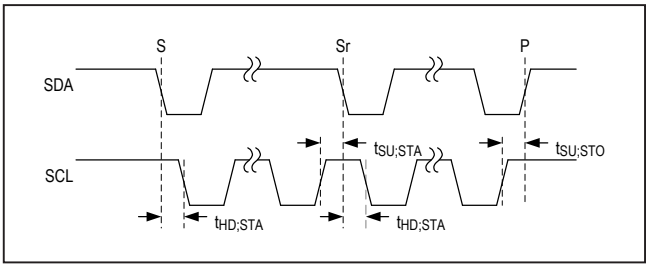


Figure 11. START and STOP Conditions

Acknowledge

Both the I2C bus master and MAX77826 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The I2C slave address of the MAX77826 is shown in Table 5.

In general, the clock signal generation for the I2C bus is the responsibility of the master device. The I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77826 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77826 does not implement I2C specification general call address. If the MAX77826 sees the general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

Table 5. Power Management Slave Address

SLAVE ADDRESS (7 bit)	SLAVE ADDRESS (Write)	SLAVE ADDRESS (Read)
110 0000	0xC0 (1100 0000)	0xC1 (1100 0001)

Communication Speed

The MAX77826 provides an I2C 3.0-compatible (3.4MHz) serial interface.

- I2C revision 3-compatible serial communications channel
  - 0Hz to 100kHz (standard mode)
  - 0Hz to 400kHz (fast mode)
  - 0Hz to 1MHz (fast mode plus)
  - 0Hz to 3.4MHz (high-speed mode)
  - Does not utilize I2C clock stretching

Operating in standard mode, fast mode and fast mode plus do not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation is (V2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I2C 3.0 specification. The major considerations with respect to the MAX77826 are:

- The I2C bus master uses current source pullups to shorten the signal rise times.
- The I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

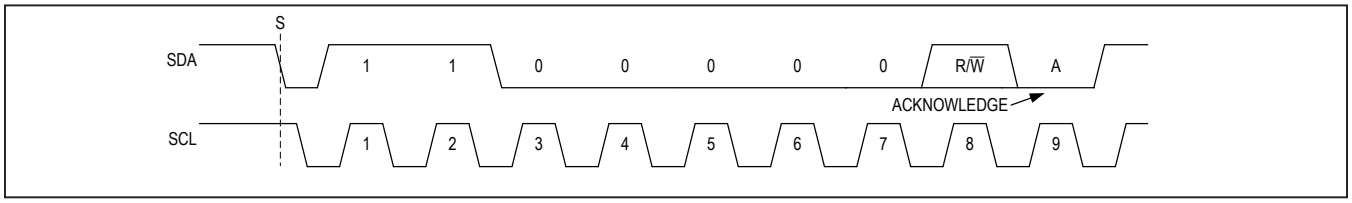


Figure 12. Slave Address Byte Example for Power Block

At power-up and after each STOP condition, the MAX77826 inputs filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in *Communication Protocols* section.

Communication Protocols

The MAX77826 supports both writing and reading from its registers. Table **TBD** shows the I2C communication protocols for each functional block. The power block uses the same communications protocols.

Writing to a Single Register

Figure 13 shows the protocol for the I2C master device to write one byte of data to the MAX77826. This protocol is the same as the SMBus specification's write byte protocol. The write byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data
8) The slave acknowledges or does not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Writing to Sequential Registers

Figure 14 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START. The writing to sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).

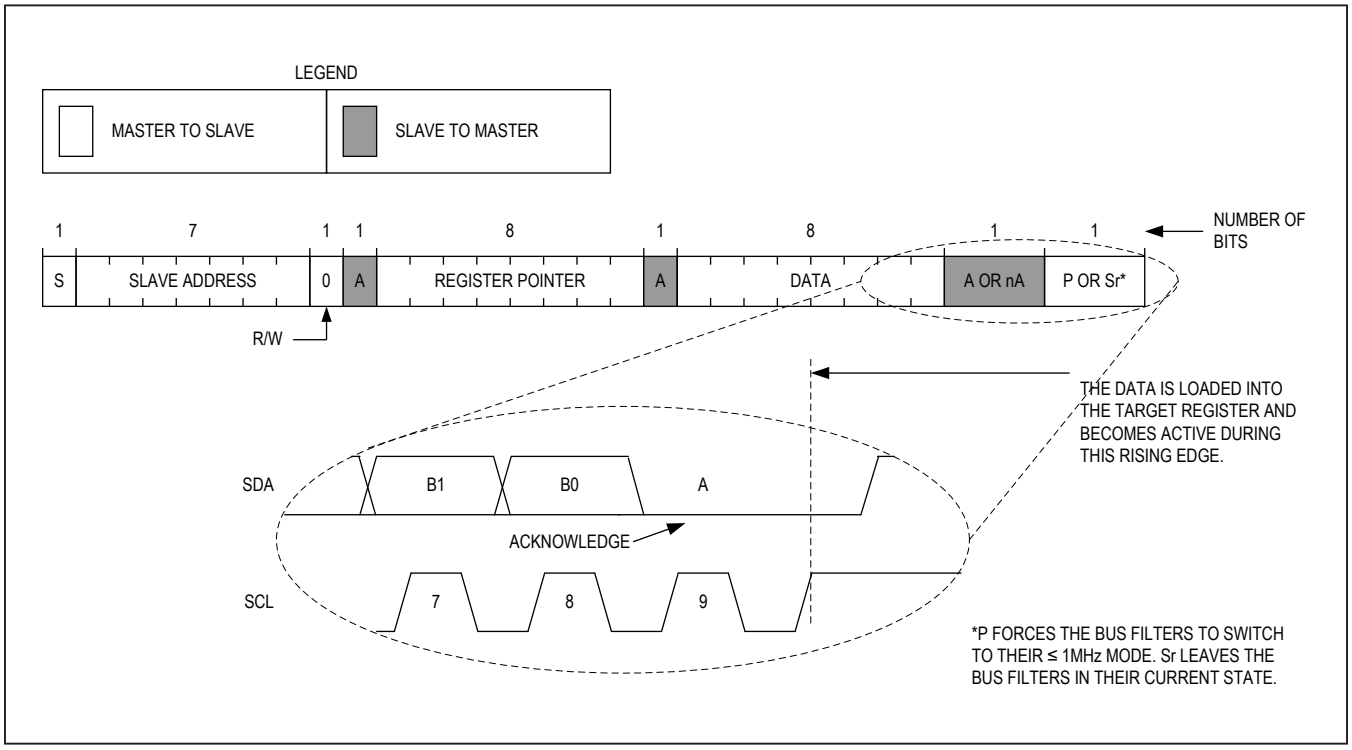


Figure 13. Writing to a Single Register with Write Byte Protocol

3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register, and the data becomes active.
8) Steps 6 and 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the master can issue an ACKNOWLEDGE (A) or a NOT ACKNOWLEDGE (nA).
10) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

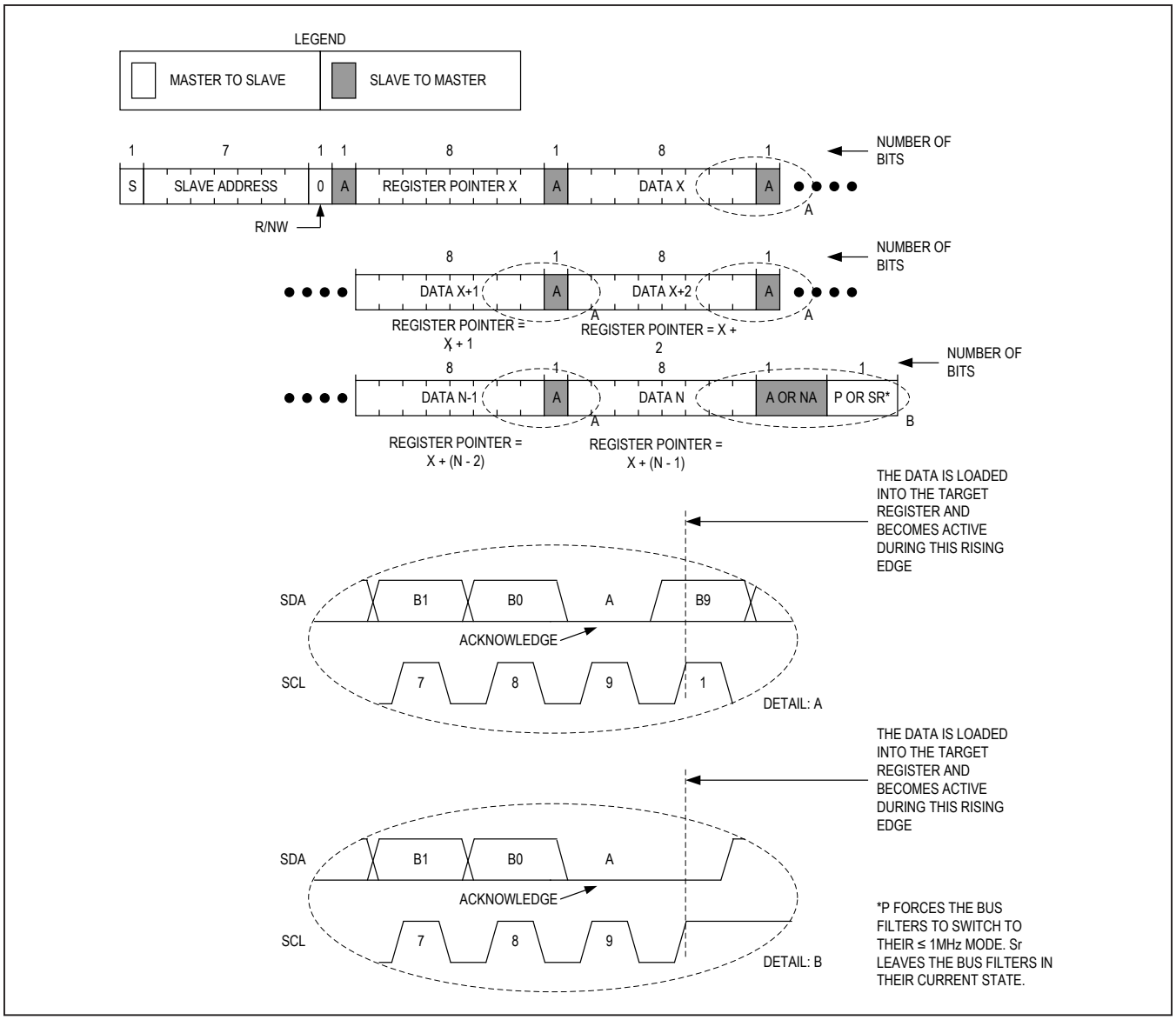


Figure 14. Writing to Sequential Registers X to N

Writing Multiple Bytes using Register-Data Pairs

Figure 15 shows the protocol for I2C master device to write multiple bytes to the MAX77826 using register-data pairs. This protocol allows I2C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a STOP condition. The multiple byte register-data pair protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8) Steps 4 to 7 are repeated as many times as the master requires.
9) The master sends a STOP condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

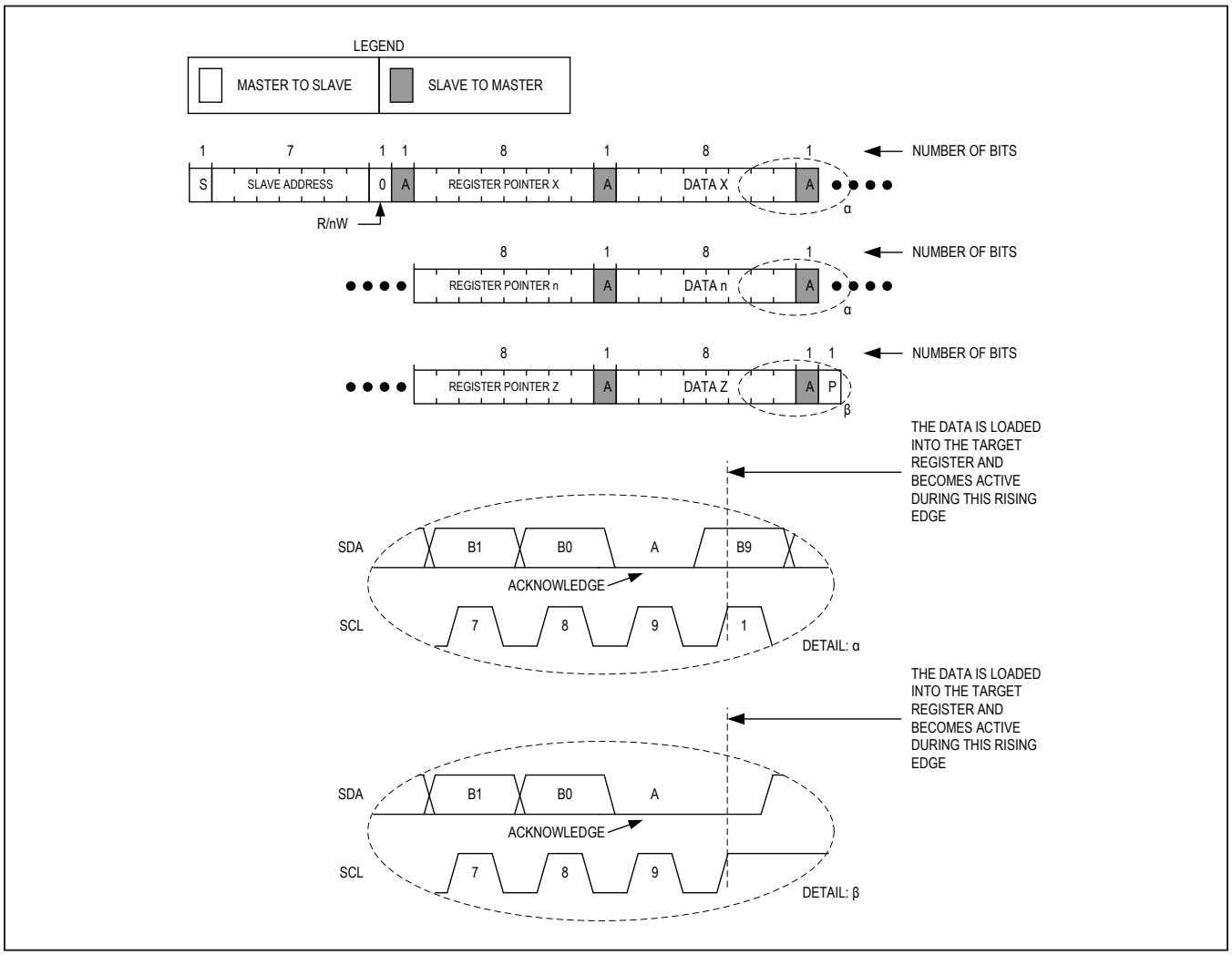


Figure 15. Writing to Multiple Registers with Multiple Byte Register-Data Pairs Protocol

Reading from a Single Register

The I2C master device reads one byte of data to the MAX77826. This protocol is the same as SMBus specification's read byte protocol. The read byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8 bit of data on the bus from the location specified by the register pointer.
10) The master issues a NOT ACKNOWLEDGE (nA).
11) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Note that every time MAX77826 receives a STOP, its register pointer is set to 0x00. If reading register 0x00 after a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

Reading from Sequential Registers

Figure 16 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data. When the master has all the data it requires, it issues a NOT ACKNOWLEDGE (nA) and a STOP (P) to end the transmission. The continuous read from sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8 bit of data on the bus from the location specified by the register pointer.
10) The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Note that every time the MAX77826 receives a STOP its register pointer is set to 0x00. If reading register 0x00 after a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

Engaging HS-Mode for Operation up to 3.4MHz

Figure 17 shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed up to 3.4MHz. The engaging HS mode protocol is as follows:

1) Begin the protocol while operating at a bus speed of 1MHz or lower.
2) The master sends a START command (S).
3) The master sends the 8-bit master code of 00001xxxb where xxxb are don't care bits.
4) The addressed slave issues a NOT ACKNOWLEDGE (nA).
5) The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.
6) The master may continue to issue high-speed read/write operations until a STOP (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. After a STOP has been issued, steps 1 to 6 in the above algorithm may be skipped.

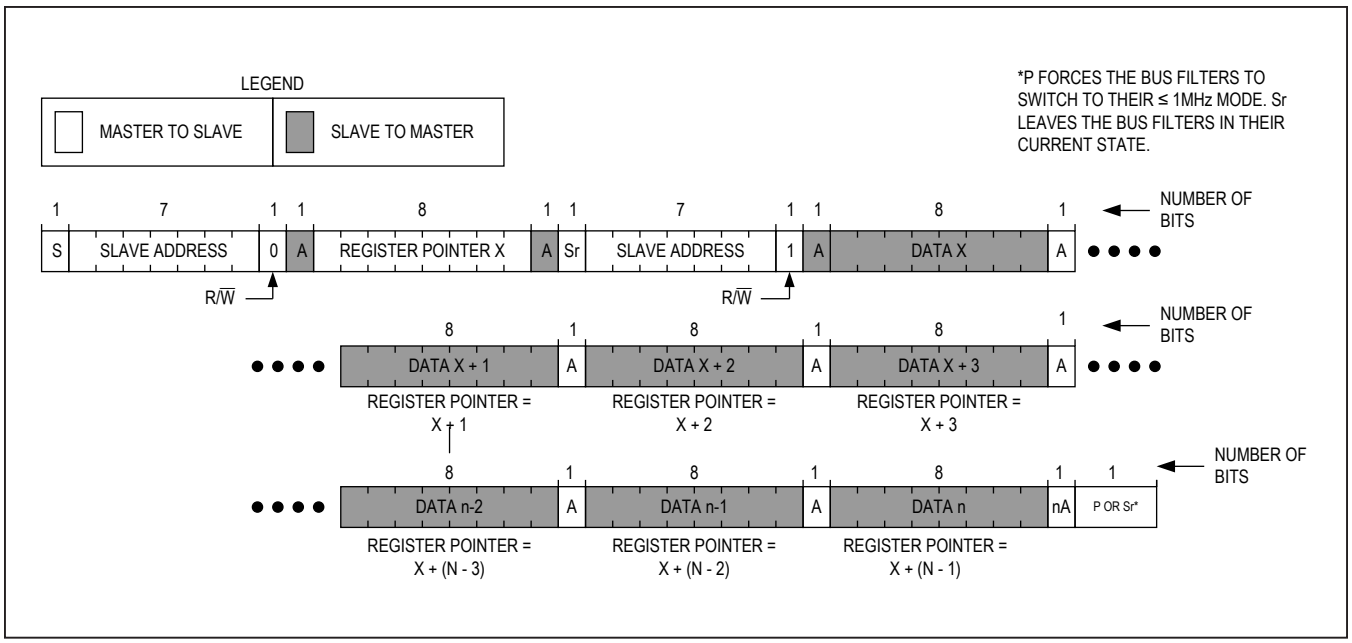


Figure 16. Reading Continuously from Sequential Registers with X to N

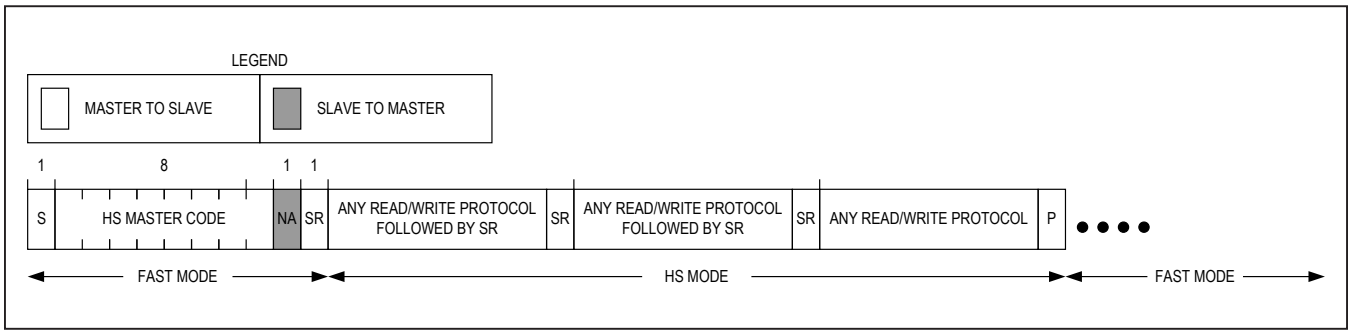


Figure 17. Engaging HS Mode

PMIC Registers

Register Reset Conditions

Type-S1: Registers are reset when V_{SYS} < POR (≈1.55V)

Type-O: Registers are reset when $V_{SYS} < V_{UVLO}$ OR $V_{IO} < V_{TH_VIO_OK}$ OR CE = LOW

Register Map

I²C Slave Address (W/R): 0xC0/0xC1

ADDR	NAME	RESET TYPE	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE
0x00	INT_SRC	Type-O	R	RSVD	RSVD	RSVD	RSVD	RSVD	BB_INT	REG_ INT	TOPSYS _INT	0x00
0x01	SYS_INT	Type-S1	R/C	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TJCT_ 120C	TJCT_ 140C	0x00
0x02	REG_ INT1	Type-S1	R/C	LDO8_ POKn	LDO7_ POKn	LDO6_ POKn	LDO5_ POKn	LDO4_ POKn	LDO3_ POKn	LDO2_ POKn	LDO1_ POKn	0x00
0x03	REG_ INT2	Type-S1	R/C	B_POKn	LDO15_ POKn	LDO14_ POKn	LDO13_ POKn	LDO12_ POKn	LDO11_ POKn	LDO10_ POKn	LDO9_ POKn	0x00
0x04	BB_ INT	Type-S1	R/C	RSVD	RSVD	RSVD	RSVD	RSVD	BB_PO_{Kn}	BB_ OVP	BB_OCP	0x00
0x05	INT_ SRC_M	Type-O	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	BB_ INT_M	REG_ INT_M	TOPSYS _INT_M	0x07
0x06	TOPSYS _INT_M	Type-O	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TJCT_ 120C_M	TJCT_ 140C_M	0x03
0x07	REG_ INT1_M	Type-O	R/W	LDO8_ POKn_M	LDO7_ POKn_M	LDO6_ POKn_M	LDO5_ POKn_M	LDO4_ POKn_M	LDO3_ POKn_M	LDO2_ POKn_M	LDO1_ POKn_M	0xFF
0x08	REG_ INT2_M	Type-O	R/W	B_ POKn_M	LDO15_ POKn_M	LDO14_ POKn_M	LDO13_ POKn_M	LDO12_ POKn_M	LDO11_ POKn_M	LDO10_ POKn_M	LDO9_ POKn_M	0xFF
0x09	BB_ INT_M	Type-O	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	BB_ POKn_M	BB_ OVP_M	BB_ OCP_M	0x07
0x0A	TOPSYS_ STAT	Type-O	R	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TJCT_ 120C	TJCT_ 140C	—
0x0B	REG_ STAT1	Type-O	R	LDO8_ POKn	LDO7_ POKn	LDO6_ POKn	LDO5_ POKn	LDO4_ POKn	LDO3_ POKn	LDO2_ POKn	LDO1_ POKn	—
0x0C	REG_ STAT2	Type-O	R	B_POKn	LDO15_ POKn	LDO14_ POKn	LDO13_ POKn	LDO12_ POKn	LDO11_ POKn	LDO10_ POKn	LDO9_ POKn	—
0x0D	BB_ STAT	Type-O	R	RSVD	RSVD	RSVD	RSVD	RSVD	BB_ POKn	BB_ OVP	BB_ OCP	—
0x0E–0x0F	RSVD											
0x10	LDO_ OPMD1	Type-O	R/W	L4_EN	L4_LPM	L3_EN	L3_LPM	L2_EN	L2_LPM	L1_EN	L1_ LPM	0x00

Register Map (continued)

I²C Slave Address (W/R): 0xC0/0xC1 (continued)

ADDR	NAME	RESET TYPE	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE
0x11	LDO_ OPMD2	Type-O	R/W	L8_EN	L8_LPM	L7_EN	L7_LPM	L6_EN	L6_LPM	L5_EN	L5_ LPM	0x00
0x12	LDO_ OPMD3	Type-O	R/W	L12_EN	L12_ LPM	L11_EN	L11_LPM	L10_EN	L10_LPM	L9_EN	L9_ LPM	0x00
0x13	LDO_ OPMD4	Type-O	R/W	RSVD	RSVD	L15_EN	L15_LPM	L14_EN	L14_LPM	L13_ EN	L13_ LPM	0x00
0x14	B_BB_ OPMD	Type-O	R/W	RSVD	RSVD	RSVD	RSVD	BB_EN	RSVD	B_EN	B_ LPM	0x00
0x15–0x1F	RSVD											
0x20	LDO1_ CFG	Type-O	R/W	L1_AD	L1_VOUT[6:0]							0xA0
0x21	LDO2_ CFG	Type-O	R/W	L2_AD	L2_VOUT[6:0]							0xA0
0x22	LDO3_ CFG	Type-O	R/W	L3_AD	L3_VOUT[6:0]							0xA0
0x23	LDO4_ CFG	Type-O	R/W	L4_AD	L4_VOUT[6:0]							0x9C
0x24	LDO5_ CFG	Type-O	R/W	L5_AD	L5_VOUT[6:0]							0xA8
0x25	LDO6_ CFG	Type-O	R/W	L6_AD	L6_VOUT[6:0]							0xA8
0x26	LDO7_ CFG	Type-O	R/W	L7_AD	L7_VOUT[6:0]							0xA8
0x27	LDO8_ CFG	Type-O	R/W	L8_AD	L8_VOUT[6:0]							0xA8
0x28	LDO9_ CFG	Type-O	R/W	L9_AD	L9_VOUT[6:0]							0xA8
0x29	LDO10_ CFG	Type-O	R/W	L10_AD	L10_VOUT[6:0]							0xD0
0x2A	LDO11 _CFG	Type-O	R/W	L11_AD	L11_VOUT[6:0]							0xD0

Register Map (continued)

I²C Slave Address (W/R): 0xC0/0xC1 (continued)

ADDR	NAME	RESET TYPE	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE
0x2B	LDO12_CFG	Type-O	R/W	L12_AD	L12_VOUT[6:0]							0xE4
0x2C	LDO13_CFG	Type-O	R/W	L13_AD	L13_VOUT[6:0]							0xE4
0x2D	LDO14_CFG	Type-O	R/W	L14_AD	L14_VOUT[6:0]							0xE4
0x2E	LDO15_CFG	Type-O	R/W	L15_AD	L15_VOUT[6:0]							0xE4
0x2F	RSVD											
0x30	BUCK_CFG	Type-O	R/W	B_RAMP[1:0]		RSVD	RSVD	B_AD	B_FPWM	RSVD	B_FSRADE	0x09
0x31	BUCK_VOUT	Type-O	R/W	B_VOUT[7:0]								0x78
0x32	BB_CFG	Type-O	R/W	RSVD	RSVD	BB_OVP_TH[1:0]		BB_AD	BB_HSKIP	BB_FPWM	RSVD	0x3C
0x33	BB_VOUT	Type-O	R/W	RSVD	BB_VOUT[6:0]							0x48
0x34–0x3F	RSVD											
0x40	BUCK_SS_FREQ	Type-O	R/W	RSVD	RSVD	RSVD	B_SS	RSVD	B_FREQ[2:0]			0x04
0x41	UVLO_FALL	Type-O	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	UVLO_F[1:0]		0x01
0x42–0xFF	RSVD											

INT_SRC

Interrupt Source Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x00	R			
BIT	NAME	POR	DESCRIPTION	
7:3	RSVD	0000 0		
2	BB_INT	0	1: Interrupt event on BUCK BOOST is detected.	
1	REG_INT	0	1: Interrupt event on BUCK or LDOs is detected.	
0	TOPSYS_INT	0	1: Interrupt event on TOPSYS is detected.	

TOPSYS_INT

TOPSYS Interrupt Register

ADDRESS	MODE		TYPE: S1	RESET VALUE: 0x00
0x01	R/C			
BIT	NAME	POR	DESCRIPTION	
7:2	RSVD	0000 00		
1	TJCT_120C	0	1: Junction temperature (TJCT) is higher than +120°C.	
0	TJCT_140C	0	1: Junction temperature (TJCT) is higher than +140°C.	

REG_INT1

Regulators Interrupt Register1

ADDRESS	MODE		TYPE: S1	RESET VALUE: 0x00
0x02	R/C			
BIT	NAME	POR	DESCRIPTION	
7	LDO8_POKn	0	1: LDO8 POKn is triggered.	
6	LDO7_POKn	0	1: LDO7 POKn is triggered.	
5	LDO6_POKn	0	1: LDO6 POKn is triggered.	
4	LDO5_POKn	0	1: LDO5 POKn is triggered.	
3	LDO4_POKn	0	1: LDO4 POKn is triggered.	
2	LDO3_POKn	0	1: LDO3 POKn is triggered.	
1	LDO2_POKn	0	1: LDO2 POKn is triggered.	
0	LDO1_POKn	0	1: LDO1 POKn is triggered.	

REG_INT2

Regulators Interrupt Register2

ADDRESS	MODE		TYPE: S1	RESET VALUE: 0x00
0x03	R/C			
BIT	NAME	POR	DESCRIPTION	
7	B_POKn	0	1: BUCK POKn is triggered.	
6	LDO15_POKn	0	1: LDO15 POKn is triggered.	
5	LDO14_POKn	0	1: LDO14 POKn is triggered.	
4	LDO13_POKn	0	1: LDO13 POKn is triggered.	
3	LDO12_POKn	0	1: LDO12 POKn is triggered.	
2	LDO11_POKn	0	1: LDO11 POKn is triggered.	
1	LDO10_POKn	0	1: LDO10 POKn is triggered.	
0	LDO9_POKn	0	1: LDO9 POKn is triggered.	

BB_INT

BUCK BOOST Interrupt Register

ADDRESS	MODE		TYPE: S1	RESET VALUE: 0x00
0x04	R/C			
BIT	NAME	POR	DESCRIPTION	
7:3	RSVD	0000 0		
2	BB_POKn	0	1: BUCK BOOST POKn is triggered.	
1	BB_OVP	0	1: BUCK BOOST OVP is triggered.	
0	BB_OCP	0	1: BUCK BOOST OCP is triggered.	

INT_SRC_M

Interrupt Source Mask Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x07
0x05	R/W			
BIT	NAME	POR	DESCRIPTION	
7:3	RSVD	0000 0		
2	BB_INT_M	1	0: Enable BUCK BOOST interrupt events. 1: Mask BUCK BOOST interrupt events.	
1	REG_INT_M	1	0: Enable REG interrupt events. 1: Mask REG interrupt events.	
0	TOPSYS_INT_M	1	0: Enable TOPSYS interrupt events. 1: Mask TOPSYS interrupt events.	

TOPSYS_INT_M

TOPSYS Interrupt Mask Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x03
0x05	R/W			
BIT	NAME	POR	DESCRIPTION	
7:2	RSVD	0000 00		
1	TJCT_120C_M	1	0: Enable TJCT_120 interrupt. 1: Mask TJCT_120 interrupt.	
0	TJCT_140C_M	1	0: Enable TJCT_140 interrupt. 1: Mask TJCT_140 interrupt.	

REG_INT1_M

Regulators Interrupt Mask Register 1

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xFF
0x07	R/W			
BIT	NAME	POR	DESCRIPTION	
7	LDO8_POKn_M	1	0: Enable LDO8 POKn interrupt. 1: Mask LDO8 POKn interrupt.	
6	LDO7_POKn_M	1	0: Enable LDO7 POKn interrupt. 1: Mask LDO7 POKn interrupt.	
5	LDO6_POKn_M	1	0: Enable LDO6 POKn interrupt. 1: Mask LDO6 POKn interrupt.	
4	LDO5_POKn_M	1	0: Enable LDO5 POKn interrupt. 1: Mask LDO5 POKn interrupt.	
3	LDO4_POKn_M	1	0: Enable LDO4 POKn interrupt. 1: Mask LDO4 POKn interrupt.	
2	LDO3_POKn_M	1	0: Enable LDO3 POKn interrupt. 1: Mask LDO3 POKn interrupt.	
1	LDO2_POKn_M	1	0: Enable LDO2 POKn interrupt. 1: Mask LDO2 POKn interrupt.	
0	LDO1_POKn_M	1	0: Enable LDO1 POKn interrupt. 1: Mask LDO1 POKn interrupt.	

REG_INT2_M

Regulators Interrupt Mask Register 2

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xFF
0x08	R/W			
BIT	NAME	POR	DESCRIPTION	
7	B_POKn_M	1	0: Enable BUCK POKn interrupt. 1: Mask BUCK POKn interrupt.	
6	LDO15_POKn_M	1	0: Enable LDO15 POKn interrupt. 1: Mask LDO15 POKn interrupt.	
5	LDO14_POKn_M	1	0: Enable LDO14 POKn interrupt. 1: Mask LDO14 POKn interrupt.	
4	LDO13_POKn_M	1	0: Enable LDO13 POKn interrupt. 1: Mask LDO13 POKn interrupt.	
3	LDO12_POKn_M	1	0: Enable LDO12 POKn interrupt. 1: Mask LDO12 POKn interrupt.	
2	LDO11_POKn_M	1	0: Enable LDO11 POKn interrupt. 1: Mask LDO11 POKn interrupt.	
1	LDO10_POKn_M	1	0: Enable LDO10 POKn interrupt. 1: Mask LDO10 POKn interrupt.	
0	LDO9_POKn_M	1	0: Enable LDO9 POKn interrupt. 1: Mask LDO9 POKn interrupt.	

BB_INT_M

BUCK BOOST Interrupt Mask Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x07
0x09	R/W			
BIT	NAME	POR	DESCRIPTION	
7:3	RSVD	0000 0		
2	BB_POKn_M	1	0: Enable BUCK BOOST POKn interrupt. 1: Mask BUCK BOOST POKn interrupt.	
1	BB_OVP_M	1	0: Enable BUCK BOOST OVP interrupt. 1: Mask BUCK BOOST OVP interrupt.	
0	BB_OCP_M	1	0: Enable BUCK BOOST OCP interrupt. 1: Mask BUCK BOOST OCP interrupt.	

TOPSYS_STAT

TOPSYS Status Register

ADDRESS	MODE		TYPE: O	RESET VALUE: N/A
0x0A	R			
BIT	NAME	POR	DESCRIPTION	
7:2	RSVD	—		
1	TJCT_120C	—	0: Junction temperature (TJCT) ≤ +120°C 1: Junction temperature (TJCT) > +120°C	
0	TJCT_140C	—	0: Junction temperature (TJCT) ≤ +140°C 1: Junction temperature (TJCT) > +140°C	

REG_STAT1

Regulators Status Register 1

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x0B	R			
BIT	NAME	POR	DESCRIPTION	
7	LDO8_POKn	0	LDO8 POKn status	
6	LDO7_POKn	0	LDO7 POKn status	
5	LDO6_POKn	0	LDO6 POKn status	
4	LDO5_POKn	0	LDO5 POKn status	
3	LDO4_POKn	0	LDO4 POKn status	
2	LDO3_POKn	0	LDO3 POKn status	
1	LDO2_POKn	0	LDO2 POKn status	
0	LDO1_POKn	0	LDO1 POKn status	

REG_STAT2

Regulators Status Register 2

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x0C	R			
BIT	NAME	POR	DESCRIPTION	
7	B_POKn	0	BUCK POKn status	
6	LDO15_POKn	0	LDO15 POKn status	
5	LDO14_POKn	0	LDO14 POKn status	
4	LDO13_POKn	0	LDO13 POKn status	
3	LDO12_POKn	0	LDO12 POKn status	
2	LDO11_POKn	0	LDO11 POKn status	
1	LDO10_POKn	0	LDO10 POKn status	
0	LDO9_POKn	0	LDO9 POKn status	

BB_STAT

BUCK BOOST Status Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x0D	R			
BIT	NAME	POR	DESCRIPTION	
7:3	RSVD	0000 0		
2	BB_POKn	0	BUCK BOOST POKn status	
1	BB_OVP	0	BUCK BOOST OVP status	
0	BB_OCP	0	BUCK BOOST OCP status	

Note: *0x0E–0x0F: RSVD.*

LDO_OPMD1

LDO Operating Mode Register 1

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x10	R/W			
BIT	NAME	POR	DESCRIPTION	
7	L4_EN	0	0: Output off 1: Output on	
6	L4_LPM	0	0: Normal mode 1: Low power mode	
5	L3_EN	0	0: Output off 1: Output on	
4	L3_LPM	0	0: Normal mode 1: Low power mode	
3	L2_EN	0	0: Output off 1: Output on	
2	L2_LPM	0	0: Normal mode 1: Low power mode	
1	L1_EN	0	0: Output off 1: Output on	
0	L1_LPM	0	0: Normal mode 1: Low power mode	

LDO_OPMD2

LDO Operating Mode Register 2

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x11	R/W			
BIT	NAME	POR	DESCRIPTION	
7	L8_EN	0	0: Output off 1: Output on	
6	L8_LPM	0	0: Normal mode 1: Low power mode	
5	L7_EN	0	0: Output off 1: Output on	
4	L7_LPM	0	0: Normal mode 1: Low power mode	
3	L6_EN	0	0: Output off 1: Output on	
2	L6_LPM	0	0: Normal mode 1: Low power mode	
1	L5_EN	0	0: Output off 1: Output on	
0	L5_LPM	0	0: Normal Mode 1: Low Power Mode	

LDO_OPMD3

LDO Operating Mode Register 3

ADDRESS	MODE		ADDRESS	RESET VALUE: 0x00
0x12	R/W			
BIT	NAME	POR	DESCRIPTION	
7	L12_EN	0	0: Output off 1: Output on	
6	L12_LPM	0	0: Normal mode 1: Low power mode	
5	L11_EN	0	0: Output off 1: Output on	
4	L11_LPM	0	0: Normal mode 1: Low power mode	
3	L10_EN	0	0: Output off 1: Output on	
2	L10_LPM	0	0: Normal mode 1: Low power mode	
1	L9_EN	0	0: Output off 1: Output on	
0	L9_LPM	0	0: Normal mode 1: Low power mode	

LDO_OPMD4

LDO Operating Mode Register 4

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x13	R/W			
BIT	NAME	POR	DESCRIPTION	
7:6	RSVD			
5	L15_EN	0	0b: Output off 1b: Output on	
4	L15_LPM	0	0b: Normal mode 1b: Low power mode	
3	L14_EN	0	0b: Output off 1b: Output on	
2	L14_LPM	0	0b: Normal mode 1b: Low power mode	
1	L13_EN	0	0b: Output off 1b: Output on	
0	L13_LPM	0	0b: Normal mode 1b: Low power mode	

B_BB_OPMD

BUCK and BUCK BOOST Operating Mode Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x14	R/W			
BIT	NAME	POR	DESCRIPTION	
7:4	RSVD	0000		
3	BB_EN	0	0: BUCK BOOST output off 1: BUCK BOOST output on	
2	RSVD	0		
1	B_EN	0	0: BUCK output off 1: BUCK output on	
0	B_LPM	0	0: Normal mode 1: Low power mode	

Note: *0x14–0x1F: RSVD.*

LDO1_CFG

LDO1 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA0		
0x20	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L1_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L1_VOUT[6:0]	010 0000	**NMOS LDO Output Voltage**			
			0x00 = 0.6000V	**0x20 = 1.0000V**	0x40 = 1.4000V	0x60 = 1.8000V
			0x01 = 0.6125V	0x21 = 1.0125V	0x41 = 1.4125V	0x61 = 1.8125V
			0x02 = 0.6250V	0x22 = 1.0250V	0x42 = 1.4250V	0x62 = 1.8250V
			0x03 = 0.6375V	0x23 = 1.0375V	0x43 = 1.4375V	0x63 = 1.8375V
			0x04 = 0.6500V	0x24 = 1.0500V	0x44 = 1.4500V	0x64 = 1.8500V
			0x05 = 0.6625V	0x25 = 1.0625V	0x45 = 1.4625V	0x65 = 1.8625V
			0x06 = 0.6750V	0x26 = 1.0750V	0x46 = 1.4750V	0x66 = 1.8750V
			0x07 = 0.6875V	0x27 = 1.0875V	0x47 = 1.4875V	0x67 = 1.8875V
			0x08 = 0.7000V	0x28 = 1.1000V	0x48 = 1.5000V	0x68 = 1.9000V
			0x09 = 0.7125V	0x29 = 1.1125V	0x49 = 1.5125V	0x69 = 1.9125V
			0x0A = 0.7250V	0x2A = 1.1250V	0x4A = 1.5250V	0x6A = 1.9250V
			0x0B = 0.7375V	0x2B = 1.1375V	0x4B = 1.5375V	0x6B = 1.9375V
			0x0C = 0.7500V	0x2C = 1.1500V	0x4C = 1.5500V	0x6C = 1.9500V
			0x0D = 0.7625V	0x2D = 1.1625V	0x4D = 1.5625V	0x6D = 1.9625V
			0x0E = 0.7750V	0x2E = 1.1750V	0x4E = 1.5750V	0x6E = 1.9750V
			0x0F = 0.7875V	0x2F = 1.1875V	0x4F = 1.5875V	0x6F = 1.9875V
			0x10 = 0.8000V	0x30 = 1.2000V	0x50 = 1.6000V	0x70 = 2.0000V
			0x11 = 0.8125V	0x31 = 1.2125V	0x51 = 1.6125V	0x71 = 2.0125V
			0x12 = 0.8250V	0x32 = 1.2250V	0x52 = 1.6250V	0x72 = 2.0250V
			0x13 = 0.8375V	0x33 = 1.2375V	0x53 = 1.6375V	0x73 = 2.0375V
			0x14 = 0.8500V	0x34 = 1.2500V	0x54 = 1.6500V	0x74 = 2.0500V
			0x15 = 0.8625V	0x35 = 1.2625V	0x55 = 1.6625V	0x75 = 2.0625V
			0x16 = 0.8750V	0x36 = 1.2750V	0x56 = 1.6750V	0x76 = 2.0750V
			0x17 = 0.8875V	0x37 = 1.2875V	0x57 = 1.6875V	0x77 = 2.0875V
			0x18 = 0.9000V	0x38 = 1.3000V	0x58 = 1.7000V	0x78 = 2.1000V
			0x19 = 0.9125V	0x39 = 1.3125V	0x59 = 1.7125V	0x79 = 2.1125V
			0x1A = 0.9250V	0x3A = 1.3250V	0x5A = 1.7250V	0x7A = 2.1250V
			0x1B = 0.9375V	0x3B = 1.3375V	0x5B = 1.7375V	0x7B = 2.1375V
			0x1C = 0.9500V	0x3C = 1.3500V	0x5C = 1.7500V	0x7C = 2.1500V
			0x1D = 0.9625V	0x3D = 1.3625V	0x5D = 1.7625V	0x7D = 2.1625V
			0x1E = 0.9750V	0x3E = 1.3750V	0x5E = 1.7750V	0x7E = 2.1750V
			0x1F = 0.9875V	0x3F = 1.3875V	0x5F = 1.7875V	0x7F = 2.1875V

LDO2_CFG

LDO2 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA0		
0x21	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L2_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L2_VOUT[6:0]	010 0000	**NMOS LDO Output Voltage**			
			0x00 = 0.6000V	**0x20 = 1.0000V**	0x40 = 1.4000V	0x60 = 1.8000V
			0x01 = 0.6125V	0x21 = 1.0125V	0x41 = 1.4125V	0x61 = 1.8125V
			0x02 = 0.6250V	0x22 = 1.0250V	0x42 = 1.4250V	0x62 = 1.8250V
			0x03 = 0.6375V	0x23 = 1.0375V	0x43 = 1.4375V	0x63 = 1.8375V
			0x04 = 0.6500V	0x24 = 1.0500V	0x44 = 1.4500V	0x64 = 1.8500V
			0x05 = 0.6625V	0x25 = 1.0625V	0x45 = 1.4625V	0x65 = 1.8625V
			0x06 = 0.6750V	0x26 = 1.0750V	0x46 = 1.4750V	0x66 = 1.8750V
			0x07 = 0.6875V	0x27 = 1.0875V	0x47 = 1.4875V	0x67 = 1.8875V
			0x08 = 0.7000V	0x28 = 1.1000V	0x48 = 1.5000V	0x68 = 1.9000V
			0x09 = 0.7125V	0x29 = 1.1125V	0x49 = 1.5125V	0x69 = 1.9125V
			0x0A = 0.7250V	0x2A = 1.1250V	0x4A = 1.5250V	0x6A = 1.9250V
			0x0B = 0.7375V	0x2B = 1.1375V	0x4B = 1.5375V	0x6B = 1.9375V
			0x0C = 0.7500V	0x2C = 1.1500V	0x4C = 1.5500V	0x6C = 1.9500V
			0x0D = 0.7625V	0x2D = 1.1625V	0x4D = 1.5625V	0x6D = 1.9625V
			0x0E = 0.7750V	0x2E = 1.1750V	0x4E = 1.5750V	0x6E = 1.9750V
			0x0F = 0.7875V	0x2F = 1.1875V	0x4F = 1.5875V	0x6F = 1.9875V
			0x10 = 0.8000V	0x30 = 1.2000V	0x50 = 1.6000V	0x70 = 2.0000V
			0x11 = 0.8125V	0x31 = 1.2125V	0x51 = 1.6125V	0x71 = 2.0125V
			0x12 = 0.8250V	0x32 = 1.2250V	0x52 = 1.6250V	0x72 = 2.0250V
			0x13 = 0.8375V	0x33 = 1.2375V	0x53 = 1.6375V	0x73 = 2.0375V
			0x14 = 0.8500V	0x34 = 1.2500V	0x54 = 1.6500V	0x74 = 2.0500V
			0x15 = 0.8625V	0x35 = 1.2625V	0x55 = 1.6625V	0x75 = 2.0625V
			0x16 = 0.8750V	0x36 = 1.2750V	0x56 = 1.6750V	0x76 = 2.0750V
			0x17 = 0.8875V	0x37 = 1.2875V	0x57 = 1.6875V	0x77 = 2.0875V
			0x18 = 0.9000V	0x38 = 1.3000V	0x58 = 1.7000V	0x78 = 2.1000V
			0x19 = 0.9125V	0x39 = 1.3125V	0x59 = 1.7125V	0x79 = 2.1125V
			0x1A = 0.9250V	0x3A = 1.3250V	0x5A = 1.7250V	0x7A = 2.1250V
			0x1B = 0.9375V	0x3B = 1.3375V	0x5B = 1.7375V	0x7B = 2.1375V
			0x1C = 0.9500V	0x3C = 1.3500V	0x5C = 1.7500V	0x7C = 2.1500V
			0x1D = 0.9625V	0x3D = 1.3625V	0x5D = 1.7625V	0x7D = 2.1625V
			0x1E = 0.9750V	0x3E = 1.3750V	0x5E = 1.7750V	0x7E = 2.1750V
			0x1F = 0.9875V	0x3F = 1.3875V	0x5F = 1.7875V	0x7F = 2.1875V

LDO3_CFG

LDO3 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA0		
0x22	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L3_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L3_VOUT[6:0]	010 0000	**NMOS LDO Output Voltage Table**			
			0x00 = 0.6000V	**0x20 = 1.0000V**	0x40 = 1.4000V	0x60 = 1.8000V
			0x01 = 0.6125V	0x21 = 1.0125V	0x41 = 1.4125V	0x61 = 1.8125V
			0x02 = 0.6250V	0x22 = 1.0250V	0x42 = 1.4250V	0x62 = 1.8250V
			0x03 = 0.6375V	0x23 = 1.0375V	0x43 = 1.4375V	0x63 = 1.8375V
			0x04 = 0.6500V	0x24 = 1.0500V	0x44 = 1.4500V	0x64 = 1.8500V
			0x05 = 0.6625V	0x25 = 1.0625V	0x45 = 1.4625V	0x65 = 1.8625V
			0x06 = 0.6750V	0x26 = 1.0750V	0x46 = 1.4750V	0x66 = 1.8750V
			0x07 = 0.6875V	0x27 = 1.0875V	0x47 = 1.4875V	0x67 = 1.8875V
			0x08 = 0.7000V	0x28 = 1.1000V	0x48 = 1.5000V	0x68 = 1.9000V
			0x09 = 0.7125V	0x29 = 1.1125V	0x49 = 1.5125V	0x69 = 1.9125V
			0x0A = 0.7250V	0x2A = 1.1250V	0x4A = 1.5250V	0x6A = 1.9250V
			0x0B = 0.7375V	0x2B = 1.1375V	0x4B = 1.5375V	0x6B = 1.9375V
			0x0C = 0.7500V	0x2C = 1.1500V	0x4C = 1.5500V	0x6C = 1.9500V
			0x0D = 0.7625V	0x2D = 1.1625V	0x4D = 1.5625V	0x6D = 1.9625V
			0x0E = 0.7750V	0x2E = 1.1750V	0x4E = 1.5750V	0x6E = 1.9750V
			0x0F = 0.7875V	0x2F = 1.1875V	0x4F = 1.5875V	0x6F = 1.9875V
			0x10 = 0.8000V	0x30 = 1.2000V	0x50 = 1.6000V	0x70 = 2.0000V
			0x11 = 0.8125V	0x31 = 1.2125V	0x51 = 1.6125V	0x71 = 2.0125V
			0x12 = 0.8250V	0x32 = 1.2250V	0x52 = 1.6250V	0x72 = 2.0250V
			0x13 = 0.8375V	0x33 = 1.2375V	0x53 = 1.6375V	0x73 = 2.0375V
			0x14 = 0.8500V	0x34 = 1.2500V	0x54 = 1.6500V	0x74 = 2.0500V
			0x15 = 0.8625V	0x35 = 1.2625V	0x55 = 1.6625V	0x75 = 2.0625V
			0x16 = 0.8750V	0x36 = 1.2750V	0x56 = 1.6750V	0x76 = 2.0750V
			0x17 = 0.8875V	0x37 = 1.2875V	0x57 = 1.6875V	0x77 = 2.0875V
			0x18 = 0.9000V	0x38 = 1.3000V	0x58 = 1.7000V	0x78 = 2.1000V
			0x19 = 0.9125V	0x39 = 1.3125V	0x59 = 1.7125V	0x79 = 2.1125V
			0x1A = 0.9250V	0x3A = 1.3250V	0x5A = 1.7250V	0x7A = 2.1250V
			0x1B = 0.9375V	0x3B = 1.3375V	0x5B = 1.7375V	0x7B = 2.1375V
			0x1C = 0.9500V	0x3C = 1.3500V	0x5C = 1.7500V	0x7C = 2.1500V
			0x1D = 0.9625V	0x3D = 1.3625V	0x5D = 1.7625V	0x7D = 2.1625V
			0x1E = 0.9750V	0x3E = 1.3750V	0x5E = 1.7750V	0x7E = 2.1750V
			0x1F = 0.9875V	0x3F = 1.3875V	0x5F = 1.7875V	0x7F = 2.1875V

LDO4_CFG

LDO4 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x9C		
0x23	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L4_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L4_VOUT[6:0]	001 1100	**PMOSLV LDO Output Voltage Table**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO5_CFG

LDO5 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA8		
0x24	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L5_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L5_VOUT[6:0]	010 1000	**PMOSLV LDO Output Voltage Table**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	**0x28 = 1.800V**	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO6_CFG

LDO6 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA8		
0x25	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L6_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L6_VOUT[6:0]	010 1000	**PMOSLV LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	**0x28 = 1.800V**	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO7_CFG

LDO7 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA8		
0x26	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L7_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L7_VOUT[6:0]	010 1000	**PMOSLV LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	**0x28 = 1.800V**	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO8_CFG

LDO8 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA8		
0x27	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L8_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L8_VOUT[6:0]	010 1000	**PMOSLV LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	**0x28 = 1.800V**	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO9_CFG

LDO9 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xA8		
0x28	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L9_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L9_VOUT[6:0]	010 1000	**PMOSLV LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	**0x28 = 1.800V**	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO10_CFG

LDO10 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xD0		
0x29	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L10_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L10_VOUT[6:0]	101 0000	**PMOSLS LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	**0x50 = 2.800V**	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO11_CFG

LDO11 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xD0		
0x29	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L10_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L10_VOUT[6:0]	101 0000	**PMOSLS LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	0x64 = 3.300V
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	**0x50 = 2.800V**	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO12_CFG

LDO12 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xE4		
0x2B	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L12_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L12_VOUT[6:0]	110 0100	**PMOSLS LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	**0x64 = 3.300V**
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO13_CFG

LDO13 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xE4		
0x2C	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L13_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L13_VOUT[6:0]	110 0100	**PMOSLS LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	**0x64 = 3.300V**
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO14_CFG

LDO14 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xE4		
0x2D	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L14_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L14_VOUT[6:0]	110 0100	**PMOSLS LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	**0x64 = 3.300V**
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

LDO15_CFG

LDO15 Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0xE4		
0x2E	R/W					
BIT	NAME	POR	DESCRIPTION			
7	L15_AD	1	**Output Active Discharge** 0: Disable **1: Enable**			
6:0	L15_VOUT[6:0]	110 0100	**PMOSLS LDO Output Voltage**			
			0x00 = 0.800V	0x20 = 1.600V	0x40 = 2.400V	0x60 = 3.200V
			0x01 = 0.825V	0x21 = 1.625V	0x41 = 2.425V	0x61 = 3.225V
			0x02 = 0.850V	0x22 = 1.650V	0x42 = 2.450V	0x62 = 3.250V
			0x03 = 0.875V	0x23 = 1.675V	0x43 = 2.475V	0x63 = 3.275V
			0x04 = 0.900V	0x24 = 1.700V	0x44 = 2.500V	**0x64 = 3.300V**
			0x05 = 0.925V	0x25 = 1.725V	0x45 = 2.525V	0x65 = 3.325V
			0x06 = 0.950V	0x26 = 1.750V	0x46 = 2.550V	0x66 = 3.350V
			0x07 = 0.975V	0x27 = 1.775V	0x47 = 2.575V	0x67 = 3.375V
			0x08 = 1.000V	0x28 = 1.800V	0x48 = 2.600V	0x68 = 3.400V
			0x09 = 1.025V	0x29 = 1.825V	0x49 = 2.625V	0x69 = 3.425V
			0x0A = 1.050V	0x2A = 1.850V	0x4A = 2.650V	0x6A = 3.450V
			0x0B = 1.075V	0x2B = 1.875V	0x4B = 2.675V	0x6B = 3.475V
			0x0C = 1.100V	0x2C = 1.900V	0x4C = 2.700V	0x6C = 3.500V
			0x0D = 1.125V	0x2D = 1.925V	0x4D = 2.725V	0x6D = 3.525V
			0x0E = 1.150V	0x2E = 1.950V	0x4E = 2.750V	0x6E = 3.550V
			0x0F = 1.175V	0x2F = 1.975V	0x4F = 2.775V	0x6F = 3.575V
			0x10 = 1.200V	0x30 = 2.000V	0x50 = 2.800V	0x70 = 3.600V
			0x11 = 1.225V	0x31 = 2.025V	0x51 = 2.825V	0x71 = 3.625V
			0x12 = 1.250V	0x32 = 2.050V	0x52 = 2.850V	0x72 = 3.650V
			0x13 = 1.275V	0x33 = 2.075V	0x53 = 2.875V	0x73 = 3.675V
			0x14 = 1.300V	0x34 = 2.100V	0x54 = 2.900V	0x74 = 3.700V
			0x15 = 1.325V	0x35 = 2.125V	0x55 = 2.925V	0x75 = 3.725V
			0x16 = 1.350V	0x36 = 2.150V	0x56 = 2.950V	0x76 = 3.750V
			0x17 = 1.375V	0x37 = 2.175V	0x57 = 2.975V	0x77 = 3.775V
			0x18 = 1.400V	0x38 = 2.200V	0x58 = 3.000V	0x78 = 3.800V
			0x19 = 1.425V	0x39 = 2.225V	0x59 = 3.025V	0x79 = 3.825V
			0x1A = 1.450V	0x3A = 2.250V	0x5A = 3.050V	0x7A = 3.850V
			0x1B = 1.475V	0x3B = 2.275V	0x5B = 3.075V	0x7B = 3.875V
			0x1C = 1.500V	0x3C = 2.300V	0x5C = 3.100V	0x7C = 3.900V
			0x1D = 1.525V	0x3D = 2.325V	0x5D = 3.125V	0x7D = 3.925V
			0x1E = 1.550V	0x3E = 2.350V	0x5E = 3.150V	0x7E = 3.950V
			0x1F = 1.575V	0x3F = 2.375V	0x5F = 3.175V	0x7F = 3.975V

Note: *0x2F: RSVD.*

BUCK_CFG

BUCK Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x09
0x30	R/W			
BIT	NAME	POR	DESCRIPTION	
7:6	B_RAMP[1:0]	00	**Rising Ramp Rate Control** 00b: 12.5mV/µs 01b: 25mV/µs 10b: 50mV/µs 11b: 100mV/µs	
5:4	RSVD	00		
3	B_AD	1	**Output Active Discharge** 0: Disable 1: Enable	
2	B_FPWM	0	**Forced PWM** 0: Turn off Forced PWM (Automatic SKIP mode operation under light load) 1: Turn on Forced PWM Mode	
1	RSVD	0		
0	B_FSRAD	1	**Falling Slew Rate Active Discharge** **0: Disable Active Discharge** BUCK is allowed to operate in SKIP mode during the time the output voltage decreases (only if B3_FPWM = 0). In SKIP mode, BUCK cannot sink current from the output capacitor and the output voltage falling slew rate is a function of the external load. If the load is heavy, the output voltage falling slew rate is limited to 6.25mV/µs. If the load is light, the output voltage falling slew rate is a function of the output capacitance and the load. Note that the internal feedback string always imposes a 2µA load on the output. **1: Enable Active Discharge** BUCK operates in forced PWM mode during the time the output voltage decreases. In forced PWM mode, BUCK can sink current from the output capacitor to ensure that the output voltage falls at the rate of 6.25mV/µs. To ensure a smooth output voltage ramp-down, forced PMW mode remains engaged for 50µs after the output voltage decreases to its target voltage.	

BUCK_VOUT

BUCK Output Voltage Setting Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x78
0x31	R/W			
BIT	NAME	POR	DESCRIPTION	
7:0	B_VOUT[7:0]	0111 1000	BUCK Output Voltage (see table immediately below)	

BUCK Output Voltage

0x00 = 0.50000V	0x20 = 0.70000V	0x40 = 0.90000V	0x60 = 1.10000V	0x80 = 1.30000V	0xA0 = 1.50000V	0xC0 = 1.70000V	0xE0 = 1.80000V
0x01 = 0.50625V	0x21 = 0.70625V	0x41 = 0.90625V	0x61 = 1.10625V	0x81 = 1.30625V	0xA1 = 1.50625V	0xC1 = 1.70625V	0xE1 = 1.80000V
0x02 = 0.51250V	0x22 = 0.71250V	0x42 = 0.91250V	0x62 = 1.11250V	0x82 = 1.31250V	0xA2 = 1.51250V	0xC2 = 1.71250V	0xE2 = 1.80000V
0x03 = 0.51875V	0x23 = 0.71875V	0x43 = 0.91875V	0x63 = 1.11875V	0x83 = 1.31875V	0xA3 = 1.51875V	0xC3 = 1.71875V	0xE3 = 1.80000V
0x04 = 0.52500V	0x24 = 0.72500V	0x44 = 0.92500V	0x64 = 1.12500V	0x84 = 1.32500V	0xA4 = 1.52500V	0xC4 = 1.72500V	0xE4 = 1.80000V
0x05 = 0.53125V	0x25 = 0.73125V	0x45 = 0.93125V	0x65 = 1.13125V	0x85 = 1.33125V	0xA5 = 1.53125V	0xC5 = 1.73125V	0xE5 = 1.80000V
0x06 = 0.53750V	0x26 = 0.73750V	0x46 = 0.93750V	0x66 = 1.13750V	0x86 = 1.33750V	0xA6 = 1.53750V	0xC6 = 1.73750V	0xE6 = 1.80000V
0x07 = 0.54375V	0x27 = 0.74375V	0x47 = 0.94375V	0x67 = 1.14375V	0x87 = 1.34375V	0xA7 = 1.54375V	0xC7 = 1.74375V	0xE7 = 1.80000V
0x08 = 0.55000V	0x28 = 0.75000V	0x48 = 0.95000V	0x68 = 1.15000V	0x88 = 1.35000V	0xA8 = 1.55000V	0xC8 = 1.75000V	0xE8 = 1.80000V
0x09 = 0.55625V	0x29 = 0.75625V	0x49 = 0.95625V	0x69 = 1.15625V	0x89 = 1.35625V	0xA9 = 1.55625V	0xC9 = 1.75625V	0xE9 = 1.80000V
0x0A = 0.56250V	0x2A = 0.76250V	0x4A = 0.96250V	0x6A = 1.16250V	0x8A = 1.36250V	0xAA = 1.56250V	0xCA = 1.76250V	0xEA = 1.80000V
0x0B = 0.56875V	0x2B = 0.76875V	0x4B = 0.96875V	0x6B = 1.16875V	0x8B = 1.36875V	0xAB = 1.56875V	0xCB = 1.76875V	0xEB = 1.80000V
0x0C = 0.57500V	0x2C = 0.77500V	0x4C = 0.97500V	0x6C = 1.17500V	0x8C = 1.37500V	0xAC = 1.57500V	0xCC = 1.77500V	0xEC = 1.80000V
0x0D = 0.58125V	0x2D = 0.78125V	0x4D = 0.98125V	0x6D = 1.18125V	0x8D = 1.38125V	0xAD = 1.58125V	0xCD = 1.78125V	0xED = 1.80000V
0x0E = 0.58750V	0x2E = 0.78750V	0x4E = 0.98750V	0x6E = 1.18750V	0x8E = 1.38750V	0xAE = 1.58750V	0xCE = 1.78750V	0xEE = 1.80000V
0x0F = 0.59375V	0x2F = 0.79375V	0x4F = 0.99375V	0x6F = 1.19375V	0x8F = 1.39375V	0xAF = 1.59375V	0xCF = 1.79375V	0xEF = 1.80000V

BUCK Output Voltage (continued)

0x10 = 0.60000V	0x30 = 0.80000V	0x50 = 1.00000V	0x70 = 1.20000V	0x90 = 1.40000V	0xB0 = 1.60000V	0xD0 = 1.80000V	0xF0 = 1.80000V
0x11 = 0.60625V	0x31 = 0.80625V	0x51 = 1.00625V	0x71 = 1.20625V	0x91 = 1.40625V	0xB1 = 1.60625V	0xD1 = 1.80000V	0xF1 = 1.80000V
0x12 = 0.61250V	0x32 = 0.81250V	0x52 = 1.01250V	0x72 = 1.21250V	0x92 = 1.41250V	0xB2 = 1.61250V	0xD2 = 1.80000V	0xF2 = 1.80000V
0x13 = 0.61875V	0x33 = 0.81875V	0x53 = 1.01875V	0x73 = 1.21875V	0x93 = 1.41875V	0xB3 = 1.61875V	0xD3 = 1.80000V	0xF3 = 1.80000V
0x14 = 0.62500V	0x34 = 0.82500V	0x54 = 1.02500V	0x74 = 1.22500V	0x94 = 1.42500V	0xB4 = 1.62500V	0xD4 = 1.80000V	0xF4 = 1.80000V
0x15 = 0.63125V	0x35 = 0.83125V	0x55 = 1.03125V	0x75 = 1.23125V	0x95 = 1.43125V	0xB5 = 1.63125V	0xD5 = 1.80000V	0xF5 = 1.80000V
0x16 = 0.63750V	0x36 = 0.83750V	0x56 = 1.03750V	0x76 = 1.23750V	0x96 = 1.43750V	0xB6 = 1.63750V	0xD6 = 1.80000V	0xF6 = 1.80000V
0x17 = 0.64375V	0x37 = 0.84375V	0x57 = 1.04375V	0x77 = 1.24375V	0x97 = 1.44375V	0xB7 = 1.64375V	0xD7 = 1.80000V	0xF7 = 1.80000V
0x18 = 0.65000V	0x38 = 0.85000V	0x58 = 1.05000V	**0x78 = 1.25000V**	0x98 = 1.45000V	0xB8 = 1.65000V	0xD8 = 1.80000V	0xF8 = 1.80000V
0x19 = 0.65625V	0x39 = 0.85625V	0x59 = 1.05625V	0x79 = 1.25625V	0x99 = 1.45625V	0xB9 = 1.65625V	0xD9 = 1.80000V	0xF9 = 1.80000V
0x1A = 0.66250V	0x3A = 0.86250V	0x5A = 1.06250V	0x7A = 1.26250V	0x9A = 1.46250V	0xBA = 1.66250V	0xDA = 1.80000V	0xFA = 1.80000V
0x1B = 0.66875V	0x3B = 0.86875V	0x5B = 1.06875V	0x7B = 1.26875V	0x9B = 1.46875V	0xBB = 1.66875V	0xDB = 1.80000V	0xFB = 1.80000V
0x1C = 0.67500V	0x3C = 0.87500V	0x5C = 1.07500V	0x7C = 1.27500V	0x9C = 1.47500V	0xBC = 1.67500V	0xDC = 1.80000V	0xFC = 1.80000V
0x1D = 0.68125V	0x3D = 0.88125V	0x5D = 1.08125V	0x7D = 1.28125V	0x9D = 1.48125V	0xBD = 1.68125V	0xDD = 1.80000V	0xFD = 1.80000V
0x1E = 0.68750V	0x3E = 0.88750V	0x5E = 1.08750V	0x7E = 1.28750V	0x9E = 1.48750V	0xBE = 1.68750V	0xDE = 1.80000V	0xFE = 1.80000V
0x1F = 0.69375V	0x3F = 0.89375V	0x5F = 1.09375V	0x7F = 1.29375V	0x9F = 1.49375V	0xBF = 1.69375V	0xDF = 1.80000V	0xFF = 1.80000V

BB_CFG

BUCK BOOST Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x3C
0x32	R/W			
BIT	NAME	POR	DESCRIPTION	
7:6	RSVD	00		
5:4	BB_OVP_TH[1:0]	11	**Output OVP Threshold** 00b: No OVP 01b: 110% of V_{OUT} 10b: 115% of V_{OUT} **11b: 120% of V_{OUT}**	
3	BB_AD	1	**Output Active Discharge** 0: Disable 1kΩ active discharge. 1: Enable 1kΩ active discharge.	
2	BB_HSKIP	1	**High-Skip Mode Enable** 0: Disable high-skip mode. **1: Enable high-skip mode.** **HSKIP function is active only when BB_FPWM = 0 and BB_HSKIP = 1.**	
1	BB_FPWM	0	**Forced PWM Enable** **0: HSKIP mode** HSKIP function is active when BB_FPWM = 0 and BB_HSKIP = 0. 1: Forced PWM	
0	RSVD	0		

BB_VOUT

BUCK BOOST Output Voltage Setting Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x48		
0x33	R/W					
BIT	NAME	POR	DESCRIPTION			
7	RSVD	0	Write 0.			
6:0	BB_VOUT[6:0]	100 0000	**BUCK BOOST Output Voltage**			
			0x00 = 2.6000V	0x20 = 3.0000V	0x40 = 3.4000V	0x60 = 3.8000V
			0x01 = 2.6125V	0x21 = 3.0125V	0x41 = 3.4125V	0x61 = 3.8125V
			0x02 = 2.6250V	0x22 = 3.0250V	0x42 = 3.4250V	0x62 = 3.8250V
			0x03 = 2.6375V	0x23 = 3.0375V	0x43 = 3.4375V	0x63 = 3.8375V
			0x04 = 2.6500V	0x24 = 3.0500V	0x44 = 3.4500V	0x64 = 3.8500V
			0x05 = 2.6625V	0x25 = 3.0625V	0x45 = 3.4625V	0x65 = 3.8625V
			0x06 = 2.6750V	0x26 = 3.0750V	0x46 = 3.4750V	0x66 = 3.8750V
			0x07 = 2.6875V	0x27 = 3.0875V	0x47 = 3.4875V	0x67 = 3.8875V
			0x08 = 2.7000V	0x28 = 3.1000V	**0x48 = 3.5000V**	0x68 = 3.9000V
			0x09 = 2.7125V	0x29 = 3.1125V	0x49 = 3.5125V	0x69 = 3.9125V
			0x0A = 2.7250V	0x2A = 3.1250V	0x4A = 3.5250V	0x6A = 3.9250V
			0x0B = 2.7375V	0x2B = 3.1375V	0x4B = 3.5375V	0x6B = 3.9375V
			0x0C = 2.7500V	0x2C = 3.1500V	0x4C = 3.5500V	0x6C = 3.9500V
			0x0D = 2.7625V	0x2D = 3.1625V	0x4D = 3.5625V	0x6D = 3.9625V
			0x0E = 2.7750V	0x2E = 3.1750V	0x4E = 3.5750V	0x6E = 3.9750V
			0x0F = 2.7875V	0x2F = 3.1875V	0x4F = 3.5875V	0x6F = 3.9875V
			0x10 = 2.8000V	0x30 = 3.2000V	0x50 = 3.6000V	0x70 = 4.0000V
			0x11 = 2.8125V	0x31 = 3.2125V	0x51 = 3.6125V	0x71 = 4.0125V
			0x12 = 2.8250V	0x32 = 3.2250V	0x52 = 3.6250V	0x72 = 4.0250V
			0x13 = 2.8375V	0x33 = 3.2375V	0x53 = 3.6375V	0x73 = 4.0375V
			0x14 = 2.8500V	0x34 = 3.2500V	0x54 = 3.6500V	0x74 = 4.0500V
			0x15 = 2.8625V	0x35 = 3.2625V	0x55 = 3.6625V	0x75 = 4.0625V
			0x16 = 2.8750V	0x36 = 3.2750V	0x56 = 3.6750V	0x76 = 4.0750V
			0x17 = 2.8875V	0x37 = 3.2875V	0x57 = 3.6875V	0x77 = 4.0875V
			0x18 = 2.9000V	0x38 = 3.3000V	0x58 = 3.7000V	0x78 = 4.1000V
			0x19 = 2.9125V	0x39 = 3.3125V	0x59 = 3.7125V	0x79 = 4.1125V
			0x1A = 2.9250V	0x3A = 3.3250V	0x5A = 3.7250V	0x7A = 4.1250V
			0x1B = 2.9375V	0x3B = 3.3375V	0x5B = 3.7375V	0x7B = 4.1375V
			0x1C = 2.9500V	0x3C = 3.3500V	0x5C = 3.7500V	0x7C = 4.1500V
			0x1D = 2.9625V	0x3D = 3.3625V	0x5D = 3.7625V	0x7D = 4.1625V
			0x1E = 2.9750V	0x3E = 3.3750V	0x5E = 3.7750V	0x7E = 4.1750V
			0x1F = 2.9875V	0x3F = 3.3875V	0x5F = 3.7875V	0x7F = 4.1875V

Note: *0x34–0x3F: RSVD.*

BUCK_SS_FREQ

BUCK Soft-Start and Switching Frequency Configuration Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x04
0x40	R/W			
BIT	NAME	POR	DESCRIPTION	
7:5	RSVD	000	Write 0.	
4	B_SS	0	**BUCK Soft-Start Slew Rate** 0: 14mV/µs 1: 25mV/µs	
3	RSVD	0	Write 0.	
2:0	B_FREQ[2:0]	100	**Multiphase Current Mode BUCK Switching Frequency** 000b: 3.6MHz 001b: 3.2MHz 010b: 2.8MHz 011b: 2.4MHz 100b: 2.0MHz 101b: 1.6MHz 110b: 1.2MHz 111b: 0.8MHz	

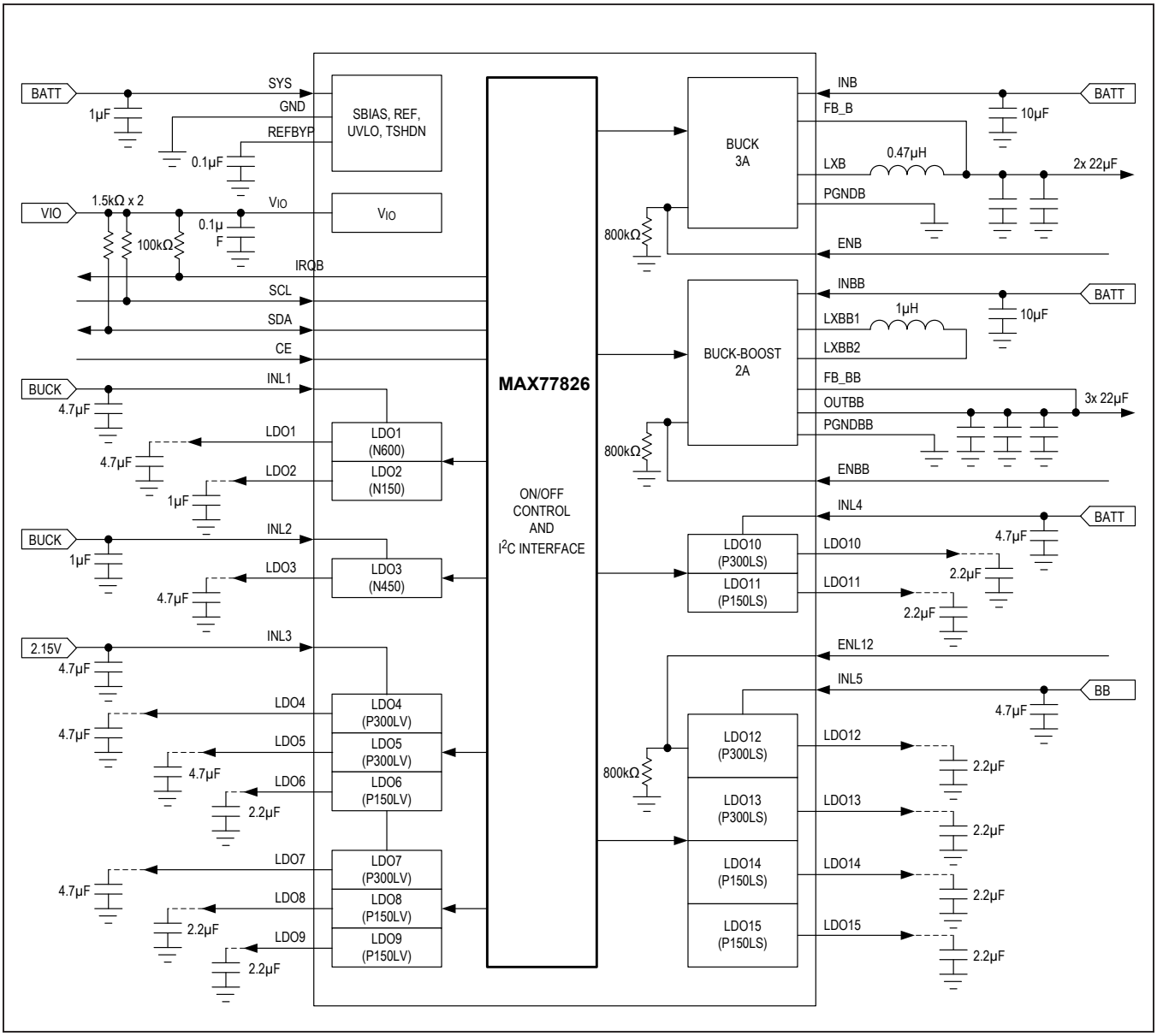
UVLO_FALL

VSYS UVLO Falling Threshold Program Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x01
0x41	R/W			
BIT	NAME	POR	DESCRIPTION	
7:2	RSVD	0000 00	Write 0000 00.	
1:0	UVLO_F[1:0]	01	**VSYS UVLO Falling Threshold** 00b: Not used 01b: 2.05V 10b: 2.25V 11b: 2.45V	

Note: *0x42–0xFF: RSVD.*

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77826EWJ+	-40°C to +85°C	49 Bumps (7 x 7) 0.4mm Pitch

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: S18B

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
49 WLP	W493E3+1	21-0728	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—

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