

Features

April 2006

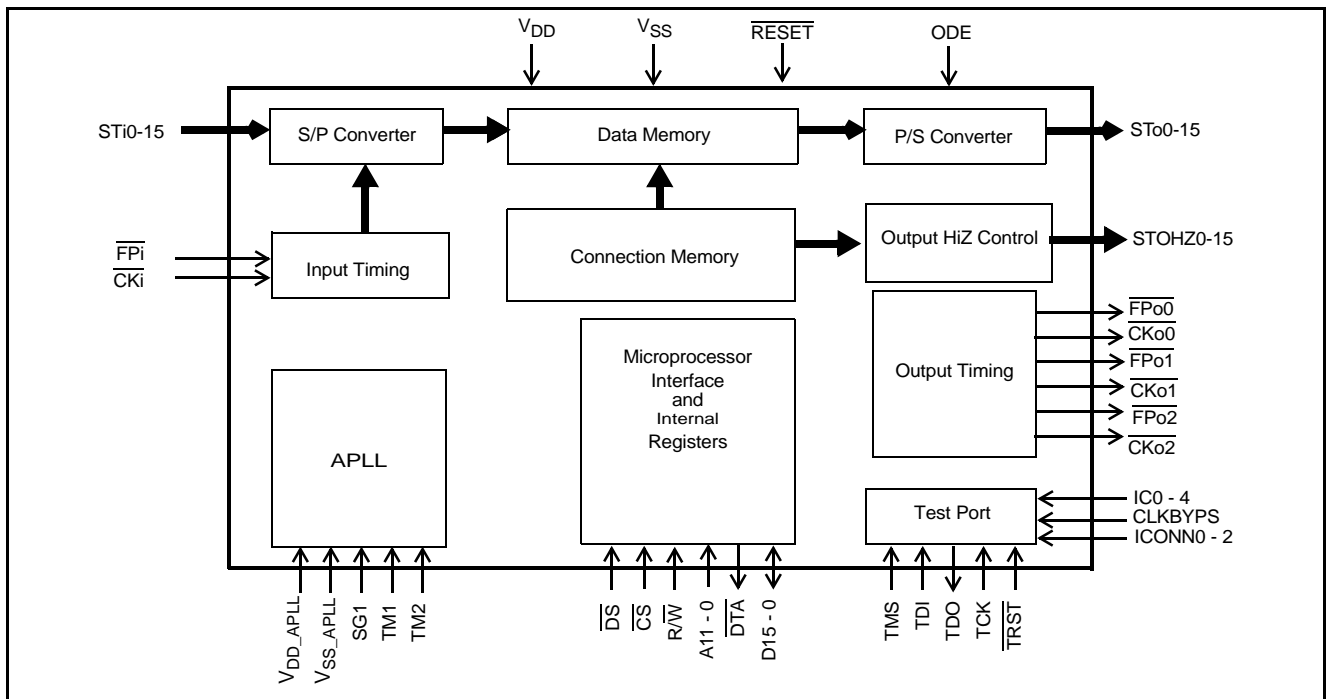
- 512 channel x 512 channel non-blocking switch at 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s operation
- Rate conversion between the ST-BUS inputs and ST-BUS outputs
- Per-stream ST-BUS input with data rate selection of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s
- Per-stream ST-BUS output with data rate selection of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s; the output data rate can be different than the input data rate
- Per-stream high impedance control output for every ST-BUS output with fractional bit advancement
- Per-stream input channel and input bit delay programming with fractional bit delay
- Per-stream output channel and output bit delay programming with fractional bit advancement
- Multiple frame pulse outputs and reference clock outputs
- Per-channel constant throughput delay

Ordering Information

| | | |
|--------------|-----------------|-----------------------|
| ZL50012/QCC | 160 Pin LQFP | Trays |
| ZL50012/GDC | 144 Ball LPGA | Trays |
| ZL50012/QCG1 | 160 Ball LQFP* | Trays, Bake & Drypack |
| ZL50012/GDG2 | 144 Ball LPGA** | Trays, Bake & Drypack |

*Pb Free Matte Tin
 **Pb Free Tin/Silver/Copper
-40°C to +85°C

- Per-channel high impedance output control
- Per-channel message mode
- Per-channel pseudo random bit sequence (PRBS) pattern generation and bit error detection
- Control interface compatible to Motorola non-multiplexed CPUs
- Connection memory block programming capability
- IEEE-1149.1 (JTAG) test port
- 3.3V I/O with 5 V tolerant input


Figure 1 - ZL50012 Functional Block Diagram

Applications

- Small and medium digital switching platforms
- Access Servers
- Time Division Multiplexers
- Computer Telephony Integration
- Digital Loop Carriers

Description

The device has sixteen ST-BUS inputs (STi0-15) and sixteen ST-BUS outputs (STo0-15). It is a non-blocking digital switch with 512 64 kb/s channels and performs rate conversion between the ST-BUS inputs and ST-BUS outputs. The ST-BUS inputs accept serial input data streams with the data rate of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s on a per-stream basis. The ST-BUS outputs deliver serial output data streams with the data rate of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s on a per-stream basis. The device also provides sixteen high impedance control outputs (STOHZ 0-15) to support the use of external high impedance control buffers.

The ZL50012 has features that are programmable on per-stream or per-channel basis including message mode, input bit delay, output bit advancement, constant throughput delay and high impedance output control.

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Changes Summary

The following table captures the changes from the July 2004 issue.

| Page | Item | Change |
|------|---|--|
| 18 | 2.1.4, "Improved Input Jitter Tolerance with Frame Boundary Determinator" | <ul style="list-style-type: none">Added a new section to describe the improved input jitter tolerance with the frame boundary determinator. |
| 37 | Table 15 -, "Control Register (CR) Bits" - bits , "FBDMODE" and , "FBDEN" | <ul style="list-style-type: none">Renamed bit 15 from Unused to FBDMODE and added description to clarify the frame boundary determinator operation.Clarified FBDEN description. |

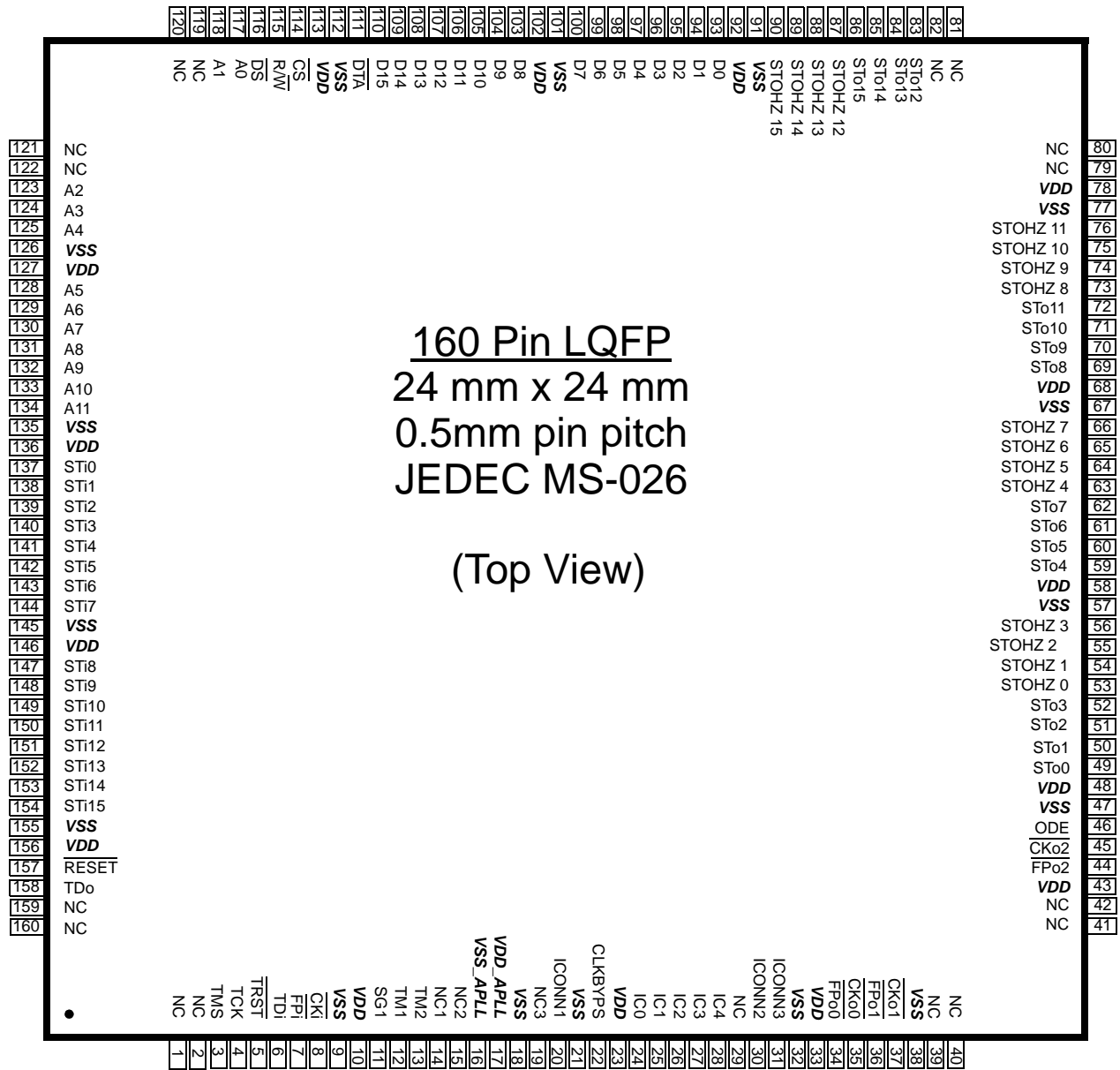


Figure 2 - 24 mm x 24 mm LQFP (JEDEC MS-026) Pinout Diagram

PINOUT DIAGRAM: (as viewed through top of package)

A1 corner identified by metallized marking, mould indent, ink dot or right-angled corner

| | | | | | | | | | | | | |
|---|-------------|-------------|-------------|-------------|-----|-----|------------|--------------|------|------|-------|-------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| A | ODE | FPo2 | FPo0 | ICONN 3 | IC1 | IC0 | ICONN 1 | NC3 | TM1 | CKi | TDi | TCK |
| B | CKo2 | CKo1 | FPo1 | CKo0 | IC3 | IC2 | CLK BYP | VDD_ APLL | SG1 | FPI | TRST | TMS |
| C | STo2 | STo1 | STOHZ 0 | ICONN 2 | NC | NC | IC4 | NC2 | NC1 | TM2 | TDo | STi15 |
| D | STo3 | STo0 | STOHZ 1 | VSS | VDD | VDD | VDD | VSS_ APLL | VSS | STi8 | RESET | STi14 |
| E | STo5 | STo4 | STOHZ 3 | STOHZ 2 | VSS | VSS | VSS | VSS | VDD | STi9 | STi13 | STi12 |
| F | STo6 | STo7 | STOHZ 4 | VDD | VSS | VSS | VSS | VSS | VDD | STi7 | STi10 | STi11 |
| G | STOHZ 6 | STOHZ 7 | STOHZ 5 | VDD | VSS | VSS | VSS | VSS | STi1 | STi6 | STi5 | STi4 |
| H | STo9 | STo10 | STo8 | VDD | VSS | VSS | VSS | VSS | STi0 | DS | STi2 | STi3 |
| J | STo11 | STOHZ 11 | STOHZ 8 | VSS | D2 | VDD | VDD | VDD | A10 | A9 | A8 | A11 |
| K | STOHZ 9 | STOHZ 15 | STo15 | STOHZ 13 | D1 | D5 | CS | D10 | D11 | A5 | A4 | A7 |
| L | STOHZ 10 | STo12 | STo13 | D3 | D15 | D4 | D7 | D12 | D14 | A2 | A3 | A6 |
| M | STo14 | STOHZ 12 | STOHZ 14 | D0 | DTA | D6 | D8 | D9 | D13 | A0 | A1 | RW |

Figure 3 - 13 mm x 13 mm 144 Ball LPGA Pinout Diagram

Pin Description

| LQFP Pin Number | LBGA Ball Number | Name | Description |
|---|---|--------------------------|--|
| 10, 23, 33, 43, 48, 58, 68, 78, 92, 102, 113, 127, 136, 146, 156 | D5, D6, D7 E9 F4, F9 G4 H4 J6, J7, J8 | V_{DD} | Power Supply for the device: +3.3 V |
| 9, 18, 21, 32, 38, 47, 57, 67, 77, 91, 101, 112, 126, 135, 145, 155 | D4, D9 E5, E6, E7, E8 F5, F6, F7, F8 G5, G6, G7, G8 H5, H6, H7, H8 J4 | V_{SS} (GND) | Ground. |
| 3 | B12 | TMS | Test Mode Select (3.3 V Tolerant Input with internal pull-up): JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven. |
| 4 | A12 | TCK | Test Clock (5 V Tolerant Input): Provides the clock to the JTAG test logic. |
| 5 | B11 | $\overline{\text{TRST}}$ | Test Reset (3.3 V Tolerant Input with internal pull-up): Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation. |
| 6 | A11 | TDi | Test Serial Data In (3.3 V Tolerant Input with internal pull-up): JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven. |
| 7 | B10 | $\overline{\text{FPi}}$ | ST-BUS Frame Pulse Input (5 V Tolerant Input): This pin accepts the frame pulse which stays low for 61 ns, 122 ns or 244 ns at the frame boundary. The frame pulse associating with the highest input data rate has to be applied to this pin. The frame pulse frequency is 8 kHz. The device also accepts positive frame pulse if the FPINP bit is high in the Internal Mode Selection register. |
| 8 | A10 | $\overline{\text{CKi}}$ | ST-BUS Clock Input (5 V Tolerant Input): This pin accepts a 4.096 MHz, 8.192 MHz or 16.384 MHz clock. The input clock frequency has to be equal to or greater than twice of the highest input data rate. The clock falling edge defines the input frame boundary. The device also allows the clock rising edge to define the frame boundary by programming the CKINP bit in the Internal Mode Selection register. |

Pin Description (continued)

| LQFP Pin Number | LBGA Ball Number | Name | Description |
|-----------------|--------------------|--------------------------|--|
| 11 | B9 | SG1 | APLL Test Control (3.3 V Input with internal pull-down): For normal operation, this input MUST be low. |
| 12 | A9 | TM1 | APLL Test Pin 1: For normal operation, this input MUST be low. |
| 13 | C10 | TM2 | APLL Test Pin 2: For normal operation, this input MUST be low. |
| 14, 15, 19 | C9, C8, A8 | NC1, NC2, NC3 | No Connection: These pins MUST be left unconnected. |
| 16 | D8 | V _{SS_APLL} | Ground for the APLL Circuit. |
| 17 | B8 | V _{DD_APLL} | Power Supply for the on-chip Analog Phase Lock Loop (APLL) Circuit: +3.3 V |
| 20 | A7 | ICONN1 | Internal Connection: In normal mode, this pin must be low. |
| 22 | B7 | CLKBYPS | Test Clock Input: For device testing only, in normal operation, this input MUST be low. |
| 24 - 28 | A6, A5, B6, B5, C7 | IC0 - 4 | Internal connection (3.3 V Tolerant Inputs with internal pull-down): In normal mode, these pins must be low. |
| 30, 31 | C4, A4 | ICONN2 - 3 | Internal Connection: In normal mode, these pins must be low. |
| 34 | A3 | $\overline{\text{FPo0}}$ | ST-BUS Frame Pulse Output 0 (5 V Tolerance Three-state Output): ST-BUS frame pulse output which stays low for 244 ns or 122 ns at the output frame boundary. Its frequency is 8 KHz. The polarity of this signal can be changed using the Internal Mode Selection register. |
| 35 | B4 | $\overline{\text{CKo0}}$ | ST-BUS Clock Output 0 (5 V Tolerant Three-state Output): A 4.094 MHz or 8.192 MHz clock output. The clock falling edge defines the output frame boundary. The polarity of this signal can be changed using the Internal Mode Selection register. |
| 36 | B3 | $\overline{\text{FPo1}}$ | ST-BUS Frame Pulse Output 1 (5 V Tolerant Three-state Output): ST-BUS frame pulse output which stays low for 61 ns or 122 ns at the output frame boundary. Its frequency is 8 KHz. The polarity of this signal can be changed using the Internal Mode Selection register. |
| 37 | B2 | $\overline{\text{CKo1}}$ | ST-BUS Clock Output 1 (5 V Tolerant Three-state Output): A 16.384 MHz or 8.192 MHz clock output. The clock falling edge defines the output frame boundary. The polarity of this signal can be changed using the Internal Mode Selection register. |

Pin Description (continued)

| LQFP Pin Number | LBGA Ball Number | Name | Description |
|---|--|---|---|
| 44 | A2 | $\overline{\text{FPo2}}$ | ST-BUS Frame Pulse Output 2 (5V Tolerant High Speed Three-state Output): ST-BUS frame pulse output which stays low for 30 ns or 61 ns at the frame boundary. Its frequency is 8 KHz. The polarity of this signal can be changed using the Internal Mode Selection register. |
| 45 | B1 | $\overline{\text{CKo2}}$ | ST-BUS Clock Output 2 (5 V Tolerant High Speed Three-state Output): A 32.768 MHz or 16.384 MHz clock output. The clock falling edge defines the output frame boundary. The polarity of this signal can be changed using the Internal Mode Selection register. |
| 46 | A1 | ODE | Output Drive Enable (5 V Tolerant Input): This is the asynchronously output enable control for the STo0 - 15 and the output driven high control for the STOHz 0 - 15 serial outputs. When it is high, the STo0 - 15 and STOHz 0 - 15 are enabled. When it is low, the STo0 - 15 are in the high impedance state and the STOHz 0 - 15 are driven high. |
| 49 - 52 59 - 62 69 - 72 83 - 86 | D2, C2, C1, D1 E2, E1, F1, F2 H3, H1, H2, J1 L2, L3, M1, K3 | STo0 - 3 STo4 - 7 STo8 - 11 STo12 - 15 | Serial Output Streams 0 to 15 (5 V Tolerant Three-state Outputs): The data rate of these output streams can be selected independently using the stream control output registers. In the 2.048 Mb/s mode, these pins have serial TDM data streams at 2.048 Mb/s with 32 channels per stream. In the 4.096 Mb/s mode, these pins have serial TDM data streams at 4.096 Mb/s with 64 channels per stream. In the 8.192 Mb/s mode, these pins have serial TDM data streams at 8.192 Mb/s with 128 channels per stream. |
| 53 - 56 63 - 66 73 - 76 87 - 90 | C3, D3, E4, E3 F3, G3, G1, G2 J3, K1, L1, J2 M2, K4, M3, K2 | STOHz 0 - 3 STOHz 4 - 7 STOHz 8 - 11 STOHz 12 - 15 | Serial Output Streams High Impedance Control 0 to 15 (5 V Tolerant Three-state Outputs): These pins are used to enable (or disable) external three-state buffers. When a output channel is in the high impedance state, the STOHz drives high for the duration of the corresponding output channel. When the STo channel is active, the STOHz drives low for the duration of the corresponding output channel. |
| 93 - 96 97 - 100 103 - 106 107 - 110 | M4, K5, J5, L4 L6, K6, M6, L7 M7, M8, K8, K9 L8, M9, L9, L5 | D0 - D3 D4 - D7 D8 - D11 D12 - D15 | Data Bus 0 - 15 (5 V Tolerant I/Os): These pins form the 16-bit data bus of the microprocessor port. |
| 111 | M5 | $\overline{\text{DTA}}$ | Data Transfer Acknowledgment (5 V Tolerant Three-state Output): This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold this pin at HIGH level. |
| 114 | K7 | $\overline{\text{CS}}$ | Chip Select (5 V Tolerant Input): Active low input used by the microprocessor to enable the microprocessor port access. |

Pin Description (continued)

| LQFP Pin Number | LBGA Ball Number | Name | Description |
|--|--|---|--|
| 115 | M12 | R \overline{W} | Read/Write (5 V Tolerant Input): This input controls the direction of the data bus lines (D0-D15) during a microprocessor access. |
| 116 | H10 | DS | Data Strobe (5 V Tolerant Input): This active low input works in conjunction with \overline{CS} to enable the microprocessor port read and write operations. |
| 117, 118 123 - 125 128 - 130 131 - 134 | M10, M11 L10, L11, K11 K10, L12, K12 J11, J10, J9, J12 | A0 - A1 A2 - A4 A5 - A7 A8 - A11 | Address 0 - 11 (5 V Tolerant Inputs): These pins form the 12-bit address bus to the internal memories and registers. |
| 137 - 139 140 - 142 143, 144 147 - 149 150 - 152 153, 154 | H9, G9, H11 H12, G12, G11 G10, F10 D10, E10, F11 F12, E12, E11 D12, C12 | STi0 - 2 STi3 - 5 STi6 - 7 STi8 - 10 STi11 - 13 STi14 - 15 | Serial Input Streams 0 to 15 (5 V Tolerant Inputs): The data rate of these input streams can be selected independently using the stream input control registers. In the 2.048 Mb/s mode, these pins accept serial TDM data streams at 2.048 Mb/s with 32 channels per stream. In the 4.096 Mb/s mode, these pins accept serial TDM data streams at 4.096 Mb/s with 64 channels per stream. In the 8.192 Mb/s mode, these pins accept serial TDM data streams at 8.192 Mb/s with 128 channels per stream. Unused serial input pins are required to connect to either Vdd or ground, through an external pull-up resistors or external pull-down resistor. |
| 157 | D11 | \overline{RESET} | Device Reset (5 V Tolerant Input): This input (active LOW) puts the device in its reset state that disables the STo0 - 15 drivers and drives the STOHZ 0 - 15 outputs to high. It also clears the device registers and internal counters. To ensure proper reset action, the reset pin must be low for longer than 1 ms. Upon releasing the reset signal to the device, the first microprocessor access can take place after 600 μ s due to the time required to stabilize the APLL block from the power down state. |
| 158 | C11 | TDo | Test Serial Data Out (3 V Tolerant Three-state Output): JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled. |
| 1, 2, 29, 39 - 42, 79 - 82, 119 - 122, 159, 160 | C5, C6 | NC | No Connection Pins. These pins are not connected to the device internally. |

1.0 Device Overview

The device uses the ST-BUS input frame pulse and the ST-BUS input clock to define the input frame boundary and timing for the ST-BUS input streams with various data rates (2.048 Mb/s, 4.096 Mb/s and/or 8.192 Mb/s). The output frame boundary is defined by the output frame pulses and the output clock timing for the ST-BUS output streams with various data rates (2.048 Mb/s, 4.096 Mb/s and/or 8.192 Mb/s).

By using Zarlink's message mode capability, microprocessor data can be broadcast to the data output streams on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS devices.

A non-multiplexed microprocessor port allows users to program the device with various operating modes and switching configurations. Users can use the microprocessor port to perform register read/write, connection memory read/write and data memory read operations. The microprocessor port has a 12-bit address bus, a 16-bit data bus and four control signals.

The device also supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

2.0 Functional Description

A functional block diagram of the ZL50012 is shown in Figure 1 on page 1.

2.1 ST-BUS Input Data Rate and Input Timing

The device has sixteen ST-BUS serial data inputs. Any of the sixteen inputs can be programmed to accept different data rates, 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s.

2.1.1 ST-BUS Input Operation Mode

Any ST-BUS input can be programmed to accept the 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s data using Bit 0 to 2 in the stream input control registers, SICR0 to SICR15 as shown in Table 20 on page 42 and Table 21 on page 44.

The maximum number of input channels is 512 channels. External pull-up or pull-down resistors are required for any unused ST-BUS inputs.

2.1.2 Frame Pulse Input and Clock Input timing

The frame pulse input \overline{FPI} accepts the frame pulse used for the **highest** input data rate. The frame pulse is an 8 kHz input signal which stays low for 244 ns, 122 ns or 61 ns for the input data rate of 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s respectively. The frequency of \overline{CKi} must be twice the highest data rate. For example, if users present the ZL50012 with 2.048 Mb/s and 8.192 Mb/s input data, the device should be programmed to accept the input clock of 16.384 MHz and the frame pulse which stays low for 61 ns.

Users have to program the CKIN2 - 0 bits in the Control Register (CR), for the width of the frame pulse low cycle and the frequency of the input clock. See Table 1 for the programming of the CKIN0, CKIN1 and CKIN2 bits in the Control Register.

| CKIN2 - 0 bits | \overline{FPI} Low Cycle | \overline{CKi} | Highest Input Data Rate |
|----------------|----------------------------|------------------|-------------------------|
| 000 | 61 ns | 16.384 MHz | 8.192 Mb/s |
| 001 | 122 ns | 8.192 MHz | 4.096 Mb/s |
| 010 | 244 ns | 4.096 MHz | 2.048 Mb/s |
| 011 - 111 | Reserved | | |

Table 1 - \overline{FPI} and \overline{CKi} Input Programming

The device also accepts positive or negative input frame pulse and ST-BUS input clock formats via the programming of the FPINP and CKINP bits in the Internal Mode Selection (IMS) register. By default, the device accepts the negative input clock format.

Figure 4, Figure 5 and Figure 6 describe the usage of CKIN2 - 0, FPINP and CKINP in the Internal Mode Selection (IMS) register:

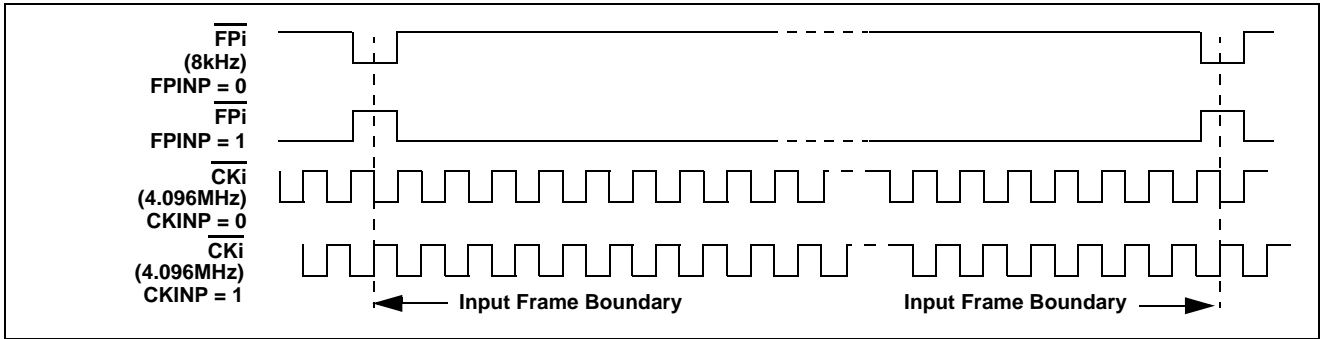


Figure 4 - Input Timing when (CKIN2 to CKIN0 bits = 010) in the Control Register

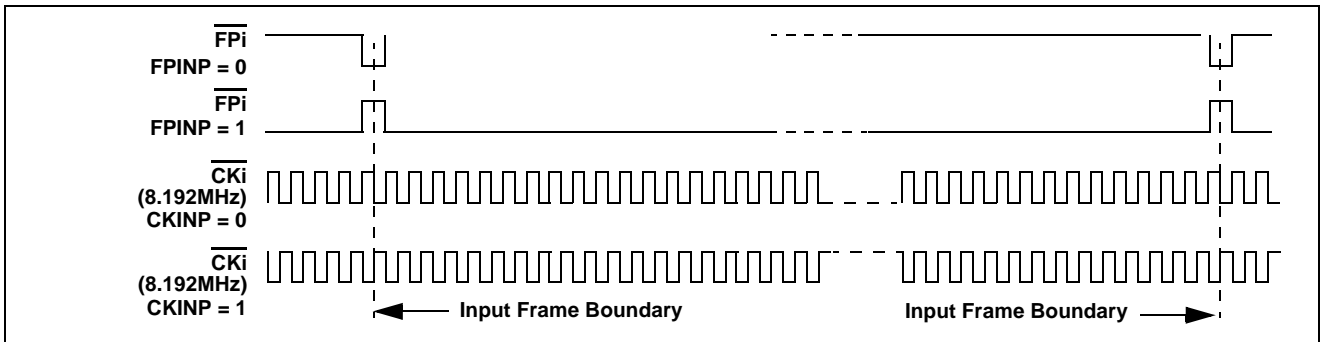


Figure 5 - Input Timing when (CKIN2 to CKIN0 bits = 001) in the Control Register

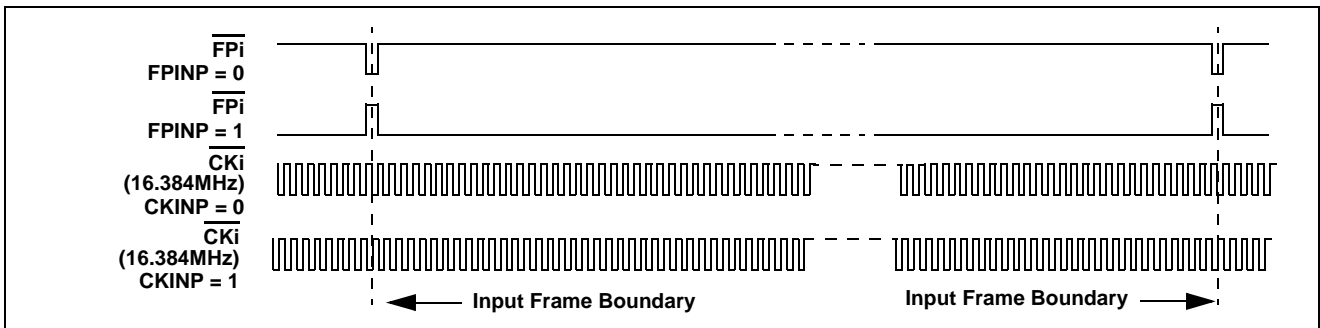


Figure 6 - Input Timing when (CKIN2 to CKIN0 bits = 000) in the Control Register

2.1.3 ST-BUS Input Timing

When the negative input frame pulse and negative input clock formats are used, the input frame boundary is defined by the falling edge of the CKi input clock while the FPi is low. When the input data rate is 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s, there are 32, 64 or 128 channels per every ST-BUS frame respectively. Figure 7 shows the details:

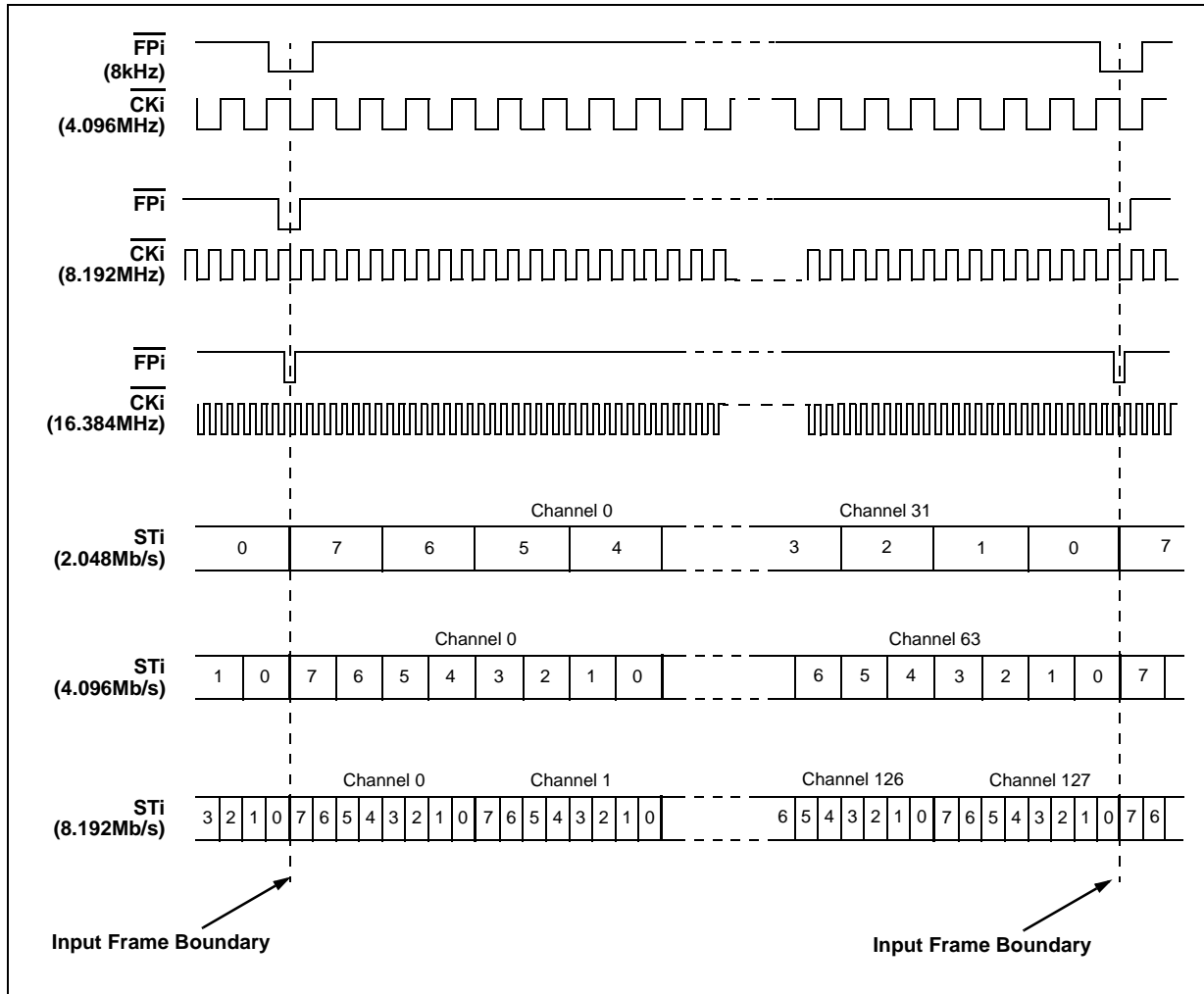


Figure 7 - ST-BUS Input Timing for Various Input Data Rates

2.1.4 Improved Input Jitter Tolerance with Frame Boundary Determinator

The ZL50012 has a Frame Boundary Determinator (FBD) allowing substantial increase of the CKi input clock jitter tolerance. The FBD circuit is enabled by setting the Control Register bits FBDEN and FBDMODE to HIGH. By default the FBD is disabled. Both the FBDEN and FBDMODE bits should be set HIGH during normal operation. The device can have 20 ns of input clock jitter tolerance (on CKi and FPi) when the FBD is fully enabled.

2.2 ST-Bus Output Data Rate and Output Timing

The device has sixteen ST-BUS serial data outputs. Any of the sixteen outputs can be programmed to deliver different data rates at 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s.

2.2.1 ST-Bus Output Operation Mode

Any ST-Bus output can be programmed to deliver the data at 2.048 Mb/s, 4.096 Mb/s or 8.192 Mb/s mode using Bit 0 to 2 in the Stream Output Control Register, SOCR0 to SOCR15 as shown in Table 24 on page 48 and Table 25 on page 49.

2.2.2 Frame Pulse Output and Clock Output Timing

The device offers three frame pulse outputs, $\overline{\text{FPo0}}$, $\overline{\text{FPo1}}$ and $\overline{\text{FPo2}}$. All output frame pulses are 8kHz output signals. By default, output frame boundary is defined by the falling edge of the $\overline{\text{CKo0}}$, $\overline{\text{CKo1}}$ or $\overline{\text{CKo2}}$ output clocks while the $\overline{\text{FPo0}}$, $\overline{\text{FPo1}}$ or $\overline{\text{FPo2}}$ output frame pulse goes low respectively.

In addition to the default settings, users can also select different output frame pulse low cycles and output clock frequencies by programming the CKFP0, CKFP1 and CKFP2 bits in the Control Register. See Table 2, Table 3 and Table 4 for the bit usage in the Control Register:

| CKFP0 | $\overline{\text{FPo0}}$ Low Cycle | $\overline{\text{CKo0}}$ |
|-------|---------------------------------------|--------------------------|
| 0 | 244 ns | 4.096 MHz |
| 1 | 122 ns | 8.192 MHz |

Table 2 - $\overline{\text{FPo0}}$ and $\overline{\text{CKo0}}$ Output Programming

| CKFP1 | $\overline{\text{FPo1}}$ | $\overline{\text{CKo1}}$ |
|-------|--------------------------|--------------------------|
| 0 | 61 ns | 16.384 MHz |
| 1 | 122 ns | 8.192 MHz |

Table 3 - $\overline{\text{FPo1}}$ and $\overline{\text{CKo1}}$ Output Programming

| CKFP2 | $\overline{\text{FPo2}}$ | $\overline{\text{CKo2}}$ |
|-------|--------------------------|--------------------------|
| 0 | 30 ns | 32.768 MHz |
| 1 | 61 ns | 16.384 MHz |

Table 4 - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Output Programming

The device also delivers positive or negative output frame pulse and ST-BUS output clock formats via the programming of the FP0P, FP1P, FP2P, CK0P, CK1P and CK2P bits in the Internal Mode Selection (IMS) register. By default, the device delivers the negative output frame pulse and negative output clock formats.

Figure 8 to Figure 13 describe the usage of the CKFP0, CKFP1, CKFP2, FP0P, FP1P, FP2P, CK0P, CK1P and CK2P in the Control Register and Internal Mode Selection Register:

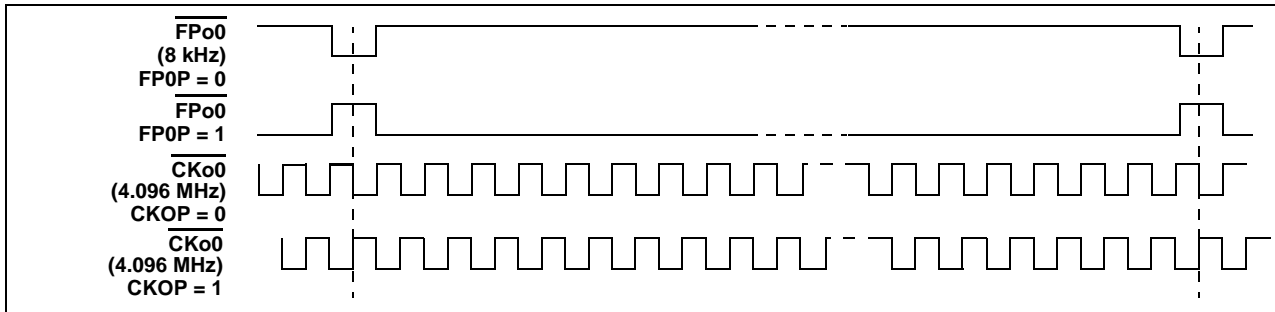


Figure 8 - $\overline{\text{FPo0}}$ and $\overline{\text{CKo0}}$ Output Timing when the CKFP0 bit = 0

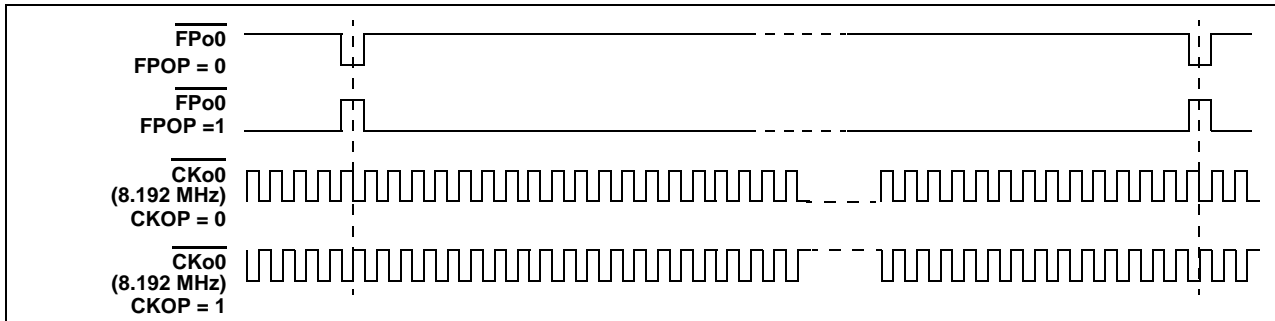


Figure 9 - $\overline{\text{FPo0}}$ and $\overline{\text{CKo0}}$ Output Timing when the CKFP0 bit = 1

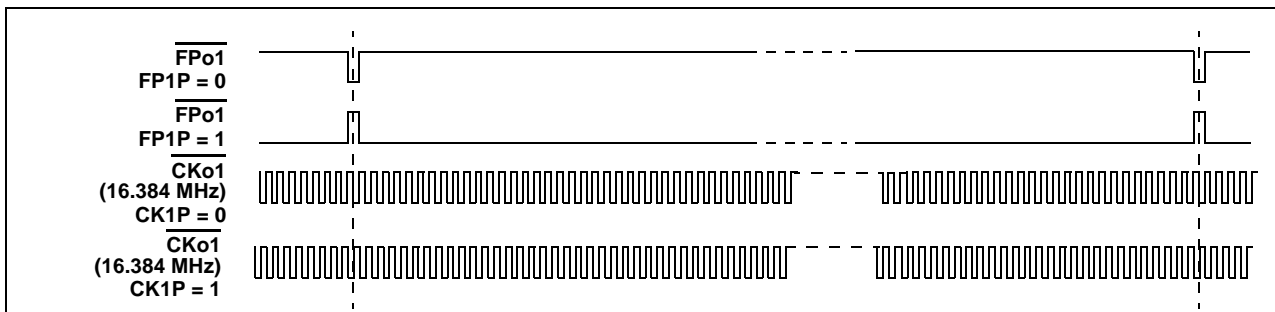


Figure 10 - $\overline{\text{FPo1}}$ and $\overline{\text{CKo1}}$ Output Timing when the CKFP1 bit = 0

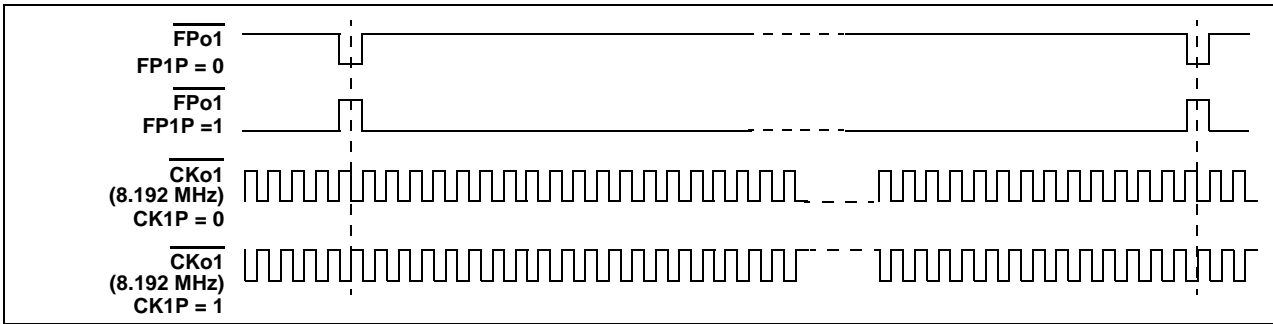


Figure 11 - $\overline{\text{FPo1}}$ and $\overline{\text{CKo1}}$ Output Timing when the CKFP1 bit = 1

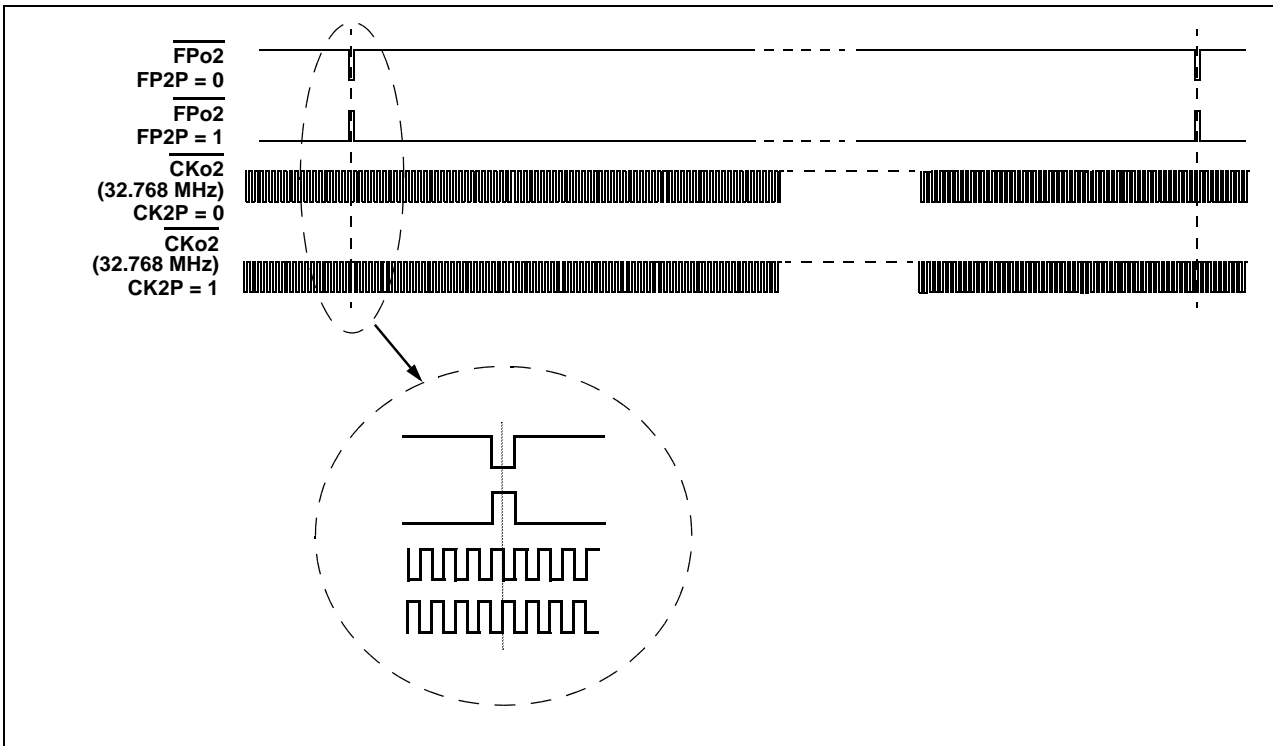


Figure 12 - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Output Timing when the CKFP2 bit = 0

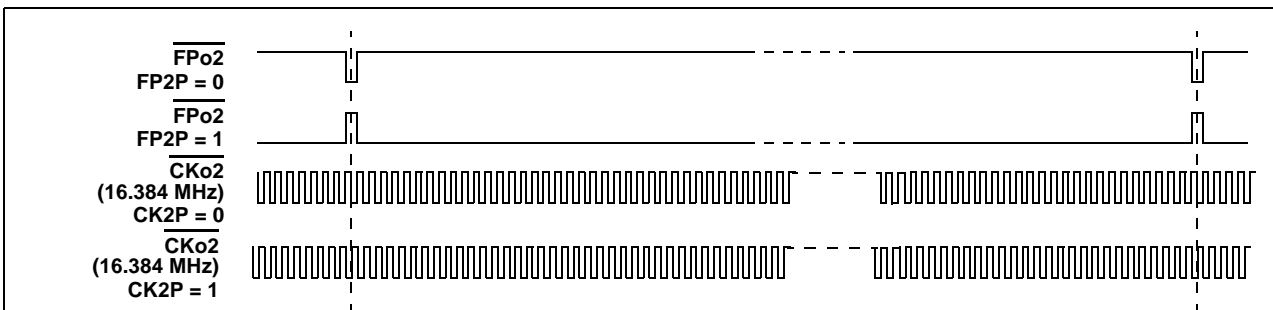


Figure 13 - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Output Timing when the CKFP2 bit = 1

2.2.3 ST-BUS Output Timing

By default, the output frame boundary is defined by the falling edge of the $\overline{CKo0}$, $\overline{CKo1}$ or $\overline{CKo2}$ output clock while the $\overline{FPo0}$, $\overline{FPo1}$ or $\overline{FPo2}$ output frame pulse goes low respectively. When the output data rates are 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s, there are 32, 64 or 128 output channels per every ST-BUS frame respectively. Figure 14 describes the details.

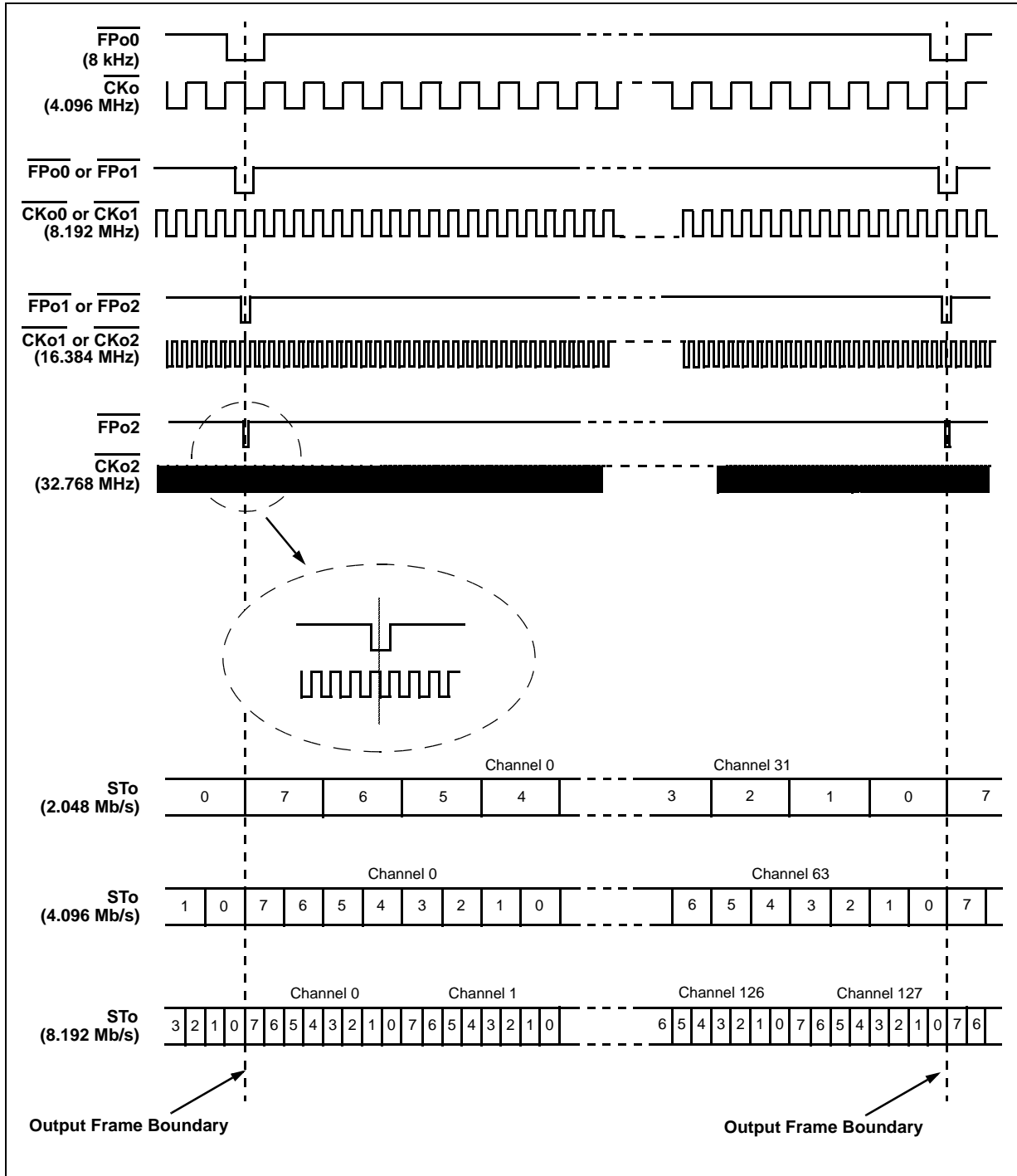


Figure 14 - ST-BUS Output Timing for Various Output Data Rates

2.3 Serial Data Input Delay and Serial Data Output Offset

Various registers are provided to adjust the input and output delays for every input and every output data stream. The input and output channel delay can vary from 0 to 31, 0 to 63 and 0 to 127 channel(s) for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s modes respectively.

The input and output bit delay can vary from 0 to 7 bits. The fractional input bit delay can vary from 1/4, 1/2, 3/4 to 4/4 bit. The fractional output bit advancement can vary from 0, 1/4, 1/2 to 3/4 bit.

2.3.1 Input Channel Delay Programming

This feature allows each input stream to have a different input frame boundary with respect to the input frame boundary defined by the FPI and CKi. By default, all input streams have channel delay of zero such that Ch0 is the first channel that appears after the input frame boundary (see Figure 15).

The input channel delay programming is enabled by setting Bit 3 to 9 in the Stream Input Delay Register (SIDR). The input channel delay can vary from 0 to 31, 0 to 63 and 0 to 127 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s modes respectively.

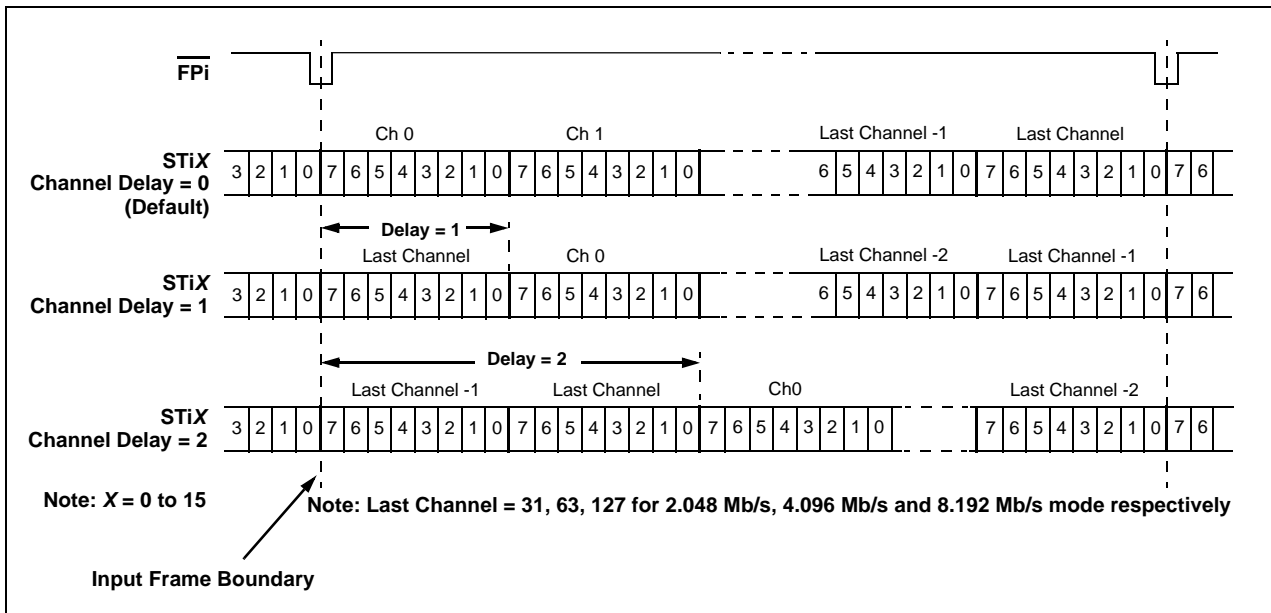


Figure 15 - Input Channel Delay Timing Diagram

2.3.2 Input Bit Delay Programming

In addition to the input channel delay programming, the input bit delay programming feature provides users with more flexibility when designing the switch matrices at high speed, in which the delay lines are easily created on PCM highways which are connected to the switch matrix cards.

By default, all input streams have zero bit delay such that Bit 7 is the first bit that appears after the input frame boundary, see Figure 16. The input delay is enabled by Bit 0 to 2 in the Stream Input Delay Registers (SIDR). The input bit delay can vary from 0 to 7 bits.

2.3.3 Fractional Input Bit Delay Programming

In addition to the input bit delay feature, the device allows users to change the sampling point of the input bit. By default, the sampling point is at 3/4 bit. Users can change the sampling point to 1/4, 1/2, 3/4 or 4/4 bit position by programming Bit 3 and 4 of the Stream Input Control Registers (SICR).

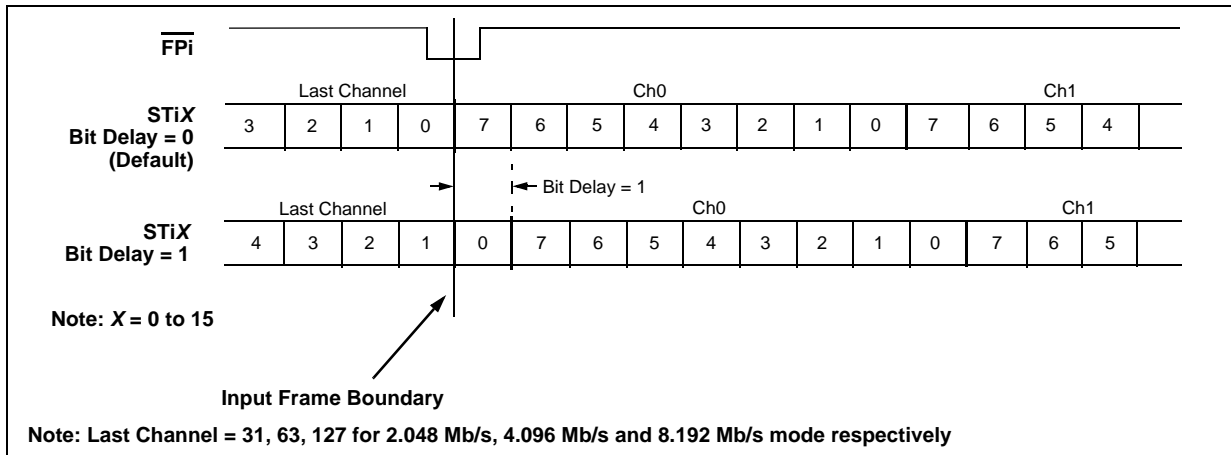


Figure 16 - Input Bit Delay Timing Diagram

2.3.4 Output Channel Delay Programming

This feature allows each output stream to have a different output frame boundary with respect to the output frame pulse (FPo0, FPo1 and FPo2) and the output clock (CKo0, CKo1 or CKo2). By default, all output streams have zero channel delay such that Ch 0 is the first channel that appears after the output frame boundary as shown in Figure 17. Different output channel delay can be set by programming Bit 5 to 11 in the Stream Output Offset Registers (SOOR). The output channel delay can vary from 0 to 31, 0 to 63 and 0 to 127 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s modes respectively.

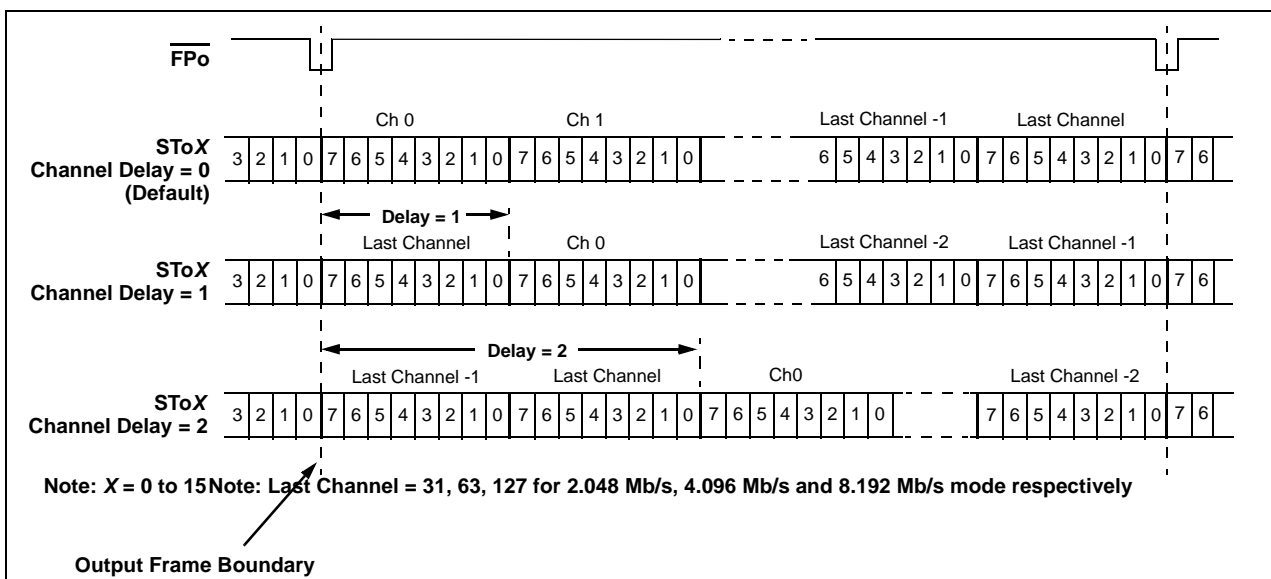


Figure 17 - Output Channel Delay Timing Diagram

2.3.5 Output Bit Delay Programming

This feature is used to delay the output data bit of individual output streams with respect to the output frame boundary. Each output stream can have its own bit delay value.

By default, all output streams have zero bit delay such that Bit 7 is the first bit that appears after the output frame boundary (see Figure 18 on page 25). Different output bit delay can be set by programming Bit 2 to 4 in the Stream Output Offset Registers. The output bit delay can vary from 0 to 7 bits.

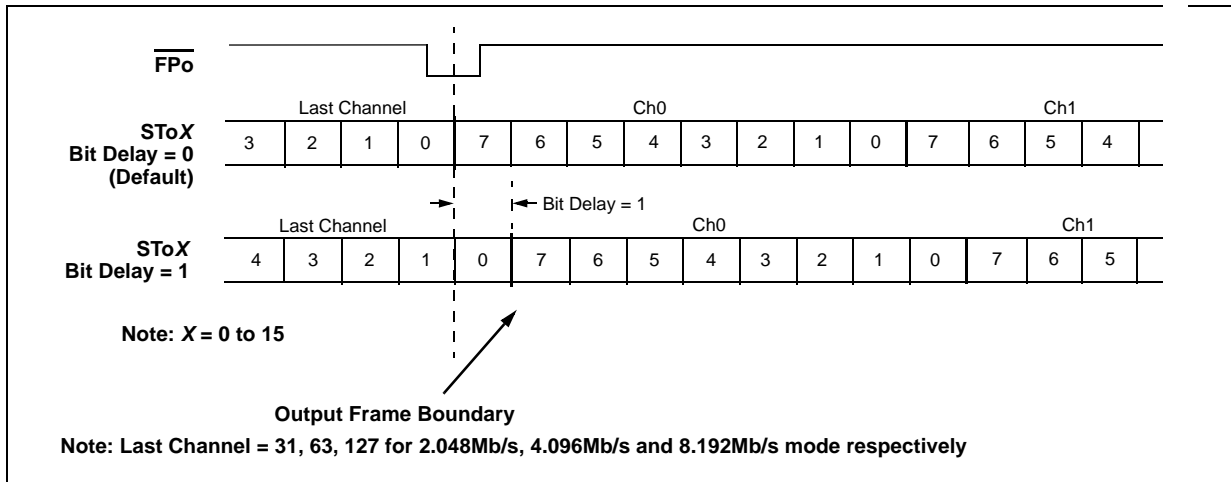


Figure 18 - Output Bit Delay Timing Diagram

2.3.6 Fractional Output Bit Advancement Programming

In addition to the output bit delay, the device is also capable of performing fractional output bit advancement. This feature offers a better resolution for the output bit delay adjustment. The fractional output bit advancement is useful in compensating for various parasitic loadings on the serial data output pins.

By default, all output streams have zero fractional bit advancement such that Bit 7 is the first bit that appears after the output frame boundary as shown in Figure 19. The fractional output bit advancement is enabled by Bit 0 to 1 in the Stream Output Offset Registers. The fractional bit advancement can vary from 0, 1/4, 1/2 or 3/4 bit.

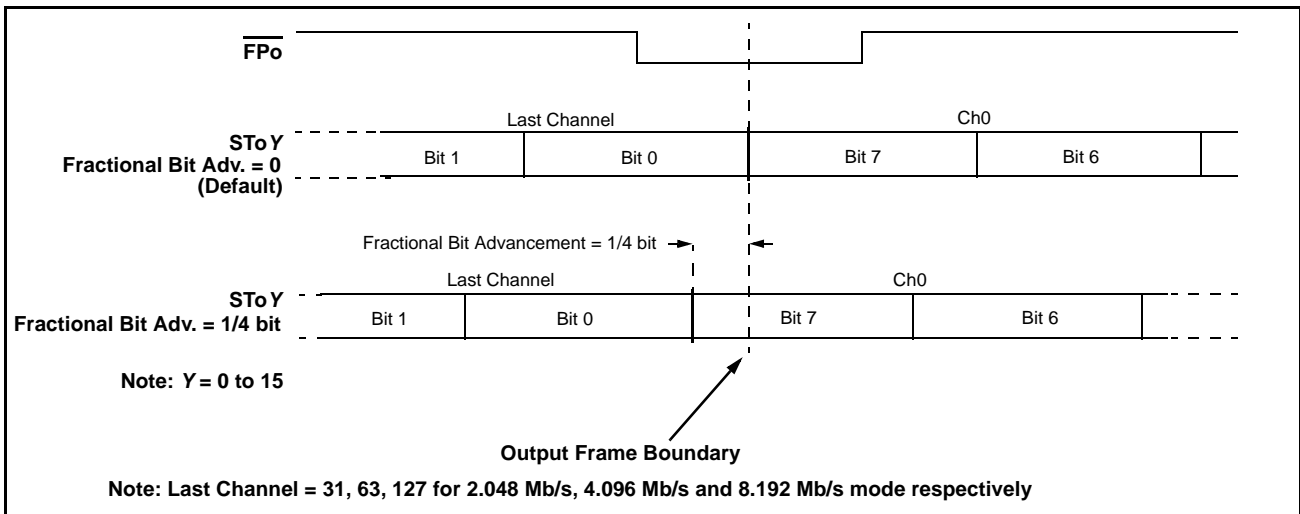


Figure 19 - Fractional Output Bit Advancement Timing Diagram

2.3.7 External High Impedance Control, STOHZ 0 to 15

The STOHZ 0 to 15 outputs are provided to control the external tristate ST-BUS drivers for per-channel high impedance operations. The STOHZ outputs are sent out in 32, 64 or 128 timeslots corresponding to the output channels for 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s output streams respectively. Each control timeslot lasts for one channel time.

When the ODE pin is high, the STOHZ 0 - 15 are enabled. When the ODE pin or the $\overline{\text{RESET}}$ pin is low, the STOHZ 0 - 15 are driven high. STOHZ outputs are also driven high if their corresponding ST-BUS outputs are not in use.

Figure 20 gives an example when channel 2 of a given ST-BUS output is programmed in the high impedance state, the corresponding STOHZ pin drives high for one channel time at the channel 2 timeslot.

By default, the output timing of the STOHZ signals follow the same timing as their corresponding STo signals including any user-programmed output channel and bit delay and fractional bit advancement. In addition, the device allows users to advance the STOHZ signals from their default positions to a maximum of four 15.2 ns steps (or four 1/4 bit steps) using Bit 3 to 5 of the Stream Output Control Register (SOCR). Bit 6 in the Stream Output Control Register selects the step resolution as 15.2 ns or 1/4 data bit. The additional advancement feature allows the STOHZ signals to better match the high impedance timing required by the external ST-BUS drivers.

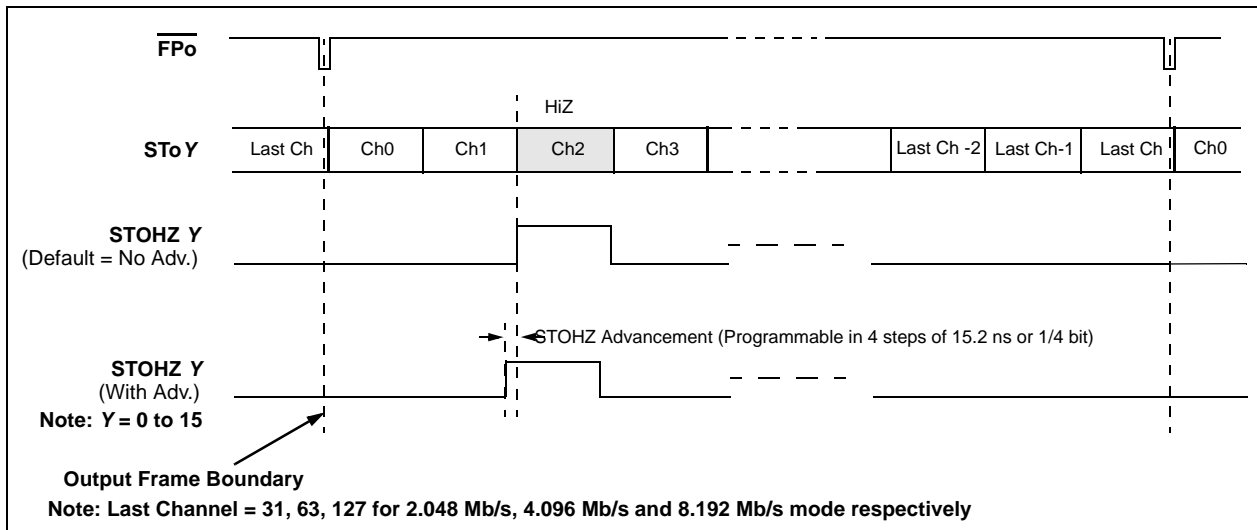


Figure 20 - Example: External High Impedance Control Timing

2.4 Data Delay Through The Switching Paths

To maintain the channel integrity in the constant delay mode, the usage of the input channel delay and output channel delay modes affect the data delay through various switching paths due to additional data buffers. The usage of these data buffers is enabled by the input and output channel delay bits (STIN#CD6-0 and STO#CD6-0) in the Stream Input Delay and Stream Output Offset Registers. However, the input and output bit delay or the input and output fractional bit offset have no impact on the overall data throughput delay.

In the following paragraphs, the data throughput delay (T) is expressed as a function of ST-BUS frames, input channel number (m), output channel number (n), input channel delay (α) and output channel delay (β). Table 5 describes the variable range for input streams and Table 6 describes the variable range for output streams. Table 7 summarizes the data throughput delay under various input channel and output channel delay conditions.

| Input Stream Data Rate | Input Channel Number (m) | Possible Input channel delay (α) |
|------------------------|--------------------------|---|
| 2 Mb/s | 0 to 31 | 1 to 31 |
| 4 Mb/s | 0 to 63 | 1 to 63 |
| 8 Mb/s | 0 to 127 | 1 to 127 |

Table 5 - Variable Range for Input Streams

| Output Stream Data Rate | Output Channel Number (n) | Possible Output channel delay (β) |
|-------------------------|---------------------------|---|
| 2 Mb/s | 0 to 31 | 1 to 31 |
| 4 Mb/s | 0 to 63 | 1 to 63 |
| 8 Mb/s | 0 to 127 | 1 to 127 |

Table 6 - Variable Range for Output Streams

| Input Channel Delay OFF Output Channel Delay OFF | Input Channel Delay ON Output Channel Delay OFF | Input Channel Delay OFF Output Channel Delay ON | Input Channel Delay ON Output Channel Delay ON |
|---|--|--|---|
| $T = 2 \text{ frames} + (n-m)$ | $T = 3 \text{ frames} - \alpha + (n-m)$ | $T = 2 \text{ frames} + \beta + (n-m)$ | $T = 3 \text{ frames} - \alpha + \beta + (n-m)$ |

Table 7 - Data Throughput Delay

By default, when the input channel delay and output channel delay are set to zero, the data throughput delay (T) is: $T = 2 \text{ frames} + (m-n)$. Figure 21 shows the throughput delay when the input Ch0 is switched to the output Ch0.

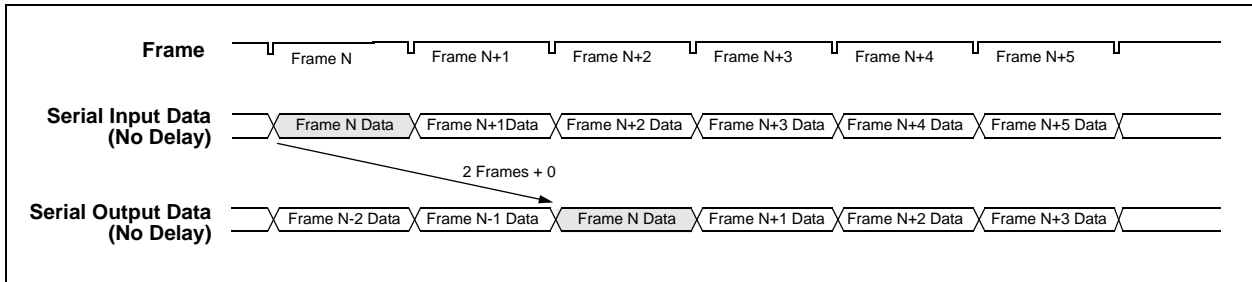


Figure 21 - Data Throughput Delay when input and output channel delay are disabled for Input Ch0 switched to Output Ch0

When the input channel delay is enabled and the output channel delay is disabled, the data throughput delay is: $T = 3 \text{ frames} - \alpha + (m-n)$. Figure 22 shows the data throughput delay when the input Ch0 is switched to the output Ch0.

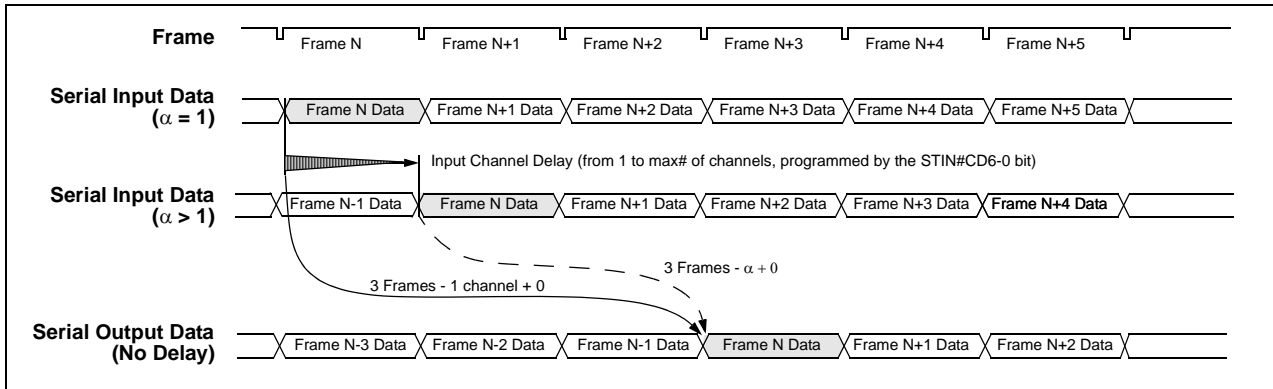


Figure 22 - Data Throughput Delay when input channel delay is enabled and output channel delay is disabled for Input Ch0 switched to Output Ch0

When the input channel delay is disabled and the output channel delay is enabled, the throughput delay is: $T = 2 \text{ frames} + \beta + (m-n)$. Figure 23 shows the data throughput delay when the input Ch0 is switched to the output Ch0.

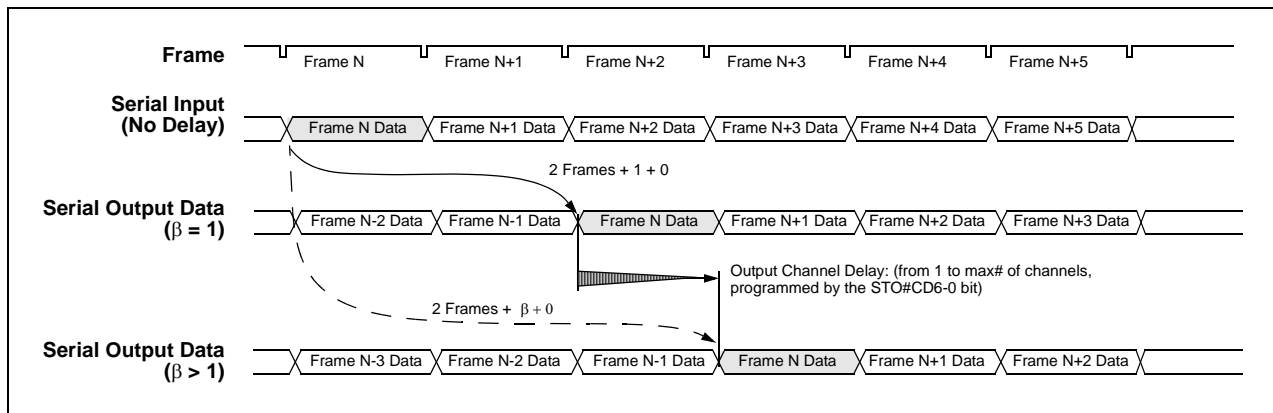


Figure 23 - Data Throughput Delay when input channel delay is disabled and output channel delay is enabled for Input Ch0 switch to Output Ch0

When the input channel delay and the output channel delay are enabled, the data throughput delay is: $T = 3 \text{ frames} - \alpha + \beta + (m-n)$. Figure 24 shows the data throughput delay when the input Ch0 is switched to the output Ch0.

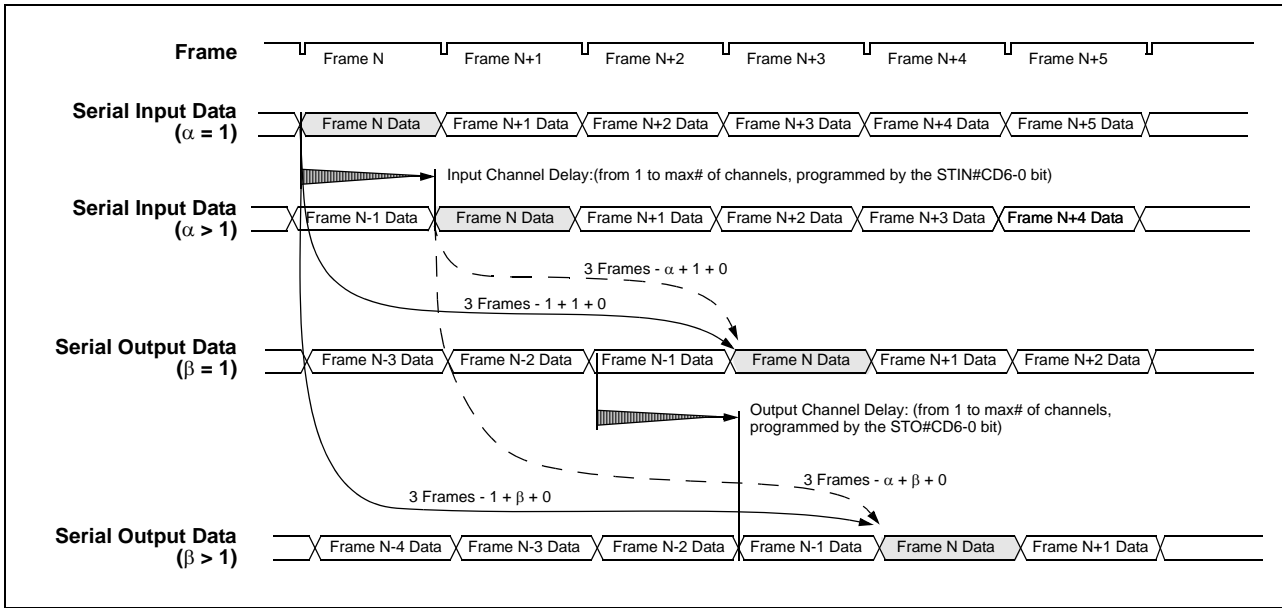


Figure 24 - Data Throughput Delay when input and output channel delay are enabled for Input Ch0 switched to Output Ch0

2.5 Connection Memory Description

The connection memory is 12-bit wide. There are 512 memory locations to support the ST-BUS serial outputs STo0-15. The address of each connection memory location corresponds to an output destination stream number and an output channel address. See Table 28 on page 52 for the connection memory address map.

When Bit 0 of the connection memory is **low**, Bit 1 to 7 define the source (input) channel address and Bit 8 to 11 define the source (input) stream address. Once the source stream and channel addresses are programmed by the microprocessor, the contents of the data memory at the selected address are switched to the mapped output stream and channel. See Table 29 on page 53 for details on the memory bit assignment when Bit 0 of the connection memory is low.

When Bit 0 of the connection memory is **high**, Bit 1 and 2 define the per-channel control modes of the output streams, the per-channel high impedance output control, the per-channel message and the per-channel BER test modes. In the message mode, the 8-bit message data located in Bit 3 to 10 of the connection memory will be transferred directly to the mapped output stream. See Table 30 on page 53 for details on the memory bit assignment when Bit 0 of the connection memory is high.

2.5.1 Connection Memory Block Programming

This feature allows fast initialization of the entire connection memory after power up. When block programming mode is enabled, the content of Bit 1 to 3 in the Internal Mode Selection (IMS) Register will be loaded into Bit 0 to 2 of all the 512 connection memory locations. The other bit positions of the connection memory will be loaded with zeros.

Memory block programming procedure:

(Assumption: The MBPE and MBPS bits are both low at the start of the procedure)

- Program Bit 1 to 3 (BPD0 to BPD2) in the IMS (Internal Mode Selection) register.
- Set the Memory Block Programming Enable (MBPE) bit in the Control Register to high to enable the block programming mode.
- Set the Memory Block Programming Start (MBPS) bit to high in the IMS Register to start the block programming. The BPD0 to BPD2 bits will be loaded into Bit 0 to 2 of the connection memory. The other bit positions of the connection memory will be loaded with zeros. The memory content after block programming is shown in Table 8.
- It takes 50 μ s for the connection memory to be loaded with the bit pattern defined by the BPD0 to BPD2 bits.
- After loading the bit pattern to the entire connection memory, the device will reset the MBPS bit to low, indicating that the process has finished.
- Upon completion of the block programming, set the MBPE bit from high to low to disable the block programming mode.

Note: Once the block programming is started, it can be terminated at any time prior to completion by setting the MBPS bit or the MBPE bit to low. If the MBPE bit is used to terminate the block programming before completion, users have to set the MBPS bit from high to low before enabling other device operation.

| | | | | | | | | | | | |
|----|----|---|---|---|---|---|---|---|------|------|------|
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BPD2 | BPD1 | BPD0 |

Table 8 - Connection Memory in Block Programming Mode

2.6 Bit Error Rate (BER) Test

The ZL50012 has one on-chip BER transmitter and one BER receiver. The transmitter can transmit onto a single STo output stream only. The transmitter provides a BER sequence ($2^{15}-1$ Pseudo Random Code) which can start from any channel in the frame and lasts from one channel up to one frame time (125 μ s). The transmitter output channel(s) are specified by programming the connection memory location(s) corresponding to the channel(s) of the selected output stream: Bit 0 to 2 of the connection memory location(s) should be programmed to the BER test mode (see Table 30 on page 53).

Multiple connection memory locations can be programmed for BER test such that the BER patterns can be transmitted for several output channels which are consecutive. If the transmitting output channels are not consecutive, the BER receiver will not compare the bit patterns correctly.

The number of output channels which the BER transmitter occupies also has to be the same as the number of channels defined in the BER Length Register. The BER Length Register defines how many BER channels to be monitored by the BER receiver.

Registers used for setting up the BER test are as follows:

- Control Register (**CR**) - The CBER bit is used to clear the bit error counter and the BER Count Register (BCR). The SBER bit is used to start or stop the BER transmitter and BER receiver.
- BER Start Receiving Register (**BSRR**) - Defines the input stream and channel from where the BER sequence will start to be compared.
- BER Length Register (**BLR**) - Defines how many channels the sequence will last.
- BER Count Register (**BCR**) - Contains the number of counted errors. When the error count reaches Hex FFFF, the bit error counter will stop so that it will not overflow. Consequently the BER Count Register will also stop at FFFF. The CBER bit in the Control Register is used to reset the bit error counter and the BER Count Register.

As described above, the SBER bit in the control register controls the BER transmitter and receiver. To carry out the BER test, users should set the SBER bit to zero to disable the BER transmitter during the programming of the connection memory for the BER test. When the BER transmitter is disabled, the transmitter output is all ones. Hence any output channel whose connection memory has been programmed to BER test mode will also output all ones. Upon the completion of programming the connection memory for the BER test, set the SBER bit to one to start the BER transmitter and receiver for the BER testing. They must be allowed to run for several frames (2 frames plus the network delay between STo and STi) before the BER receiver can correctly identify errors in the pattern. Thus after this time the bit error counter should be reset by using the CBER bit in the Control Register - set CBER to one then back to zero. From now on, the count will be the actual number of errors which occurred during the test. The count will stop at FFFF and the counter will not increment even if more errors occurred.

2.7 Quadrant frame programming

By programming the input stream control registers (SICR0 to 15), users can divide one frame of input data into four quadrant frames and can force the Least Significant Bit (LSB, bit 0 in Figure 7 on page 18), of every input channel in these quadrants into "1" for the bit robbed signaling purpose. The four quadrant frames are defined as shown in Table 9.

| Data Rate | Quadrant 0 | Quadrant 1 | Quadrant 2 | Quadrant 3 |
|------------|------------|-------------|-------------|--------------|
| 2.048 Mb/s | Ch 0 to 7 | Ch 8 to 15 | Ch 16 to 23 | Ch 24 to 31 |
| 4.096 Mb/s | Ch 0 to 15 | Ch 16 to 31 | Ch 32 to 47 | Ch 48 to 63 |
| 8.192 Mb/s | Ch 0 to 31 | Ch 32 to 63 | Ch 64 to 95 | Ch 96 to 127 |

Table 9 - Definition of the Four Quadrant Frames

When a quadrant frame enable bit (STIN#QEN0, STIN#QEN1, STIN#QEN2 or STIN#QEN3) is set to high, the LSB of every input channels in the quadrant is forced to "1". See Table 10 to Table 13 for details:

| STIN#QEN0 | Action |
|-----------|---|
| 1 | Replace LSB of every channel in Quadrant 0 with "1" |
| 0 | No bit replacement occurs in Quadrant 0 |

Table 10 - Quadrant Frame 0 LSB Replacement

| STIN#QEN1 | Action |
|-----------|---|
| 1 | Replace LSB of every channel in Quadrant 1 with "1" |
| 0 | No bit replacement occurs in Quadrant 1 |

Table 11 - Quadrant Frame 1 LSB Replacement

| STIN#QEN2 | Action |
|-----------|---|
| 1 | Replace LSB of every channel in Quadrant 2 with "1" |
| 0 | No bit replacement occurs in Quadrant 2 |

Table 12 - Quadrant Frame 2 LSB Replacement

| STIN#QEN3 | Action |
|-----------|---|
| 1 | Replace LSB of every channel in Quadrant 3 with "1" |
| 0 | No bit replacement occurs in Quadrant 3 |

Table 13 - Quadrant Frame 3 LSB Replacement

2.8 Microprocessor Port

The device supports the non-multiplexed microprocessor. The microprocessor port consists of a 16-bit parallel data bus (D0 to 15), a 12-bit address bus (A0 to 11) and four control signals (\overline{CS} , \overline{DS} , $\overline{R/W}$ and \overline{DTA}). The parallel microprocessor port provides fast access to the internal registers, the connection and the data memories.

The connection memory locations can be read or written via the 16-bit microprocessor port. On the other hand, the data memory locations can only be read (but not written) from the microprocessor port.

For the connection memory write operation, D0 to 11 of the data bus will be used and D12 to 15 are ignored (D12 to 15 should be driven low). For the connection memory read operation, D0 to D11 will be used and D12 to D15 will output zeros. For the data memory read operation, D0 to D7 will be used and D8 to D15 will output zeros.

See Table 28 on page 52 for the address mapping of the data memory. Refer to Figure 36 on page 65 for the microprocessor port timing.

3.0 Device Reset and Initialization

The \overline{RESET} pin is used to reset the device. When the pin is low, it synchronously puts the device in its reset state. It disables the ST00 - 15 outputs, drives the STOZH 0 - 15 outputs to high, clears the device registers and the internal counters.

Upon power up, the device should be initialized as follows:

- Set ODE pin to low to disable the ST00-15 output and to drive the STOZH 0-15 to high.
- Set the \overline{TRST} pin to low to disable the JTAG TAP controller.
- Reset the device by pulsing the \overline{RESET} pin to low for longer than 1ms.
- After releasing the \overline{RESET} pin from low to high, wait for 600 μ s for the APLL module to be stabilized before starting the first microprocessor port access cycle.
- Program the register to define the frequency of the \overline{CKi} input.
- Wait for 600 μ s for the APLL module to be stabilized before starting the next microprocessor port access cycle.
- Use the memory block programming mode to initialize the connection memory.
- Release the ODE pin to high after the connection memory is programmed such that bus contention will not occur at the serial stream outputs ST00-15.

4.0 JTAG Support

The ZL50012 JTAG interface conforms to the Boundary-Scan IEEE1149.1 standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

4.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50012 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)** - TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Select Input (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.

- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.
- **Test Reset (TRST)** - Resets the JTAG scan structure. This pin is internally pulled to Vdd when it is not driven from an external source.

4.2 Instruction Register

The ZL50012 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG Interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

4.3 Test Data Register

As specified in IEEE 1149.1, the ZL50012 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50012 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO.
- **The Device Identification Register** - The JTAG device ID for the ZL50012 is 0C35C14B_H.

| | |
|------------------------|---------------------|
| Version<31:28>: | 0000 |
| Part No. <27:12>: | 1100 0011 0101 1100 |
| Manufacturer ID<11:1>: | 0001 0100 101 |
| LSB<0>: | 1 |

4.4 BSDL

A BSDL (Boundary Scan Description Language) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149 test interface.

5.0 Register Address Mapping

| External Address A11 - A0 | CPU Access | Register |
|------------------------------|------------|---|
| 000 _H | R/W | Control Register, CR |
| 001 _H | R/W | Internal Mode Selection, IMS |
| 010 _H | R/W | BER Start Receive Register, BSRR |
| 011 _H | R/W | BER Length Register, BLR |
| 012 _H | Read Only | BER Count Register, BCR |
| 030 _H | Read Only | Reserved |
| 031 _H | Read Only | Reserved |
| 032 _H | Read Only | Reserved |
| 100 _H | R/W | Stream0 Input Control Register, SICR0 |
| 101 _H | R/W | Stream0 Input Delay Register, SIDR0 |
| 102 _H | R/W | Stream1 Input Control Register, SICR1 |
| 103 _H | R/W | Stream1 Input Delay Register, SIDR1 |
| 104 _H | R/W | Stream2 Input Control Register, SICR2 |
| 105 _H | R/W | Stream2 Input Delay Register, SIDR2 |
| 106 _H | R/W | Stream3 Input Control Register, SICR3 |
| 107 _H | R/W | Stream3 Input Delay Register, SIDR3 |
| 108 _H | R/W | Stream4 Input Control Register, SICR4 |
| 109 _H | R/W | Stream4 Input Delay Register, SIDR4 |
| 10A _H | R/W | Stream5 Input Control Register, SICR5 |
| 10B _H | R/W | Stream5 Input Delay Register, SIDR5 |
| 10C _H | R/W | Stream6 Input Control Register, SICR6 |
| 10D _H | R/W | Stream6 Input Delay Register, SIDR6 |
| 10E _H | R/W | Stream7 Input Control Register, SICR7 |
| 10F _H | R/W | Stream7 Input Delay Register, SIDR7 |
| 110 _H | R/W | Stream8 Input Control Register, SICR8 |
| 111 _H | R/W | Stream8 Input Delay Register, SIDR8 |
| 112 _H | R/W | Stream9 Input Control Register, SICR9 |
| 113 _H | R/W | Stream9 Input Delay Register, SIDR9 |
| 114 _H | R/W | Stream10 Input Control Register, SICR10 |
| 115 _H | R/W | Stream10 Input Delay Register, SIDR10 |
| 116 _H | R/W | Stream11 Input Control Register, SICR11 |
| 117 _H | R/W | Stream11 Input Delay Register, SIDR11 |
| 118 _H | R/W | Stream12 Input Control Register, SICR12 |
| 119 _H | R/W | Stream12 Input Delay Register, SIDR12 |
| 11A _H | R/W | Stream13 Input Control Register, SICR13 |

Table 14 - Address Map for Device Specific Registers

| External Address A11 - A0 | CPU Access | Register |
|--------------------------------------|-------------------|--|
| 11B _H | R/W | Stream13 Input Delay Register, SIDR13 |
| 11C _H | R/W | Stream14 Input Control Register, SICR14 |
| 11D _H | R/W | Stream14 Input Delay Register, SIDR14 |
| 11E _H | R/W | Stream15 Input Control Register, SICR15 |
| 11F _H | R/W | Stream15 Input Delay Register, SIDR15 |
| 200 _H | R/W | Stream0 Output Control Register, SOCR0 |
| 201 _H | R/W | Stream0 Output Delay Register, SOOR0 |
| 202 _H | R/W | Stream1 Output Control Register, SOCR1 |
| 203 _H | R/W | Stream1 Output Delay Register, SOOR1 |
| 204 _H | R/W | Stream2 Output Control Register, SOCR2 |
| 205 _H | R/W | Stream2 Output Delay Register, SOOR2 |
| 206 _H | R/W | Stream3 Output Control Register, SOCR3 |
| 207 _H | R/W | Stream3 Output Delay Register, SOOR3 |
| 208 _H | R/W | Stream4 Output Control Register, SOCR4 |
| 209 _H | R/W | Stream4 Output Delay Register, SOOR4 |
| 20A _H | R/W | Stream5 Output Control Register, SOCR5 |
| 20B _H | R/W | Stream5 Output Delay Register, SOOR5 |
| 20C _H | R/W | Stream6 Output Control Register, SOCR6 |
| 20D _H | R/W | Stream6 Output Delay Register, SOOR6 |
| 20E _H | R/W | Stream7 Output Control Register, SOCR7 |
| 20F _H | R/W | Stream7 Output Delay Register, SOOR7 |
| 210 _H | R/W | Stream8 Output Control Register, SOCR8 |
| 211 _H | R/W | Stream8 Output Delay Register, SOOR8 |
| 212 _H | R/W | Stream9 Output Control Register, SOCR9 |
| 213 _H | R/W | Stream9 Output Delay Register, SOOR9 |
| 214 _H | R/W | Stream10 Output Control Register, SOCR10 |
| 215 _H | R/W | Stream10 Output Delay Register, SOOR10 |
| 216 _H | R/W | Stream11 Output Control Register, SOCR11 |
| 217 _H | R/W | Stream11 Output Delay Register, SOOR11 |
| 218 _H | R/W | Stream12 Output Control Register, SOCR12 |
| 219 _H | R/W | Stream12 Output Delay Register, SOOR12 |
| 21A _H | R/W | Stream13 Output Control Register, SOCR13 |
| 21B _H | R/W | Stream13 Output Delay Register, SOOR13 |
| 21C _H | R/W | Stream14 Output Control Register, SOCR14 |
| 21D _H | R/W | Stream14 Output Delay Register, SOOR14 |
| 21E _H | R/W | Stream15 Output Control Register, SOCR15 |
| 21F _H | R/W | Stream15 Output Delay Register, SOOR15 |

Table 14 - Address Map for Device Specific Registers

6.0 Detail Register Description

| External Read/Write Address: 000 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|-----------------------------------|--|--------|--------|--------|--------|--------|--------|------|------|------|-----|-----|-----|-----------|-----------------------------------|-------------------------|-----|-------|------------|-----|--------|-----------|-----|--------|-----------|-----------|----------|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | | | | | | |
| FBD MODE | 0 | FBD EN | CKIN 2 | CKIN 1 | CKIN 0 | CKFP 2 | CKFP 1 | CKFP 0 | CBER | SBER | MBPE | OSB | MS2 | MS1 | MS0 | | | | | | | | | | | | | | |
| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | FBD-MODE | Frame Boundary Determination Mode Select. When either the FBDEN or FBDMODE bit is set low, the frame boundary discriminator (FBD) is disabled. When both the FBDEN and FBDMODE bits are set HIGH, the frame discriminator (FBD) is enabled. The device will have 20 ns of input clock jitter tolerance (on CK _i and FP _i) when the FBD is enabled. By default, the FBDEN and FBDMODE bits are Low. Both the FBDEN and FBDMODE bits should be set HIGH during normal operation. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | Unused | Reserved. In normal functional mode, this bit MUST be set to zero. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | FBDEN | Frame Boundary Determinator Enable. When either the FBDEN or FBDMODE bit is set low, the frame boundary discriminator (FBD) is disabled. When both the FBDEN and FBDMODE bits are set HIGH, the frame discriminator (FBD) is enabled. The device will have 20 ns of input clock jitter tolerance (on CK _i and FP _i) when the FBD is enabled. By default, the FBDEN and FBDMODE bits are Low. Both the FBDEN and FBDMODE bits should be set HIGH during normal operation. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 - 10 | CKIN2-0 | Input ST Bus Clock ($\overline{\text{CKi}}$) and Frame Pulse ($\overline{\text{FPi}}$) Selection. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CKIN2 - 0</th><th>$\overline{\text{FPi}}$ Low Cycle</th><th>$\overline{\text{CKi}}$</th></tr> </thead> <tbody> <tr> <td>000</td><td>61 ns</td><td>16.384 MHz</td></tr> <tr> <td>001</td><td>122 ns</td><td>8.192 MHz</td></tr> <tr> <td>010</td><td>244 ns</td><td>4.096 MHz</td></tr> <tr> <td>011 - 111</td><td colspan="2">Reserved</td></tr> </tbody> </table> | | | | | | | | | | | | | CKIN2 - 0 | $\overline{\text{FPi}}$ Low Cycle | $\overline{\text{CKi}}$ | 000 | 61 ns | 16.384 MHz | 001 | 122 ns | 8.192 MHz | 010 | 244 ns | 4.096 MHz | 011 - 111 | Reserved | |
| CKIN2 - 0 | $\overline{\text{FPi}}$ Low Cycle | $\overline{\text{CKi}}$ | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 61 ns | 16.384 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | 122 ns | 8.192 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 244 ns | 4.096 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 - 111 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | CKFP2 | Output ST Bus clock $\overline{\text{CKo2}}$ and frame pulse $\overline{\text{FPo2}}$ Selection. When this bit is low, CK _{o2} is 32.768 MHz clock and FP _{o2} is 30 ns wide frame pulse When this bit is high, CK _{o2} is 16.384 MHz clock and FP _{o2} is 61 ns wide frame pulse | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | CKFP1 | Output ST Bus clock $\overline{\text{CKo1}}$ and frame pulse $\overline{\text{FPo1}}$ Selection. When this bit is low, CK _{o1} is 16.384 MHz clock and FP _{o1} is 61 ns wide frame pulse When this bit is high, CK _{o1} is 8.192 MHz clock and FP _{o1} is 122 ns wide frame pulse | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | CKFP0 | Output ST Bus clock $\overline{\text{CKo0}}$ and frame pulse $\overline{\text{FPo0}}$ Selection. When this bit is low, CK _{o0} is 4.096 MHz clock and FP _{o0} is 244 ns wide frame pulse When this bit is high, CK _{o0} is 8.192 MHz clock and FP _{o0} is 122 ns wide frame pulse | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 15 - Control Register (CR) Bits

| External Read/Write Address: 000 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|------------------------------|---|---------|-------------|--------|--------|--------|--------|------|------|------|-----|-----|-----|-----|-------------------------------|------------------|---------|------------------------------|------------|------------------|-----------|----------|-----|-------------|---|---|---|-----|-------------|---|---|---|-----|-------------|---|---|---|--------|--------|
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FBD MODE | 0 | FBD EN | CKIN 2 | CKIN 1 | CKIN 0 | CKFP 2 | CKFP 1 | CKFP 0 | CBER | SBER | MBPE | OSB | MS2 | MS1 | MS0 | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | CBER | Bit Error Rate Counter Clear: When this bit is high, it resets the internal bit error counter and the content of the bit error count register (BCR) to zero. Upon completion of the reset, set this bit to zero. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | SBER | Bit Error Rate Test Start: When this bit is high, it enables the BER transmitter and receiver; starts the bit error rate test. The bit error test result is kept in the bit error count (BCR) register. Upon the completion of the BER test, set this bit to zero. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | MBPE | Memory Block Programming Enable: When this bit is high, the connection memory block programming mode is enabled to program Bit 0 to Bit 2 of the connection memory. When it is low, the memory block programming mode is disabled. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | OSB | Output Stand By Bit: This bit enables the STo0 - 15 and the STOHz 0 -15 serial outputs. The following table describes the HiZ control of the serial data outputs: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>$\overline{\text{RESET}}$ Pin</th> <th>ODE Pin</th> <th>OSB Bit</th> <th>STo0-15</th> <th>STOHz 0-15</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>X</td> <td>HiZ</td> <td>Driven High</td> </tr> <tr> <td>1</td> <td>0</td> <td>X</td> <td>HiZ</td> <td>Driven High</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>HiZ</td> <td>Driven High</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Active</td> <td>Active</td> </tr> </tbody> </table> | | | | | | | | | | | | | | $\overline{\text{RESET}}$ Pin | ODE Pin | OSB Bit | STo0-15 | STOHz 0-15 | 0 | X | X | HiZ | Driven High | 1 | 0 | X | HiZ | Driven High | 1 | 1 | 0 | HiZ | Driven High | 1 | 1 | 1 | Active | Active |
| $\overline{\text{RESET}}$ Pin | ODE Pin | OSB Bit | STo0-15 | STOHz 0-15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | X | X | HiZ | Driven High | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | X | HiZ | Driven High | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | HiZ | Driven High | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | Active | Active | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 - 0 | MS2-0 | Memory Select Bit. These bits are used to select connection memory or data memory: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>MS2 - 0</th> <th>Memory Selection</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Connection Memory Read/Write</td> </tr> <tr> <td>001</td> <td>Data memory Read</td> </tr> <tr> <td>010 - 111</td> <td>Reserved</td> </tr> </tbody> </table> | | | | | | | | | | | | | | MS2 - 0 | Memory Selection | 000 | Connection Memory Read/Write | 001 | Data memory Read | 010 - 111 | Reserved | | | | | | | | | | | | | | | | | |
| MS2 - 0 | Memory Selection | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | Connection Memory Read/Write | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | Data memory Read | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 - 111 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 15 - Control Register (CR) Bits (continued)

| External Read/Write Address: 001 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | | |
|---|----------|--|----|-------|-------|------|------|------|------|------|------|----------|----------|----------|------|--|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | CKINP | FPINP | CK2P | FP2P | CK1P | FP1P | CK0P | FP0P | BPD 2 | BPD 1 | BPD 0 | MBPS | |
| Bit | Name | Description | | | | | | | | | | | | | | |
| 15 - 12 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. | | | | | | | | | | | | | | |
| 11 | CKINP | ST Bus Clock Input ($\overline{\text{CKi}}$) Polarity. When this bit is low, the $\overline{\text{CKi}}$ falling edge aligns with the frame boundary. When this bit is high, the $\overline{\text{CKi}}$ rising edge aligns with the frame boundary. | | | | | | | | | | | | | | |
| 10 | FPINP | Frame Pulse Input ($\overline{\text{FPi}}$) Polarity. When this bit is low, the input frame pulse $\overline{\text{FPi}}$ should have the negative frame pulse format. When this bit is high, the input frame pulse $\overline{\text{FPi}}$ should have the positive frame pulse format. | | | | | | | | | | | | | | |
| 9 | CK2P | ST Bus Clock Output ($\overline{\text{CKo2}}$) Polarity. When this bit is low, the output clock $\overline{\text{CKo2}}$ falling edge aligns with the frame boundary. When this bit is high, the output clock $\overline{\text{CKo2}}$ rising edge aligns with the frame boundary. | | | | | | | | | | | | | | |
| 8 | FP2P | Frame Pulse Output ($\overline{\text{FPo2}}$) Polarity. When this bit is low, the output frame pulse $\overline{\text{FPo2}}$ has the negative frame pulse format. When this bit is high, the output frame pulse $\overline{\text{FPo2}}$ has the positive frame pulse format. | | | | | | | | | | | | | | |
| 7 | CK1P | ST Bus Clock Output ($\overline{\text{CKo1}}$) Polarity. When this bit is low, the output clock $\overline{\text{CKo1}}$ falling edge aligns with the frame boundary. When this bit is high, the output clock $\overline{\text{CKo1}}$ rising edge aligns with the frame boundary. | | | | | | | | | | | | | | |
| 6 | FP1P | Frame Pulse Output ($\overline{\text{FPo1}}$) Polarity. When this bit is low, the output frame pulse $\overline{\text{FPo1}}$ has the negative frame pulse format. When this bit is high, the output frame pulse $\overline{\text{FPo1}}$ has the positive frame pulse format. | | | | | | | | | | | | | | |
| 5 | CK0P | ST Bus Clock Output ($\overline{\text{CKo0}}$) Polarity. When this bit is low, the output clock $\overline{\text{CKo0}}$ falling edge aligns with the frame boundary. When this bit is high, the output clock $\overline{\text{CKo0}}$ rising edge aligns with the frame boundary. | | | | | | | | | | | | | | |
| 4 | FP0P | Frame Pulse Output ($\overline{\text{FPo0}}$) Polarity. When this bit is low, the output frame pulse $\overline{\text{FPo0}}$ has the negative frame pulse format. When this bit is high, the output frame pulse $\overline{\text{FPo0}}$ has the positive frame pulse format. | | | | | | | | | | | | | | |
| 3 - 1 | BPD2 - 0 | Block Programming Data: These bits refer to the value to be loaded into the connection memory. Whenever the memory block programming feature is activated. After the MBPE bit in the control register is set to high and the MBPS bit is set to high, the contents of the bits BPD0 to BPD2 are loaded into Bit 0 to Bit 2 of the connection memory. Bit 3 to Bit 11 of the connection memory are zeroed. | | | | | | | | | | | | | | |

Table 16 - Internal Mode Selection (IMS) Register Bits

| External Read/Write Address: 001 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | |
|---|------|---|----|-------|-------|------|------|------|------|------|------|----------|----------|----------|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | CKINP | FPINP | CK2P | FP2P | CK1P | FP1P | CK0P | FP0P | BPD 2 | BPD 1 | BPD 0 | MBPS |
| Bit | Name | Description | | | | | | | | | | | | | |
| 0 | MBPS | <p>Memory Block Programming Start: A zero to one transition of this bit starts the memory block programming function. The MBPS, BPD0 to BPD2 bits in this register must be defined in the same write operation. Once the MBPE bit in the control register is set to high, the device requires 50 μs to complete the block programming. After the programming function has finished, the MBPS bit returns to low indicating the operation is completed. When the MBPS is high, the MBPS or MBPE can be set to low to abort the programming operation.</p> <p>To ensure proper block programming operation, when MBPS is high the BPD0 to BPD2 bits in this register must not be changed.</p> <p>Whenever the microprocessor writes a one to the MBPS bit, the block programming function is started, the user must maintain the same logical value to the other bits in this register to avoid any change in the device setting.</p> | | | | | | | | | | | | | |

Table 16 - Internal Mode Selection (IMS) Register Bits (continued)

| External Read/Write Address: 010 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | |
|---|-----------|--|-----------|-----------|-----------|-----------|---|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | BR SA3 | BR SA2 | BR SA1 | BR SA0 | 0 | 0 | BR CA6 | BR CA5 | BR CA4 | BR CA3 | BR CA2 | BR CA1 | BR CA0 |
| Bit | Name | Description | | | | | | | | | | | | | |
| 15 - 13 8 - 7 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. | | | | | | | | | | | | | |
| 12 - 9 | BRSA3 - 0 | BER Receive Stream Address Bits: The binary value of these bits refers to the input stream which receives the BER data. | | | | | | | | | | | | | |
| 6 - 0 | BRCA6 - 0 | BER Receive Channel Address Bits: The binary value of these bits refers to the input channel in which the BER data starts to be compared. | | | | | | | | | | | | | |

Table 17 - BER Start Receiving Register (BSRR) Bits

| External Read/Write Address: 011 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | |
|---|---------|--|----|----|----|---|---|-----|-----|-----|-----|-----|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BL7 | BL6 | BL5 | BL4 | BL3 | BL2 | BL1 | BL0 |
| Bit | Name | Description | | | | | | | | | | | | | |
| 15 - 8 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. | | | | | | | | | | | | | |
| 7 - 0 | BL7 - 0 | BER Length Bits: The binary value of these bits refers to the number of channels. The maximum numbers of BER channels are 32, 64 and 128 for the data rate of 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s modes respectively. The minimum number of BER channel is 1. If these bits are set to zero, no BER test will be performed. | | | | | | | | | | | | | |

Table 18 - BER Length Register (BLR) Bits

| External Read Address: 012 _H Reset Value: 0000 _H | | | | | | | | | | | | | | | |
|---|----------|---|----------|----------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BC 15 | BC 14 | BC 13 | BC 12 | BC 11 | BC 10 | BC 9 | BC 8 | BC 7 | BC 6 | BC 5 | BC 4 | BC 3 | BC 2 | BC 1 | BC 0 |
| Bit | Name | Description | | | | | | | | | | | | | |
| 15 - 0 | BC15 - 0 | BER Count Bits: The binary value of these bits refers to the bit error counts. When it reaches its maximum value of Hex FFFF, the value will not be changed any more | | | | | | | | | | | | | |

Table 19 - BER Count Register (BCR) Bits

External Read/Write Address: 100_H, 102_H, 104_H, 106_H, 108_H, 10A_H, 10C_H, 10E_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|---|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SICR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN0 QEN3 | STIN0 QEN2 | STIN0 QEN1 | STIN0 QEN0 | STIN0 SMP1 | STIN0 SMP0 | STIN0 DR2 | STIN0 DR1 | STIN0 DR0 |
| SICR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN1 QEN3 | STIN1 QEN2 | STIN1 QEN1 | STIN1 QEN0 | STIN1 SMP1 | STIN1 SMP0 | STIN1 DR2 | STIN1 DR1 | STIN1 DR0 |
| SICR2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN2 QEN3 | STIN2 QEN2 | STIN2 QEN1 | STIN2 QEN0 | STIN2 SMP1 | STIN2 SMP0 | STIN2 DR2 | STIN2 DR1 | STIN2 DR0 |
| SICR3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN3 QEN3 | STIN3 QEN2 | STIN3 QEN1 | STIN3 QEN0 | STIN3 SMP1 | STIN3 SMP0 | STIN3 DR2 | STIN3 DR1 | STIN3 DR0 |
| SICR4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN4 QEN3 | STIN4 QEN2 | STIN4 QEN1 | STIN4 QEN0 | STIN4 SMP1 | STIN4 SMP0 | STIN4 DR2 | STIN4 DR1 | STIN4 DR0 |
| SICR5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN5 QEN3 | STIN5 QEN2 | STIN5 QEN1 | STIN5 QEN0 | STIN5 SMP1 | STIN5 SMP0 | STIN5 DR2 | STIN5 DR1 | STIN5 DR0 |
| SICR6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN6 QEN3 | STIN6 QEN2 | STIN6 QEN1 | STIN6 QEN0 | STIN6 SMP1 | STIN6 SMP0 | STIN6 DR2 | STIN6 DR1 | STIN6 DR0 |
| SICR7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN7 QEN3 | STIN7 QEN2 | STIN7 QEN1 | STIN7 QEN0 | STIN7 SMP1 | STIN7 SMP0 | STIN7 DR2 | STIN7 DR1 | STIN7 DR0 |

| Bit | Name | Description |
|--------|-----------|--|
| 15 - 9 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. |
| 8 | STIN#QEN3 | Quadrant Frame 3 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch24 to 31, Ch48 to 63 and Ch96 to 127 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s mode respectively. |
| 7 | STIN#QEN2 | Quadrant Frame 2 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch16 to 23, Ch32 to 47 and Ch64 to 95 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s mode respectively. |
| 6 | STIN#QEN1 | Quadrant Frame 1 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch8 to 15, Ch16 to 31 and Ch32 to 63 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s mode respectively. |
| 5 | STIN#QEN0 | Quadrant Frame 0 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch0 to 7, Ch8 to 15 and Ch16 to 31 for 2.048 Mb/s, the 4.096 Mb/s and 8.192 Mb/s mode respectively. |

Table 20 - Stream Input Control Register 0 to 7 (SICR0 to SICR7)

External Read/Write Address: 100_H, 102_H, 104_H, 106_H, 108_H, 10A_H, 10C_H, 10E_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|---|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SICR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN0 QEN3 | STIN0 QEN2 | STIN0 QEN1 | STIN0 QEN0 | STIN0 SMP1 | STIN0 SMP0 | STIN0 DR2 | STIN0 DR1 | STIN0 DR0 |
| SICR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN1 QEN3 | STIN1 QEN2 | STIN1 QEN1 | STIN1 QEN0 | STIN1 SMP1 | STIN1 SMP0 | STIN1 DR2 | STIN1 DR1 | STIN1 DR0 |
| SICR2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN2 QEN3 | STIN2 QEN2 | STIN2 QEN1 | STIN2 QEN0 | STIN2 SMP1 | STIN2 SMP0 | STIN2 DR2 | STIN2 DR1 | STIN2 DR0 |
| SICR3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN3 QEN3 | STIN3 QEN2 | STIN3 QEN1 | STIN3 QEN0 | STIN3 SMP1 | STIN3 SMP0 | STIN3 DR2 | STIN3 DR1 | STIN3 DR0 |
| SICR4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN4 QEN3 | STIN4 QEN2 | STIN4 QEN1 | STIN4 QEN0 | STIN4 SMP1 | STIN4 SMP0 | STIN4 DR2 | STIN4 DR1 | STIN4 DR0 |
| SICR5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN5 QEN3 | STIN5 QEN2 | STIN5 QEN1 | STIN5 QEN0 | STIN5 SMP1 | STIN5 SMP0 | STIN5 DR2 | STIN5 DR1 | STIN5 DR0 |
| SICR6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN6 QEN3 | STIN6 QEN2 | STIN6 QEN1 | STIN6 QEN0 | STIN6 SMP1 | STIN6 SMP0 | STIN6 DR2 | STIN6 DR1 | STIN6 DR0 |
| SICR7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | STIN7 QEN3 | STIN7 QEN2 | STIN7 QEN1 | STIN7 QEN0 | STIN7 SMP1 | STIN7 SMP0 | STIN7 DR2 | STIN7 DR1 | STIN7 DR0 |

| Bit | Name | Description | | | | | | | | | | | | |
|-------------|---|--|-------------|----------------|-----|---|-----|------------|-----|------------|-----|------------|-----------|----------|
| 4 - 3 | STIN#SMP1 - 0 | Input Data Sampling Point Selection Bits: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>STIN#SMP1-0</th> <th>Sampling Point</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>3/4 point</td> </tr> <tr> <td>01</td> <td>4/4 point</td> </tr> <tr> <td>10</td> <td>1/4 point</td> </tr> <tr> <td>11</td> <td>2/4 point</td> </tr> </tbody> </table> | STIN#SMP1-0 | Sampling Point | 00 | 3/4 point | 01 | 4/4 point | 10 | 1/4 point | 11 | 2/4 point | | |
| STIN#SMP1-0 | Sampling Point | | | | | | | | | | | | | |
| 00 | 3/4 point | | | | | | | | | | | | | |
| 01 | 4/4 point | | | | | | | | | | | | | |
| 10 | 1/4 point | | | | | | | | | | | | | |
| 11 | 2/4 point | | | | | | | | | | | | | |
| 2 - 0 | STIN#DR2 - 0 | Input Data Rate Selection Bits: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>STIN#DR2-0</th> <th>Data Rate</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Disabled - External pull-up or pull-down is required for ST-BUS input</td> </tr> <tr> <td>001</td> <td>2.048 Mb/s</td> </tr> <tr> <td>010</td> <td>4.096 Mb/s</td> </tr> <tr> <td>011</td> <td>8.192 Mb/s</td> </tr> <tr> <td>100 - 111</td> <td>Reserved</td> </tr> </tbody> </table> | STIN#DR2-0 | Data Rate | 000 | Disabled - External pull-up or pull-down is required for ST-BUS input | 001 | 2.048 Mb/s | 010 | 4.096 Mb/s | 011 | 8.192 Mb/s | 100 - 111 | Reserved |
| STIN#DR2-0 | Data Rate | | | | | | | | | | | | | |
| 000 | Disabled - External pull-up or pull-down is required for ST-BUS input | | | | | | | | | | | | | |
| 001 | 2.048 Mb/s | | | | | | | | | | | | | |
| 010 | 4.096 Mb/s | | | | | | | | | | | | | |
| 011 | 8.192 Mb/s | | | | | | | | | | | | | |
| 100 - 111 | Reserved | | | | | | | | | | | | | |

Note: # denotes input stream from 0 to 7

Table 20 - Stream Input Control Register 0 to 7 (SICR0 to SICR7) (continued)

| External Read/Write Address: 110 _H , 112 _H , 114 _H , 116 _H , 118 _H , 11A _H , 11C _H , 11E _H Reset Value: 0000 _H | | | | | | | | | | | | | | | | |
|--|-----------|----|--|----|----|----|---|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|---------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SICR8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN8 QEN3 | STIN8 QEN2 | STIN8 QEN1 | STIN8 QEN0 | STIN8 SMP1 | STIN8 SMP0 | STIN8 DR2 | STIN8 DR1 | STIN8 DR0 |
| SICR9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN9 QEN3 | STIN9 QEN2 | STIN9 QEN1 | STIN9 QEN0 | STIN9 SMP1 | STIN9 SMP0 | STIN9 DR2 | STIN9 DR1 | STIN9 DR0 |
| SICR10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN10 QEN3 | STIN10 QEN2 | STIN10 QEN1 | STIN10 QEN0 | STIN10 SMP1 | STIN10 SMP0 | STIN10 DR2 | STIN10 DR1 | STIN10 DR0 |
| SICR11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN11 QEN3 | STIN11 QEN2 | STIN11 QEN1 | STIN11 QEN0 | STIN11 SMP1 | STIN11 SMP0 | STIN11 DR2 | STIN11 DR1 | STIN11 DR0 |
| SICR12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN12 QEN3 | STIN12 QEN2 | STIN12 QEN1 | STIN12 QEN0 | STIN12 SMP1 | STIN12 SMP0 | STIN12 DR2 | STIN12 DR1 | STIN12 DR0 |
| SICR13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN13 QEN3 | STIN13 QEN2 | STIN13 QEN1 | STIN13 QEN0 | STIN13 SMP1 | STIN13 SMP0 | STIN13 DR2 | STIN13 DR1 | STIN13 DR0 |
| SICR14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN14 QEN3 | STIN14 QEN2 | STIN14 QEN1 | STIN14 QEN0 | STIN14 SMP1 | STIN14 SMP0 | STIN14 DR2 | STIN14 DR1 | STIN14 DR0 |
| SICR15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN15 QEN3 | STIN15 QEN2 | STIN15 QEN1 | STIN15 QEN0 | STIN15 SMP1 | STIN15 SMP0 | STIN15 DR2 | STIN15 DR1 | STIN15 DR0 |
| Bit | Name | | Description | | | | | | | | | | | | | |
| 15 - 9 | Unused | | Reserved. In normal functional mode, these bits MUST be set to zero. | | | | | | | | | | | | | |
| 8 | STIN#QEN3 | | Quadrant Frame 3 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch24 to 31, Ch48 to 63 and Ch96 to 127 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s mode respectively. | | | | | | | | | | | | | |
| 7 | STIN#QEN2 | | Quadrant Frame 2 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch16 to 23, Ch32 to 47 and Ch64 to 95 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s mode respectively. | | | | | | | | | | | | | |
| 6 | STIN#QEN1 | | Quadrant Frame 1 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch8 to 15, Ch16 to 31 and Ch32 to 63 for the 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s mode respectively. | | | | | | | | | | | | | |
| 5 | STIN#QEN0 | | Quadrant Frame 0 Enable. When this bit is low, the device is in normal operation mode. When this bit is high, the LSB of every channel in this quadrant frame is replaced by "1". This quadrant frame is defined as Ch0 to 7, Ch8 to 15 and Ch16 to 31 for 2.048 Mb/s, the 4.096 Mb/s and 8.192 Mb/s mode respectively. | | | | | | | | | | | | | |

Table 21 - Stream Input Control Register 8 to 15 (SICR8 to SICR15)

External Read/Write Address: 110_H, 112_H, 114_H, 116_H, 118_H, 11A_H, 11C_H, 11E_H
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|---|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SICR8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN8 QEN3 | STIN8 QEN2 | STIN8 QEN1 | STIN8 QEN0 | STIN8 SMP1 | STIN8 SMP0 | STIN8 DR2 | STIN8 DR1 | STIN8 DR0 |
| SICR9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN9 QEN3 | STIN9 QEN2 | STIN9 QEN1 | STIN9 QEN0 | STIN9 SMP1 | STIN9 SMP0 | STIN9 DR2 | STIN9 DR1 | STIN9 DR0 |
| SICR10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN10 QEN3 | STIN10 QEN2 | STIN10 QEN1 | STIN10 QEN0 | STIN10 SMP1 | STIN10 SMP0 | STIN10 DR2 | STIN10 DR1 | STIN10 DR0 |
| SICR11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN11 QEN3 | STIN11 QEN2 | STIN11 QEN1 | STIN11 QEN0 | STIN11 SMP1 | STIN11 SMP0 | STIN11 DR2 | STIN11 DR1 | STIN11 DR0 |
| SICR12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN12 QEN3 | STIN12 QEN2 | STIN12 QEN1 | STIN12 QEN0 | STIN12 SMP1 | STIN12 SMP0 | STIN12 DR2 | STIN12 DR1 | STIN12 DR0 |
| SICR13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN13 QEN3 | STIN13 QEN2 | STIN13 QEN1 | STIN13 QEN0 | STIN13 SMP1 | STIN13 SMP0 | STIN13 DR2 | STIN13 DR1 | STIN13 DR0 |
| SICR14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN14 QEN3 | STIN14 QEN2 | STIN14 QEN1 | STIN14 QEN0 | STIN14 SMP1 | STIN14 SMP0 | STIN14 DR2 | STIN14 DR1 | STIN14 DR0 |
| SICR15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN15 QEN3 | STIN15 QEN2 | STIN15 QEN1 | STIN15 QEN0 | STIN15 SMP1 | STIN15 SMP0 | STIN15 DR2 | STIN15 DR1 | STIN15 DR0 |

| Bit | Name | Description | | | | | | | | | | | | |
|-------------|---|---|-------------|----------------|-----|---|-----|------------|-----|------------|-----|------------|-----------|----------|
| 4 - 3 | STIN#SMP1 - 0 | Input Data Sampling Point Selection Bits: <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="width:20%;">STIN#SMP1-0</th> <th style="width:80%;">Sampling Point</th> </tr> </thead> <tbody> <tr> <td style="text-align:center;">00</td> <td style="text-align:center;">3/4 point</td> </tr> <tr> <td style="text-align:center;">01</td> <td style="text-align:center;">4/4 point</td> </tr> <tr> <td style="text-align:center;">10</td> <td style="text-align:center;">1/4 point</td> </tr> <tr> <td style="text-align:center;">11</td> <td style="text-align:center;">2/4 point</td> </tr> </tbody> </table> | STIN#SMP1-0 | Sampling Point | 00 | 3/4 point | 01 | 4/4 point | 10 | 1/4 point | 11 | 2/4 point | | |
| STIN#SMP1-0 | Sampling Point | | | | | | | | | | | | | |
| 00 | 3/4 point | | | | | | | | | | | | | |
| 01 | 4/4 point | | | | | | | | | | | | | |
| 10 | 1/4 point | | | | | | | | | | | | | |
| 11 | 2/4 point | | | | | | | | | | | | | |
| 2 - 0 | STIN#DR2 - 0 | Input Data Rate Selection Bits: <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="width:20%;">STIN#DR2-0</th> <th style="width:80%;">Data Rate</th> </tr> </thead> <tbody> <tr> <td style="text-align:center;">000</td> <td style="text-align:center;">Disabled - External pull-up or pull-down is required for ST-BUS input</td> </tr> <tr> <td style="text-align:center;">001</td> <td style="text-align:center;">2.048 Mb/s</td> </tr> <tr> <td style="text-align:center;">010</td> <td style="text-align:center;">4.096 Mb/s</td> </tr> <tr> <td style="text-align:center;">011</td> <td style="text-align:center;">8.192 Mb/s</td> </tr> <tr> <td style="text-align:center;">100 - 111</td> <td style="text-align:center;">Reserved</td> </tr> </tbody> </table> | STIN#DR2-0 | Data Rate | 000 | Disabled - External pull-up or pull-down is required for ST-BUS input | 001 | 2.048 Mb/s | 010 | 4.096 Mb/s | 011 | 8.192 Mb/s | 100 - 111 | Reserved |
| STIN#DR2-0 | Data Rate | | | | | | | | | | | | | |
| 000 | Disabled - External pull-up or pull-down is required for ST-BUS input | | | | | | | | | | | | | |
| 001 | 2.048 Mb/s | | | | | | | | | | | | | |
| 010 | 4.096 Mb/s | | | | | | | | | | | | | |
| 011 | 8.192 Mb/s | | | | | | | | | | | | | |
| 100 - 111 | Reserved | | | | | | | | | | | | | |

Note: # denotes input stream from 8 to 15

Table 21 - Stream Input Control Register 8 to 15 (SICR8 to SICR15) (continued)

External Read/Write Address: 101_H, 103_H, 105_H, 107_H, 109_H, 10B_H, 10D_H, 10F_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SIDR0 | 0 | 0 | 0 | 0 | 0 | 0 | STIN0 CD6 | STIN0 CD5 | STIN0 CD4 | STIN0 CD3 | STIN0 CD2 | STIN0 CD1 | STIN0 CD0 | STIN0 BD2 | STIN0 BD1 | STIN0 BD0 |
| SIDR1 | 0 | 0 | 0 | 0 | 0 | 0 | STIN1 CD6 | STIN1 CD5 | STIN1 CD4 | STIN1 CD3 | STIN1 CD2 | STIN1 CD1 | STIN1 CD0 | STIN1 BD2 | STIN1 BD1 | STIN1 BD0 |
| SIDR2 | 0 | 0 | 0 | 0 | 0 | 0 | STIN2 CD6 | STIN2 CD5 | STIN2 CD4 | STIN2 CD3 | STIN2 CD2 | STIN2 CD1 | STIN2 CD0 | STIN2 BD2 | STIN2 BD1 | STIN2 BD0 |
| SIDR3 | 0 | 0 | 0 | 0 | 0 | 0 | STIN3 CD6 | STIN3 CD5 | STIN3 CD4 | STIN3 CD3 | STIN3 CD2 | STIN3 CD1 | STIN3 CD0 | STIN3 BD2 | STIN3 BD1 | STIN3 BD0 |
| SIDR4 | 0 | 0 | 0 | 0 | 0 | 0 | STIN4 CD6 | STIN4 CD5 | STIN4 CD4 | STIN4 CD3 | STIN4 CD2 | STIN4 CD1 | STIN4 CD0 | STIN4 BD2 | STIN4 BD1 | STIN4 BD0 |
| SIDR5 | 0 | 0 | 0 | 0 | 0 | 0 | STIN5 CD6 | STIN5 CD5 | STIN5 CD4 | STIN5 CD3 | STIN5 CD2 | STIN5 CD1 | STIN5 CD0 | STIN5 BD2 | STIN5 BD1 | STIN5 BD0 |
| SIDR6 | 0 | 0 | 0 | 0 | 0 | 0 | STIN6 CD6 | STIN6 CD5 | STIN6 CD4 | STIN6 CD3 | STIN6 CD2 | STIN6 CD1 | STIN6 CD0 | STIN6 BD2 | STIN6 BD1 | STIN6 BD0 |
| SIDR7 | 0 | 0 | 0 | 0 | 0 | 0 | STIN7 CD6 | STIN7 CD5 | STIN7 CD4 | STIN7 CD3 | STIN7 CD2 | STIN7 CD1 | STIN7 CD0 | STIN7 BD2 | STIN7 BD1 | STIN7 BD0 |

| Bit | Name | Description |
|---------|--------------|--|
| 15 - 10 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. |
| 9 - 3 | STIN#CD6 - 0 | Input Stream# Channel Delay Bits: The binary value of these bits refers to the number of channels that the input stream will be delayed. This value should not exceed the maximum channel number of the stream. Zero means no delay. |
| 2 - 0 | STIN#BD2 - 0 | Input Stream# Bit Delay Bits: The binary value of these bits refers to the number of bits that the input stream will be delayed. This maximum value is 7. Zero means no delay. |

Note: # denotes input stream from 0 to 7

Table 22 - Stream Input Delay Register 0 to 7 (SIDR0 to SIDR7)

External Read/Write Address: 111_H, 113_H, 115_H, 117_H, 119_H, 11B_H, 11D_H, 11F_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SIDR8 | 0 | 0 | 0 | 0 | 0 | 0 | STIN8 CD6 | STIN8 CD5 | STIN8 CD4 | STIN8 CD3 | STIN8 CD2 | STIN8 CD1 | STIN8 CD0 | STIN8B BD2 | STIN8B BD1 | STIN8B BD0 |
| SIDR9 | 0 | 0 | 0 | 0 | 0 | 0 | STIN9 CD6 | STIN9 CD5 | STIN9 CD4 | STIN9 CD3 | STIN9 CD2 | STIN9 CD1 | STIN9 CD0 | STIN9B BD2 | STIN9B BD1 | STIN9B BD0 |
| SIDR10 | 0 | 0 | 0 | 0 | 0 | 0 | STIN10 CD6 | STIN10 CD5 | STIN10 CD4 | STIN10 CD3 | STIN10 CD2 | STIN10 CD1 | STIN10 CD0 | STIN10 BD2 | STIN10 BD1 | STIN10 BD0 |
| SIDR11 | 0 | 0 | 0 | 0 | 0 | 0 | STIN11 CD6 | STIN11 CD5 | STIN11 CD4 | STIN11 CD3 | STIN11 CD2 | STIN11 CD1 | STIN11 CD0 | STIN11 BD2 | STIN11 BD1 | STIN11 BD0 |
| SIDR12 | 0 | 0 | 0 | 0 | 0 | 0 | STIN12 CD6 | STIN12 CD5 | STIN12 CD4 | STIN12 CD3 | STIN12 CD2 | STIN12 CD1 | STIN12 CD0 | STIN12 BD2 | STIN12 BD1 | STIN12 BD0 |
| SIDR13 | 0 | 0 | 0 | 0 | 0 | 0 | STIN13 CD6 | STIN13 CD5 | STIN13 CD4 | STIN13 CD3 | STIN13 CD2 | STIN13 CD1 | STIN13 CD0 | STIN13 BD2 | STIN13 BD1 | STIN13 BD0 |
| SIDR14 | 0 | 0 | 0 | 0 | 0 | 0 | STIN14 CD6 | STIN14 CD5 | STIN14 CD4 | STIN14 CD3 | STIN14 CD2 | STIN14 CD1 | STIN14 CD0 | STIN14 BD2 | STIN14 BD1 | STIN14 BD0 |
| SIDR15 | 0 | 0 | 0 | 0 | 0 | 0 | STIN15 CD6 | STIN15 CD5 | STIN15 CD4 | STIN15 CD3 | STIN15 CD2 | STIN15 CD1 | STIN15 CD0 | STIN15 BD2 | STIN15 BD1 | STIN15 BD0 |

| Bit | Name | Description |
|---------|--------------|--|
| 15 - 10 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. |
| 9 - 3 | STIN#CD6 - 0 | Input Stream# Channel Delay Bits: The binary value of these bits refers to the number of channels that the input stream will be delayed. This value should not exceed the maximum channel number of the stream. Zero means no delay. |
| 2 - 0 | STIN#BD2 - 0 | Input Stream# Bit Delay Bits: The binary value of these bits refers to the number of bits that the input stream will be delayed. This maximum value is 7. Zero means no delay. |

Note: # denotes input stream from 8 to 15

Table 23 - Stream Input Delay Register 8 to 15 (SIDR8 to SIDR15)

External Read/Write Address: 200_H, 202_H, 204_H, 206_H, 208_H, 20A_H, 20C_H, 20E_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|---|---|---|--------------|--------------|--------------|--------------|-------------|-------------|-------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOCR0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ0 AC | STOHZ0 A2 | STOHZ0 A1 | STOHZ0 A0 | STO0 DR2 | STO0 DR1 | STO0 DR0 |
| SOCR1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ1 AC | STOHZ1 A2 | STOHZ1 A1 | STOHZ1 A0 | STO1 DR2 | STO1 DR1 | STO1 DR0 |
| SOCR2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ2 AC | STOHZ2 A2 | STOHZ2 A1 | STOHZ2 A0 | STO2 DR2 | STO2 DR1 | STO2 DR0 |
| SOCR3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ3 AC | STOHZ3 A2 | STOHZ3 A1 | STOHZ3 A0 | STO3 DR2 | STO3 DR1 | STO3 DR0 |
| SOCR4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ4 AC | STOHZ4 A2 | STOHZ4 A1 | STOHZ4 A0 | STO4 DR2 | STO4 DR1 | STO4 DR0 |
| SOCR5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ5 AC | STOHZ5 A2 | STOHZ5 A1 | STOHZ5 A0 | STO5 DR2 | STO5 DR1 | STO5 DR0 |
| SOCR6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ6 AC | STOHZ6 A2 | STOHZ6 A1 | STOHZ6 A0 | STO6 DR2 | STO6 DR1 | STO6 DR0 |
| SOCR7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ7 AC | STOHZ7 A2 | STOHZ7 A1 | STOHZ7 A0 | STO7 DR2 | STO7 DR1 | STO7 DR0 |

| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | | |
|------------|--|--|------------|--|--|------------------------------|--------|------------|-----|------------|---------|------------|-----------|----------|-----|---------|---------|-----|---------|---------|---------|----------|----------|
| 15 - 7 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. | | | | | | | | | | | | | | | | | | | | | |
| 6 | STOHZ#AC | STOHZ Advancement Control. When this bit is low, the advancement unit is 15.2ns. When this bit is high, the advancement unit is 1/4 bit. | | | | | | | | | | | | | | | | | | | | | |
| 5 - 3 | STOHZ#A2 - 0 | STOHZ Additional Advancement Bits: <table border="1" style="margin: 5px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>STOHZ#A2-0</th> <th>Additional Advancement (STOHZ#AC = 0)</th> <th>Additional Advancement (STOHZ#AC = 1)</th> </tr> </thead> <tbody> <tr><td>000</td><td>0.0 ns</td><td>0 bit</td></tr> <tr><td>001</td><td>15.2 ns</td><td>1/4 bit</td></tr> <tr><td>010</td><td>30.5 ns</td><td>1/2 bit</td></tr> <tr><td>011</td><td>45.7 ns</td><td>3/4 bit</td></tr> <tr><td>100</td><td>61.0 ns</td><td>4/4 bit</td></tr> <tr><td>101-111</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> | STOHZ#A2-0 | Additional Advancement (STOHZ#AC = 0) | Additional Advancement (STOHZ#AC = 1) | 000 | 0.0 ns | 0 bit | 001 | 15.2 ns | 1/4 bit | 010 | 30.5 ns | 1/2 bit | 011 | 45.7 ns | 3/4 bit | 100 | 61.0 ns | 4/4 bit | 101-111 | Reserved | Reserved |
| STOHZ#A2-0 | Additional Advancement (STOHZ#AC = 0) | Additional Advancement (STOHZ#AC = 1) | | | | | | | | | | | | | | | | | | | | | |
| 000 | 0.0 ns | 0 bit | | | | | | | | | | | | | | | | | | | | | |
| 001 | 15.2 ns | 1/4 bit | | | | | | | | | | | | | | | | | | | | | |
| 010 | 30.5 ns | 1/2 bit | | | | | | | | | | | | | | | | | | | | | |
| 011 | 45.7 ns | 3/4 bit | | | | | | | | | | | | | | | | | | | | | |
| 100 | 61.0 ns | 4/4 bit | | | | | | | | | | | | | | | | | | | | | |
| 101-111 | Reserved | Reserved | | | | | | | | | | | | | | | | | | | | | |
| 2 - 0 | STO#DR2 - 0 | Output Data Rate Selection Bits: <table border="1" style="margin: 5px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>STO#DR2-0</th> <th>Output Data Rate</th> </tr> </thead> <tbody> <tr><td>000</td><td>STo HiZ STOHZ driven high</td></tr> <tr><td>001</td><td>2.048 Mb/s</td></tr> <tr><td>010</td><td>4.096 Mb/s</td></tr> <tr><td>011</td><td>8.192 Mb/s</td></tr> <tr><td>100 - 111</td><td>Reserved</td></tr> </tbody> </table> | STO#DR2-0 | Output Data Rate | 000 | STo HiZ STOHZ driven high | 001 | 2.048 Mb/s | 010 | 4.096 Mb/s | 011 | 8.192 Mb/s | 100 - 111 | Reserved | | | | | | | | | |
| STO#DR2-0 | Output Data Rate | | | | | | | | | | | | | | | | | | | | | | |
| 000 | STo HiZ STOHZ driven high | | | | | | | | | | | | | | | | | | | | | | |
| 001 | 2.048 Mb/s | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 4.096 Mb/s | | | | | | | | | | | | | | | | | | | | | | |
| 011 | 8.192 Mb/s | | | | | | | | | | | | | | | | | | | | | | |
| 100 - 111 | Reserved | | | | | | | | | | | | | | | | | | | | | | |

Note: # denotes input stream from 0 to 7

Table 24 - Stream Output Control Register 0 to 7 (SOCR0 to SOCR7)

External Read/Write Address: 210_H, 212_H, 214_H, 216_H, 218_H, 21A_H, 21C_H, 21E_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|---|---|---|---|---------------|---------------|---------------|---------------|--------------|--------------|--------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| SOCR8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ8 AC | STOHZ8 A2 | STOHZ8 A1 | STOHZ8 A0 | STO8 DR2 | STO8 DR1 | STO8 DR0 |
| SOCR9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ9 AC | STOHZ9 A2 | STOHZ9 A1 | STOHZ9 A0 | STO9 DR2 | STO9 DR1 | STO9 DR0 |
| SOCR10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ10 AC | STOHZ10 A2 | STOHZ10 A1 | STOHZ10 A0 | STO10 DR2 | STO10 DR1 | STO10 DR0 |
| SOCR11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ11 AC | STOHZ11 A2 | STOHZ11 A1 | STOHZ11 A0 | STO11 DR2 | STO11 DR1 | STO11 DR0 |
| SOCR12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ12 AC | STOHZ12 A2 | STOHZ12 A1 | STOHZ12 A0 | STO12 DR2 | STO12 DR1 | STO12 DR0 |
| SOCR13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ13 AC | STOHZ13 A2 | STOHZ13 A1 | STOHZ13 A0 | STO13 DR2 | STO13 DR1 | STO13 DR0 |
| SOCR14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ14 AC | STOHZ14 A2 | STOHZ14 A1 | STOHZ14 A0 | STO14 DR2 | STO14 DR1 | STO14 DR0 |
| SOCR15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STOHZ15 AC | STOHZ15 A2 | STOHZ15 A1 | STOHZ15 A0 | STO15 DR2 | STO15 DR1 | STO15 DR0 |

| Bit | Name | Description | | | | | | | | | | | | | | | | | | | | | |
|------------|---------------------------------------|--|------------|---------------------------------------|---------------------------------------|------------------------------|--------|------------|-----|------------|---------|------------|-----------|----------|-----|---------|---------|-----|---------|---------|---------|----------|----------|
| 15 - 7 | Unused | Reserved. In normal functional mode, these bits MUST be set to zero. | | | | | | | | | | | | | | | | | | | | | |
| 6 | STOHZ#AC | STOHZ Advancement Control. When this bit is low, the advancement unit is 15.2 ns. When this bit is high, the advancement unit is 1/4 bit. | | | | | | | | | | | | | | | | | | | | | |
| 5 - 3 | STOHZ#A2 - 0 | STOHZ Additional Advancement Bits: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>STOHZ#A2-0</th> <th>Additional Advancement (STOHZ#AC = 0)</th> <th>Additional Advancement (STOHZ#AC = 1)</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0.0 ns</td> <td>0 bit</td> </tr> <tr> <td>001</td> <td>15.2 ns</td> <td>1/4 bit</td> </tr> <tr> <td>010</td> <td>30.5 ns</td> <td>1/2 bit</td> </tr> <tr> <td>011</td> <td>45.7 ns</td> <td>3/4 bit</td> </tr> <tr> <td>100</td> <td>61.0 ns</td> <td>4/4 bit</td> </tr> <tr> <td>101-111</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> | STOHZ#A2-0 | Additional Advancement (STOHZ#AC = 0) | Additional Advancement (STOHZ#AC = 1) | 000 | 0.0 ns | 0 bit | 001 | 15.2 ns | 1/4 bit | 010 | 30.5 ns | 1/2 bit | 011 | 45.7 ns | 3/4 bit | 100 | 61.0 ns | 4/4 bit | 101-111 | Reserved | Reserved |
| STOHZ#A2-0 | Additional Advancement (STOHZ#AC = 0) | Additional Advancement (STOHZ#AC = 1) | | | | | | | | | | | | | | | | | | | | | |
| 000 | 0.0 ns | 0 bit | | | | | | | | | | | | | | | | | | | | | |
| 001 | 15.2 ns | 1/4 bit | | | | | | | | | | | | | | | | | | | | | |
| 010 | 30.5 ns | 1/2 bit | | | | | | | | | | | | | | | | | | | | | |
| 011 | 45.7 ns | 3/4 bit | | | | | | | | | | | | | | | | | | | | | |
| 100 | 61.0 ns | 4/4 bit | | | | | | | | | | | | | | | | | | | | | |
| 101-111 | Reserved | Reserved | | | | | | | | | | | | | | | | | | | | | |
| 2 - 0 | STO#DR2 - 0 | Output Data Rate Selection Bits: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>STO#DR2-0</th> <th>Output Data Rate</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>STo HiZ STOHZ driven high</td> </tr> <tr> <td>001</td> <td>2.048 Mb/s</td> </tr> <tr> <td>010</td> <td>4.096 Mb/s</td> </tr> <tr> <td>011</td> <td>8.192 Mb/s</td> </tr> <tr> <td>100 - 111</td> <td>Reserved</td> </tr> </tbody> </table> | STO#DR2-0 | Output Data Rate | 000 | STo HiZ STOHZ driven high | 001 | 2.048 Mb/s | 010 | 4.096 Mb/s | 011 | 8.192 Mb/s | 100 - 111 | Reserved | | | | | | | | | |
| STO#DR2-0 | Output Data Rate | | | | | | | | | | | | | | | | | | | | | | |
| 000 | STo HiZ STOHZ driven high | | | | | | | | | | | | | | | | | | | | | | |
| 001 | 2.048 Mb/s | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 4.096 Mb/s | | | | | | | | | | | | | | | | | | | | | | |
| 011 | 8.192 Mb/s | | | | | | | | | | | | | | | | | | | | | | |
| 100 - 111 | Reserved | | | | | | | | | | | | | | | | | | | | | | |

Note: # denotes input stream from 8 to 15

Table 25 - Stream Output Control Register 8 to 15 (SOCR8 to SOCR15)

External Read/Write Address: 201_H, 203_H, 205_H, 207_H, 209_H, 20B_H, 20D_H, 20F_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOOR0 | 0 | 0 | 0 | 0 | STO0 CD6 | STO0 CD5 | STO0 CD4 | STO0 CD3 | STO0 CD2 | STO0 CD1 | STO0 CD0 | STO0 BD2 | STO0 BD1 | STO0 BD0 | STO0 FA1 | STO0 FA0 |
| SOOR1 | 0 | 0 | 0 | 0 | STO1 CD6 | STO1 CD5 | STO1 CD4 | STO1 CD3 | STO1 CD2 | STO1 CD1 | STO1 CD0 | STO1 BD2 | STO1 BD1 | STO1 BD0 | STO1 FA1 | STO1 FA0 |
| SOOR2 | 0 | 0 | 0 | 0 | STO2 CD6 | STO2 CD5 | STO2 CD4 | STO2 CD3 | STO2 CD2 | STO2 CD1 | STO2 CD0 | STO2 BD2 | STO2 BD1 | STO2 BD0 | STO2 FA1 | STO2 FA0 |
| SOOR3 | 0 | 0 | 0 | 0 | STO3 CD6 | STO3 CD5 | STO3 CD4 | STO3 CD3 | STO3 CD2 | STO3 CD1 | STO3 CD0 | STO3 BD2 | STO3 BD1 | STO3 BD0 | STO3 FA1 | STO3 FA0 |
| SOOR4 | 0 | 0 | 0 | 0 | STO4 CD6 | STO4 CD5 | STO4 CD4 | STO4 CD3 | STO4 CD2 | STO4 CD1 | STO4 CD0 | STO4 BD2 | STO4 BD1 | STO4 BD0 | STO4 FA1 | STO4 FA0 |
| SOOR5 | 0 | 0 | 0 | 0 | STO5 CD6 | STO5 CD5 | STO5 CD4 | STO5 CD3 | STO5 CD2 | STO5 CD1 | STO5 CD0 | STO5 BD2 | STO5 BD1 | STO5 BD0 | STO5 FA1 | STO5 FA0 |
| SOOR6 | 0 | 0 | 0 | 0 | STO6 CD6 | STO6 CD5 | STO6 CD4 | STO6 CD3 | STO6 CD2 | STO6 CD1 | STO6 CD0 | STO6 BD2 | STO6 BD1 | STO6 BD0 | STO6 FA1 | STO6 FA0 |
| SOOR7 | 0 | 0 | 0 | 0 | STO7 CD6 | STO7 CD5 | STO7 CD4 | STO7 CD3 | STO7 CD2 | STO7 CD1 | STO7 CD0 | STO7 BD2 | STO7 BD1 | STO7 BD0 | STO7 FA1 | STO7 FA0 |

| Bit | Name | Description | | | | | | | | | | |
|-----------|-------------|---|-----------|-------------|----|---|----|---------|----|---------|----|---------|
| 15 - 12 | Unused | Reserved. | | | | | | | | | | |
| 11 - 5 | STO#CD6-0 | Output Stream# Channel Delay Bits: The binary value of these bits refers to the number of channels that the output stream is to be delayed. This value should not exceed the maximum channel number of the stream. Zero means no delay. | | | | | | | | | | |
| 4 - 2 | STO#BD2-0 | Output Stream# Bit Delay Selection Bits: The binary value of these bits refers to the number of bits that the output stream is to be delayed. The maximum value is 7. Zero means no delay. | | | | | | | | | | |
| 1 - 0 | STO#FA1-0 | Output Stream# Fractional Advancement Bits <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>STO#FA1-0</th> <th>Advanced By</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0</td> </tr> <tr> <td>01</td> <td>1/4 bit</td> </tr> <tr> <td>10</td> <td>2/4 bit</td> </tr> <tr> <td>11</td> <td>3/4 bit</td> </tr> </tbody> </table> | STO#FA1-0 | Advanced By | 00 | 0 | 01 | 1/4 bit | 10 | 2/4 bit | 11 | 3/4 bit |
| STO#FA1-0 | Advanced By | | | | | | | | | | | |
| 00 | 0 | | | | | | | | | | | |
| 01 | 1/4 bit | | | | | | | | | | | |
| 10 | 2/4 bit | | | | | | | | | | | |
| 11 | 3/4 bit | | | | | | | | | | | |

Note: # denotes input stream from 0 to 7

Table 26 - Stream Output Offset Register 0 to 7 (SOOR0 to SOOR7)

External Read/Write Address: 211_H, 213_H, 215_H, 217_H, 219_H, 21B_H, 21D_H, 21F_H,
 Reset Value: 0000_H

| | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|--------------|--------------|--------------|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOOR8 | 0 | 0 | 0 | 0 | STO8C D6 | STO8 CD5 | STO8 CD4 | STO8 CD3 | STO8 CD2 | STO8 CD1 | STO8 CD0 | STO8B BD2 | STO8 BD1 | STO8 BD0 | STO8 FA1 | STO8 FA0 |
| SOOR9 | 0 | 0 | 0 | 0 | STO9C D6 | STO9 CD5 | STO9 CD4 | STO9 CD3 | STO9 CD2 | STO9 CD1 | STO9 CD0 | STO9B BD2 | STO9 BD1 | STO9 BD0 | STO9 FA1 | STO9 FA0 |
| SOOR10 | 0 | 0 | 0 | 0 | STO10C D6 | STO10 CD5 | STO10 CD4 | STO10 CD3 | STO10 CD2 | STO10 CD1 | STO10 CD0 | STO10B BD2 | STO10 BD1 | STO10 BD0 | STO10 FA1 | STO10 FA0 |
| SOOR11 | 0 | 0 | 0 | 0 | STO11C D6 | STO11 CD5 | STO11 CD4 | STO11 CD3 | STO11 CD2 | STO11 CD1 | STO11 CD0 | STO11B BD2 | STO11 BD1 | STO11 BD0 | STO11 FA1 | STO11 FA0 |
| SOOR12 | 0 | 0 | 0 | 0 | STO12C D6 | STO12 CD5 | STO12 CD4 | STO12 CD3 | STO12 CD2 | STO12 CD1 | STO12 CD0 | STO12B BD2 | STO12 BD1 | STO12 BD0 | STO12 FA1 | STO12 FA0 |
| SOOR13 | 0 | 0 | 0 | 0 | STO13C D6 | STO13 CD5 | STO13 CD4 | STO13 CD3 | STO13 CD2 | STO13 CD1 | STO13 CD0 | STO13B BD2 | STO13 BD1 | STO13 BD0 | STO13 FA1 | STO13 FA0 |
| SOOR14 | 0 | 0 | 0 | 0 | STO14C D6 | STO14 CD5 | STO14 CD4 | STO14 CD3 | STO14 CD2 | STO14 CD1 | STO14 CD0 | STO14B BD2 | STO14 BD1 | STO14 BD0 | STO14 FA1 | STO14 FA0 |
| SOOR15 | 0 | 0 | 0 | 0 | STO15C D6 | STO15 CD5 | STO15 CD4 | STO15 CD3 | STO15 CD2 | STO15 CD1 | STO15 CD0 | STO15B BD2 | STO15 BD1 | STO15 BD0 | STO15 FA1 | STO15 FA0 |

| Bit | Name | Description | | | | | | | | | | |
|-----------|-------------|---|-----------|-------------|----|---|----|---------|----|---------|----|---------|
| 15 - 12 | Unused | Reserved. | | | | | | | | | | |
| 11 - 5 | STO#CD6-0 | Output Stream# Channel Delay Bits: The binary value of these bits refers to the number of channels that the output stream is to be delayed. This value should not exceed the maximum channel number of the stream. Zero means no delay. | | | | | | | | | | |
| 4 - 2 | STO#BD2-0 | Output Stream# Bit Delay Selection Bits: The binary value of these bits refers to the number of bits that the output stream is to be delayed. The maximum value is 7. Zero means no delay. | | | | | | | | | | |
| 1 - 0 | STO#FA1-0 | Output Stream# Fractional Advancement Bits <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>STO#FA1-0</th> <th>Advanced By</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0</td> </tr> <tr> <td>01</td> <td>1/4 bit</td> </tr> <tr> <td>10</td> <td>2/4 bit</td> </tr> <tr> <td>11</td> <td>3/4 bit</td> </tr> </tbody> </table> | STO#FA1-0 | Advanced By | 00 | 0 | 01 | 1/4 bit | 10 | 2/4 bit | 11 | 3/4 bit |
| STO#FA1-0 | Advanced By | | | | | | | | | | | |
| 00 | 0 | | | | | | | | | | | |
| 01 | 1/4 bit | | | | | | | | | | | |
| 10 | 2/4 bit | | | | | | | | | | | |
| 11 | 3/4 bit | | | | | | | | | | | |

Note: # denotes input stream from 8 to 15

Table 27 - Stream Output Offset Register 8 to 15 (SOOR8 to SOOR15)

7.0 Memory Address Mappings

When A11 is high, the data or the connection memory can be accessed by the microprocessor port. The Bit 0 to Bit 2 in the control register determine the access to the data or connection memory

| MSB (Note 1) | Stream Address (ST. 0-15) | | | | | Channel Address (Ch 0-127) | | | | | | | |
|-----------------|------------------------------|----|----|----|-----------|-------------------------------|----|----|----|----|----|----|-----------------|
| | A10 | A9 | A8 | A7 | Stream # | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Channel # |
| 1 | 0 | 0 | 0 | 0 | Stream 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Ch 0 |
| 1 | 0 | 0 | 0 | 1 | Stream 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Ch 1 |
| 1 | 0 | 0 | 1 | 0 | Stream 2 | . | . | . | . | . | . | . | . |
| 1 | 0 | 0 | 1 | 1 | Stream 3 | . | . | . | . | . | . | . | . |
| 1 | 0 | 1 | 0 | 0 | Stream 4 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | Ch 30 |
| 1 | 0 | 1 | 0 | 1 | Stream 5 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Ch 31 (Note 2) |
| 1 | 0 | 1 | 1 | 0 | Stream 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Ch 32 |
| 1 | 0 | 1 | 1 | 1 | Stream 7 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Ch 33 |
| 1 | 0 | 1 | 0 | 0 | Stream 8 | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | 0 | 1 | 1 | 1 | 1 | 1 | 0 | Ch 62 |
| . | . | . | . | . | . | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Ch 63 (Note 3) |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 0 | Stream 14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Ch 126 |
| 1 | 1 | 1 | 1 | 1 | Stream 15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Ch 127 (Note 4) |

Notes:
 1. MSB of address must be high for access to data and connection memory positions. MSB must be low for access to registers.
 2. Channels 0 to 31 are used when serial stream is at 2.048 Mb/s.
 3. Channels 0 to 63 are used when serial stream is at 4.096 Mb/s.
 4. Channels 0 to 127 are used when serial stream is at 8.192 Mb/s.

Table 28 - Address Map for Memory Locations (512 x 512 DX, MSB of address = 1)

8.0 Connection Memory Bit Assignment

When the CMM bit (Bit0) is zero, the connection is in normal switching mode. When the CMM bit is one, the connection memory is in special transmission mode.

| | | | | | | | | | | | |
|--|------|------|------|------|------|------|------|------|------|------|---------------|
| 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | |
| SSA3 | SSA2 | SSA1 | SSA0 | SCA6 | SCA5 | SCA4 | SCA3 | SCA2 | SCA1 | SCA0 | CMM =0 |

| Bit | Name | Description |
|--------|--------|---|
| 11 - 8 | SSA3-0 | Source Stream Address. The binary value of these 4 bits represents the input stream number. |
| 7 - 1 | SCA6-0 | Source Channel Address. The binary value of these 7 bits represents the input channel number. |
| 0 | CMM=0 | Connection Memory Mode = 0. If this bit is set low, the connection memory is in normal switching mode. Bit 1 to 11 represent the source stream number and channel number. |

Table 29 - Connection Memory Bit Assignment when the CMM bit = 0

| | | | | | | | | | | | |
|--|------|------|------|------|------|------|------|------|------|------|---------------|
| 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | |
| 0 | MSG7 | MSG6 | MSG5 | MSG4 | MSG3 | MSG2 | MSG1 | MSG0 | PCC1 | PCC0 | CMM =1 |

| Bit | Name | Description | | | | | | | | | | | | | | | |
|--------|--------|---|-----|------|--------|---|---|----------------------|---|---|--------------|---|---|---------------|---|---|----------|
| 11 | Unused | Reserved. | | | | | | | | | | | | | | | |
| 10 - 3 | MSG7-0 | Message Data Bits: 8-bit data for the message mode. | | | | | | | | | | | | | | | |
| 2 - 1 | PCC1-0 | Per-Channel Control Bits: These two bits control outputs. <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>PCC</th> <th>PCC0</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Per Channel Tristate</td> </tr> <tr> <td>0</td> <td>1</td> <td>Message Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>BER Test Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table> | PCC | PCC0 | Output | 0 | 0 | Per Channel Tristate | 0 | 1 | Message Mode | 1 | 0 | BER Test Mode | 1 | 1 | Reserved |
| PCC | PCC0 | Output | | | | | | | | | | | | | | | |
| 0 | 0 | Per Channel Tristate | | | | | | | | | | | | | | | |
| 0 | 1 | Message Mode | | | | | | | | | | | | | | | |
| 1 | 0 | BER Test Mode | | | | | | | | | | | | | | | |
| 1 | 1 | Reserved | | | | | | | | | | | | | | | |
| 0 | CMM=1 | Connection Memory Mode = 1. If this bit is set high, the connection memory is in the per-channel control mode which is per-channel tristate, per-channel message mode or per-channel BER mode. | | | | | | | | | | | | | | | |

Table 30 - Connection Memory Bits Assignment when the CMM bit = 1

Absolute Maximum Ratings*

| | Parameter | Symbol | Min. | Max | Units |
|---|---------------------------------------|-------------|------|----------------|-------|
| 1 | I/O Supply Voltage | V_{DD} | -0.5 | 5.0 | V |
| 2 | Input Voltage | V_{I_3V} | -0.5 | $V_{DD} + 0.5$ | V |
| 3 | Input Voltage (5 V tolerant inputs) | V_{I_5V} | -0.5 | 7.0 | V |
| 4 | Continuous Current at digital outputs | I_o | | 15 | mA |
| 5 | Package power dissipation | P_D | | 0.75 | W |
| 6 | Storage temperature | T_S | - 55 | +125 | °C |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ. [‡] | Max | Units |
|---|--------------------------------------|-------------|------|-------------------|----------|-------|
| 1 | Operating Temperature | T_{OP} | -40 | 25 | +85 | °C |
| 2 | Positive Supply | V_{DD} | 3.0 | 3.3 | 3.6 | V |
| 3 | Input Voltage | V_I | 0 | | V_{DD} | V |
| 4 | Input Voltage on 5 V Tolerant Inputs | V_{I_5V} | 0 | | 5.5 | V |

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics[†] - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ. [‡] | Max | Units | Test Conditions |
|----|---|----------------------|------|-------------------|--------|--------------------|---|
| 1 | Supply Current | I_{DD} | | | 250 | mA | Output unloaded |
| 2 | Input High Voltage | V_{IH} | 2.0 | | | V | |
| 3 | Input Low Voltage | V_{IL} | | | 0.8 | V | |
| 4 | Input Leakage (input pins) Input Leakage (bi-directional pins) | I_{IL} I_{BL} | | | 5 5 | μ A μ A | $0 \leq V_{IN} \leq V_{DD_IO}$ See Note 1 |
| 5 | Weak Pullup Current | I_{PU} | | -33 | | μ A | Input at 0 V |
| 6 | Weak Pulldown Current | I_{PD} | | 33 | | μ A | Input at V_{DD_IO} |
| 7 | Input Pin Capacitance | C_I | | 3 | | pF | |
| 8 | Output High Voltage | V_{OH} | 2.4 | | | V | $I_{OH} = 10\text{mA}$ |
| 9 | Output Low Voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 10\text{mA}$ |
| 10 | Output High Impedance Leakage | I_{OZ} | | | 5 | μ A | $0 < V < V_{DD}$ |
| 11 | Output Pin Capacitance | C_O | | 5 | 10 | pF | |

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

AC Electrical Characteristics[†] - Timing Parameter Measurement Voltage Levels

| | Characteristics | Sym. | Level | Units | Conditions |
|---|----------------------------------|----------|-----------------|-------|------------|
| 1 | CMOS Threshold | V_{CT} | $0.5V_{DD_IO}$ | V | |
| 2 | Rise/Fall Threshold Voltage High | V_{HM} | $0.7V_{DD_IO}$ | V | |
| 3 | Rise/Fall Threshold Voltage Low | V_{LM} | $0.3V_{DD_IO}$ | V | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics[†] - \overline{FPI} and \overline{CKi} Timing when CKIN2 to 0 bits = 000

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|----------------------|------|-------------------|------|-------|-------|
| 1 | \overline{FPI} Input Frame Pulse Width | t_{FPIW} | 40 | 61 | 115 | ns | |
| 2 | \overline{FPI} Input Frame Pulse Setup Time | $t_{FPI S}$ | 20 | | 40 | ns | |
| 3 | \overline{FPI} Input Frame Pulse Hold Time | $t_{FPI H}$ | 20 | | 40 | ns | |
| 4 | \overline{CKi} Input Clock Period | t_{CKIP} | 55 | 61 | 67 | ns | |
| 5 | \overline{CKi} Input Clock High Time | t_{CKIH} | 27 | | 33 | ns | |
| 6 | \overline{CKi} Input Clock Low Time | t_{CKIL} | 27 | | 33 | ns | |
| 7 | \overline{CKi} Input Clock Rise/Fall Time | t_{rCKi}, t_{fCKi} | 0 | | 3 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - \overline{FPI} and \overline{CKi} Timing when CKIN2 to 0 bits = 001

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|----------------------|------|-------------------|------|-------|-------|
| 1 | \overline{FPI} Input Frame Pulse Width | t_{FPIW} | 90 | 122 | 220 | ns | |
| 2 | \overline{FPI} Input Frame Pulse Setup Time | $t_{FPI S}$ | 45 | | 90 | ns | |
| 3 | \overline{FPI} Input Frame Pulse Hold Time | $t_{FPI H}$ | 45 | | 90 | ns | |
| 4 | \overline{CKi} Input Clock Period | t_{CKIP} | 110 | 122 | 135 | ns | |
| 5 | \overline{CKi} Input Clock High Time | t_{CKIH} | 63 | | 69 | ns | |
| 6 | \overline{CKi} Input Clock Low Time | t_{CKIL} | 63 | | 69 | ns | |
| 7 | \overline{CKi} Input Clock Rise/Fall Time | t_{rCKi}, t_{fCKi} | 0 | | 3 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - \overline{FPI} and \overline{CKi} Timing when CKIN2 to 0 bits = 010

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|----------------------|------|-------------------|------|-------|-------|
| 1 | \overline{FPI} Input Frame Pulse Width | t_{FPIW} | 90 | 244 | 420 | ns | |
| 2 | \overline{FPI} Input Frame Pulse Setup Time | $t_{FPI S}$ | 110 | | 135 | ns | |
| 3 | \overline{FPI} Input Frame Pulse Hold Time | $t_{FPI H}$ | 120 | | 145 | ns | |
| 4 | \overline{CKi} Input Clock Period | t_{CKIP} | 220 | 244 | 270 | ns | |
| 5 | \overline{CKi} Input Clock High Time | t_{CKIH} | 110 | | 135 | ns | |
| 6 | \overline{CKi} Input Clock Low Time | t_{CKIL} | 110 | | 135 | ns | |
| 7 | \overline{CKi} Input Clock Rise/Fall Time | t_{rCKi}, t_{fCKi} | 0 | | 3 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

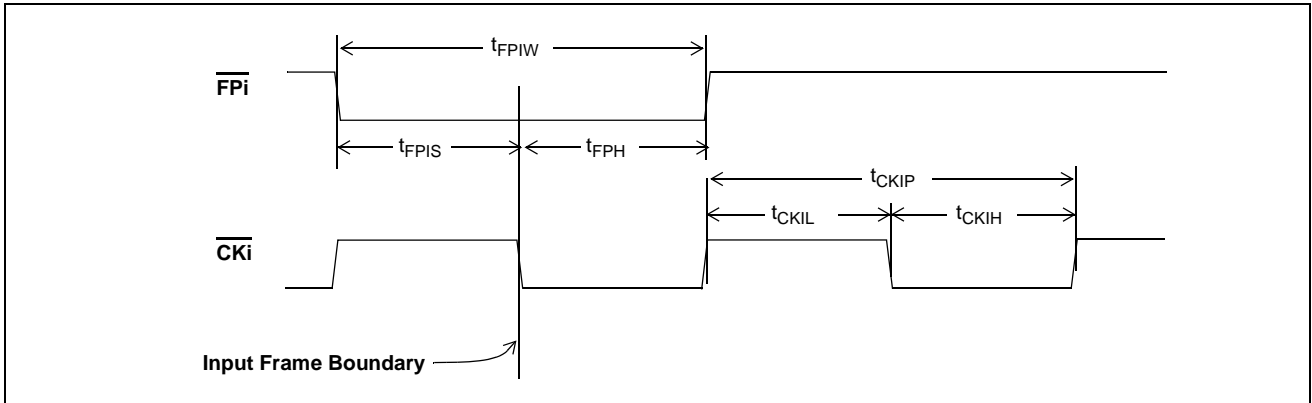


Figure 25 - Frame Pulse Input and Clock Input Timing Diagram

AC Electrical Characteristics[†] - Frame Boundary Timing with Input Clock Cycle-to-cycle Variation

| | Characteristic | Sym. | Min. | Typ [‡] | Max. | Units | Notes |
|---|--|------------------|------|------------------|------|-------|-------|
| 1 | CKi Input Clock cycle-to-cycle variation | t _{CKV} | 0 | | 50 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

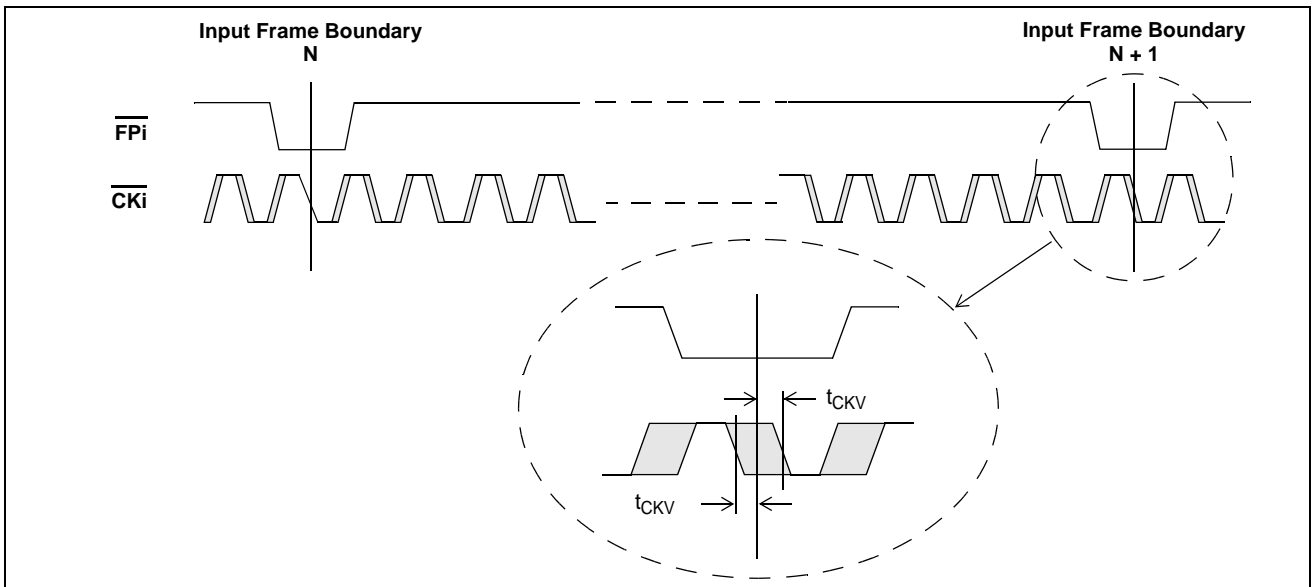


Figure 26 - Frame Boundary Timing with Input Clock (cycle-to-cycle) Variation

AC Electrical Characteristics[†] - Frame Boundary Timing with Input Frame Pulse Cycle-to-cycle Variation

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|--|-----------|------|-------------------|------|-------|-------|
| 1 | FPI Input Frame Pulse cycle-to-cycle variation | t_{FPV} | 0 | | 50 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

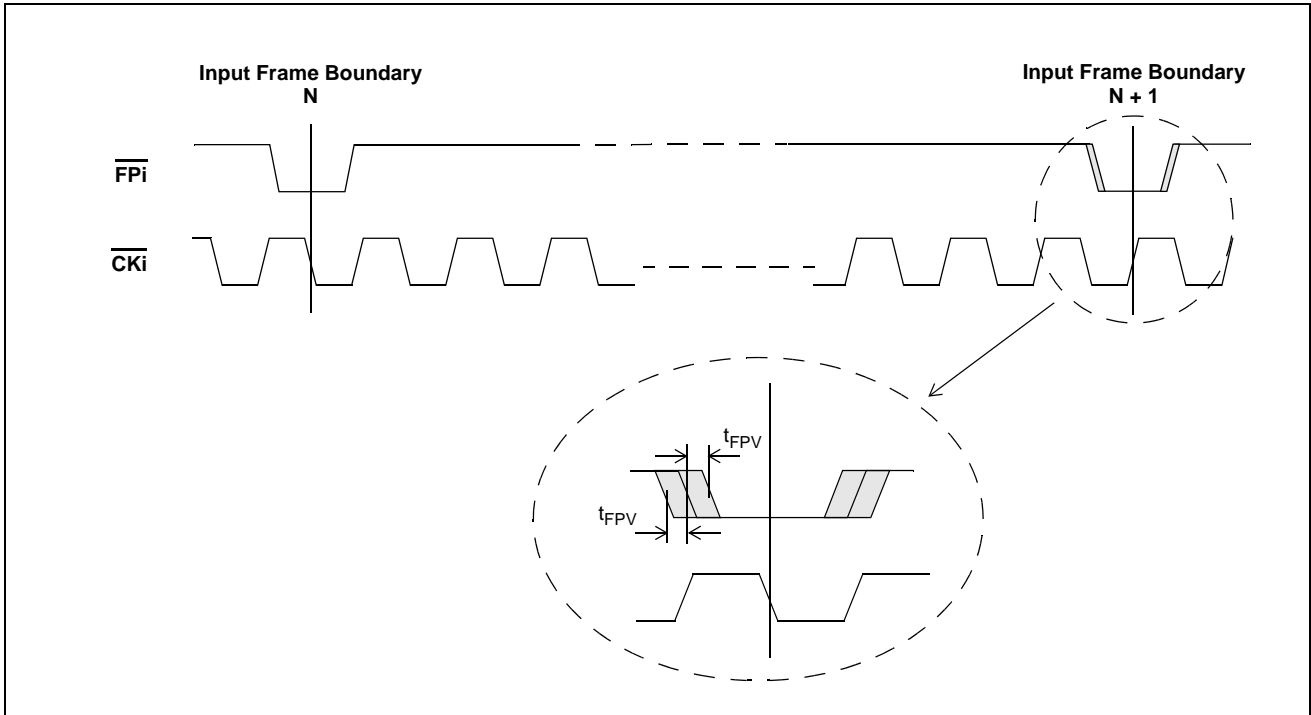


Figure 27 - Frame Boundary Timing with Input Frame Pulse (cycle-to-cycle) Variation

AC Electrical Characteristics - Input and Output Frame Boundary Alignment

| | Characteristic | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|-------------------------------|------------|------|------|------|-------|---|
| 2 | Input and Output Frame Offset | t_{FBOS} | 1 | | 18 | ns | Measured when there is no jitter on the CKi and FPI inputs. |

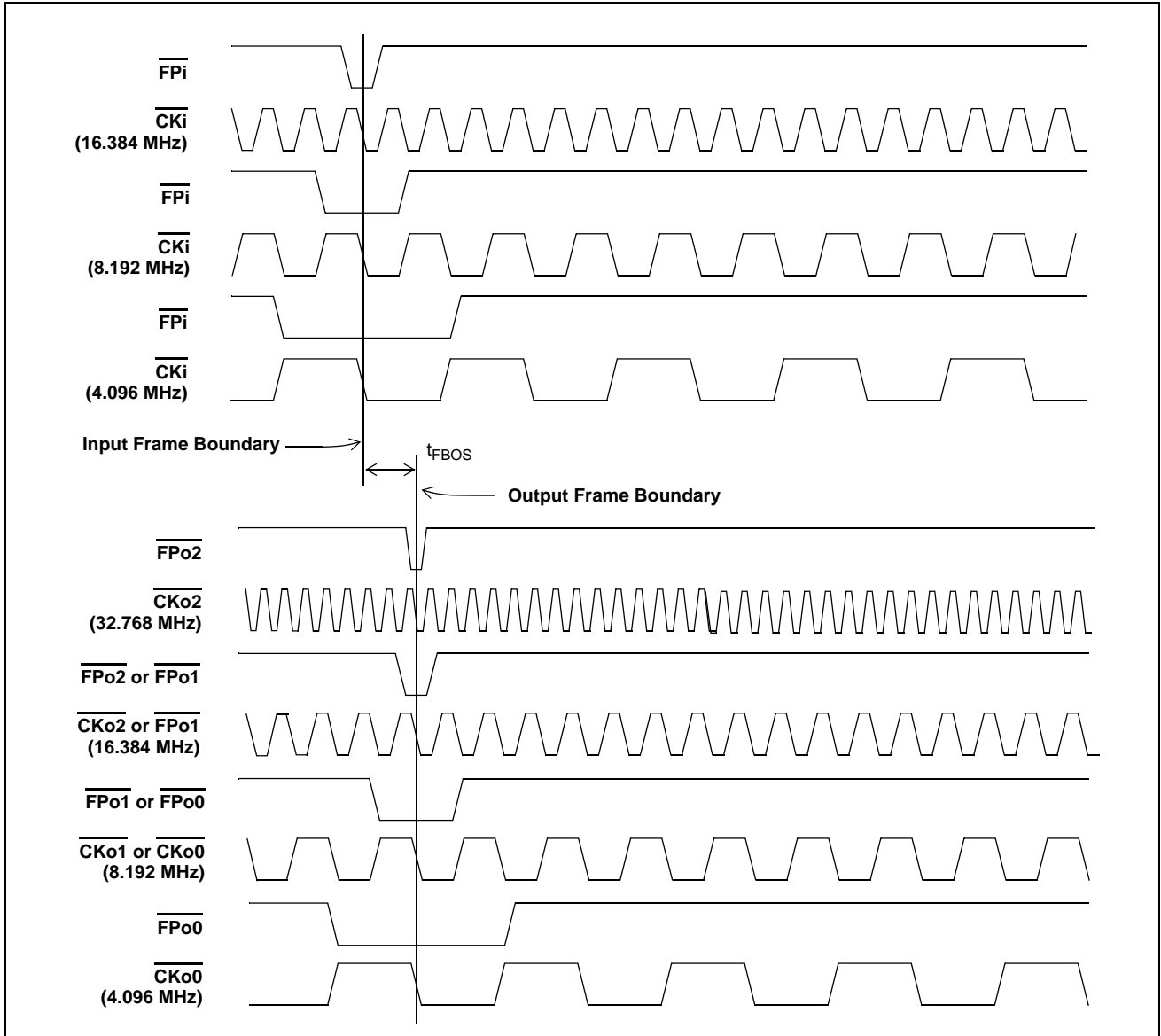


Figure 28 - Input and Output Frame Boundary Offset

AC Electrical Characteristics[†] - $\overline{\text{FPo0}}$ and $\overline{\text{CKo0}}$ Timing when $\text{CKFP0} = 0$

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|------------------------------------|------|-------------------|------|-------|-------------------|
| 1 | $\overline{\text{FPo0}}$ Output Pulse Width | t_{FPW0} | 220 | 244 | 270 | ns | $C_L=30\text{pF}$ |
| 2 | $\overline{\text{FPo0}}$ Output Delay from the $\overline{\text{CKo0}}$ falling edge to the output frame boundary | t_{FODF0} | 115 | | 130 | ns | |
| 3 | $\overline{\text{FPo0}}$ Output Delay from the output frame boundary to the $\overline{\text{CKo0}}$ Rising edge | t_{FODR0} | 115 | | 130 | ns | |
| 4 | $\overline{\text{CKo0}}$ Output Clock Period | t_{CKP0} | 220 | 244 | 270 | ns | $C_L=30\text{pF}$ |
| 5 | $\overline{\text{CKo0}}$ Output High Time | t_{CKH0} | 115 | | 130 | ns | |
| 6 | $\overline{\text{CKo0}}$ Output Low Time | t_{CKL0} | 115 | | 130 | ns | |
| 7 | $\overline{\text{CKo0}}$ Output Rise/Fall Time | $t_{\text{rCK0}}, t_{\text{fCK0}}$ | | | 10 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - $\overline{\text{FPo0}}$ and $\overline{\text{CKo0}}$ Timing when $\text{CKFP0} = 1$

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|------------------------------------|------|-------------------|------|-------|-------------------|
| 1 | $\overline{\text{FPo0}}$ Output Pulse Width | t_{FPW0} | 108 | 122 | 140 | ns | $C_L=30\text{pF}$ |
| 2 | $\overline{\text{FPo0}}$ Output Delay from the $\overline{\text{CKo0}}$ falling edge to the output frame boundary | t_{FODF0} | 54 | | 68 | ns | |
| 3 | $\overline{\text{FPo0}}$ Output Delay from the output frame boundary to the $\overline{\text{CKo0}}$ Rising edge | t_{FODR0} | 54 | | 68 | ns | |
| 4 | $\overline{\text{CKo0}}$ Output Clock Period | t_{CKP0} | 108 | 122 | 140 | ns | $C_L=30\text{pF}$ |
| 5 | $\overline{\text{CKo0}}$ Output High Time | t_{CKH0} | 54 | | 69 | ns | |
| 6 | $\overline{\text{CKo0}}$ Output Low Time | t_{CKL0} | 54 | | 69 | ns | |
| 7 | $\overline{\text{CKo0}}$ Output Rise/Fall Time | $t_{\text{rCK0}}, t_{\text{fCK0}}$ | | | 10 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

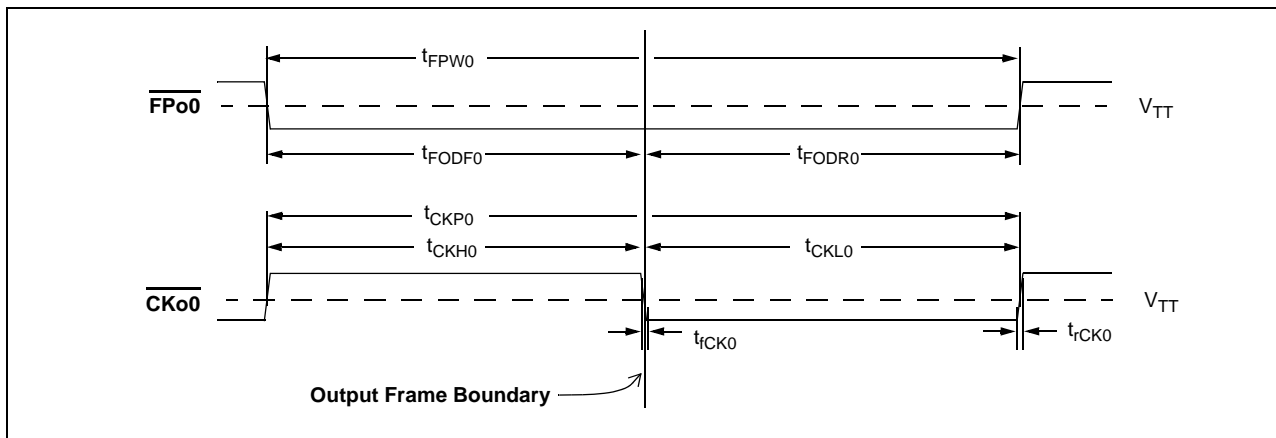


Figure 29 - $\overline{\text{FPo0}}$ and $\overline{\text{CKo0}}$ Timing Diagram

AC Electrical Characteristics[†] - $\overline{\text{FPo1}}$ and $\overline{\text{CKo1}}$ Timing when CKFP1 = 0

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|------------------------------------|------|-------------------|------|-------|-------------------|
| 1 | $\overline{\text{FPo1}}$ Output Pulse Width | t_{FPW1} | 47 | 61 | 75 | ns | $C_L=30\text{pF}$ |
| 2 | $\overline{\text{FPo1}}$ Output Delay from the $\overline{\text{CKo1}}$ falling edge to the output frame boundary | t_{FODF1} | 20 | | 40 | ns | |
| 3 | $\overline{\text{FPo1}}$ Output Delay from the output frame boundary to the $\overline{\text{CKo1}}$ Rising edge | t_{FODR1} | 20 | | 40 | ns | |
| 4 | $\overline{\text{CKo1}}$ Output Clock Period | t_{CKP1} | 47 | 61 | 75 | ns | $C_L=30\text{pF}$ |
| 5 | $\overline{\text{CKo1}}$ Output High Time | t_{CKH1} | 20 | | 40 | ns | |
| 6 | $\overline{\text{CKo1}}$ Output Low Time | t_{CKL1} | 20 | | 40 | ns | |
| 7 | $\overline{\text{CKo1}}$ Output Rise/Fall Time | $t_{\text{rCK1}}, t_{\text{fCK1}}$ | | | 10 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - $\overline{\text{FPo1}}$ and $\overline{\text{CKo1}}$ Timing when CKFP1 = 1

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|------------------------------------|------|-------------------|------|-------|-------------------|
| 1 | $\overline{\text{FPo1}}$ Output Pulse Width | t_{FPW1} | 108 | 122 | 140 | ns | $C_L=30\text{pF}$ |
| 2 | $\overline{\text{FPo1}}$ Output Delay from the $\overline{\text{CKo1}}$ falling edge to the output frame boundary | t_{FODF1} | 54 | | 68 | ns | |
| 3 | $\overline{\text{FPo1}}$ Output Delay from the output frame boundary to the $\overline{\text{CKo1}}$ Rising edge | t_{FODR1} | 54 | | 68 | ns | |
| 4 | $\overline{\text{CKo1}}$ Output Clock Period | t_{CKP1} | 108 | 122 | 140 | ns | $C_L=30\text{pF}$ |
| 5 | $\overline{\text{CKo1}}$ Output High Time | t_{CKH1} | 54 | | 69 | ns | |
| 6 | $\overline{\text{CKo1}}$ Output Low Time | t_{CKL1} | 54 | | 69 | ns | |
| 7 | $\overline{\text{CKo1}}$ Output Rise/Fall Time | $t_{\text{rCK1}}, t_{\text{fCK1}}$ | | | 10 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

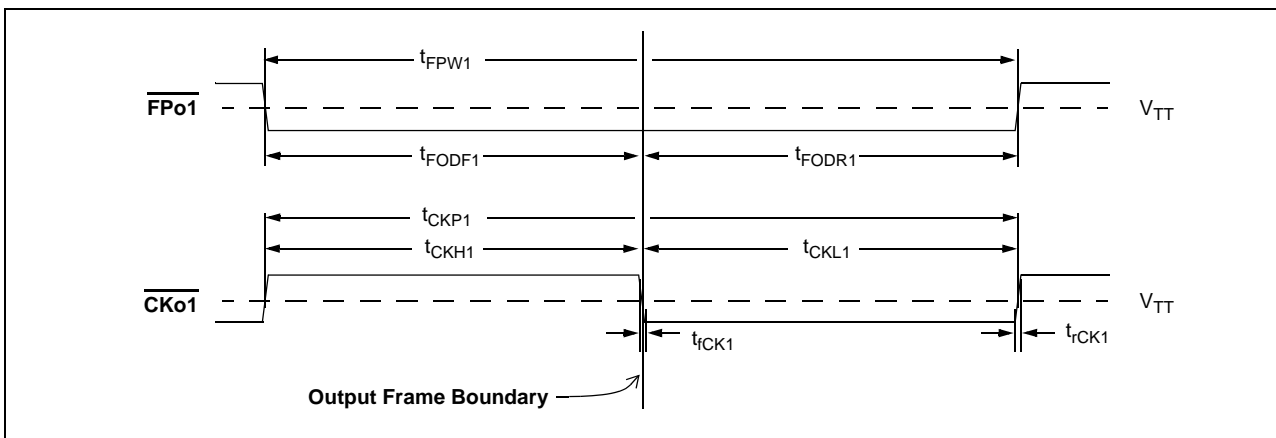


Figure 30 - $\overline{\text{FPo1}}$ and $\overline{\text{CKo1}}$ Timing Diagram

AC Electrical Characteristics[†] - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Timing when CKFP2 = 0

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|------------------------------------|------|-------------------|------|-------|-------------------|
| 1 | $\overline{\text{FPo2}}$ Output Pulse Width | t_{FPW2} | 15 | 30 | 45 | ns | $C_L=30\text{pF}$ |
| 2 | $\overline{\text{FPo2}}$ Output Delay from the $\overline{\text{CKo2}}$ falling edge to the output frame boundary | t_{FODF2} | 8 | | 22 | ns | |
| 3 | $\overline{\text{FPo2}}$ Output Delay from the output frame boundary to the $\overline{\text{CKo2}}$ Rising edge | t_{FODR2} | 8 | | 22 | ns | |
| 4 | $\overline{\text{CKo2}}$ Output Clock Period | t_{CKP2} | 15 | 30 | 45 | ns | $C_L=30\text{pF}$ |
| 5 | $\overline{\text{CKo2}}$ Output High Time | t_{CKH2} | 8 | | 22 | ns | |
| 6 | $\overline{\text{CKo2}}$ Output Low Time | t_{CKL2} | 8 | | 22 | ns | |
| 7 | $\overline{\text{CKo2}}$ Output Rise/Fall Time | $t_{\text{rCK2}}, t_{\text{fCK2}}$ | | | 7 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Timing when CKFP2 = 1

| | Characteristic | Sym. | Min. | Typ. [‡] | Max. | Units | Notes |
|---|---|------------------------------------|------|-------------------|------|-------|-------------------|
| 1 | $\overline{\text{FPo2}}$ Output Pulse Width | t_{FPW2} | 47 | 61 | 75 | ns | $C_L=30\text{pF}$ |
| 2 | $\overline{\text{FPo2}}$ Output Delay from the $\overline{\text{CKo2}}$ falling edge to the output frame boundary | t_{FODF2} | 20 | | 40 | ns | |
| 3 | $\overline{\text{FPo2}}$ Output Delay from the output frame boundary to the $\overline{\text{CKo2}}$ Rising edge | t_{FODR2} | 20 | | 40 | ns | |
| 4 | $\overline{\text{CKo2}}$ Output Clock Period | t_{CKP2} | 47 | 61 | 75 | ns | $C_L=30\text{pF}$ |
| 5 | $\overline{\text{CKo2}}$ Output High Time | t_{CKH2} | 20 | | 40 | ns | |
| 6 | $\overline{\text{CKo2}}$ Output Low Time | t_{CKL2} | 20 | | 40 | ns | |
| 7 | $\overline{\text{CKo2}}$ Output Rise/Fall Time | $t_{\text{rCK2}}, t_{\text{fCK2}}$ | | | 10 | ns | |

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

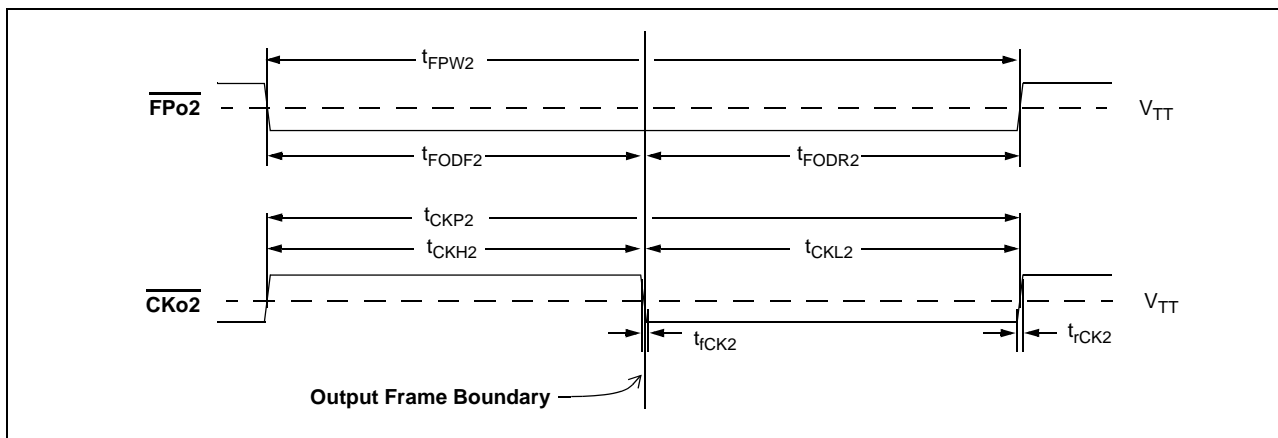


Figure 31 - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Timing Diagram

AC Electrical Characteristics† - ST-BUS Input Timing

| | Characteristic | Sym. | Min. | Typ.‡ | Max. | Units | Test Conditions |
|---|----------------|------------|------|-------|------|-------|-----------------|
| 1 | STi Setup Time | | | | | | |
| | 2.048 Mb/s | t_{SIS2} | 3 | | | ns | |
| | 4.096 Mb/s | t_{SIS4} | 3 | | | ns | |
| 2 | STi Hold Time | | | | | | |
| | 2.048 Mb/s | t_{SIH2} | 3 | | | ns | |
| | 4.096 Mb/s | t_{SIH4} | 3 | | | ns | |
| | 8.192 Mb/s | t_{SIH8} | 3 | | | ns | |

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

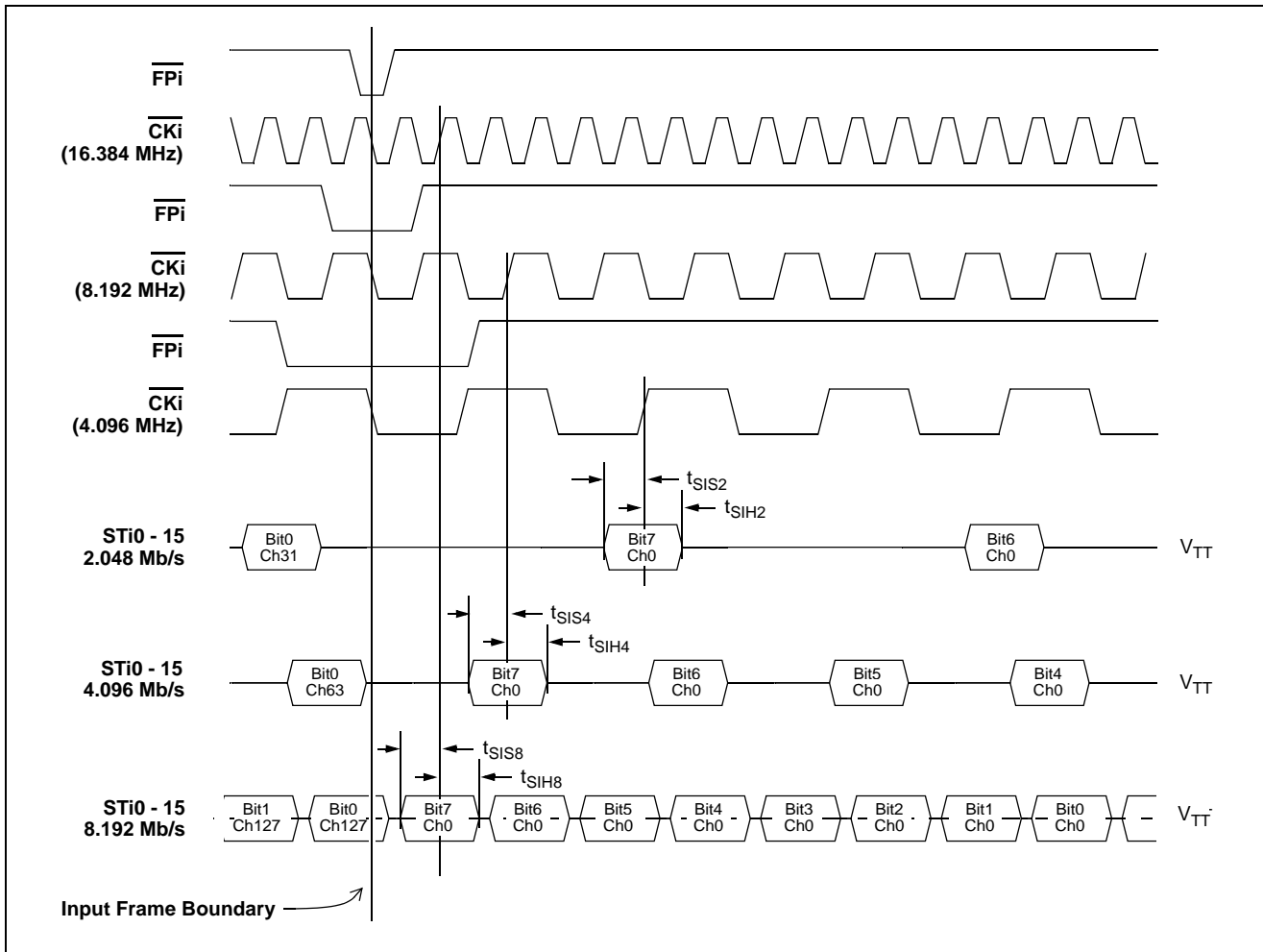


Figure 32 - ST-BUS Inputs (STi0 - 15) Timing Diagram

AC Electrical Characteristics† - ST-BUS Output Timing

| | Characteristic | Sym. | Min. | Typ.‡ | Max. | Units | Test Conditions |
|---|---|--|------|-------|----------------|----------------|-----------------|
| 1 | STo Delay - Active to Active @2.048 Mb/s @4.096 Mb/s @8.192 Mb/s | t_{SOD2} t_{SOD4} t_{SOD8} | | | 10 10 10 | ns ns ns | $C_L = 30pF$ |

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, V_{DD} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

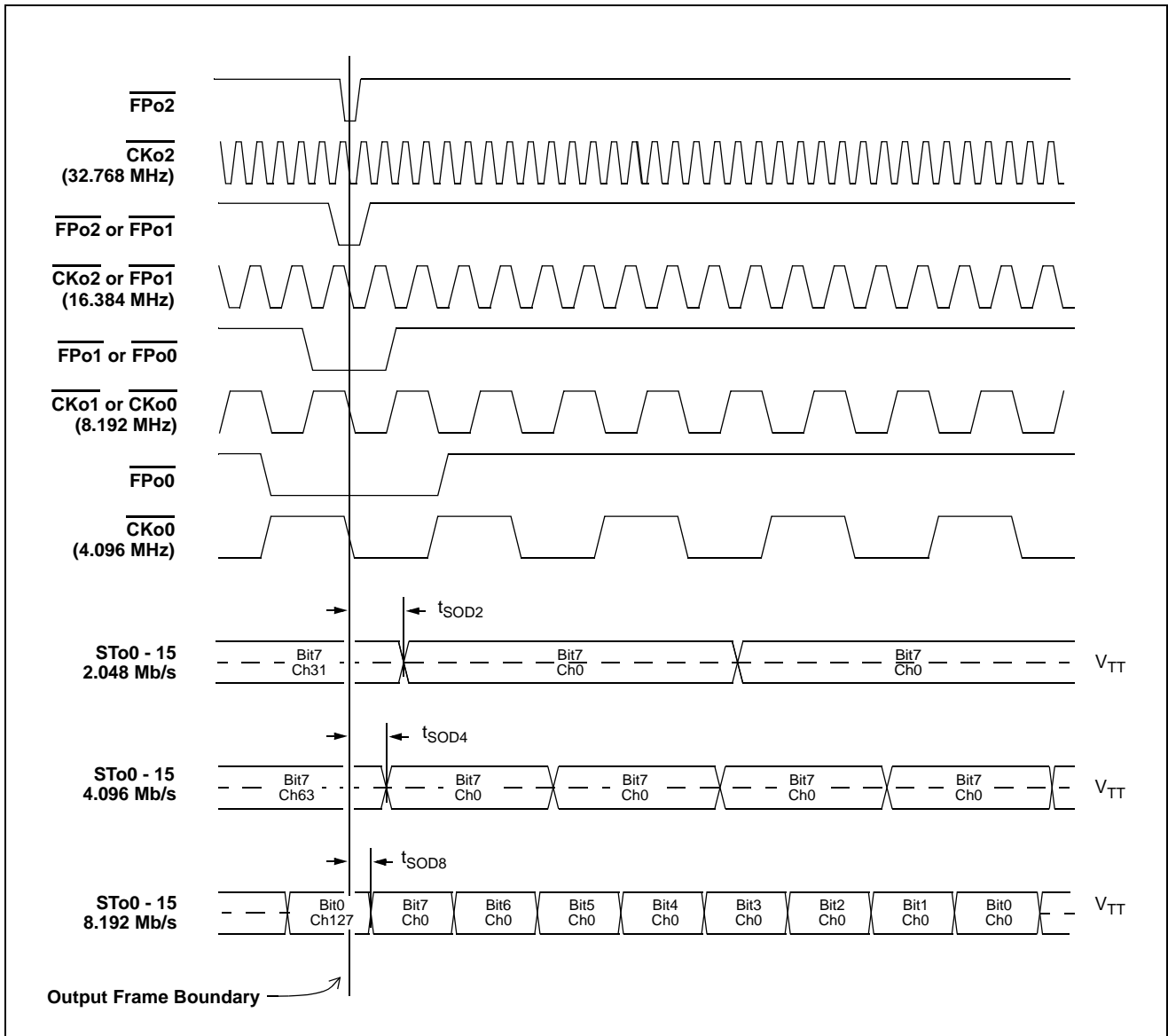


Figure 33 - ST-BUS Outputs (STo0 - 15) Timing Diagram

AC Electrical Characteristics† - ST-BUS Output Tristate Timing

| | Characteristic | Sym. | Min. | Typ.‡ | Max. | Units | Test Conditions |
|---|--|------------------|------|-------|----------------|----------------|---|
| 1 | STo Delay - Active to High-Z STo Delay - High-Z to Active 2.048 Mb/s 4.096 Mb/s 8.192 Mb/s | t_{DZ}, t_{ZD} | | | 15 15 15 | ns ns ns | $R_L=1K,$ $C_L=30pF,$ See Note 1. |
| 2 | Output Driver Enable (ODE) Delay - High-Z to Active 2.048 Mb/s 4.096 Mb/s 8.192 Mb/s | t_{ZD_ODE} | | | 45 45 45 | ns ns ns | |
| 2 | Output Driver Disable (ODE) Delay - Active to High-Z 2.048 Mb/s 4.096 Mb/s 8.192 Mb/s | t_{DZ_ODE} | | | 30 30 30 | ns ns ns | |

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

* Note 1: High Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel the time taken to discharge C_L .

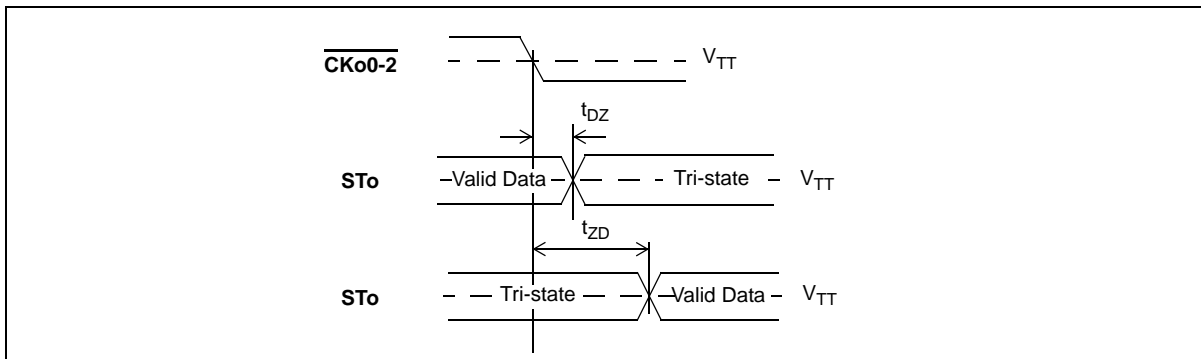


Figure 34 - Serial Output and External Control

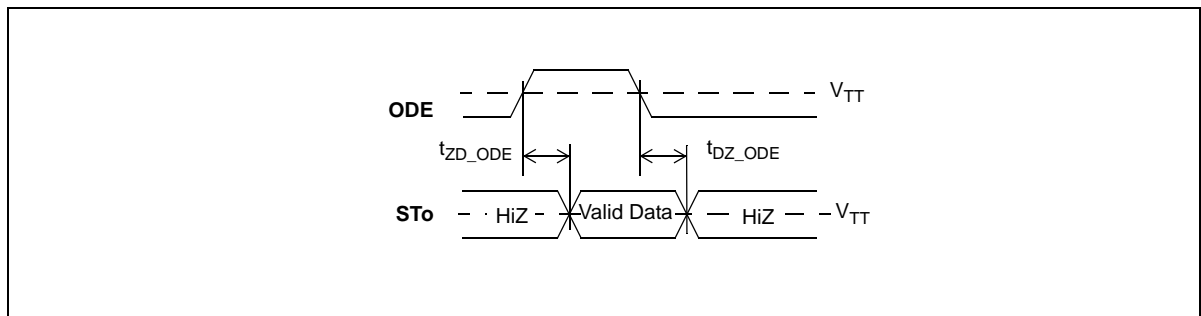


Figure 35 - Output Driver Enable (ODE)

AC Electrical Characteristics - Motorola Non-Multiplexed Bus Mode

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Test Conditions ² |
|----|---|-----------|------|------|--------------------|----------|------------------------------|
| 1 | \overline{CS} setup from \overline{DS} falling | t_{CSS} | 0 | | | ns | |
| 2 | R/\overline{W} setup from \overline{DS} falling | t_{RWS} | 10 | | | ns | |
| 3 | Address setup from \overline{DS} falling | t_{ADS} | 5 | | | ns | |
| 4 | \overline{DS} delay from the rising edge of \overline{DTA} to the falling edge of the \overline{DS} | t_{DSD} | 50 | | | ns | |
| 5 | \overline{CS} delay from the rising edge of \overline{DTA} to the falling edge of the \overline{CS} | t_{CSD} | 50 | | | ns | |
| 6 | \overline{CS} hold after \overline{DS} rising | t_{CSH} | 0 | | | ns | |
| 7 | R/\overline{W} hold after \overline{DS} rising | t_{RWH} | 0 | | | ns | |
| 8 | Address hold after \overline{DS} rising | t_{ADH} | 0 | | | ns | |
| 9 | Data setup from \overline{DTA} Low on Read | t_{DDR} | 20 | | | ns | $C_L=30pF$ |
| 10 | Data hold on read | t_{DHR} | 3 | | 9 | ns | $C_L=30pF, R_L=1K$ (Note 1) |
| 11 | Data setup from \overline{DS} falling on write | t_{WDS} | 10 | | | ns | |
| 12 | Data hold on write | t_{DHW} | 0 | | | ns | |
| 13 | Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory | t_{AKD} | | | 120/105 200/150 | ns ns | $C_L=30pF$ $C_L=30pF$ |
| 14 | Acknowledgment Hold Time | t_{AKH} | | | 20 | ns | $C_L=30pF, R_L=1K$ (Note 1) |

Note 1: High Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .
 Note 2: A delay of 600 microseconds must be applied before the first microprocessor access is performed after the RESET pin is set high.

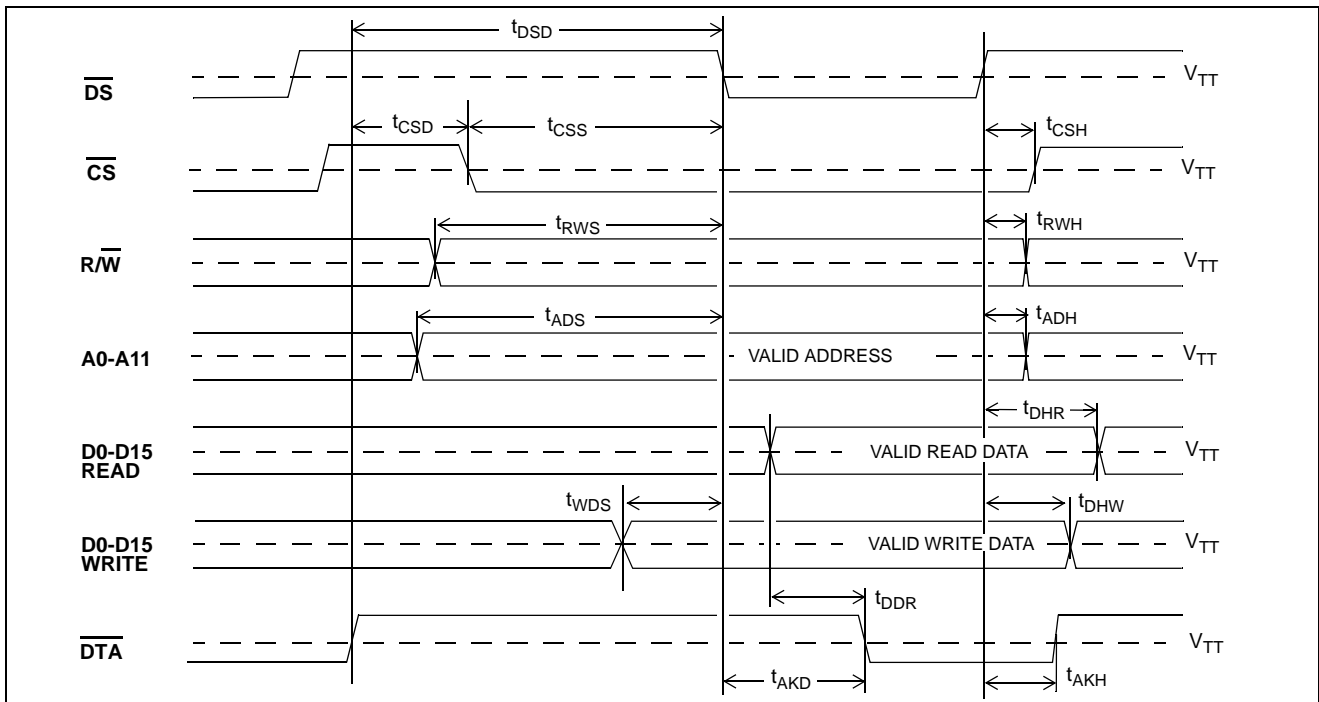


Figure 36 - Motorola Non-Multiplexed Bus Timing

AC Electrical Characteristics† - JTAG Test Port and $\overline{\text{Reset}}$ Pin Timing

| | Characteristic | Sym. | Min. | Typ. | Max. | Units | Notes |
|----|---------------------------------------|--------------------|------|------|------|-------|-------------------|
| 1 | TCK Clock Period | t_{TCKP} | 100 | | | ns | |
| 2 | TCK Clock Pulse Width High | t_{TCKH} | 80 | | | ns | |
| 3 | TCK Clock Pulse Width Low | t_{TCKL} | 80 | | | ns | |
| 4 | TMS Set-up Time | t_{TMSS} | 10 | | | ns | |
| 5 | TMS Hold Time | t_{TMSH} | 10 | | | ns | |
| 6 | TDi Input Set-up Time | t_{TDis} | 20 | | | ns | |
| 7 | TDi Input Hold Time | t_{TDIH} | 60 | | | ns | |
| 8 | TDo Output Delay | t_{TDOD} | | 25 | | ns | $C_L=30\text{pF}$ |
| 9 | $\overline{\text{TRST}}$ pulse width | t_{TRSTW} | 200 | | | ns | |
| 10 | $\overline{\text{Reset}}$ pulse width | t_{RSTW} | 1.0 | | | ms | |

†Characteristics are over recommended operating conditions unless otherwise stated.

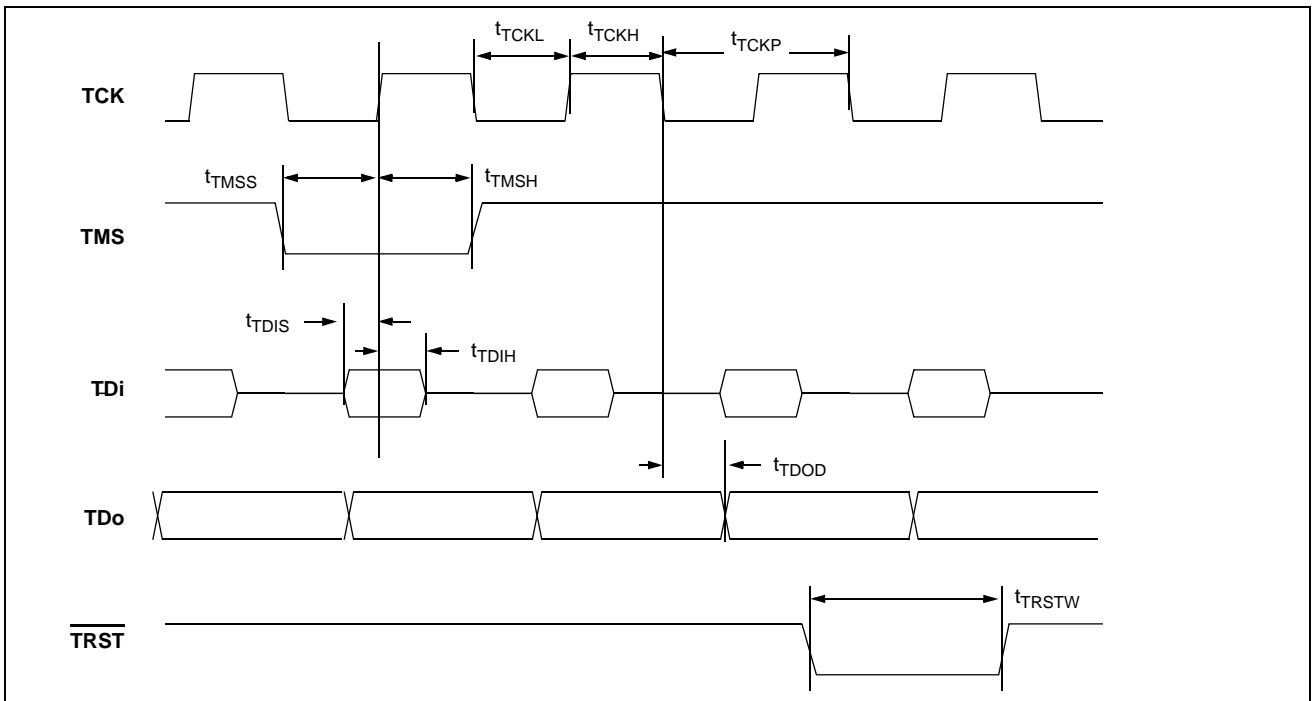


Figure 37 - JTAG Test Port Timing Diagram

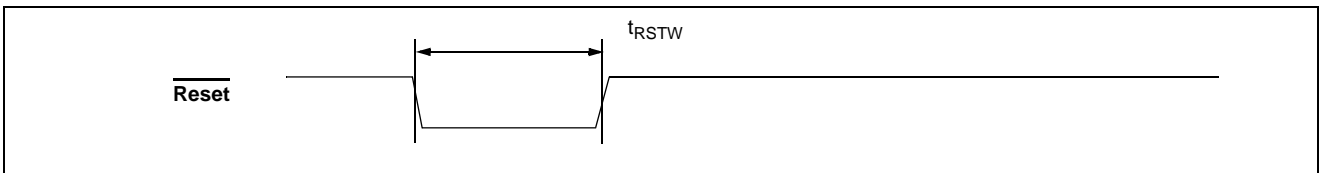
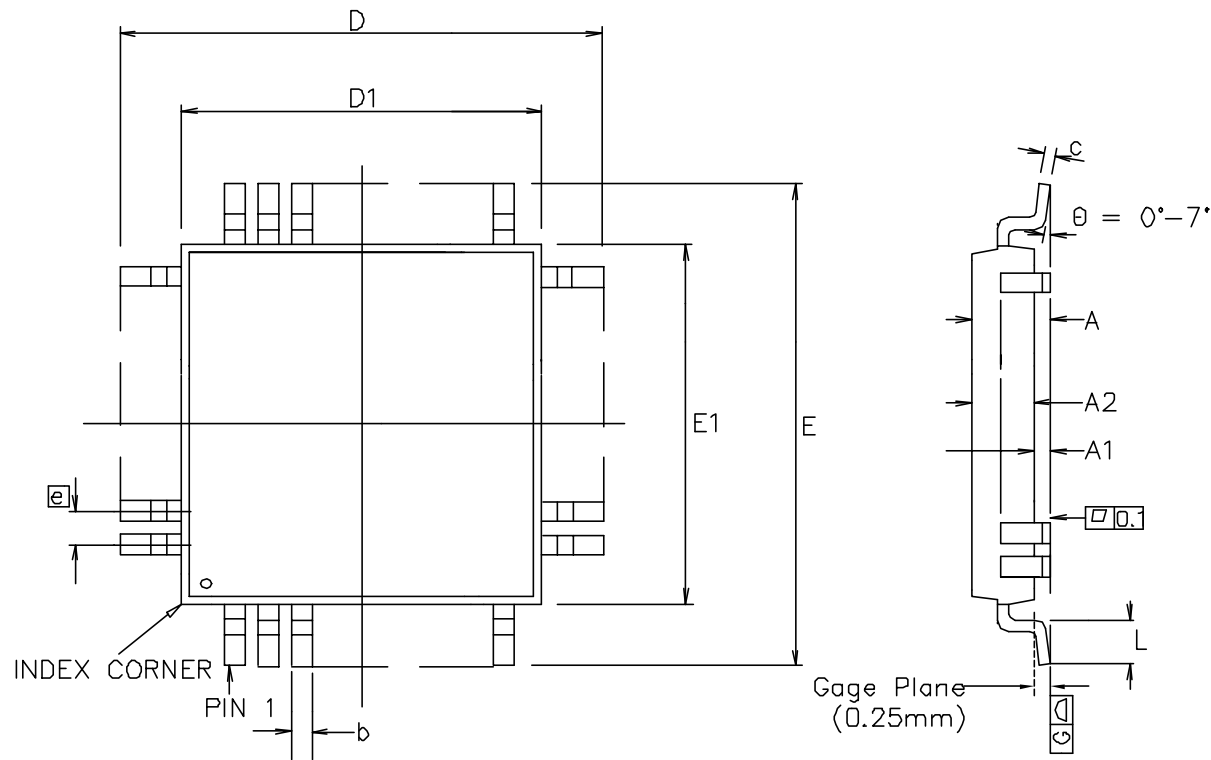


Figure 38 - $\overline{\text{Reset}}$ Pin Timing Diagram




| Symbol | Control Dimensions in millimetres | | Altern. Dimensions in inches | |
|--------------|--------------------------------------|------|---------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 1.60 | --- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 1.35 | 1.45 | 0.053 | 0.057 |
| D | 26.00 BSC | | 1.024 BSC | |
| D1 | 24.00 BSC | | 0.945 BSC | |
| E | 26.00 BSC | | 1.024 BSC | |
| E1 | 24.00 BSC | | 0.945 BSC | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| e | 0.50 BSC | | 0.020 BSC | |
| b | 0.17 | 0.27 | 0.007 | 0.011 |
| c | 0.09 | 0.20 | 0.004 | 0.008 |
| Pin features | | | | |
| N | 160 | | | |
| ND | 40 | | | |
| NE | 40 | | | |
| NOTE | SQUARE | | | |

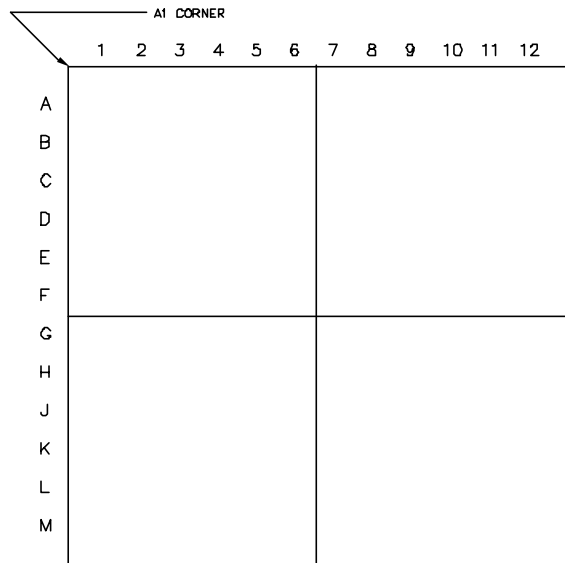
Conforms to JEDEC MS-026 BGA Iss. C
Except for number of pins.

Notes:

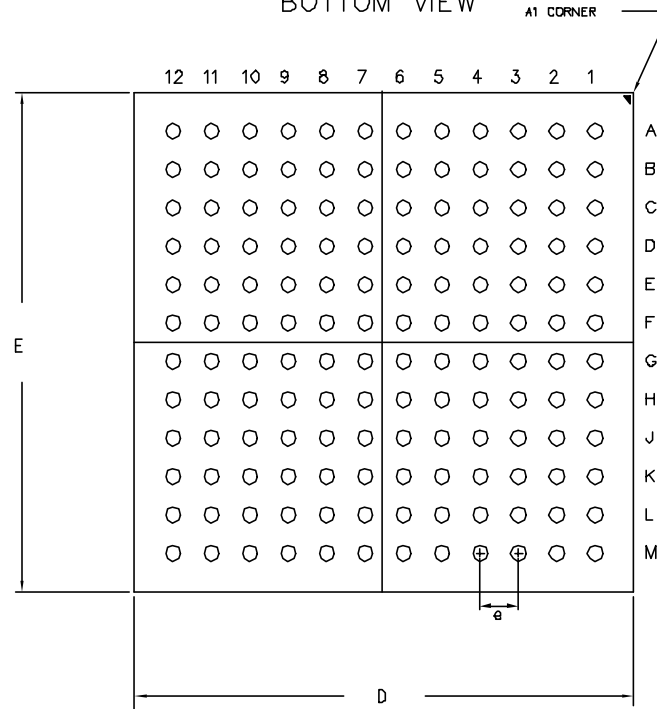
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protrusion.
5. Dimension b does not include dambar protrusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

| | | | | | | |
|---|---------|---------|---------|---|------------------------|--|
| © Zarlink Semiconductor 2002 All rights reserved. | | | |  ZARLINK SEMICONDUCTOR | Previous package codes | Package Code |
| ISSUE | 1 | 2 | 3 | | | Package Outline for 160 Lead LQFP (QC) (24x24x1.4)mm + 2.0mm (footprint) |
| ACN | 201652 | 207156 | 213835 | | | |
| DATE | 12Dec96 | 16Jul99 | 11Dec02 | | | |
| APPRD. | | | | | | GPD00269 |

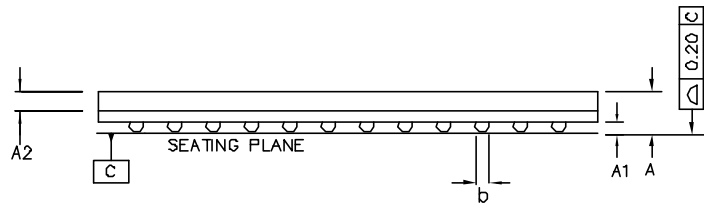
TOP VIEW



BOTTOM VIEW



| DIMENSION | MIN | MAX |
|--------------------------|----------|-------|
| A | — | 1.25 |
| A1 | 0.25 | 0.35 |
| A2 | 0.53 REF | |
| D | 12.95 | 13.05 |
| E | 12.95 | 13.05 |
| b | 0.35 | 0.45 |
| e | 1.00 | |
| N | 144 | |
| Conforms to JEDEC MO-192 | | |



SIDE VIEW

NOTES: -

1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

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| ISSUE | 1 | 2 | | |
|--------|---------|---------|--|--|
| ACN | 213740 | 213834 | | |
| DATE | 15Nov02 | 11Dec02 | | |
| APPRD. | | | | |



Package Code GD

Previous package codes

Package Outline for
144Ball LPGA
13x13x1.25mm

GPD00805



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