

# MC10EP35, MC100EP35

## 3.3V / 5V ECL JK Flip-Flop

### Description

The MC10/100EP35 is a higher speed/low voltage version of the EL35 JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

The 100 Series contains temperature compensation.

### Features

- 410 ps Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- Pb-Free Packages are Available



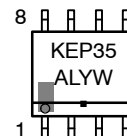
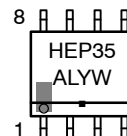
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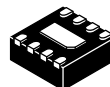
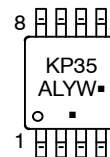
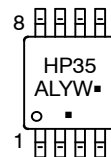
### MARKING DIAGRAMS\*



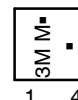
**SOIC-8**  
**D SUFFIX**  
**CASE 751**



**TSSOP-8**  
**DT SUFFIX**  
**CASE 948R**



**DFN8**  
**MN SUFFIX**  
**CASE 506AA**



|    |         |   |                     |
|----|---------|---|---------------------|
| H  | = MC10  | A | = Assembly Location |
| K  | = MC100 | L | = Wafer Lot         |
| 5R | = MC10  | Y | = Year              |
| 3M | = MC100 | W | = Work Week         |
|    |         | M | = Date Code         |
|    |         | ▪ | = Pb-Free Package   |

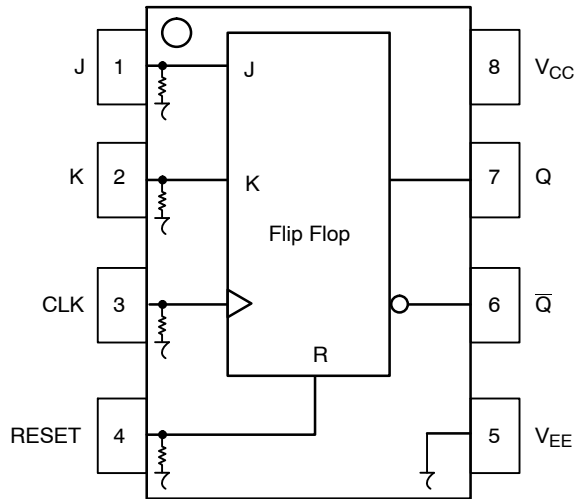
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN             | FUNCTION                                                                                                                                                                       |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK*            | ECL Clock Inputs                                                                                                                                                               |
| J*, K*          | ECL Signal Inputs                                                                                                                                                              |
| RESET*          | ECL Asynchronous Reset                                                                                                                                                         |
| Q, $\bar{Q}$    | ECL Data Outputs                                                                                                                                                               |
| V <sub>CC</sub> | Positive Supply                                                                                                                                                                |
| V <sub>EE</sub> | Negative Supply                                                                                                                                                                |
| EP              | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

\* Pins will default LOW when left open.

**Table 2. TRUTH TABLE**

| J | K | RESET | CLK | Q <sub>n+1</sub> |
|---|---|-------|-----|------------------|
| L | L | L     | Z   | Q <sub>n</sub>   |
| L | H | L     | Z   | L                |
| H | L | L     | Z   | H                |
| H | H | L     | Z   | $\bar{Q}_n$      |
| X | X | H     | X   | L                |

Z = LOW to HIGH Transition

**Table 3. ATTRIBUTES**

| Characteristics                                               |                        | Value                |
|---------------------------------------------------------------|------------------------|----------------------|
| Internal Input Pulldown Resistor                              |                        | 75 kΩ                |
| Internal Input Pullup Resistor                                |                        | N/A                  |
| ESD Protection                                                | Human Body Model       | > 4 kV               |
|                                                               | Machine Model          | > 200 V              |
|                                                               | Charged Device Model   | > 2 kV               |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb Pkg                 | Pb-Free Pkg          |
|                                                               | SOIC-8                 | Level 1              |
|                                                               | TSSOP-8                | Level 3              |
|                                                               | DFN8                   | Level 1              |
| Flammability Rating                                           | Oxygen Index: 28 to 34 | UL-94 V-0 @ 0.125 in |
| Transistor Count                                              |                        | 77 Devices           |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                        |                      |

1. For additional information, see Application Note AND8003/D.

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**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating      | Unit         |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|-------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 6           | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | -6          | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6     | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100   | mA<br>mA     |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | -40 to +85  | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | -65 to +150 | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | 8 SOIC<br>8 SOIC                                                     | 190<br>130  | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | 8 SOIC                                                               | 41 to 44    | °C/W         |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | 8 TSSOP<br>8 TSSOP                                                   | 185<br>140  | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | 8 TSSOP                                                              | 41 to 44    | °C/W         |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | DFN8<br>DFN8                                                         | 129<br>84   | °C/W<br>°C/W |
| T <sub>sol</sub> | Wave Solder<br>Pb<br>Pb-Free                       | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C     |                                                                      | 265<br>265  | °C           |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | (Note 2)                                       | DFN8                                                                 | 35 to 40    | °C/W         |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 5. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 3)

| Symbol   | Characteristic                    | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|----------|-----------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|          |                                   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$ | Power Supply Current              | 30    | 40   | 50   | 30   | 40   | 50   | 30   | 40   | 50   | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 4)      | 2165  | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 4)       | 1365  | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV            |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2090  |      | 2415 | 2155 |      | 2480 | 2215 |      | 2540 | mV            |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | 1365  |      | 1690 | 1460 |      | 1755 | 1490 |      | 1815 | mV            |
| $I_{IH}$ | Input HIGH Current                |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                 | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

4. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 6. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 5)

| Symbol   | Characteristic                    | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|----------|-----------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|          |                                   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$ | Power Supply Current              | 30    | 40   | 50   | 30   | 40   | 50   | 30   | 40   | 50   | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 6)      | 3865  | 3940 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 6)       | 3065  | 3190 | 3315 | 3130 | 3255 | 3380 | 3190 | 3315 | 3440 | mV            |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3790  |      | 4115 | 3855 |      | 4180 | 3915 |      | 4240 | mV            |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | 3065  |      | 3390 | 3130 |      | 3455 | 3190 |      | 3515 | mV            |
| $I_{IH}$ | Input HIGH Current                |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                 | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

6. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 7)

| Symbol   | Characteristic                    | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|----------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|          |                                   | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$ | Power Supply Current              | 30    | 40    | 50    | 30    | 40    | 50    | 30    | 40    | 50    | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 8)      | -1135 | -1010 | -885  | -1070 | -945  | -820  | -1010 | -885  | -760  | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 8)       | -1935 | -1810 | -1685 | -1870 | -1745 | -1620 | -1810 | -1685 | -1560 | mV            |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | -1210 |       | -885  | -1145 |       | -820  | -1085 |       | -760  | mV            |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | -1935 |       | -1610 | -1870 |       | -1545 | -1810 |       | -1485 | mV            |
| $I_{IH}$ | Input HIGH Current                |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                 | 0.5   |       |       | 0.5   |       |       | 0.5   |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with  $V_{CC}$ .

8. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

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**Table 8. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 9)

| Symbol   | Characteristic                    | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|----------|-----------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|          |                                   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$ | Power Supply Current              | 30    | 40   | 50   | 30   | 40   | 50   | 30   | 40   | 50   | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 10)     | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 10)      | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV            |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV            |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | 1355  |      | 1675 | 1355 |      | 1675 | 1355 |      | 1675 | mV            |
| $I_{IH}$ | Input HIGH Current                |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                 | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

10. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 9. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 11)

| Symbol   | Characteristic                    | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|----------|-----------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|          |                                   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$ | Power Supply Current              | 30    | 40   | 50   | 30   | 40   | 50   | 30   | 40   | 50   | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 12)     | 3855  | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 12)      | 3055  | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV            |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3775  |      | 4120 | 3775 |      | 4120 | 3775 |      | 4120 | mV            |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | 3055  |      | 3375 | 3055 |      | 3375 | 3055 |      | 3375 | mV            |
| $I_{IH}$ | Input HIGH Current                |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                 | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

12. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 10. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 13)

| Symbol   | Characteristic                    | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|----------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|          |                                   | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$ | Power Supply Current              | 30    | 40    | 50    | 30    | 40    | 50    | 30    | 40    | 50    | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 14)     | -1145 | -1020 | -895  | -1145 | -1020 | -895  | -1145 | -1020 | -895  | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 14)      | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | mV            |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | -1225 |       | -880  | -1225 |       | -880  | -1225 |       | -880  | mV            |
| $V_{IL}$ | Input LOW Voltage (Single-Ended)  | -1945 |       | -1625 | -1945 |       | -1625 | -1945 |       | -1625 | mV            |
| $I_{IH}$ | Input HIGH Current                |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current                 | 0.5   |       |       | 0.5   |       |       | 0.5   |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. Input and output parameters vary 1:1 with  $V_{CC}$ .

14. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

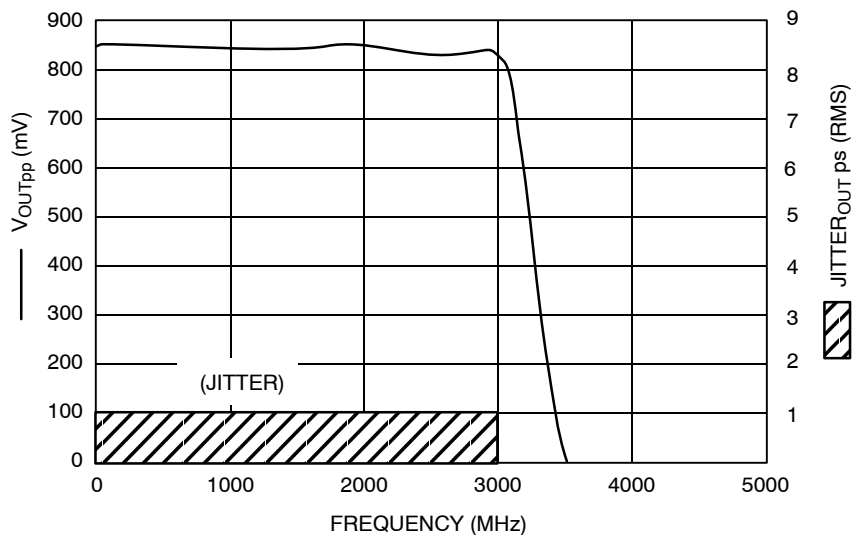
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**Table 11. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 15)

| Symbol                   | Characteristic                                                     | -40°C      |          |     | 25°C       |          |     | 85°C       |          |     | Unit |
|--------------------------|--------------------------------------------------------------------|------------|----------|-----|------------|----------|-----|------------|----------|-----|------|
|                          |                                                                    | Min        | Typ      | Max | Min        | Typ      | Max | Min        | Typ      | Max |      |
| $f_{\max}$               | Maximum Frequency<br>(See Figure 2. $F_{\max}/\text{JITTER}$ )     |            | > 3      |     |            | > 3      |     |            | > 3      |     | GHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to<br>Output Differential R, CLK to Q, $\bar{Q}$ | 200        | 400      | 480 | 200        | 410      | 490 | 200        | 420      | 575 | ps   |
| $t_{RR}$                 | Reset Recovery                                                     | 150        | 80       |     | 150        | 90       |     | 150        | 100      |     | ps   |
| $t_S$<br>$t_H$           | Setup Time<br>Hold Time                                            | 150<br>150 | 50<br>50 |     | 150<br>150 | 50<br>50 |     | 150<br>150 | 80<br>80 |     | ps   |
| $t_{PW}$                 | Minimum Pulse width<br>RESET                                       | 550        | 400      |     | 550        | 400      |     | 550        | 400      |     | ps   |
| $t_{\text{JITTER}}$      | Cycle-to-Cycle Jitter<br>(See Figure 2. $F_{\max}/\text{JITTER}$ ) |            | 0.2      | < 1 |            | 0.2      | < 1 |            | 0.2      | < 1 | ps   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times<br>(20% – 80%) Q, $\bar{Q}$                 | 70         | 120      | 170 | 80         | 130      | 180 | 100        | 150      | 200 | ps   |

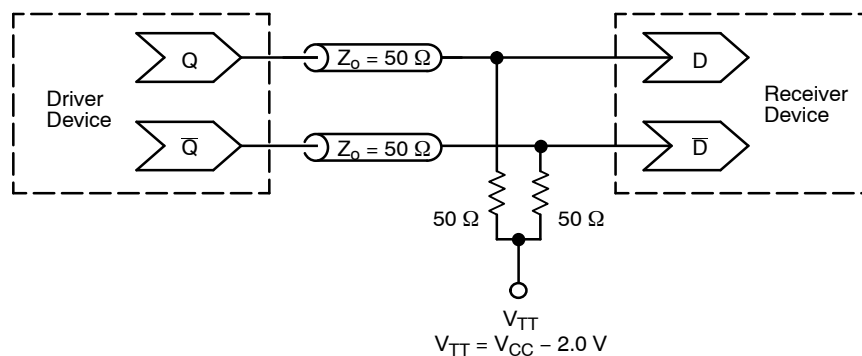
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

15. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .



**Figure 2.  $F_{\max}/\text{Jitter}$**

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**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device         | Package              | Shipping <sup>†</sup> |
|----------------|----------------------|-----------------------|
| MC10EP35D      | SOIC-8               | 98 Units / Rail       |
| MC10EP35DG     | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC10EP35DR2    | SOIC-8               | 2500 / Tape & Reel    |
| MC10EP35DR2G   | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC10EP35DT     | TSSOP-8              | 100 Units / Rail      |
| MC10EP35DTG    | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |
| MC10EP35DTR2   | TSSOP-8              | 2500 / Tape & Reel    |
| MC10EP35DTR2G  | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC10EP35MNR4   | DFN8                 | 1000 / Tape & Reel    |
| MC10EP35MNR4G  | DFN8<br>(Pb-Free)    | 1000 / Tape & Reel    |
| MC100EP35D     | SOIC-8               | 98 Units / Rail       |
| MC100EP35DG    | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC100EP35DR2   | SOIC-8               | 2500 / Tape & Reel    |
| MC100EP35DR2G  | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC3100EP35DT   | TSSOP-8              | 100 Units / Rail      |
| MC3100EP35DTG  | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |
| MC100EP35DTR2  | TSSOP-8              | 2500 / Tape & Reel    |
| MC100EP35DTR2G | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC100EP35MNR4  | DFN8                 | 1000 / Tape & Reel    |
| MC100EP35MNR4G | DFN8<br>(Pb-Free)    | 1000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MC10EP35, MC100EP35

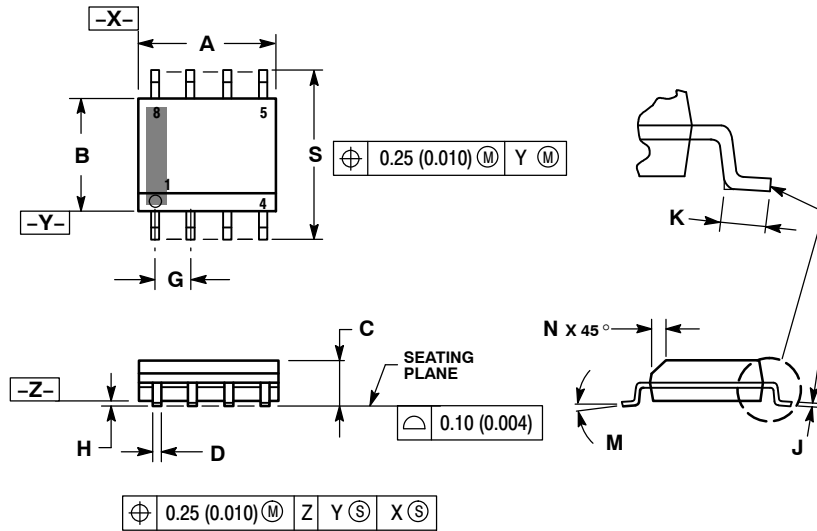
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10EP35, MC100EP35

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

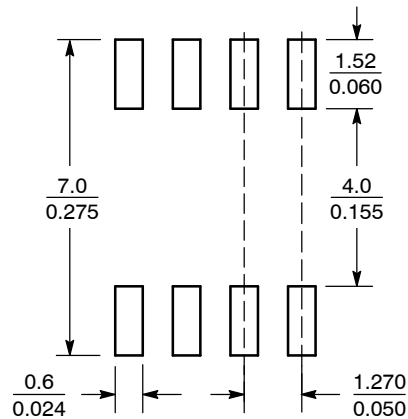


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## SOLDERING FOOTPRINT\*



SCALE 6:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

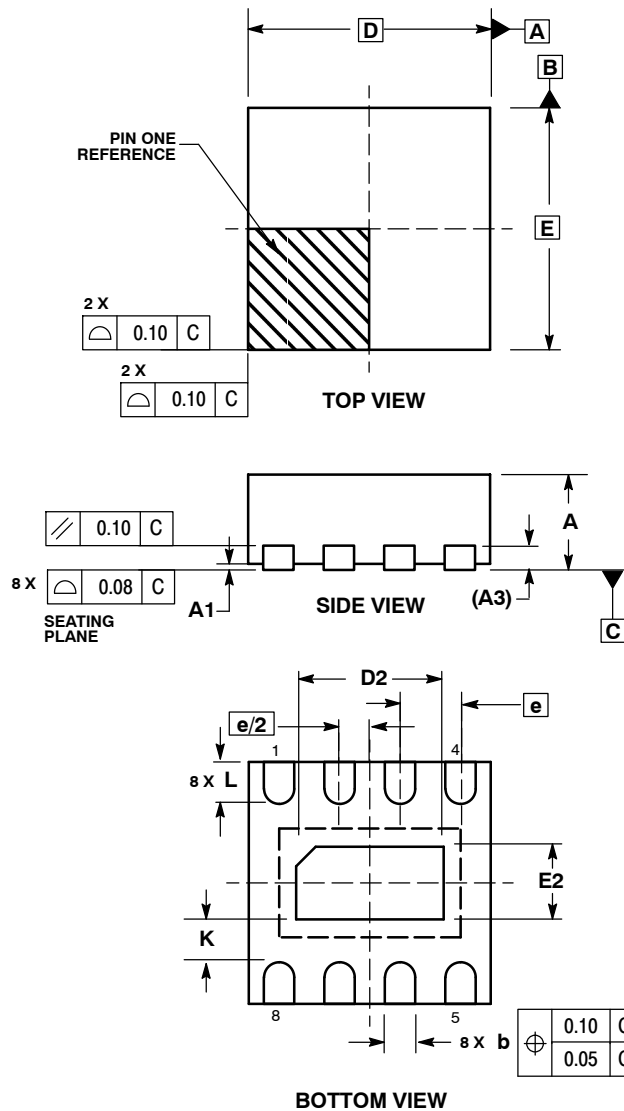
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



# MC10EP35, MC100EP35

## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.20 | 0.30 |
| D           | 2.00 | BSC  |
| D2          | 1.10 | 1.30 |
| E           | 2.00 | BSC  |
| E2          | 0.70 | 0.90 |
| e           | 0.50 | BSC  |
| K           | 0.20 | ---  |
| L           | 0.25 | 0.35 |

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