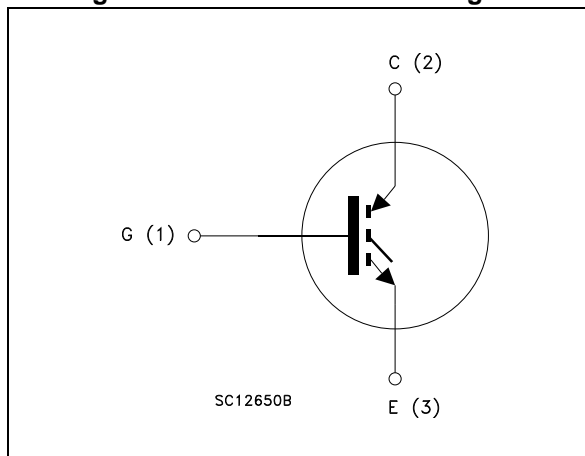


Figure 1. Internal schematic diagram



Features

- High frequency operation up to 50 kHz
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- High current capability

Applications

- High frequency inverters
- UPS, motor drivers
- HF, SMPS and PFC in both hard switch and resonant topologies

Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STGB20NC60V	GB20NC60V	D ² PAK	Tape and reel
STGP20NC60V	GP20NC60V	TO-220	Tube
STGW20NC60V	GW20NC60V	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at 25 °C	60	A
$I_C^{(1)}$	Collector current (continuous) at 100 °C	30	A
$I_{CL}^{(2)}$	Turn-off latching current	100	A
$I_{CP}^{(3)}$	Pulsed collector current	100	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25$ °C	200	W
T_j	Operating junction temperature	- 55 to 150	°C

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. $V_{clamp} = 80\%(V_{CES})$, $T_j = 150$ °C, $R_G = 10$ Ω, $V_{GE} = 15$ V

3. Pulse width limited by max junction temperature allowed

Table 3. Thermal resistance

Symbol	Parameter	Value		Unit
		TO-247	TO-220 D ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	0.62		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	62.5	°C/W

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage ($V_{GE} = 0$)	$I_C = 1 \text{ mA}$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE}=15 \text{ V}, I_C= 20 \text{ A}$ $V_{GE}=15 \text{ V}, I_C= 20 \text{ A}, T_C= 125^{\circ}\text{C}$		1.8 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE}= V_{GE}, I_C= 250 \mu\text{A}$	3.75		5.75	V
I_{CES}	Collector-emitter cut-off current ($V_{GE} = 0$)	$V_{CE} = 600 \text{ V}$ $V_{CE} = 600 \text{ V}, T_C=125^{\circ}\text{C}$			10 1	μA mA
I_{GES}	Gate-emitter cut-off current ($V_{CE} = 0$)	$V_{GE} = \pm 20 \text{ V}$			± 100	nA
$g_{fs}^{(1)}$	Forward transconductance	$V_{CE} = 15 \text{ V}, I_C= 20 \text{ A}$		15		S

1. Pulse duration = 300 μs , duty cycle 1.5%

Table 5. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GE}=0$	-	2200	-	pF
C_{oes}	Output capacitance		-	225	-	pF
C_{res}	Reverse transfer capacitance		-	50	-	pF
Q_g	Total gate charge	$V_{CE} = 390 \text{ V}, I_C = 20 \text{ A},$ $V_{GE} = 15 \text{ V},$ (see Figure 17)	-	100	-	nC
Q_{ge}	Gate-emitter charge		-	16	-	nC
Q_{gc}	Gate-collector charge		-	45	-	nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$ $R_G = 3.3\ \Omega$, $V_{GE} = 15\text{ V}$, (see Figure 16)	-	31	-	ns
t_r	Current rise time		-	11	-	ns
$(di/dt)_{on}$	Turn-on current slope		-	1600	-	A/ μ s
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$ $R_G = 3.3\ \Omega$, $V_{GE} = 15\text{ V}$, $T_C = 125\text{ }^\circ\text{C}$ (see Figure 16)	-	31	-	ns
t_r	Current rise time		-	11.5	-	ns
$(di/dt)_{on}$	Turn-on current slope		-	1500	-	A/ μ s
$t_{r(Voff)}$	Off voltage rise time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$, $R_G = 3.3\ \Omega$, $V_{GE} = 15\text{ V}$ (see Figure 18)	-	28	-	ns
$t_{d(off)}$	Turn-off delay time		-	100	-	ns
t_f	Current fall time		-	75	-	ns
$t_{r(Voff)}$	Off voltage rise time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$, $R_G = 3.3\ \Omega$, $V_{GE} = 15\text{ V}$, $T_C = 125\text{ }^\circ\text{C}$ (see Figure 18)	-	66	-	ns
$t_{d(off)}$	Turn-off delay time		-	150	-	ns
t_f	Current fall time		-	130	-	ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching losses	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$ $R_G = 3.3\ \Omega$, $V_{GE} = 15\text{ V}$, (see Figure 18)	-	220	-	μ J
$E_{off}^{(1)}$	Turn-off switching losses		-	330	-	μ J
E_{ts}	Total switching losses		-	550	-	μ J
E_{on}	Turn-on switching losses	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$ $R_G = 3.3\ \Omega$, $V_{GE} = 15\text{ V}$, $T_C = 125\text{ }^\circ\text{C}$ (see Figure 18)	-	450	-	μ J
$E_{off}^{(1)}$	Turn-off switching losses		-	770	-	μ J
E_{ts}	Total switching losses		-	1220	-	μ J

1. Turn-off losses include also the tail of the collector current.

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

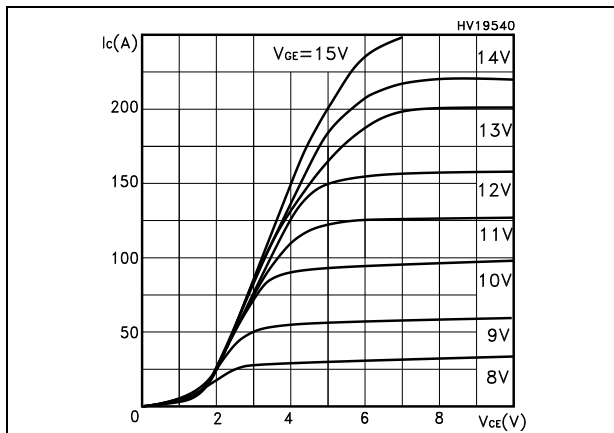


Figure 3. Transfer characteristics

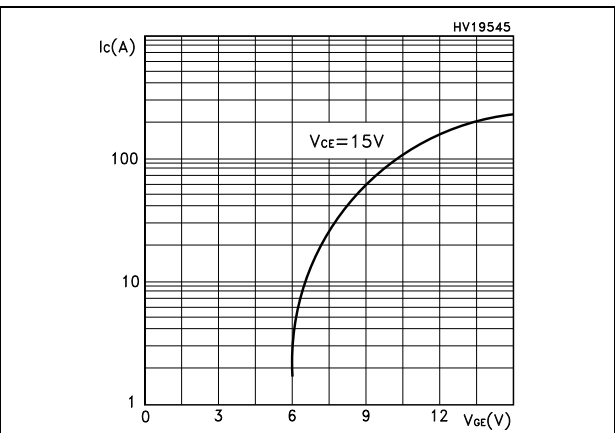


Figure 4. Transconductance

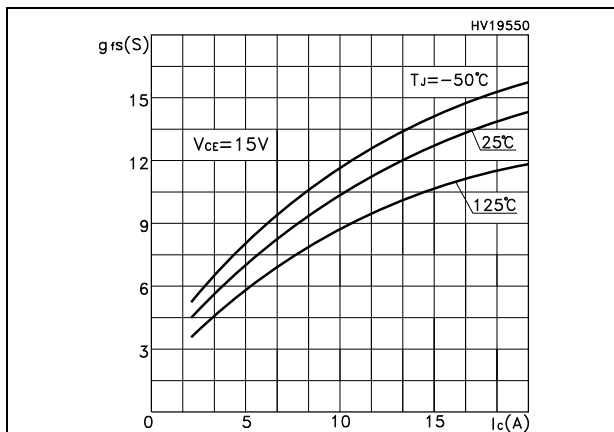


Figure 5. Collector-emitter on voltage vs temperature

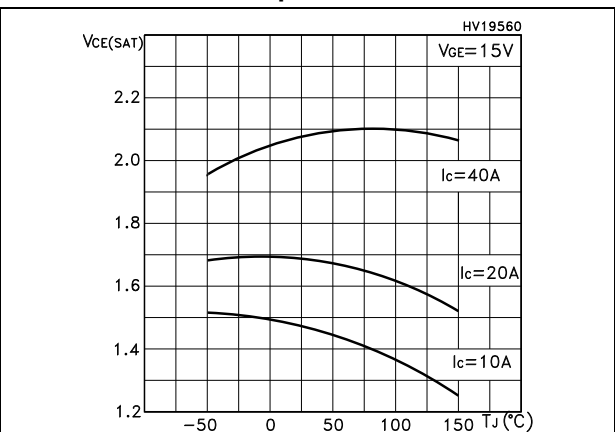


Figure 6. Gate charge vs gate-source voltage

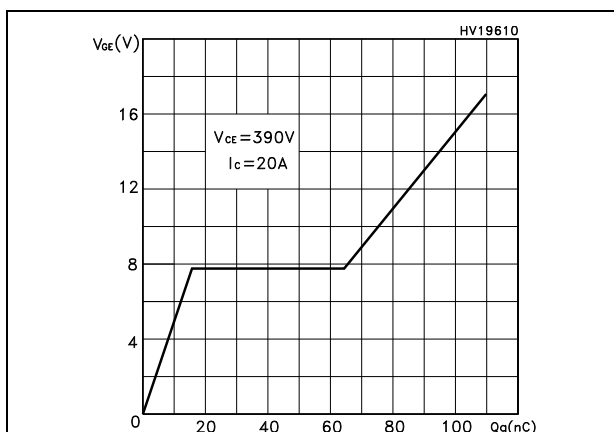


Figure 7. Capacitance variations

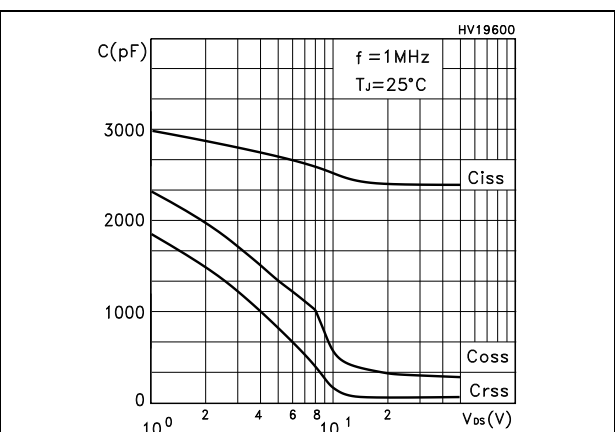


Figure 8. Normalized gate threshold voltage vs temperature

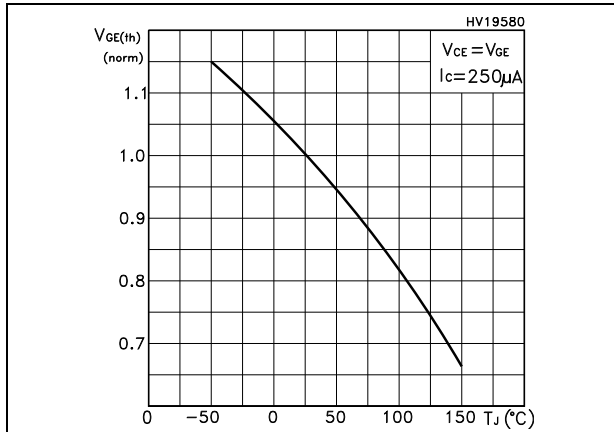


Figure 9. Collector-emitter on voltage vs collector current

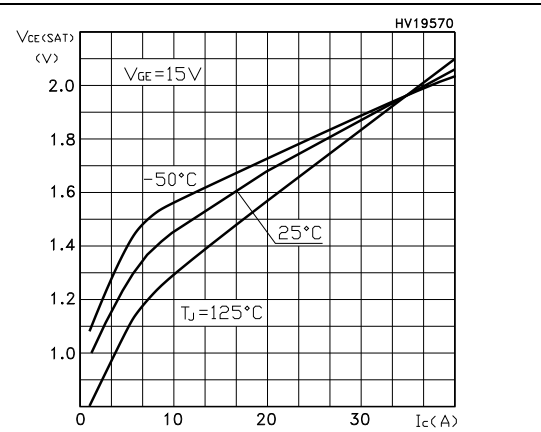


Figure 10. Normalized breakdown voltage vs temperature

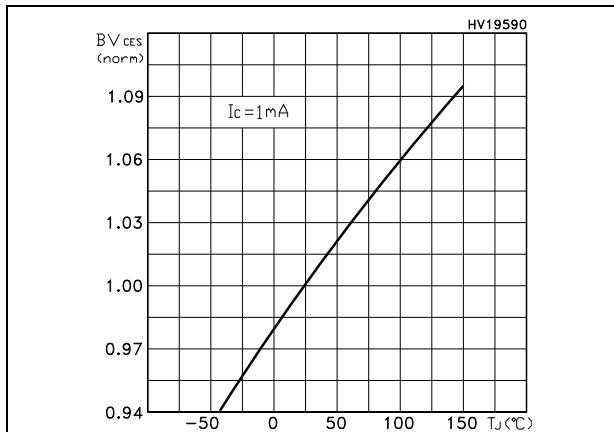


Figure 11. Switching losses vs temperature

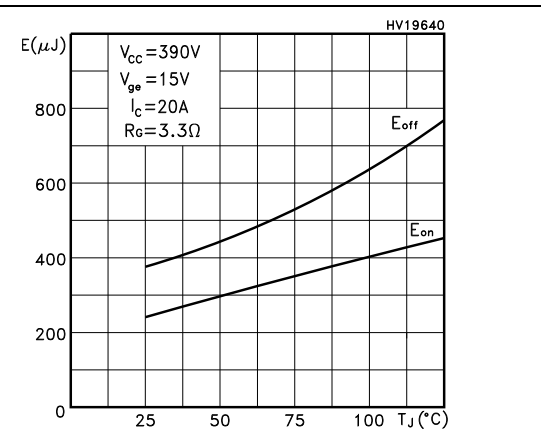


Figure 12. Switching losses vs gate resistance

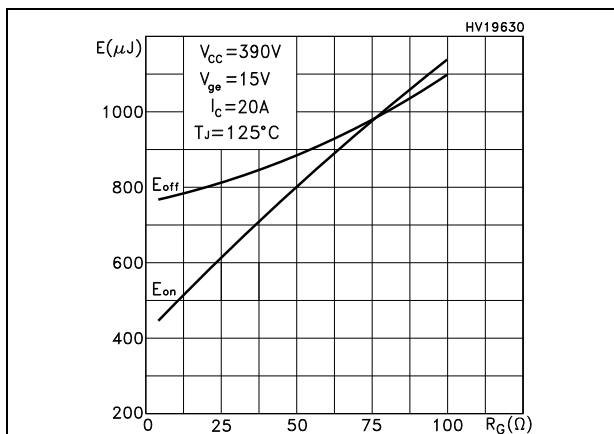


Figure 13. Switching losses vs collector current

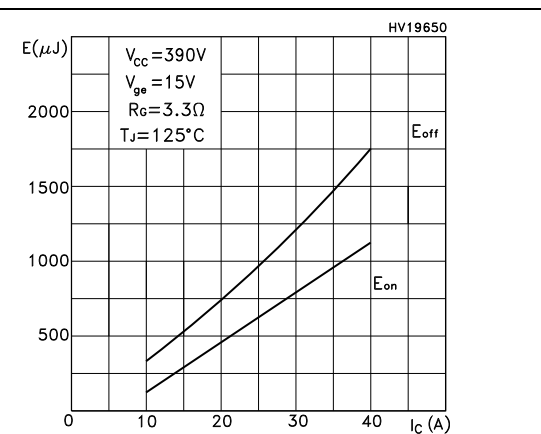


Figure 14. Thermal impedance

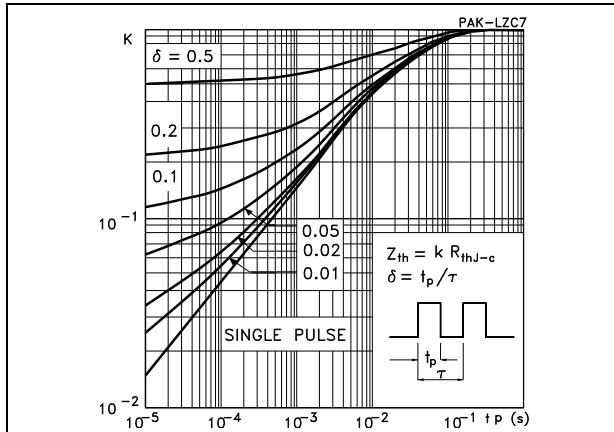
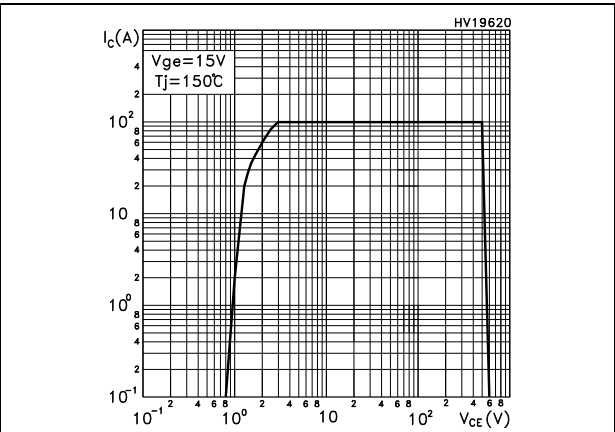


Figure 15. Turn-off SOA



3 Test circuits

Figure 16. Test circuit for inductive load switching

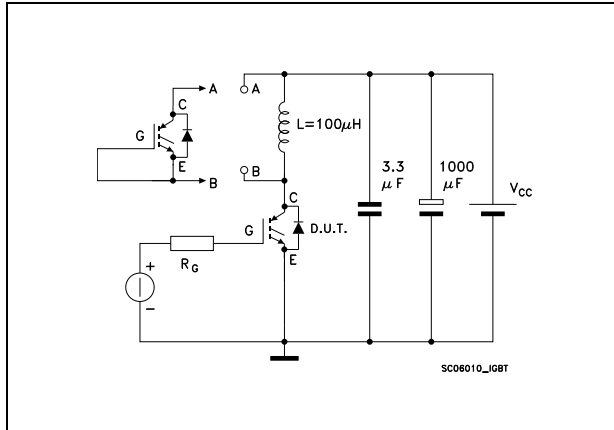


Figure 17. Gate charge test circuit

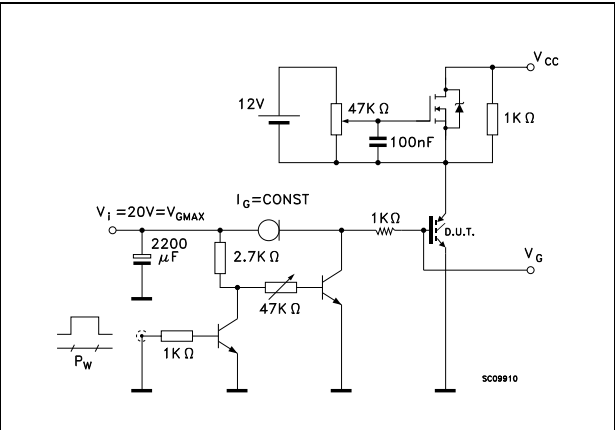
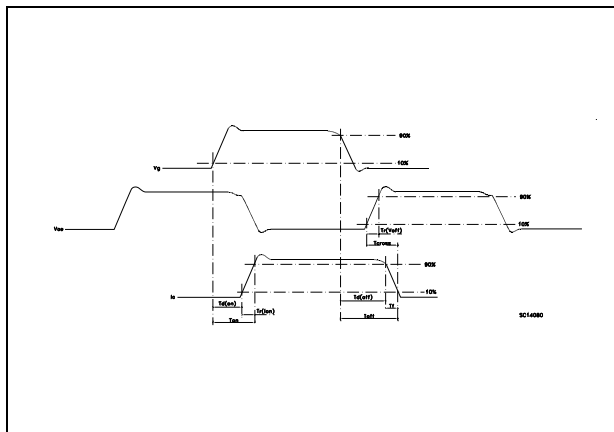


Figure 18. Switching waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK type A package information

Figure 19. D²PAK (TO-263) type A package outline

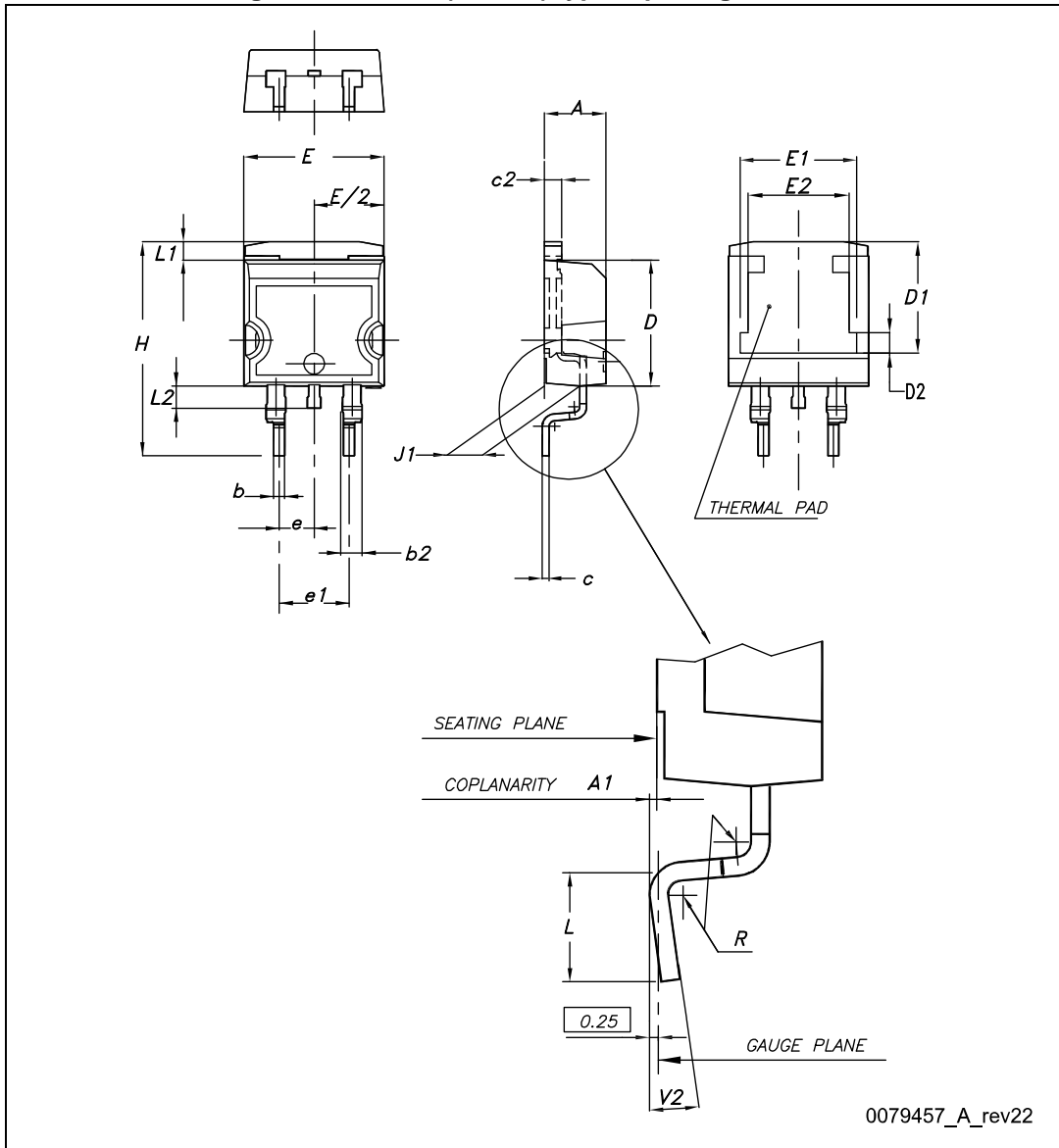
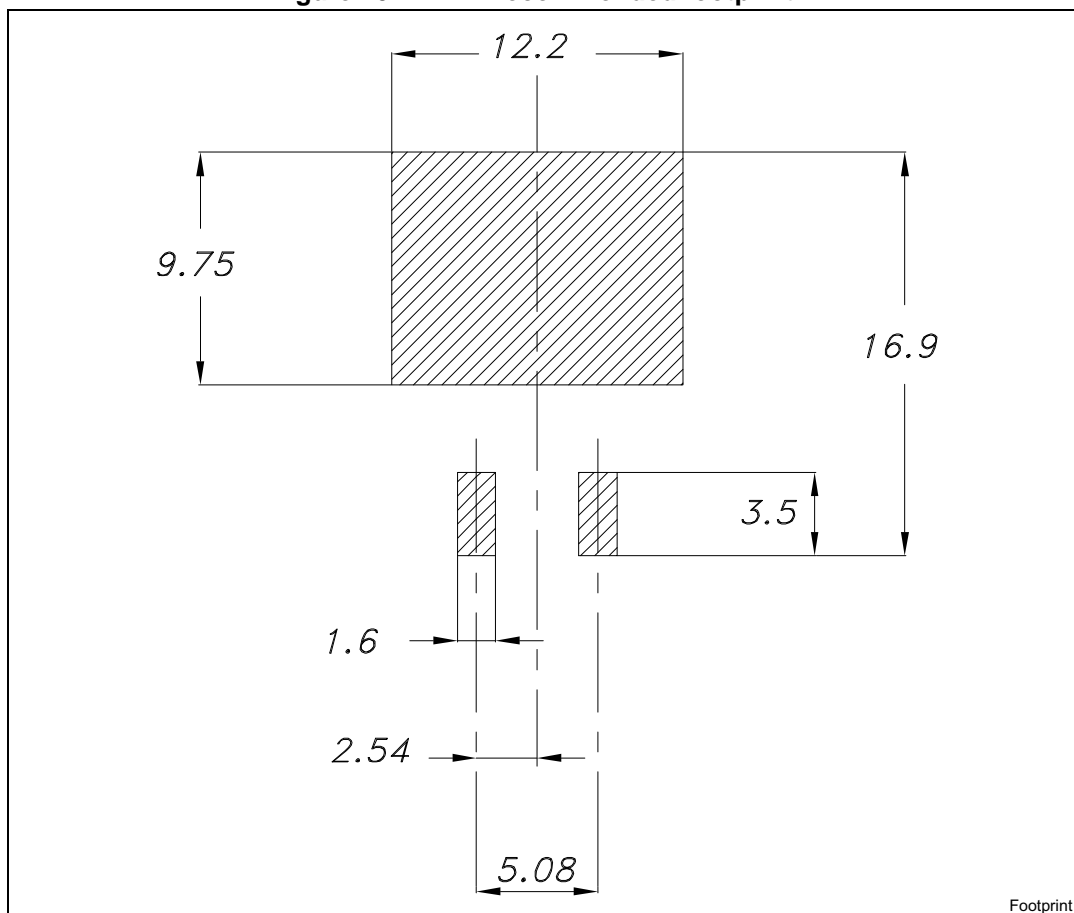


Table 8. D²PAK (TO-263) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D²PAK recommended footprint^(a)



a. All dimension are in millimeters

4.2 TO-220 type A package information

Figure 21. TO-220 type A package outline

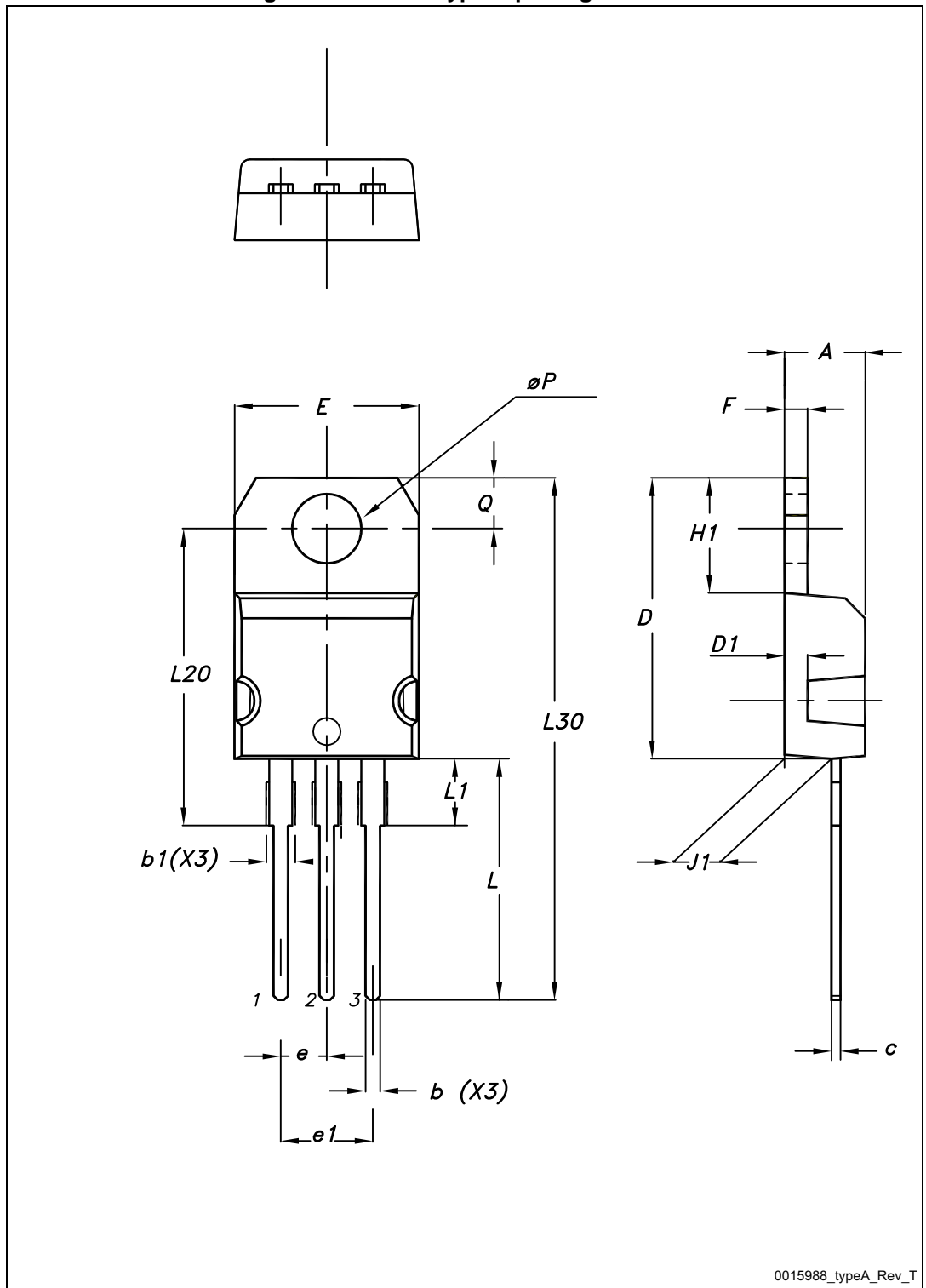


Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-247 package information

Figure 22. TO-247 package outline

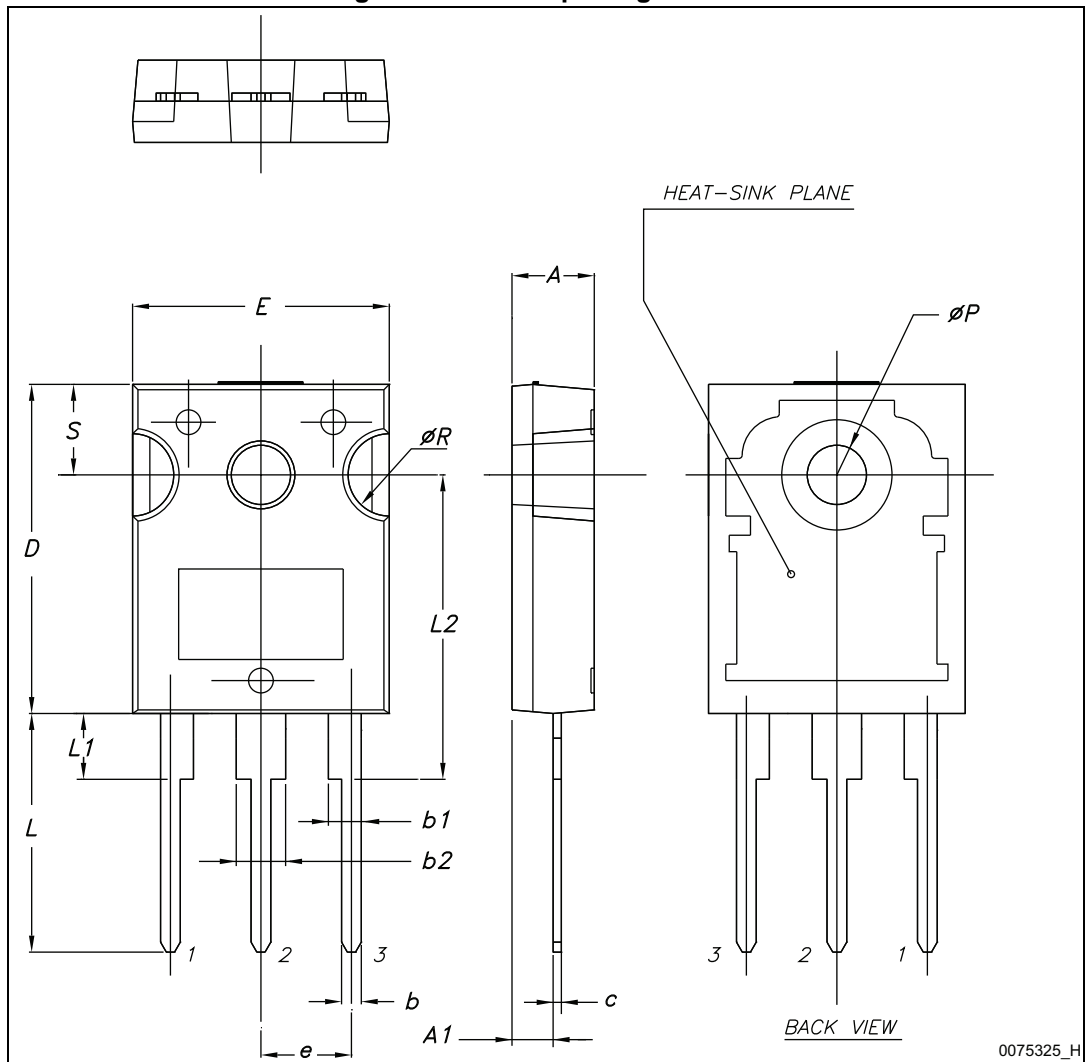


Table 10. TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Packing information

Figure 23. Tape

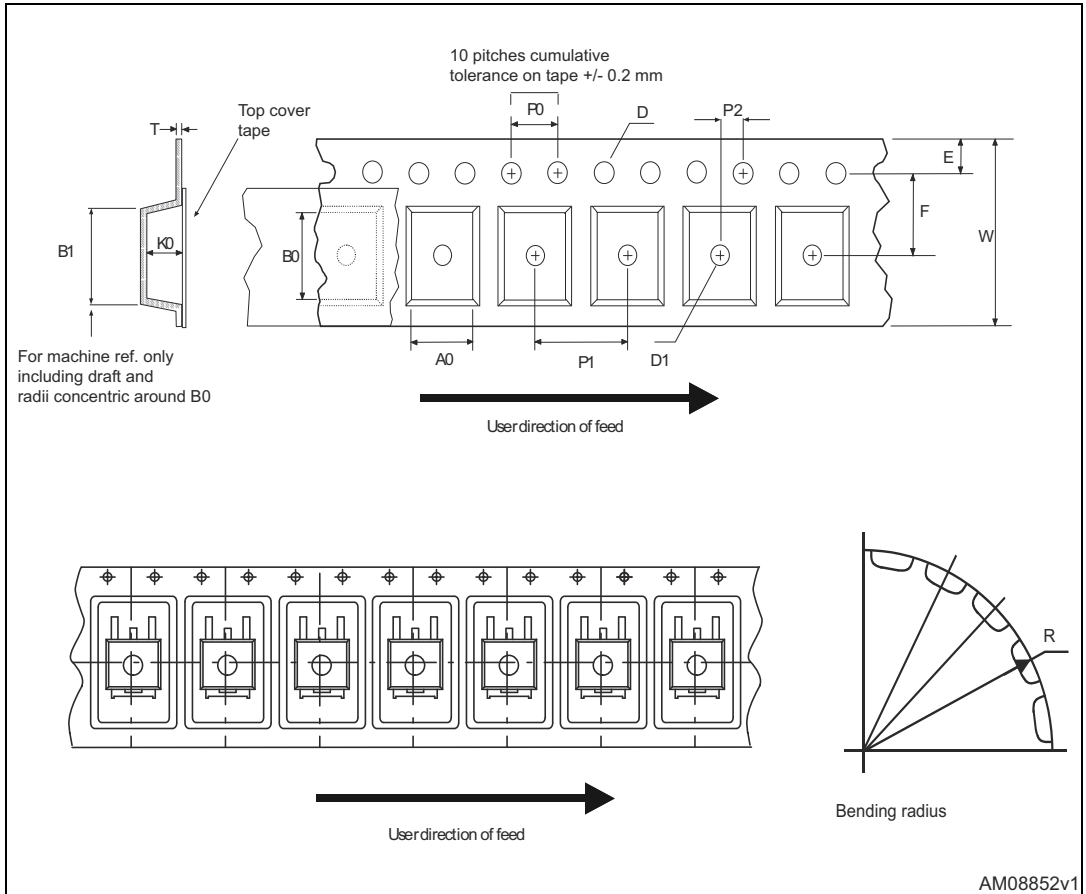


Figure 24. Reel

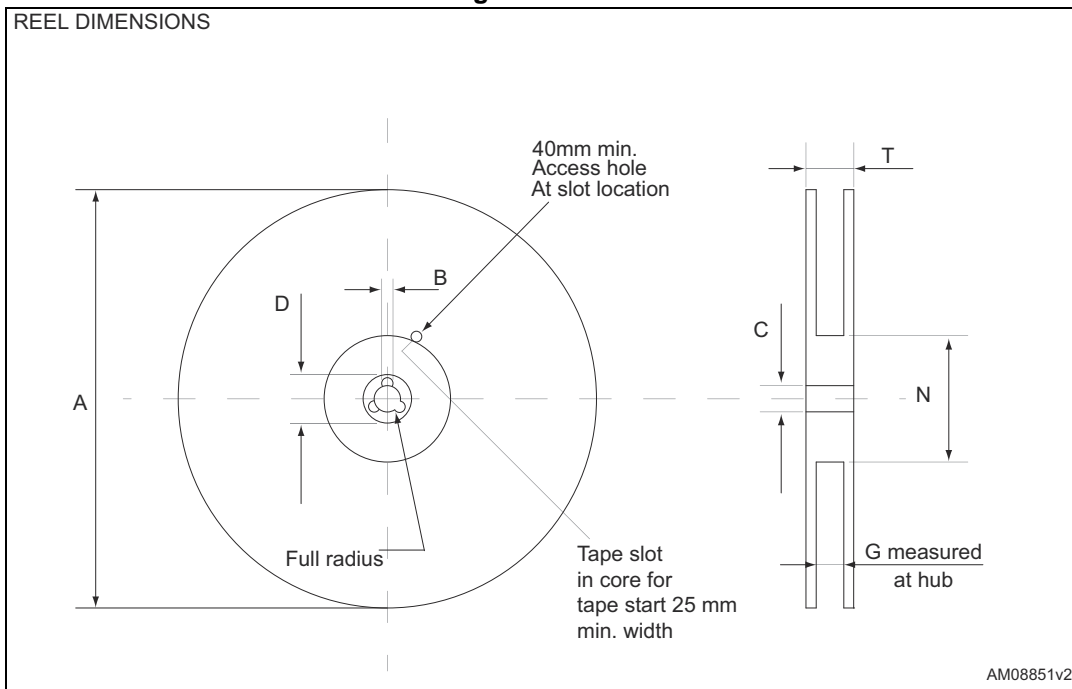


Table 11. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Jun-2004	4	Stylesheet update. No content change
14-May-2008	5	Inserted D ² PAK
18-Jun-2015	6	Updated Table 1: Device summary . Updated Section 4: Package information and Section 5: Packing information .

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- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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