

## Passivated Assembled Circuit Elements, 40 A



PACE-PAK (D-19)

### FEATURES

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200  $V_{RRM}/V_{DRM}$
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved
- RoHS compliant



### DESCRIPTION

The P400 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

### PRODUCT SUMMARY

$I_D$	40 A
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### MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	CHARACTERISTICS	VALUES	UNITS
$I_D$	80 °C	40	A
$I_{FSM}$	50 Hz	385	A
	60 Hz	400	
$I^2t$	50 Hz	745	A <sup>2</sup> s
	60 Hz	680	
$I^2\sqrt{t}$		7450	A <sup>2</sup> √s
$V_{RRM}$	Range	400 to 1200	V
$V_{ISOL}$		2500	V
$T_J$		- 40 to 125	°C

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}$ MAXIMUM AT $T_J$ MAXIMUM mA
P401, P421, P431	400	500	10
P402, P422, P432	600	700	
P403, P423, P433	800	900	
P404, P424, P434	1000	1100	
P405, P425, P435	1200	1300	



ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum DC output current at case temperature	$I_D$	Full bridge circuits		40	A
				80	°C
Maximum peak, one-cycle non-repetitive on-state or forward current	$I_{TSM}$ , $I_{FSM}$	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	A
		t = 8.3 ms			
		t = 10 ms	100 % $V_{RRM}$ reapplied		
		t = 8.3 ms			
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	A <sup>2</sup> s
		t = 8.3 ms			
		t = 10 ms	100 % $V_{RRM}$ reapplied		
		t = 8.3 ms			
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied $I^2t$ for time $t_x = I^2\sqrt{t} \cdot \sqrt{t_x}$		7450	A <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		0.83	V
High level value of threshold voltage	$V_{T(TO)2}$	$I > \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		1.03	
Low level value of on-state slope resistance	$r_{\theta 1}$	$(16.7\% \times \pi \times I_{T(AV)}) < I < \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		9.61	mΩ
High level value of on-state slope resistance	$r_{\theta 2}$	$I > \pi \times I_{T(AV)}$ , $T_J = T_J$ maximum		7.01	
Maximum on-state voltage drop	$V_{TM}$	$I_{TM} = \pi \times I_{T(AV)}$ , $T_J = 25\text{ °C}$		1.4	V
Maximum forward voltage drop	$V_{FM}$	$I_{TM} = \pi \times I_{T(AV)}$ , $T_J = 25\text{ °C}$		1.4	V
Maximum non-repetitive rate of rise of turned-on current	dI/dt	$T_J = 125\text{ °C}$ from 0.67 $V_{DRM}$ $I_{TM} = \pi \times I_{T(AV)}$ , $I_g = 500\text{ mA}$ , $t_r < 0.5\text{ }\mu\text{s}$ , $t_p > 6\text{ }\mu\text{s}$		200	A/μs
Maximum holding current	$I_H$	$T_J = 25\text{ °C}$ anode supply = 6 V, resistive load		130	mA
Maximum latching current	$I_L$			250	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = 125\text{ °C}$ , exponential to 0.67 $V_{DRM}$ gate open		200	V/μs
Maximum peak reverse and off-state leakage current at $V_{RRM}$ , $V_{DRM}$	$I_{RRM}$ , $I_{DRM}$	$T_J = 125\text{ °C}$ , gate open circuit		10	mA
Maximum peak reverse leakage current	$I_{RRM}$	$T_J = 25\text{ °C}$		100	μA
RMS isolation voltage	$V_{ISOL}$	50 Hz, circuit to base, all terminals shorted, $T_J = 25\text{ °C}$ , t = 1 s		2500	V



<b>TRIGGERING</b>					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	$P_{GM}$			8	W
Maximum average gate power	$P_{G(AV)}$			2	
Maximum peak gate current	$I_{GM}$			2	A
Maximum peak negative gate voltage	$-V_{GM}$			10	V
Maximum gate voltage required to trigger	$V_{GT}$	$T_J = -40\text{ °C}$	Anode supply = 6 V resistive load	3	V
		$T_J = 25\text{ °C}$		2	
		$T_J = 125\text{ °C}$		1	
Maximum gate current required to trigger	$I_{GT}$	$T_J = -40\text{ °C}$		90	mA
		$T_J = 25\text{ °C}$		60	
		$T_J = 125\text{ °C}$		35	
Maximum gate voltage that will not trigger	$V_{GD}$	$T_J = 125\text{ °C}$ , rated $V_{DRM}$ applied		0.2	V
Maximum gate current that will not trigger	$I_{GD}$			2	mA

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction operating and storage temperature range	$T_J, T_{Stg}$			- 40 to 125	°C
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation		1.05	K/W
Maximum thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth and greased		0.10	
Mounting torque, base to heatsink <sup>(1)</sup>				4	Nm
Approximate weight				58	g
				2.0	oz.

**Note**

<sup>(1)</sup> A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound

<b>CIRCUIT TYPE AND CODING (1)</b>			
	<b>CIRCUIT "0"</b>	<b>CIRCUIT "2"</b>	<b>CIRCUIT "3"</b>
Terminal positions			
Schematic diagram			
	Single phase hybrid bridge common cathode	Single phase hybrid bridge doubler	Single phase all SCR bridge
Basic series	P40.	P42.	P43.
With voltage suppression	P40.K	P42.K	P43.K
With freewheeling diode	P40.W	-	-
With both voltage suppression and freewheeling diode	P40.KW	-	-

**Note**

(1) To complete code refer to Voltage Ratings table, i.e.: For 600 V P40.W complete code is P402W

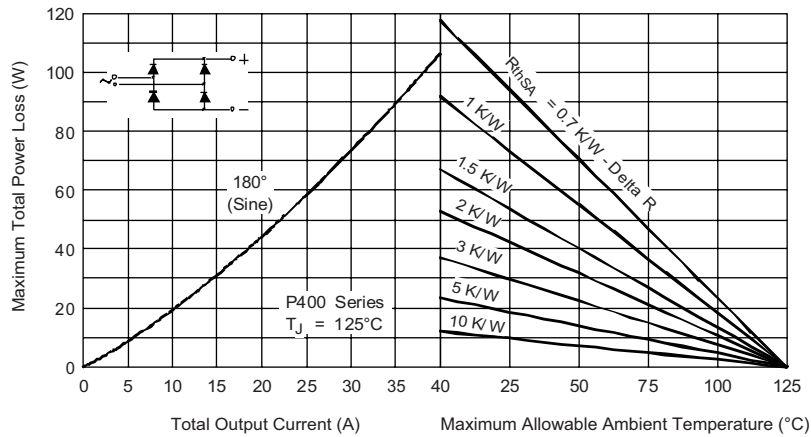


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

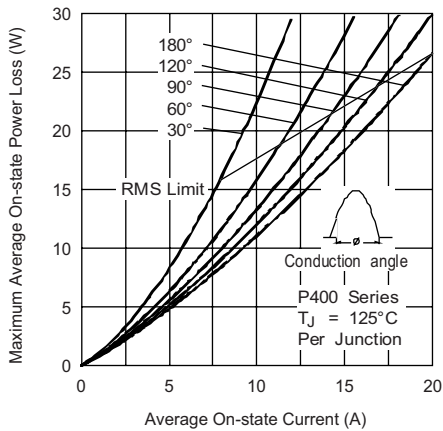


Fig. 2 - On-State Power Loss Characteristics

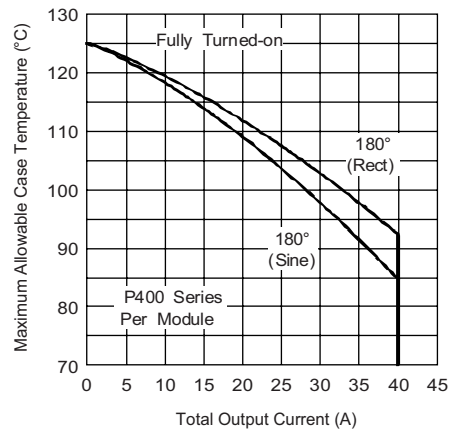


Fig. 4 - Current Ratings Characteristics

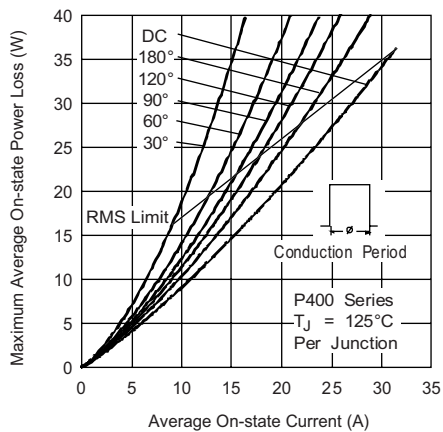


Fig. 3 - On-State Power Loss Characteristics



Fig. 5 - On-State Voltage Drop Characteristics

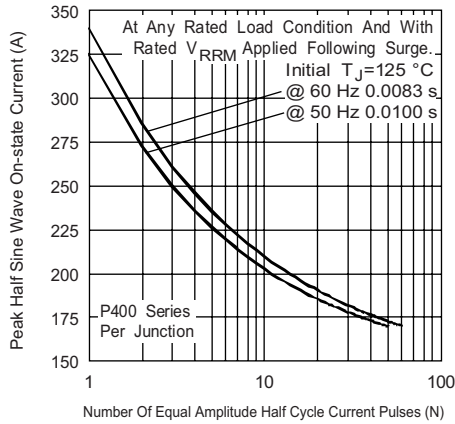


Fig. 6 - Maximum Non-Repetitive Surge Current

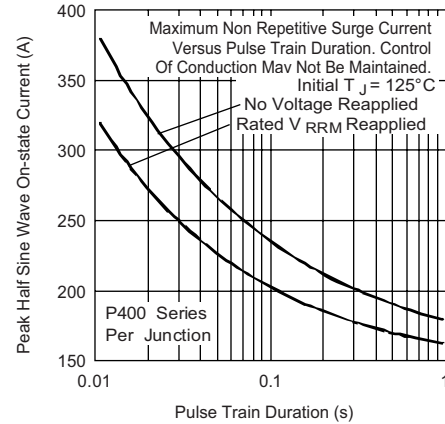


Fig. 7 - Maximum Non-Repetitive Surge Current

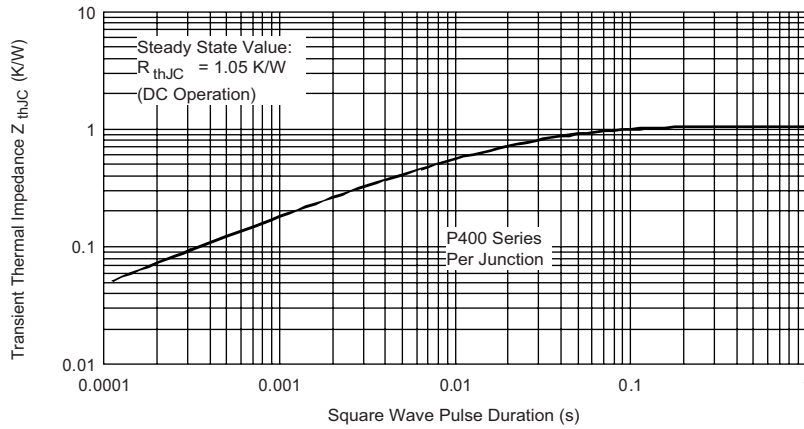


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

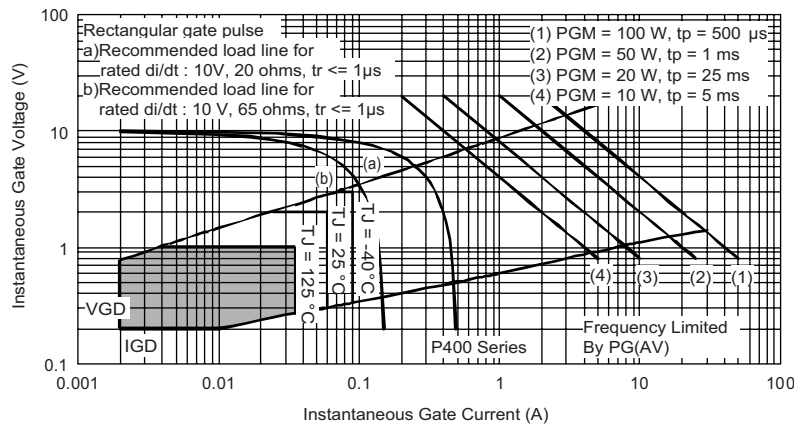


Fig. 9 - Gate Characteristics

### LINKS TO RELATED DOCUMENTS

Dimensions

<http://www.vishay.com/doc?95335>

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