FAIRCHILD SEMICONDUCTOR®

March 2009

# FDS6679AZ
# P-Channel PowerTrench® MOSFET
**-30V, -13A, 9mΩ**

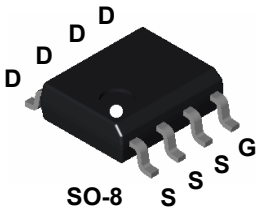
## General Description

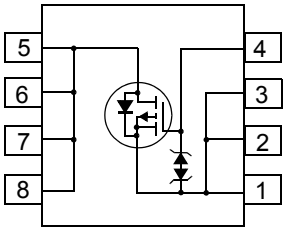
This P-Channel MOSFET is producted using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

## Features

- Max $r_{DS(on)}$ = 9.3mΩ at $V_{GS}$ = -10V, $I_D$ = -13A
- Max $r_{DS(on)}$ = 14.8mΩ at $V_{GS}$ = -4.5V, $I_D$ = -11A
- Extended $V_{GS}$ range (-25V) for battery applications
- HBM ESD protection level of 6kV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handing capability
- RoHS Compliant




## MOSFET Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | -30 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±25 | V |
| $I_D$ | Drain Current -Continuous | (Note 1a) | -13 | A |
| | -Pulsed | | -65 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1.0 | |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | | -55 to +150 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance , Junction to Ambient (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance , Junction to Case (Note 1) | 25 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|
| FDS6679AZ | FDS6679AZ | 13" | 12mm | 2500 units |

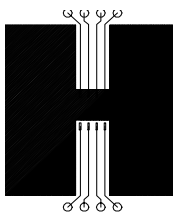
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## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

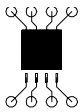
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = -250μA, $V_{GS}$ = 0V | -30 | | | V |
| $\frac{\Delta B_{VDSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250μA, referenced to 25°C | | -20 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -24V, $V_{GS}$=0V | | | -1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±25V, $V_{DS}$=0V | | | ±10 | μA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250μA | -1 | -1.9 | -3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = -250μA, referenced to 25°C | | 6.5 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = -10V, $I_D$ = -13A | | 7.7 | 9.3 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -11A | | 11.8 | 14.8 | |
| | | $V_{GS}$ = -10V, $I_D$ = -13A, $T_J$ = 125°C | | 10.7 | 13.4 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -5V, $I_D$ = -13A | | 55 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -15V, $V_{GS}$ = 0V, f = 1MHz | | 2890 | 3845 | pF |
| $C_{oss}$ | Output Capacitance | | | 500 | 665 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 495 | 745 | pF |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -15V, $I_D$ = -1A $V_{GS}$ = -10V, $R_{GS}$ = 6Ω | | 13 | 24 | ns |
| $t_r$ | Rise Time | | | 15 | 27 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 210 | 336 | ns |
| $t_f$ | Fall Time | | | 92 | 148 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -15V, $V_{GS}$ = -10V, $I_D$ = -13A | | 68 | 96 | nC |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -15V, $V_{GS}$ = -5V, $I_D$ = -13A | | 38 | 54 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | 10 | | nC |
| $Q_{gd}$ | Gate to Drain Charge | | | 17 | | nC |
| **Drain-Source Diode Characteristic** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = -2.1A | | -0.7 | -1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = -13A, di/dt = 100A/μs | | | 40 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | $I_F$ = -13A, di/dt = 100A/μs | | | -31 | nC |

**Notes:**

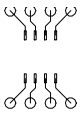
**1:** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 $in^2$ pad of 2 oz copper



b)105°C/W when mounted on a .04 $in^2$ pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

Scale 1 : 1 on letter size paper

**2:** Pulse Test:Pulse Width <300μs, Duty Cycle <2.0%

**3:** The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

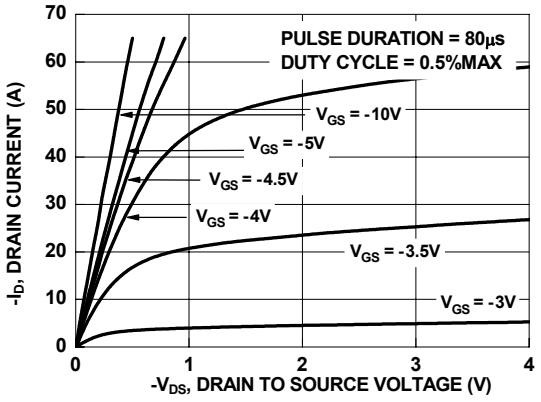



**Figure 1. On Region Characteristics**

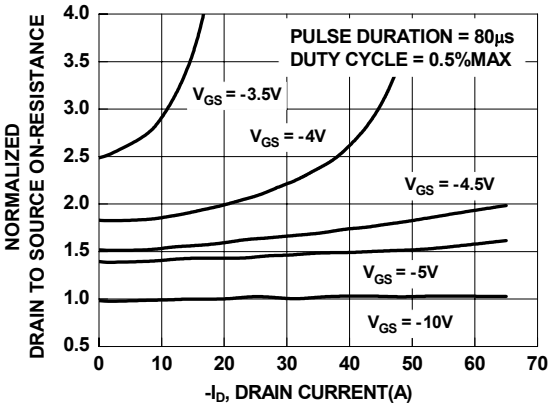



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

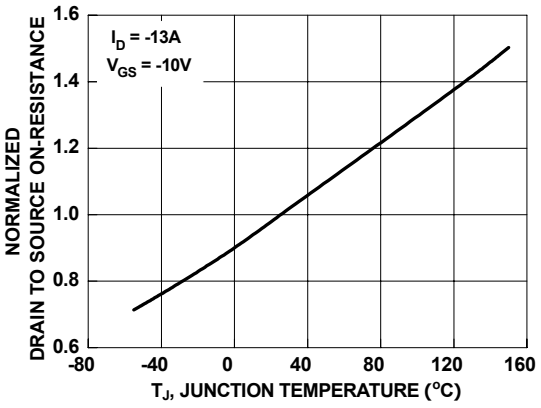



**Figure 3. Normalized On Resistance vs Junction Temperature**

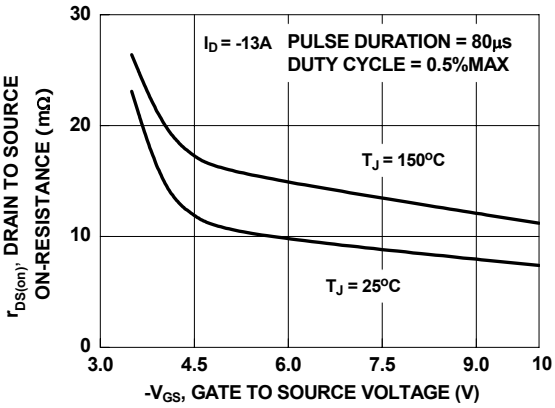



**Figure 4. On-Resistance vs Gate to Source Voltage**

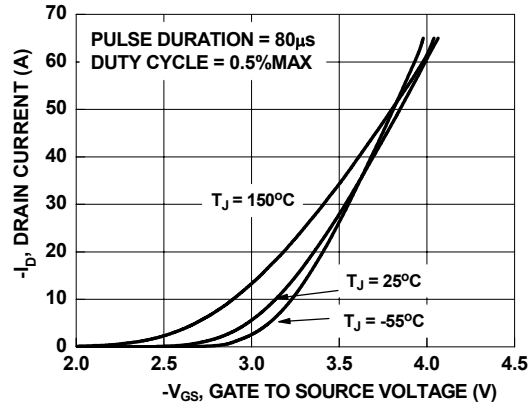



**Figure 5. Transfer Characteristics**

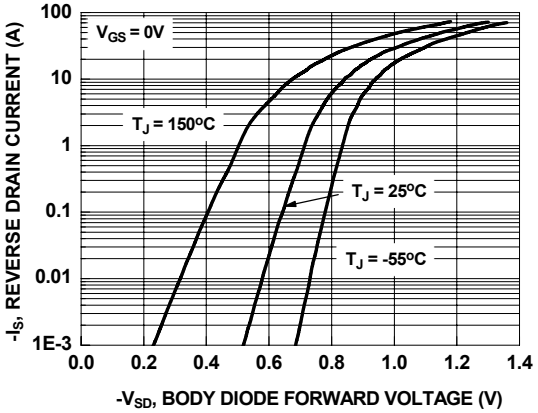



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

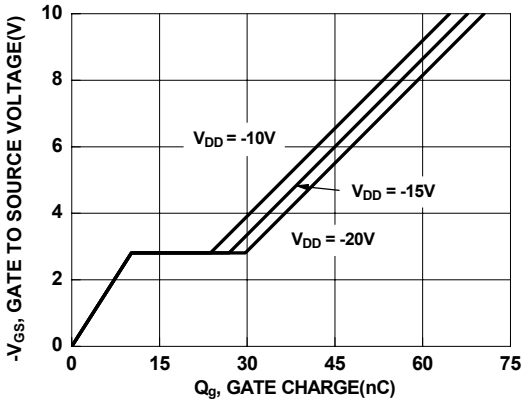



**Figure 7. Gate Charge Characteristics**

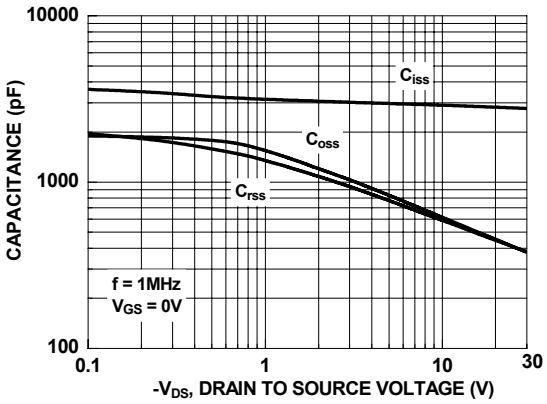



**Figure 8. Capacitance vs Drain to Source Voltage**

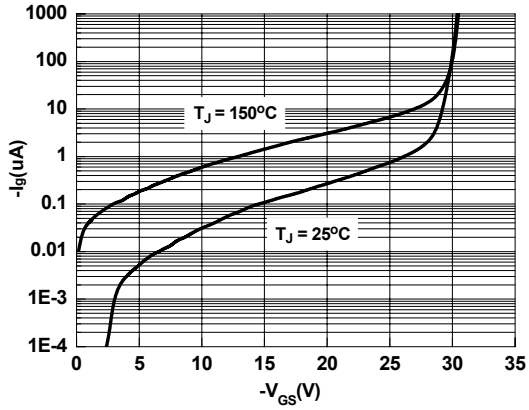



**Figure 9. $I_g$ vs $V_{GS}$**

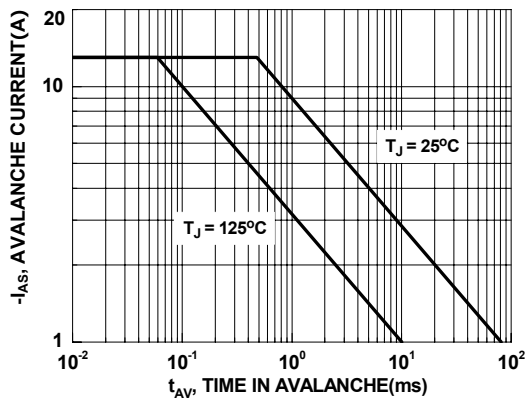



**Figure 10. Unclamped Inductive Switching Capability**

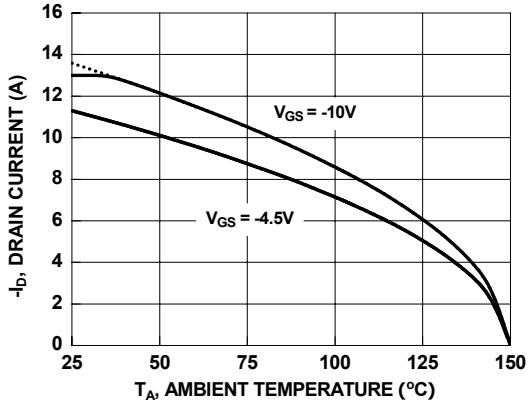



**Figure 11. Maximum Continuous Drain Current vs Ambient Temperature**

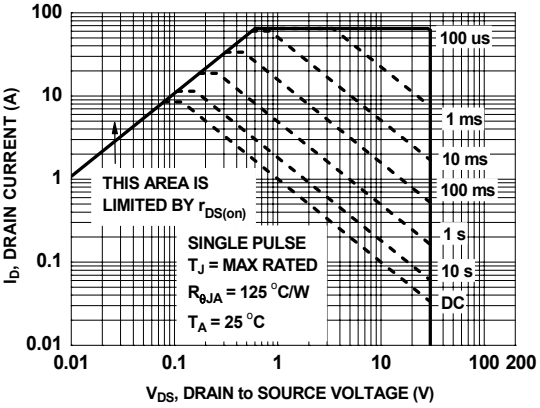



**Figure 12. Forward Bias Safe Operating Area**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

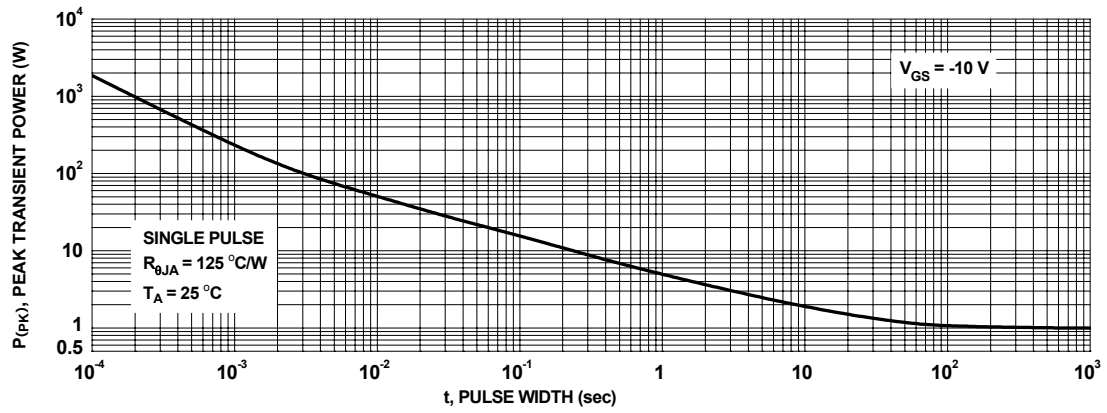



**Figure 13. Single Pulse Maximum Power Dissipation**

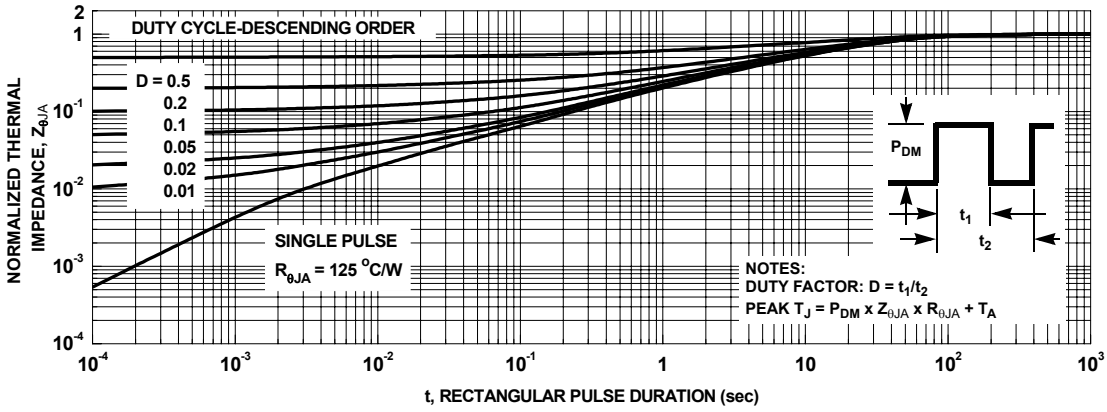



**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

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Rev. I39

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