LatticeMico32/DSP Development Board

User's Guide

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Introduction

This document describes the features and functionality of the LatticeMico32/DSP Development Board. This board is designed as a hardware platform for design and development with the LatticeMico32 microprocessor, as well as for the LatticeMico8 microcontroller, and for various DSP functions.

This document describes the numerous functional elements of the board. The schematics of the board can be found in the appendix at the end of this document.

Features

- LatticeECP™ FPGA with 33,800 LUT4s, 131 kbit of embedded RAM, 4 PLLs, and 360 user I/O pins
- Lattice MachXO™ with 640 LUTs
- Serial Flash with 8 Mbit for non-volatile storage of FPGA configuration data.
- DDR SODIMM socket for DDR SDRAM modules (DDR1, 100-133MHz, 32-bit data bus)
- Parallel Flash 2x128 Mbit, organized as 8M 32-bit words
- SRAM 2x4 Mbit, organized as 256K 32-bit words
- USB 2.0 connector and integrated ispDOWNLOAD® cable for programming the FPGA
- Flywire connector for programming using an ispDOWNLOAD cable (available separately)
- 9-pin RS232 serial port (230 Kbps)
- 15-pin VGA (64 color encoding)
- Ethernet 10/100 M full/half duplex
- Two USB 2.0 compatible host connectors
- One USB 2.0 compatible target connector
- One USB OTG (On-the-Go) connector
- Expansion connector with 46 user I/Os
- 12x12 prototyping area for the integration of individual components (connections to the FPGA)
- 8x6 prototyping area for the integration of individual components (connections to the MachXO)
- Sigma Delta D/A converter
- Crimp connector with 5 signal pairs for high-speed data transfer
- Audio interface (line-in, line-out, and microphone) CODEC
- LCD connector for character displays, with contrast potentiometer
- 25 MHz oscillator with clock distribution buffer
- Eight LEDs with test points for each LED
- Two-character 7-segment display
- Green LED to indicate the proper operation of the 3.3V and 2.5 V power supplies
- Blue LED which shows the configuration status ("DONE")
- Red LED to signal that the FPGA can be configured ("INIT")
- Yellow LED indicating the FPGA PROGRAM# I/O is asserted ("PROGRAM#")
- 3x4 key matrix

- Four DIP switches
- Single step key
- Program key to initiate the configuration sequence of the FPGA
- Reset key
- 5V power supply
- Switching regulator for the generation of the 3.3V I/O voltage, the 2.5V DDR and LVDS voltages and the 1.2V core voltage

Getting Started

1. Unpack all components and compare them to the packaging list. All boards leave the factory fully tested. Detailed information can be found in the Troubleshooting section of this document.
2. Place the board in front of you so that the keyboard is on the left side.
3. Take the regulated DC power supply which has been supplied with the package and connect it to the power jack on the board. Two green power-on LEDs will illuminate to confirm that power is correctly applied to the board (regulating 5V to 3.3V and 2.5V).
4. To check the basic functionality, please see the Troubleshooting section of this document.

A number of example and demonstration programs are available for the LatticeMico32/DSP Development board. Check the Lattice web site at: www.latticesemi.com/boards (and navigate to the correct board) to find additional documentation, and design and programming files.

Note: Unless described otherwise, positional statements (left, right etc.) refer to the board positioned in front of you so that the key pad is in the bottom left corner.

Related Literature

- **LatticeMico32 Development Kit User's Guide**: This guide includes a tutorial for using the LatticeMico32 System software with the LatticeMico32/DSP Development Board.
- **LatticeMico32/DSP Demonstration**: This includes a documented demonstration of a DSP example using the LatticeMico32/DSP Development board.

These documents can be downloaded from the Lattice web site at: www.latticesemi.com/boards. Select the **FPGA/FPSC Boards -> LatticeMico32/DSP Development board** and click on the **User Manuals** link.

Overview

The following block diagram gives you an overview of the functionality of your LatticeMico32/DSP Development Board. Subsequent pages illustrate the position of connectors, user interfaces, and modules.

Figure 1. LatticeMico32/DSP Development Board Block Diagram

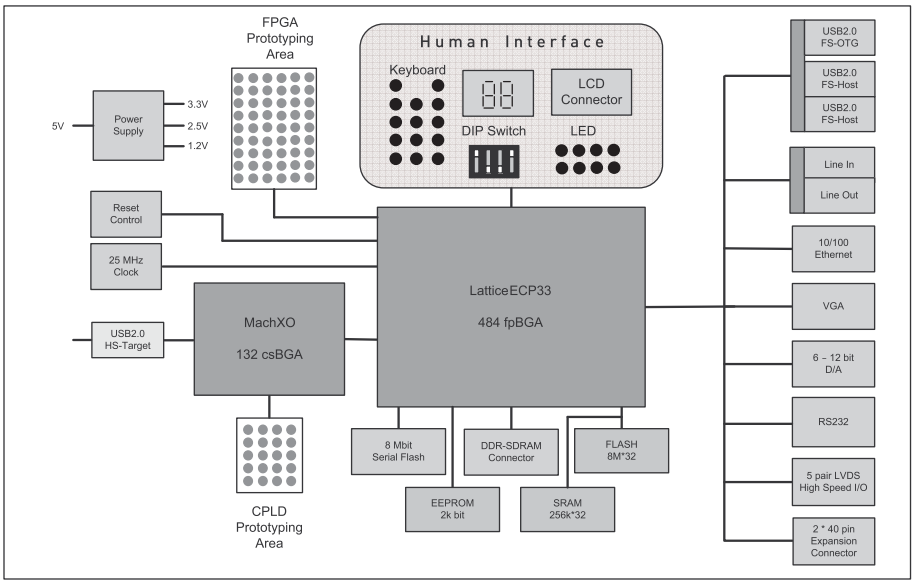


Table 1. Board Defaults

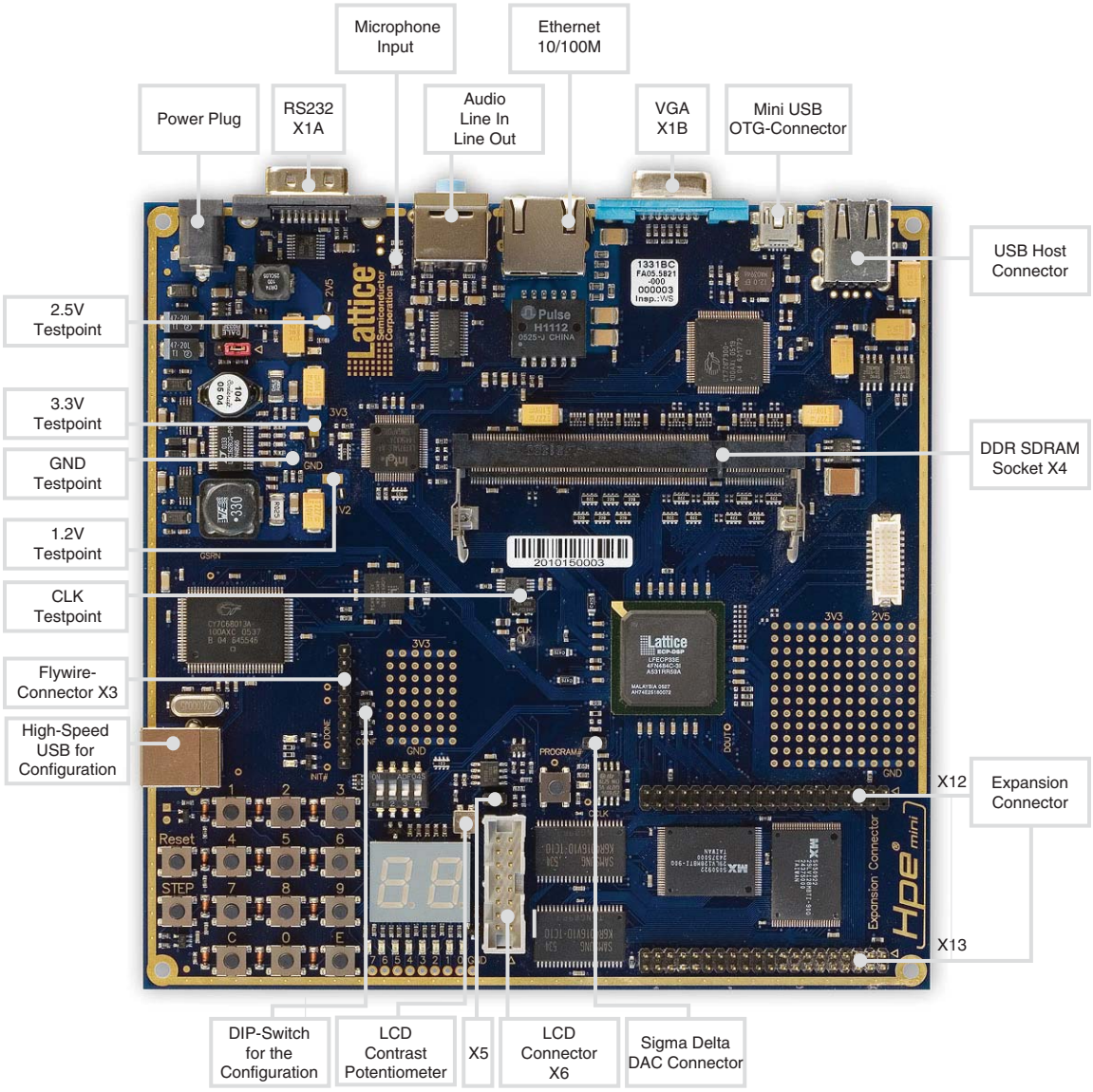
Item	Type	Default Status	Comments
LatticeECP33	FPGA	Programmed	The bitstream is based on Example PlatformA and the LED7SegsTest project. The LED7SegsTest.mem and LED7SegsTest.bit files are included in the LED7SegsTest project. Visual indications of operation are: • Left to Right and Right to Left scanning of the 8 LEDs. • Upcount and roll over of the 7 segment displays from 0 to 99 decimal at ~1 second intervals.
LCD Backlight (X5)	Jumper	Open	Backlight is off.
Configuration Switch	TMS Switch	Off (Down)	LatticeECP33 device can be programmed.
Sigma Delta DAC Converter	Jumper	Open	
Contrast Control	Reostat	Varible	Not set to any specific level.
4-place DIP - Logic 1	Switch	Off	Logic 0 on selected pins - see Table 18.
SODIMM DDR 400 Setting (X18)	Jumper	Shorts Pins 1 and 2	Set to below DDR400 memory use.

Peripheral Interfaces

This section describes all peripheral interfaces of the LatticeMico32/DSP Development Board in alphabetical order.

Figure 2 shows the position of peripheral interfaces available on the board.

Figure 2. Peripheral Interfaces



Audio Interface

The audio interface has two connectors for 3.5 mm stereo jacks. The upper one is for line-out, the lower for line-in. They are connected to the audio codec TLV320AIC23BIPW from Texas Instruments.

Table 2. Audio Codec U1001 Pin Definitions

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
3	CODEC BCLK	W1	21	CODEC CS#	W4
4	CODEC DIN	W2	6	CODEC DOUT	W3
5	CODEC LRCIN	AA1	7	CODEC LRCOUT	Y2
25	CODEC MCLK	Y3	24	CODEC SCLK	Y1
23	CODEC SDIN	AA2	22	CODEC MODE	V4

The signal CODEC CS# has a pull-up resistor of 10 kΩ. The Signal CODEC MODE selects the interface to use for the codec. Driving it high corresponds to SPI, low to I^2C.

Detailed information on the audio codec can be found at the Texas Instruments web site at www.ti.com.

Clock Sources

A 25 MHz oscillator supplies the FPGA (primary clock pin A10 and PLL input V1), the MachXO (pin A8), the Ethernet controller and the Expansion Connector (pin 29 of X12). The frequency can be measured via testpoint CLK. A 25MHz input clock is required by the Ethernet controller. To generate other clock frequencies, use the PLLs of the FPGA. You can find detailed information for the usage of the PLLs on the Lattice web site and in the LatticeECP/EC Family Data Sheet.

The USB controller requires a 24 MHz quartz oscillator for configuration. Another 12 MHz quartz supplies the USB host/peripheral controller.

DDR SODIMM Socket for DDR SDRAM Modules

The board includes a standard DDR1 SODIMM socket with 200 contacts (DDR SDRAM Module is not included). The upper four bytes of the data bus are not connected. Thus, only half of the capacity of the memory module is available.

The DDR SODIMM socket is factory configured to provide a regulated 2.5V. DDR400 modules require a power supply of 2.6V (±0.1V). To support DDR400, you must short-circuit pins 2 and 3 of connector X18. Position 1-2 is used for 2.5V mode. If you have your board in front of you so that the power supply is in the upper left corner, pin 1 is the right-most one and is marked with a copper etched triangle.

Note:In bank 2, there are four DQSs. Two of them do not have the required DQ pins available. Therefore, only two DDR interfaces are valid. So, the LatticeECP33 can have a 16-bit DDR interface.

Table 3. DDR SODIMM Socket (X4) - Data Bus, n.c. ... Not Connected

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
11	DDR DQS0	A16	47	DDR DQS2	H18
12	DDR DM0	B15	48	DDR DM2	H19
5	DDR DQ0	A14	41	DDR DQ16	D21
7	DDR DQ1	B14	43	DDR DQ17	F20
13	DDR DQ2	A15	49	DDR DQ18	G21
17	DDR DQ3	B16	53	DDR DQ19	G20
6	DDR DQ4	A17	42	DDR DQ20	H20
8	DDR DQ5	B17	44	DDR DQ21	J19
14	DDR DQ6	A18	50	DDR DQ22	J18
18	DDR DQ7	B18	54	DDR DQ23	H17
25	DDR DQS1	D21	61	DDR DQS3	J20
26	DDR DM1	D21	62	DDR DM3	K20

Table 3. DDR SODIMM Socket (X4) - Data Bus, n.c. ... Not Connected (Continued)

19	DDR DQ8	B22	55	DDR DQ24	F22
23	DDR DQ9	B21	59	DDR DQ25	G22
29	DDR DQ10	C21	65	DDR DQ26	H22
31	DDR DQ11	C22	67	DDR DQ27	H21
20	DDR DQ12	E20	56	DDR DQ28	K19
24	DDR DQ13	E18	60	DDR DQ29	K18
30	DDR DQ14	F19	66	DDR DQ30	L18
32	DDR DQ15	F18	68	DDR DQ31	L19

Table 4. DDR SODIMM Socket (X4) - Address Bus

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
112	DDR A0	D16	111	DDR A1	C16
110	DDR A2	E15	109	DDR A3	D15
108	DDR A4	C15	107	DDR A5	E14
106	DDR A6	D14	105	DDR A7	C14
102	DDR A8	E13	101	DDR A9	D13
115	DDR A10	E16	100	DDR A11	C13
99	DDR A12	B13	123	DDR A13	C17
117	DDR BA0	E17	116	DDR BA1	D17

Table 5. DDR SODIMM Socket (X4) - Other Signals

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
35	DDR CK0+	B12	37	DDR CK0-	A12
160	DDR CK1+	A20	158	DDR CK1-	B19
96	DDR CKE0	A13	95	DDR CKE1	C12
118	DDR RAS#	C18	119	DDR WE#	D18
120	DDR CAS#	A19	121	DDR S0#	C19

Ethernet Interface

An Intel LXT971A is included for Ethernet PHY. This is an IEEE-compliant Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications, full and half duplex. For more information, please refer to the data sheet of this component.

Table 6. Ethernet Controller U0801 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
4	HPE RESOUT#	H6	42	ETH MDIO	K4
43	ETH MDC	K5	45	ETH RXD3	F2
46	ETH RXD2	G3	47	ETH RXD1	G2
48	ETH RXD0	G1	49	ETH RXDV	J4
52	ETH RXCLK	K1	53	ETH RXER	J5
54	ETH TXER	J2	55	ETH TXEN	J3
56	ETH TXCLK	J1	57	ETH TXD0	H1
58	ETH TXD1	H2	59	ETH TXD2	H3
60	ETH TXD3	H4	62	ETH COL	K2
63	ETH CRS	K3	64	ETH MDINTR#	F1

Expansion Connector

The expansion connector provides 46 user I/Os connected to the FPGA. The remaining pins serve as power and clock supplies for expansion boards. The expansion connector is configured as two 2x20 100mil centered pin headers (X12 and X13). Tables 7 and 8 describe the connections to the FPGA.

Table 7. Expansion Connector X12

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	GND	—	2	n.c. (coding)	—
3	VCC2V5	—	4	EXPCON IO29	W21
5	EXPCON IO30	W20	6	EXPCON IO31	W19
7	EXPCON IO32	Y20	8	EXPCON IO33	AA22
9	EXPCON IO34	AA21	10	EXPCON IO35	AB21
11	EXPCON IO36	T17	12	EXPCON IO37	T14
13	EXPCON IO38	T13	14	EXPCON IO39	U14
15	EXPCON IO40	U13	16	EXPCON IO41	U12
17	EXPCON IO42	U11	18	EXPCON IO43	V14
19	EXPCON IO44	V13	20	EXPCON IO45	W13
21	VCC5V0	—	22	GND	—
23	VCC2V5	—	24	GND	—
25	VCC3V3	—	26	GND	—
27	VCC3V3	—	28	GND	—
29	EXPCON OSC	—	30	GND	—
31	EXPCON CLKIN	—	32	GND	—
33	EXPCON CLKOUT	—	34	GND	—
35	VCC3V3	—	36	GND	—
37	VCC3V3	—	38	GND	—
39	VCC3V3	—	40	GND	—

Table 8. Expansion Connector X13

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	HPE RESET#	—	2	GND	—
3	EXPCON IO0	K22	4	EXPCON IO01	K21
5	EXPCON IO2	L22	6	EXPCON IO03	L21
7	EXPCON IO4	L20	8	EXPCON IO05	M22
9	EXPCON IO6	M21	10	EXPCON IO07	M20
11	EXPCON IO8	M19	12	EXPCON IO09	M18
13	EXPCON IO10	N22	14	EXPCON IO11	N21
15	EXPCON IO12	N20	16	EXPCON IO13	N19
17	EXPCON IO14	N18	18	EXPCON IO15	P22
19	GND	—	20	VCC3V3	—
21	EXPCON IO16	P21	22	GND	—
23	EXPCON IO17	P20	24	GND	—
25	EXPCON IO18	P18	26	GND	—
27	EXPCON IO19	P19	28	EXPCON IO20	R22
29	EXPCON IO21	R21	30	GND	—
31	EXPCON IO22	R19	32	EXPCON IO23	R18

Table 8. Expansion Connector X13 (Continued)

33	EXPCON IO24	R17	34	GND	—
35	EXPCON IO25	T22	36	EXPCON IO26	T18
37	EXPCON IO27	U22	38	CARDSEL#	V20
39	EXPCON IO28	V19	40	GND	—

ispDOWNLOAD Cable Connector

There are two ways to configure the programmable Lattice devices on the board. The USB connector requires a standard USB cable, and is described later in this document. Connector X3 is available to connect a Lattice ispDOWNLOAD cable. An ispDOWNLOAD cable is used to program IEEE 1532 compliant programmable devices. Lattice provides either a parallel port or a USB port download cable. The FPGA and CPLD are programmed using the cable and ispVM® programming software.

DIP switch SW0302[1] controls the device to be configured: the FPGA or the MachXO. If it is on (in top position), the MachXO is selected; if off, the FPGA is selected.

The ispVM System software can be downloaded from the Lattice web site at: www.latticesemi.com/ispvm.

Note: Do not change the switch when the configuration of a device is in progress!

Note: The board as configured from the factory, has a built-in USB ispDOWNLOAD cable. The built-in cable and an external ispDOWNLOAD cable cannot be used at the same time.

Table 9. ispDOWNLOAD Connector X3 Pin Definition

Pin	Signal Name	Pin	Signal Name
1	VCC3V3	2	JTAG_TDO
3	JTAG_TDI	4	JTAG_PROG
5	JTAG_TRST	6	JTAG_TMS
7	GND	8	JTAG_TCK
9	JTAG_DONE	10	JTAG_INIT

High-Speed LVDS Connector

On the right side of the board there is a 20-pin jack for connecting crimp cables. Five LVDS signal pairs of the FPGA are wired with the connector (see Table 10). This interface serves as a means for high-speed data transfer.

Figure 3. 20-pin DF13 Connector by Hirose

1. Caption on the board: CONF.

Table 10. High-Speed Connector X14 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	HSCON DAT0-	E21	2	HSCON DAT0+	D22
3	GND	—	4	GND	—
5	HSCON DAT1-	G19	6	HSCON DAT1+	G18
7	GND	—	8	GND	—
9	HSCON DAT2-	F21	10	HSCON DAT2+	E22
11	GND	—	12	GND	—
13	HSCON DAT3-	J22	14	HSCON DAT3+	J21
15	GND	—	16	GND	—
17	HSCON DAT4-	G17	18	HSCON DAT4+	F17
19	GND	—	20	GND	—

LCD Connector (Optional)

The LCD connector is a 16-pin header with a standard pinning for LCD modules with back-light (e.g. Truly MTC-C202DPRN-1N). In order to use an LCD module, attach it to the connector via a 16-pin ribbon cable.

Note: The LCD module is tied to a 5V supply. The LatticeECP33 to LCD interface is 3.3V.

Put a jumper on connector X5 to turn on the backlight of the LCD. The contrast of the LCD module is adjustable with the potentiometer R0526, because different LCD modules need different voltages for the best contrast.

Figure 4. LCD Panel (Not Included)

Table 11. LCD Connector X6 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	GND	—	2	VCC5V	—
3	CONTRAST	—	4	LCD REGSEL	P3
5	LCD RW	P4	6	LCD ENABLE	P5
7	SEG A#/DB0	M3	8	SEG B#/DB1	M4
9	SEG C#/DB2	M5	10	SEG D#/DB3	N1
11	SEG E#/DB4	N2	12	SEG F#/DB5	N3
13	SEG G#/DB6	N4	14	SEG DP#/DB7	N5
15	BACKLIGHT	—	16	GND	—

Serial Interface

The board includes an RS232 serial interface port. The interface provides transmit (TX), receive (RX), and hardware handshaking. The MAXIM MAX3232 data sheet provides detailed information on the interface circuit. A 9-pin female to 9-pin female null modem cable is required.

Table 12. Serial Interface X1C Pin Definitions

Signal	Direction	Sub-D Pin	RS232 Function	FPGA Pin
RS TXD LVTTL	Out	3	Transmit Data	L1
RS RTS LVTTL	Out	7	Request to Send	L2
RS RXD LVTTL	In	2	Receive Data	M2
RS CTS LVTTL	In	8	Clear to Send	M1

Sigma Delta D/A Converter

The board includes a low-pass filter connected to a dedicated pin of the FPGA. With this, a sigma delta converter can be realized. Great results can be achieved by using a resolution of 8 to 10 bits. Example VHDL code is provided.

Power Supply

Four different voltages are needed: 3.3V I/O voltage, 2.5V DDR and LVDS voltages as well as 1.2V core voltage. The 3.3V supply draws up to 1A, the 2.5V and 1.2V supplies up to 2A of current.

For more information, see the power supply information in the Components section of this document.

Test Points

In order to check the various voltage levels used, several test points are provided. There is one test point for 1.2V, 2.5V, 3.3V, one for ground, and one for accessing the 25MHz oscillator. The 25MHz clock signal can be checked with another test point.

USB Host/Peripheral Interface

There are one USB peripheral and two USB host connectors on board. These are connected to the Cypress CY7C67300 USB Host/Peripheral Controller U0702. This controller is compliant with the Universal Serial Bus Specification 2.0. You can transmit and receive serial data at both full-speed (12 Mbps) and low-speed (1.5 Mbps) data rates. For more information, please refer to the data sheet of the USB controller. U0703 and U0704 are USB power control switches, which must be enabled by the user via the USB PWEN signals. The USB OC signal pulls low to indicate voltage, current and thermal issues.

Table 13. USB GPIO Connections (U0702)

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
94	USB GPIO0	B7	93	USB GPIO1	C7
92	USB GPIO2	D7	91	USB GPIO3	E7
90	USB GPIO4	F7	89	USB GPIO5	A8
87	USB GPIO6	B8	86	USB GPIO7	C8
66	USB GPIO8	D8	65	USB GPIO9	E8
61	USB GPIO10	F8	60	USB GPIO11	A9
59	USB GPIO12	B9	58	USB GPIO13	C9
57	USB GPIO14	D9	56	USB GPIO15	E9
55	USB GPIO16	F9	54	USB GPIO17	G9
53	USB GPIO18	B10	52	USB GPIO19	C10
50	USB GPIO20	D10	49	USB GPIO21	E10
48	USB GPIO22	F10	47	USB GPIO23	G10
46	USB GPIO24	B11	45	USB GPIO25	C11
44	USB GPIO26	D11	43	USB GPIO27	E11
42	USB GPIO28	E12	41	USB GPIO29	pulled up

Table 14. Additional USB GPIO Connections (U0702, U0704, and U0704)

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
U0703:1	USB PWEN0	B2	U0703:2	USB OC0#	E1
U0703:4	USB PWEN1	C2	U0703:3	USB OC1#	D1
U0704:1	USB PWEN2	C3	U0704:2	USB OC2#	D2
U0702:85	HPE RESOUT#	B3			

USB Configuration Connector

In addition to the ispDOWNLOAD connector, the FPGA and the MachXO can also be configured by a standard USB connection. The USB target connector is wired to the Cypress CY7C68013A device (U0301).

This programming method requires the use of the ispVM System software. This can be downloaded from the Lattice web site at: www.latticesemi.com/ispvm.

This connection will appear to the ispVM System software as if a regular USB-based ispDOWNLOAD cable is connected to the PC.

The CY7C68013A in combination with the MachXO CPLD acts as a built-in ispDOWNLOAD cable. The MachXO is connected to the ispDOWNLOAD Connector X3, and can program the LatticeECP33. The LatticeECP33 can be programmed when DIP switch SW0302 is 'off' (pushed down).

Note: Like the ispDOWNLOAD connector, the MachXO drives the JTAG signals when it is programmed for USB configuration. Only use the built-in ispDOWNLOAD cable or an external ispDOWNLOAD cable exclusively. It is not recommended to switch between cables without first power cycling the board. Failure to follow this recommendation may cause unpredictable results and may possibly damage the board.

Table 15. Connections Between the USB Controller (CY7C68013A) and the MachXO Device

Cypress Pin	Signal name	MachXO Pin	Cypress Pin	Signal Name	MachXO Pin
34	GP D0	G14	35	GP D1	G13
36	GP D2	H14	37	GP D3	H13
44	GP D4	H12	45	GP D5	J13
46	GP D6	J12	47	GP D7	K14
80	GP D8	K13	81	GP D9	K12
82	GP D10	L14	83	GP D11	M13
95	GP D12	M14	96	GP D13	M12
97	GP D14	N14	98	GP D15	N13
57	GP ADR0	H1	58	GP ADR1	H2
59	GP ADR2	J1	60	GP ADR3	J3
61	GP ADR4	K1	62	GP ADR5	K2
63	GP ADR6	L1	64	GP ADR7	L3
93	GP ADR8	M1	69	GP SLOE	M3
67	GP INT0	N7	68	GP INT1	M6
71	GP FIFOADR0	M4	72	GP FIFOADR1	N4
70	GP WU2	N3	73	GP PKTEND	P5
74	GP SLCS#	E3	79	USBCF WAKE	N9
3	GP RDY0	D3	4	GP RDY1	E2
5	GP RDY2	F2	6	GP RDY3	F3
7	GP RDY4	G1	8	GP RDY5	G2
54	GP CTL0	D1	55	GP CTL1	C3

Table 15. Connections Between the USB Controller (CY7C68013A) and the MachXO Device (Continued)

56	GP CTL2	C2	51	GP CTL3	C1
52	GP CTL4	B2	76	GP CTL5	B1
23	GP T0	M2	24	GP T1	N1
25	GP T2	P1	28	GP BKPT	F12
100	USB CLK O	M7	26	GP IFCLK	M8
41	GP RXD0	E13	40	GP TXD0	E14
43	GP RXD1	F13	42	GP TXD1	F14

VGA Interface

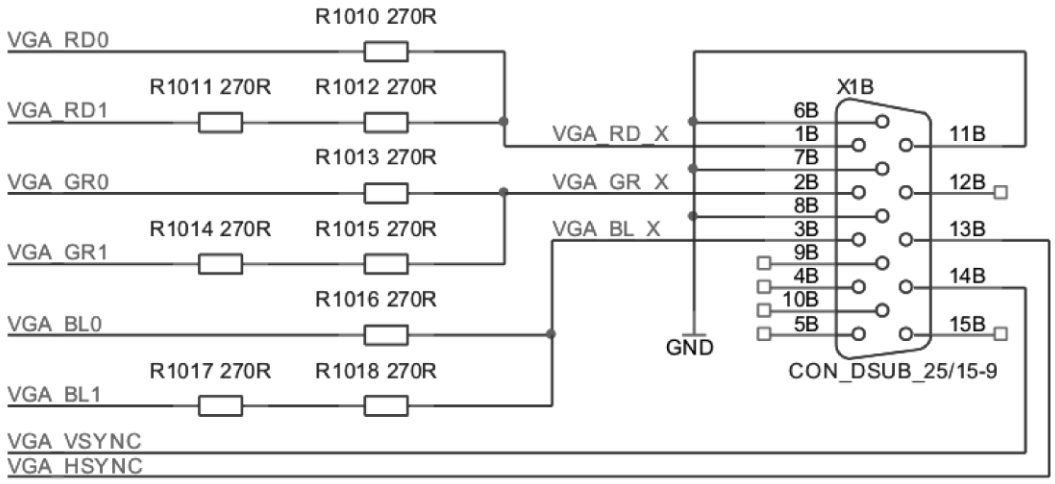
The board includes a VGA connector for driving a VGA monitor. The VGA interface is connected to a 15-pin plug socket. The pin definitions are listed in Table 16.

VGA RD0 and VGA RD1 are both connected to pin 1, but have different series resistors (see Figure 5). Thus, a 6-bit VGA interface is realized. Figure 5 shows the connection of the RGB signals. The FPGA is responsible for generating correct HSYNC and VSYNC sweep frequencies. Understand the SYNC frequencies of the VGA monitor being connected to the VGA plug and adjust the FPGA frequencies as required.

Table 16. VGA Connector X1B Pin Definition, n.c. ... Not Connected

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	VGA RD0	A3	1	VGA RD1	B4
2	VGA GR0	A4	2	VGA GR1	B5
3	VGA BL0	A5	3	VGA BL1	B6
4	n.c.	—	5	n.c.	—
6	GND	—	7	GND	—
8	GND	—	9	n.c.	—
10	GND	—	11	n.c.	—
12	n.c.	—	13	VGA HSYNC	A7
14	VGA VSYNC	A6	15	n.c.	—

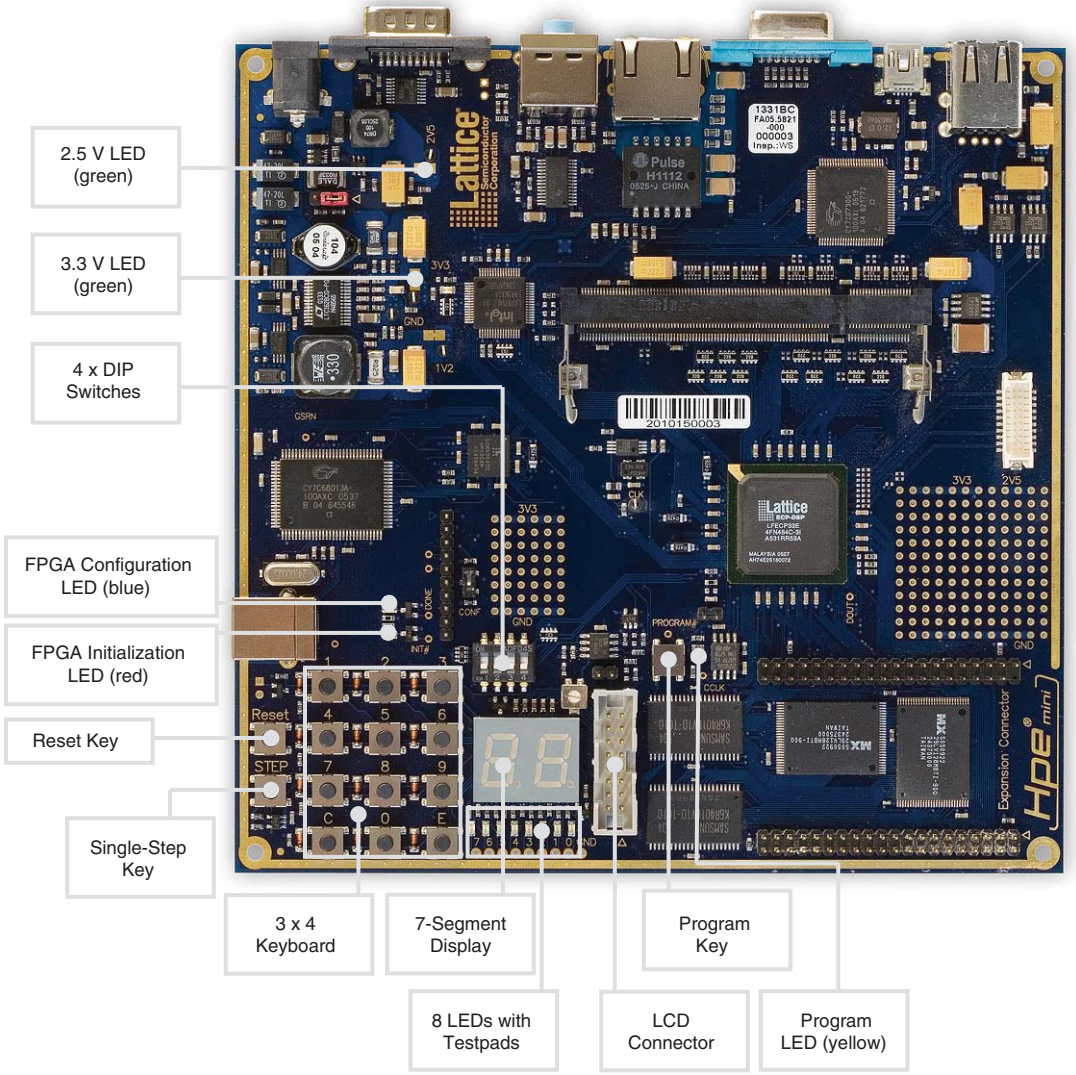
Figure 5. VGA Connector



User Interface

Figure 6 shows the position of the user interface elements.

Figure 6. User Interface Features



7-Segment Display

The 7-segment display is wired as follows:

Table 17. 7 Segment Display U0502 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
A	SED_A#	M3	E	SED_E#	N2
B	SED_B#	M4	F	SED_F#	N3
C	SED_C#	M5	G	SED_G#	N4
D	SED_D#	N1	D, P	SED_DP#	N5
left	SED_CA0#	P1	right	SED_CA1#	P2
common			common		

The signals of the 7-segment display are low-active, which means that with a logic '0', the segment is lit. SEG A# ... SEG F# and SEG DP# drive not only the two 7-segment displays, but also the LCD. To write different data to these three components, the user must drive the signals alternately to the components. This can be realized with the signals SEG CA0#, SEG CA1# and LCD ENABLE. They serve to activate the two 7-segment displays and the LCD, respectively.

DIP Switches

There is a 4-bit DIP switch on the board. When the switch is turned to the on position, a logic '1' will be seen. The connections are in Table 18.

Table 18. DIP Switches SW0514 Connection

Switch	Signal Name	FPGA Pin	Switch	Signal Name	FPGA Pin
SW315			**SW316**		
1	DSW0	R2	2	DSW1	R3
3	DSW2	R4	4	DSW3	R5

LEDs

Eight LEDs can be used for custom status signaling. They are low-active; with a logic '0' the LED is on. You can control the LEDs via the signals below.

Table 19. LED LD0501 ... LD0508 Connection

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	LED0#	E3	5	LED4#	F5
2	LED1#	E4	6	LED5#	G4
3	LED2#	E5	7	LED6#	G5
4	LED3#	F4	8	LED7#	H5

Key Matrix

The board also features a key matrix with 12 push-buttons, which are not debounced. They must be driven with three column lines and can be read with four rows. The following table shows the connections.

Table 20. Key Matrix with the Keys SW302 ... SW313 Definition

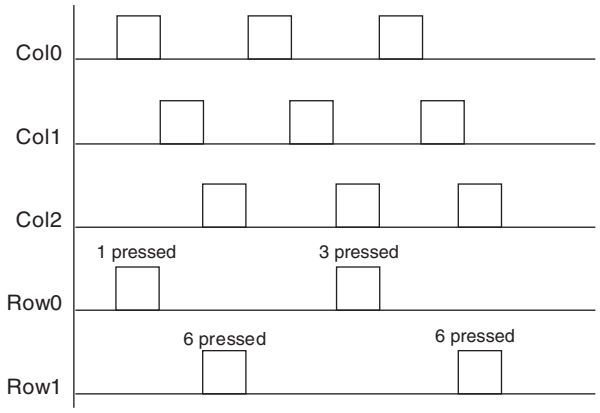
Signal Name	TST_COL0	TST_COL1	TST_COL2
TST_ROW0	1	2	3
TST_ROW1	4	5	6
TST_ROW2	7	8	9
TST_ROW3	C	0	E

Table 21. Key Matrix with the Keys SW302 ... SW313 Connection

Signal Name	FPGA Pin	Signal Name	FPGA Pin
TST_ROW0	T1	TST_COL0	U4
TST_ROW1	T2	TST_COL1	U6
TST_ROW2	T3	TST_COL2	V5
TST_ROW3	R1		

To query all keys of the matrix, you must poll the column driver signals (TST COL0, TST COL1, and TST COL2). If you press a key, a logic '1' appears in the corresponding row. The following diagram explains the functionality:

Figure 7. Polling of the Key Matrix



You do not need the polling method if only four keys are used. Connect the column driver signals of one column to VCC, the other two to GND and query the row data signals.

CPU Reset Key

The CPU reset key is a global reset. Please refer to the Reset Chip section of this document for detailed information.

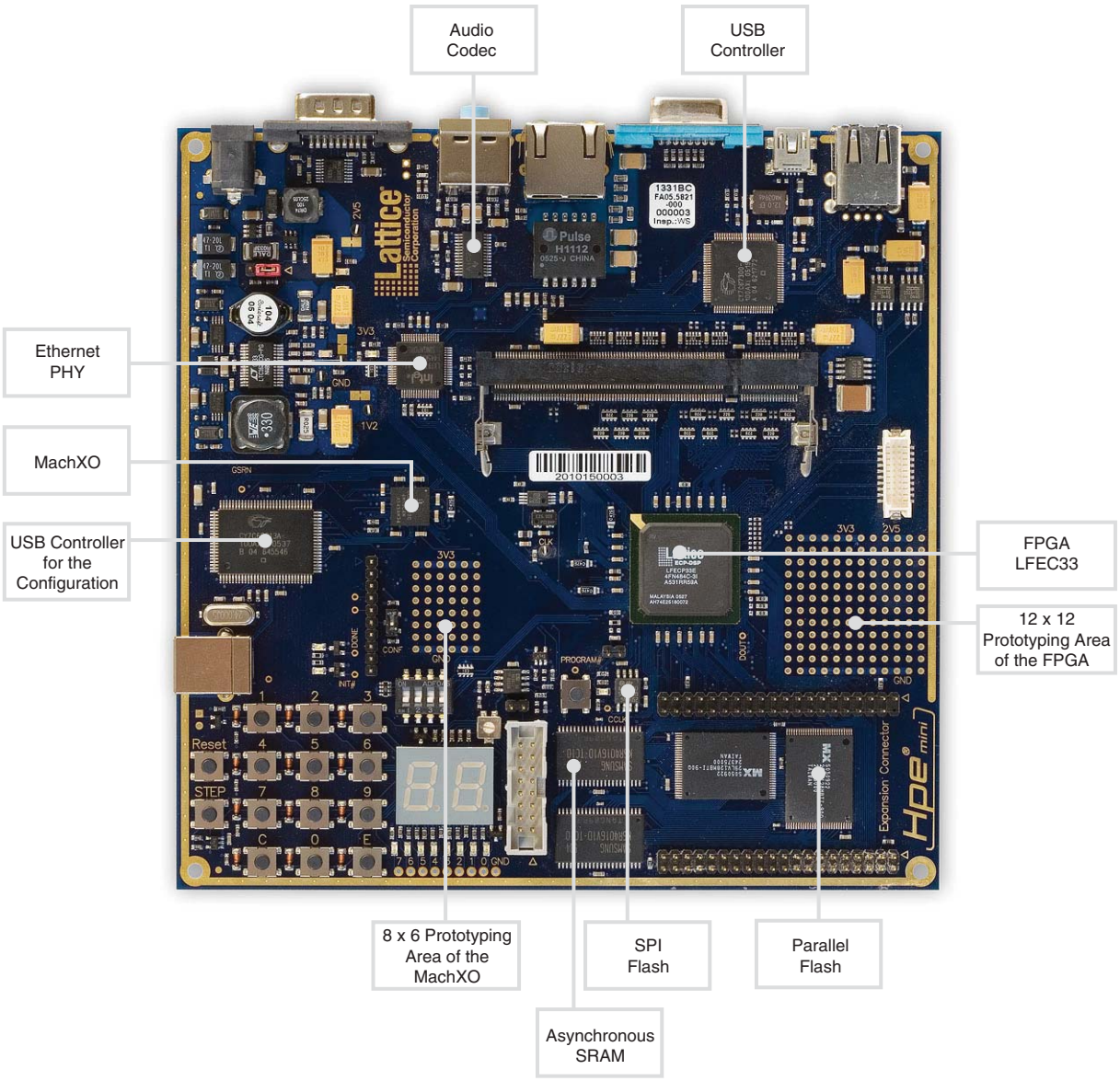
Single Step Key

The single step key is connected to a normal input of the FPGA and can be used by the application as required. This key is connected to a Schmitt trigger, meaning it is debounced. This key is used as a single clock for testing your design.

Components

Figure 8 illustrates the position of major components.

Figure 8. Components



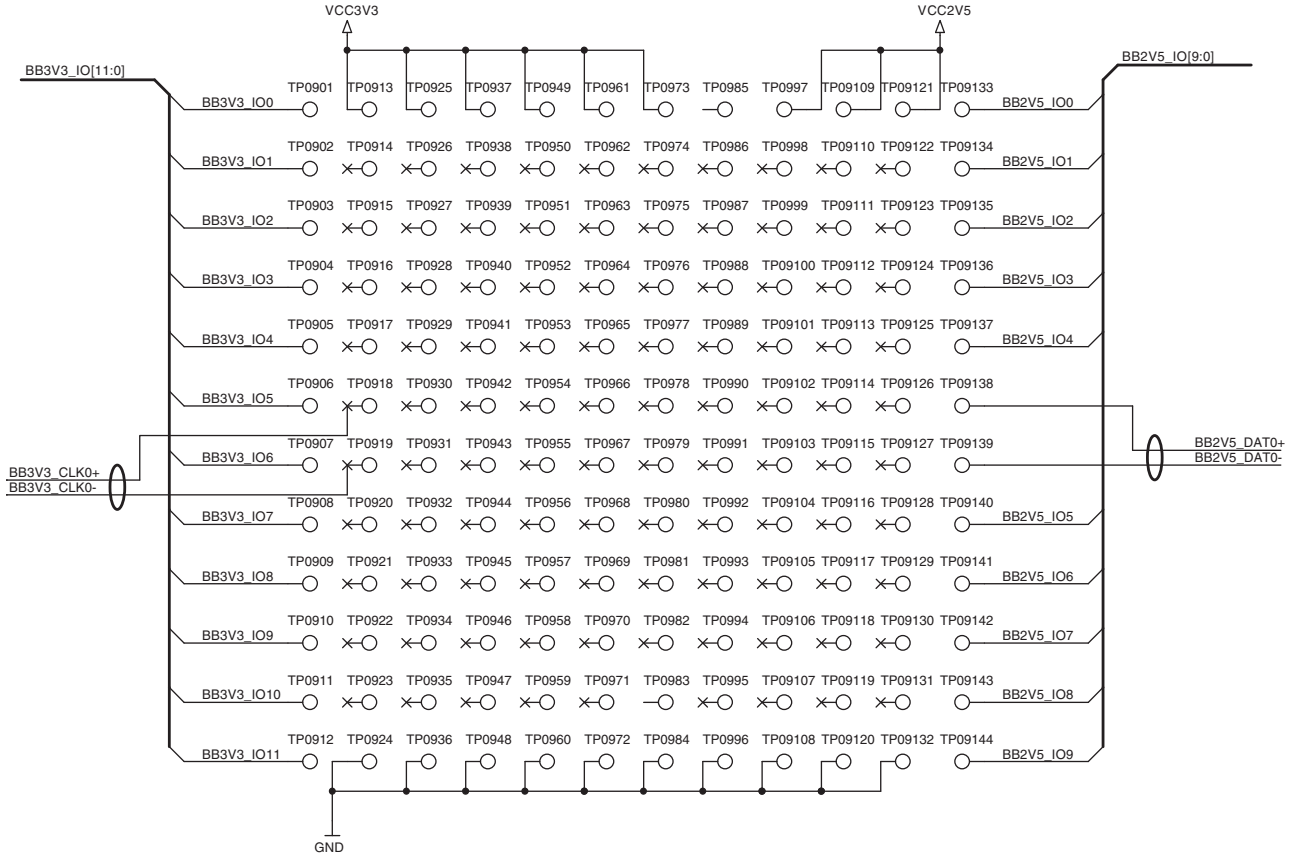
12 x 12 FPGA Prototyping Area of The FPGA

A 12x12 prototyping area is available on the right side of the board. The lead-wire spacing of the prototyping area is 100mil (2.54 mm). Figure 10 shows the prototyping area in top view. 14 plated-through-holes on its left side are connected to the FPGA. Eight through-holes on the right side are wired to a 2.5V I/O bank. In the top row of the prototyping area there are six connections to the 3.3V power supply as well as three to 2.5V. The bottom row has ten plated-through-holes connected to GND.

Table 22. FPGA Connections for the 12x12 Prototyping Area

FPGA Pin	Signal Name	LRF Pin	FPGA Pin	Signal Name	LRF Pin
AB13	BB3V3 IO0	TP0901	AB12	BB3V3 IO1	TP0902
AA12	BB3V3 IO2	TP0903	Y12	BB3V3 IO3	TP0904
W12	BB3V3 IO4	TP0905	V12	BB3V3 IO5	TP0906
V11	BB3V3 IO6	TP0907	U10	BB3V3 IO7	TP0908
T10	BB3V3 IO8	TP0909	U9	BB3V3 IO9	TP0910
T9	BB3V3 IO10	TP0911	U8	BB3V3 IO11	TP0912
AB10	BB3V3 CLK0+	TP0918	AB11	BB3V3 CLK0-	TP0919
F11	BB2V5 IO0	TP09133	F12	BB2V5 IO1	TP09134
F13	BB2V5 IO2	TP09135	G13	BB2V5 IO3	TP09136
F14	BB2V5 IO4	TP09137	G14	BB2V5 IO5	TP09140
F15	BB2V5 IO6	TP09141	F16	BB2V5 IO7	TP09142
—	VCC3V3	TP0913	—	VCC3V3	TP0925
—	VCC3V3	TP0937	—	VCC3V3	TP0949
—	VCC3V3	TP0961	—	VCC3V3	TP0973
—	VCC2V5	TP0997	—	VCC2V5	TP09109
—	VCC2V5	TP09121			
—	GND	TP0924	—	GND	TP0936
—	GND	TP0948	—	GND	TP0960
—	GND	TP0972	—	GND	TP0984
—	GND	TP0996	—	GND	TP09108
—	GND	TP09120	—	GND	TP09132

Figure 9. Schematic Illustration of the Prototyping Area



8 x 6 MachXO Prototyping Area

There is a second prototyping area connected to the MachXO. Its lead-wire spacing is also 100mil (2.54 mm). 22 drill holes are connected to the MachXO. The topmost row is connected to the 3.3V power supply; the bottom-most to ground.

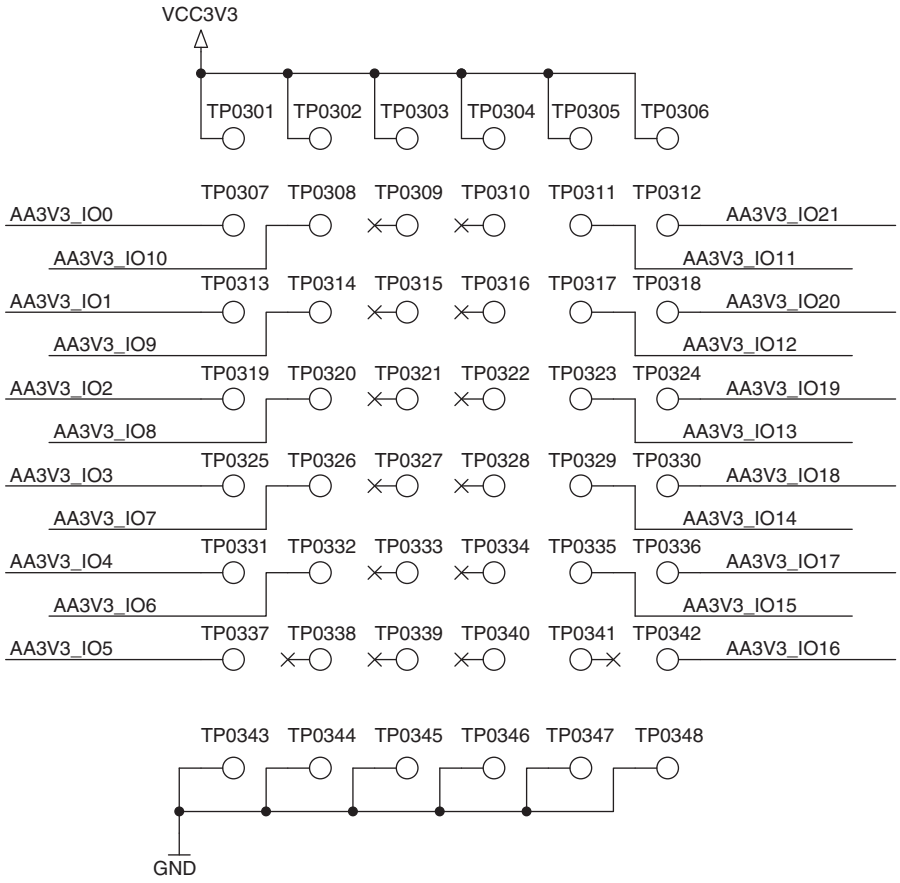
Table 23. MachXO Connections for the 8x6 Prototyping Area

MachXO Pin	Signal Name	LRF Pin	MachXO Pin	Signal Name	LRF Pin
A6	AA3V3 IO0	TP0307	B6	AA3V3 IO1	TP0313
C6	AA3V3 IO2	TP0319	B7	AA3V3 IO3	TP0325
B8	AA3V3 IO4	TP0331	B14	AA3V3 IO5	TP0337
B10	AA3V3 IO6	TP0332	C10	AA3V3 IO7	TP0326
A11	AA3V3 IO8	TP0320	C11	AA3V3 IO9	TP0314
A12	AA3V3 IO10	TP0308	B12	AA3V3 IO11	TP0311
B12	AA3V3 IO12	TP0311	A13	AA3V3 IO13	TP0323
B13	AA3V3 IO14	TP0329	A14	AA3V3 IO15	TP0335
C14	AA3V3 IO16	TP0342	C13	AA3V3 IO17	TP0336
D12	AA3V3 IO18	TP0330	D14	AA3V3 IO19	TP0324
N6	AA3V3 IO20	TP0318	G3	AA3V3 IO21	TP0312
—	VCC3V3	TP0301	—	VCC3V3	TP0302
—	VCC3V3	TP0303	—	VCC3V3	TP0304
—	VCC3V3	TP0305	—	VCC3V3	TP0306

Table 23. MachXO Connections for the 8x6 Prototyping Area (Continued)

—	GND	TP0343	—	GND	TP0344
—	GND	TP0345	—	GND	TP0346
—	GND	TP0347	—	GND	TP0348

Figure 10. Schematic Illustration of the Prototyping Area



Asynchronous SRAM

The board is populated with two asynchronous K6R4016V1D-TC10 SRAMs from Samsung. Every one of them is 4 Mbit in size with a data bus width of 16 bits. They are wired as one memory with a 32-bit data bus and a depth of 256 k. The 18-bit address bus, the data bus and the control signals are connected directly to the FPGA.

MachXO

The LCMXO640 is a non-volatile, instant-on, reprogrammable logic device. It supports "background programming" (i.e., the device can be programmed while in operation).

The MachXO comes preprogrammed from the factory. The factory program permits the CY7C68013A/MachXO combination to work as a built-in USB ispDOWNLOAD cable. Using ispVM software the built-in download cable permits the FPGA, and SPI PROM, to be programmed. It is not recommended for the MachXO to be reprogrammed. However, the MachXO does provide some connections to the LatticeECP33 FPGA, and to an 8x6 prototyping area.

For further information, please consult the MachXO Family Data Sheet.

Table 24. Interface Between the MachXO and the FPGA

MachXO Pin	Signal Name	MachXO Pin	MachXO Pin	Signal Name	MachXO Pin
A1	MACHXO IO0	C1	A2	MACHXO IO1	E2
A3	MACHXO IO2	F3	B3	MACHXO IO3	R6
A4	MACHXO IO4	U3	C4	MACHXO IO5	V3
A5	MACHXO IO6	V2	C8	MACHXO CLK	B1

FPGA

The LFECP33 represents the heart of the board. It has the following features:

- 32.8 k Look-Up Tables (LUTs)
- 131 kbit distributed RAM
- 498 kbit EBR SRAM
- 54 EBR SRAM blocks
- Four PLLs
- 360 user I/Os available
- DDR memory support (DDR400)
- Supported I/O standards: LVCMOS, LVTTL, SSTL, HSTL, LVDS

The ispLEVER design software can be used to develop/modify programs for the FPGA using Verilog or VHDL design entry methods. For more information on the ispLEVER software, see www.latticesemi.com/software.

Sample programs for the FPGA are available on-line as well. These can be found at www.latticesemi.com/boards. Select **FPGA/FPSC Boards -> LatticeMico32/DSP Development board** and click on the **Design Files** link.

For further information please consult the LatticeECP/EC Family Data Sheet.

Parallel Flash

Two parallel MX29LV128MBTI-90Q Flash components from Macronics are provided on the board for program code and data. As with the SRAM, a 32-bit data bus is realized with these two devices. Thus, Flash can be accessed as a 8Mx32 memory. The 23-bit address bus, the data bus and the control signals are connected directly to the FPGA.

SPI Flash

The LatticeECP33 FPGA is an SRAM-based programmable device, and is therefore volatile. In order for it to be automatically configured upon power-up, a non-volatile 8 Mbit SPI Flash device is provided. The SPI Flash can be programmed with configuration bitstream data. The SPI Flash can be configured either through the ispDOWNLOAD connector or via the integrated USB configuration interface.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2 FPGA device and render the board inoperable.*

To program the SPI Flash configuration device, use the FPGA Loader function of the ispVM System software. The FPGA Loader programming scheme provides an in-system JTAG programming method for configuration devices. The FPGA acts as a bridge between the JTAG interface and the SPI interface of the serial configuration device.

Configure the SPI Flash as follows:

1. In the ispVM System software, choose **Edit -> Add Device** to open the Device Information dialog box.

2. Click **Select** to open the Select Device dialog box.
3. From the Device Family drop-down list, select **FPGA Loader**. The FPGA Loader opens and displays a setup menu in the left pane and instructions in the right pane.
4. From the menu, select **CPLD or FPGA Device** to display the Device Configuration dialog.
5. Click **Select** to open the Select Device dialog box. Select device family **LatticeECP**, device **LFECP33E**, and package **484 fpBGA** from the drop-down lists.
6. Click **OK** to return to the FPGA Loader.
7. Click the **Browse** button under FPGA Loader Application Specific Data File and press the **Default** button to use the standard IP provided for SPI configuration. Click **Close** to return to the FPGA Loader.
8. Select **Fast Program** from the menu to open the data file dialog, and then select the configuration data[1] with which you want the FPGA to be programmed.
9. Under **Configuration Data Setup**, browse to select the programming file you wish to load into the SPI Flash. This is the file that will ultimately be downloaded to the LFECP33E device.
10. Select **Flash Device** from the menu to open the Flash configuration dialog.
11. Under Flash Device, click **Select**. Select **SPI Serial Flash** from the drop-down menu and select **SPI-M25P80**, **STMicro** and **8-pin SOIC**. Click **OK** to return to the FPGA Loader.
12. If desired, select **Hardware Setup** to display general information about the configuration process.
13. Click **OK** to exit the FPGA Loader, add the devices and return to the ispVM System software window.
14. Click **GO**. The ispVM System software programs the SPI Flash via the FPGA.
15. Disconnect and then reconnect the power supply. The FPGA will take about three seconds to be programmed by the SPI Flash.

Power Supply

Power is supplied via a 2.1 mm DC power jack in the top left corner of the board. The board is protected against reversed power supply. The input supply is 5V DC.

A two-phase synchronous step-down switching regulator generates the 3.3V (1A max.) I/O voltage and the 1.2V (2A max.) core voltage.

Note: If you use a power supply other than the one included in the shipment, make sure it supplies regulated 5V.

Reset Chip

After power-up, a power surveillance chip (U0601) waits until the 5V supply and the 3.3V I/O voltage are stable. Then, after 200 ms, it drives the signal HPE RESET# (pin B3 of the FPGA) high. If you press the reset button, the supervisory circuit will generate a low on the HPE RESET# signal.

The surveillance chip has an I^2C serial 2 kbit CMOS EEPROM. The four most significant bits of the 8-bit slave address are programmable; the default being 1010. Detailed information on the reset circuit and the I^2C interface can be found in the data sheet of the Catalyst Semiconductor CAT1026.

Troubleshooting

If your board is not working properly, please follow these steps for diagnosis.

1. Usually a file with the ending .bit.

1. Check the 3.3V and 2.5V LEDs to ensure that the power supply is working correctly.
2. Make sure that the INIT LED is lit.
3. Load test program 1[1].
4. Make sure the FPGA has been configured properly (DONE LED must be lit).
5. Start test program 1 (for a detailed description see the Program 1 - Peripheral Test section of this document).

Circuit diagrams for the localization of errors can be found in the appendix.

Electrical Specifications

Power requirement: regulated 5V DC
Input current: 2000 mA

Mechanical Specifications

Dimensions: 160 mm [L] x 160 mm [W] x 31 mm [H]
Net weight: 160 g
Temperature range: 0 to 50°C

FPGA Pin Information

Table 25. Pin Table

Pin Name	Signal Name	Appliance
F21	HS DAT2-	High-speed LVDS Connector
E22	HS DAT2+	High-speed LVDS Connector
F11	BB2V5 IO0	FPGA Prototyping Area
F12	BB2V5 IO1	FPGA Prototyping Area
F13	BB2V5 IO2	FPGA Prototyping Area
G13	BB2V5 IO3	FPGA Prototyping Area
F14	BB2V5 IO4	FPGA Prototyping Area
G14	BB2V5 IO5	FPGA Prototyping Area
F15	BB2V5 IO6	FPGA Prototyping Area
F16	BB2V5 IO7	FPGA Prototyping Area
F17	HS DAT4+	High-speed LVDS Connector
G17	HS DAT4-	High-speed LVDS Connector
AB11	BB3V3 CLK0-	FPGA Prototyping Area
AB10	BB3V3 CLK0+	FPGA Prototyping Area
AB13	BB3V3 IO0	FPGA Prototyping Area
AB12	BB3V3 IO1	FPGA Prototyping Area
T9	BB3V3 IO10	FPGA Prototyping Area
U8	BB3V3 IO11	FPGA Prototyping Area
AA12	BB3V3 IO2	FPGA Prototyping Area
Y12	BB3V3 IO3	FPGA Prototyping Area
W12	BB3V3 IO4	FPGA Prototyping Area
V12	BB3V3 IO5	FPGA Prototyping Area
V11	BB3V3 IO6	FPGA Prototyping Area

1. If the content of the serial configuration Flash has not been overwritten since the time the board was shipped, you can alternatively unplug the power supply and then plug it in again.

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
U10	BB3V3 IO7	FPGA Prototyping Area
T10	BB3V3 IO8	FPGA Prototyping Area
U9	BB3V3 IO9	FPGA Prototyping Area
V20	CARDSEL#	FPGA Prototyping Area
T20	CCLK	Configuration
Y21	CCLK	Configuration
U18	CFG0	Configuration
U19	CFG1	Configuration
T19	CFG2	Configuration
A10	CLK FPGA	Clock
W1	CODEC BCLK	Audio Codec
W4	CODEC CS#	Audio Codec
W2	CODEC DIN	Audio Codec
W3	CODEC DOUT	Audio Codec
AA1	CODEC LRCIN	Audio Codec
Y2	CODEC LRCOUT	Audio Codec
Y3	CODEC MCLK	Audio Codec
V4	CODEC MODE	Audio Codec
Y1	CODEC SCLK	Audio Codec
AA2	CODEC SDIN	Audio Codec
V21	CSSPIN	Configuration
U7	DAC DIG	DAC
D16	DDR A0	DDR RAM
C16	DDR A1	DDR RAM
E16	DDR A10	DDR RAM
C13	DDR A11	DDR RAM
B13	DDR A12	DDR RAM
C17	DDR A13	DDR RAM
E15	DDR A2	DDR RAM
D15	DDR A3	DDR RAM
C15	DDR A4	DDR RAM
E14	DDR A5	DDR RAM
D14	DDR A6	DDR RAM
C14	DDR A7	DDR RAM
E13	DDR A8	DDR RAM
D13	DDR A9	DDR RAM
E17	DDR BA0	DDR RAM
D17	DDR BA1	DDR RAM
A19	DDR CAS#	DDR RAM
A12	DDR CK0-	DDR RAM
B12	DDR CK0+	DDR RAM
B19	DDR CK1-	DDR RAM
A20	DDR CK1+	DDR RAM
A13	DDR CKE0	DDR RAM

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
C12	DDR CKE1	DDR RAM
B15	DDR DM0	DDR RAM
C20	DDR DM1	DDR RAM
H19	DDR DM2	DDR RAM
K20	DDR DM3	DDR RAM
A14	DDR DQ0	DDR RAM
B14	DDR DQ1	DDR RAM
C21	DDR DQ10	DDR RAM
C22	DDR DQ11	DDR RAM
E20	DDR DQ12	DDR RAM
E18	DDR DQ13	DDR RAM
F19	DDR DQ14	DDR RAM
F18	DDR DQ15	DDR RAM
D21	DDR DQ16	DDR RAM
F20	DDR DQ17	DDR RAM
G21	DDR DQ18	DDR RAM
G20	DDR DQ19	DDR RAM
A15	DDR DQ2	DDR RAM
H20	DDR DQ20	DDR RAM
J19	DDR DQ21	DDR RAM
J18	DDR DQ22	DDR RAM
H17	DDR DQ23	DDR RAM
F22	DDR DQ24	DDR RAM
G22	DDR DQ25	DDR RAM
H22	DDR DQ26	DDR RAM
H21	DDR DQ27	DDR RAM
K19	DDR DQ28	DDR RAM
K18	DDR DQ29	DDR RAM
B16	DDR DQ3	DDR RAM
L18	DDR DQ30	DDR RAM
L19	DDR DQ31	DDR RAM
A17	DDR DQ4	DDR RAM
B17	DDR DQ5	DDR RAM
A18	DDR DQ6	DDR RAM
B18	DDR DQ7	DDR RAM
B22	DDR DQ8	DDR RAM
B21	DDR DQ9	DDR RAM
A16	DDR DQS0	DDR RAM
D20	DDR DQS1	DDR RAM
H18	DDR DQS2	DDR RAM
J20	DDR DQS3	DDR RAM
C18	DDR RAS#	DDR RAM
C19	DDR S0#	DDR RAM
B20	DDR S1#	DDR RAM

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
D12	DDR VREF	DDR RAM
E19	DDR VREF	DDR RAM
D18	DDR WE#	DDR RAM
W22	DOUT	Configuration
R2	DSW0	DIP Switch
R3	DSW1	DIP Switch
R4	DSW2	DIP Switch
R5	DSW3	DIP Switch
T5	EC TCK	Configuration
U5	EC TDI	Configuration
U1	EC TDO	Configuration
T4	EC TMS	Configuration
K2	ETH COL	Ethernet
K3	ETH CRS	Ethernet
K5	ETH MDC	Ethernet
F1	ETH MDINTR#	Ethernet
K4	ETH MDIO	Ethernet
K1	ETH RXCLK	Ethernet
G1	ETH RXD0	Ethernet
G2	ETH RXD1	Ethernet
G3	ETH RXD2	Ethernet
F2	ETH RXD3	Ethernet
J4	ETH RXDV	Ethernet
J5	ETH RXER	Ethernet
J1	ETH TXCLK	Ethernet
H1	ETH TXD0	Ethernet
H2	ETH TXD1	Ethernet
H3	ETH TXD2	Ethernet
H4	ETH TXD3	Ethernet
J3	ETH TXEN	Ethernet
J2	ETH TXER	Ethernet
U20	EXPCON CLKIN	Expansion Connector
Y22	EXPCON CLKOUT	Expansion Connector
K22	EXPCON IO0	Expansion Connector
K21	EXPCON IO1	Expansion Connector
N22	EXPCON IO10	Expansion Connector
N21	EXPCON IO11	Expansion Connector
N20	EXPCON IO12	Expansion Connector
N19	EXPCON IO13	Expansion Connector
N18	EXPCON IO14	Expansion Connector
P22	EXPCON IO15	Expansion Connector
P21	EXPCON IO16	Expansion Connector
P20	EXPCON IO17	Expansion Connector
P18	EXPCON IO18	Expansion Connector

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
P19	EXPCON IO19	Expansion Connector
L22	EXPCON IO2	Expansion Connector
R22	EXPCON IO20	Expansion Connector
R21	EXPCON IO21	Expansion Connector
R19	EXPCON IO22	Expansion Connector
R18	EXPCON IO23	Expansion Connector
R17	EXPCON IO24	Expansion Connector
T22	EXPCON IO25	Expansion Connector
T18	EXPCON IO26	Expansion Connector
U22	EXPCON IO27	Expansion Connector
V19	EXPCON IO28	Expansion Connector
W21	EXPCON IO29	Expansion Connector
L21	EXPCON IO3	Expansion Connector
W20	EXPCON IO30	Expansion Connector
W19	EXPCON IO31	Expansion Connector
Y20	EXPCON IO32	Expansion Connector
AA22	EXPCON IO33	Expansion Connector
AA21	EXPCON IO34	Expansion Connector
AB21	EXPCON IO35	Expansion Connector
T17	EXPCON IO36	Expansion Connector
T14	EXPCON IO37	Expansion Connector
T13	EXPCON IO38	Expansion Connector
U14	EXPCON IO39	Expansion Connector
L20	EXPCON IO4	Expansion Connector
U13	EXPCON IO40	Expansion Connector
U12	EXPCON IO41	Expansion Connector
U11	EXPCON IO42	Expansion Connector
V14	EXPCON IO43	Expansion Connector
V13	EXPCON IO44	Expansion Connector
W13	EXPCON IO45	Expansion Connector
M22	EXPCON IO5	Expansion Connector
M21	EXPCON IO6	Expansion Connector
M20	EXPCON IO7	Expansion Connector
M19	EXPCON IO8	Expansion Connector
M18	EXPCON IO9	Expansion Connector
AA5	FLASH BYTE#	FLASH/SRAM
Y5	FLASH CE#	FLASH/SRAM
Y6	FLASH RESET#	FLASH/SRAM
W6	FLASH RY/BY# A	FLASH/SRAM
W5	FLASH RY/BY# B	FLASH/SRAM
AB5	FLASH WP#/ACC	FLASH/SRAM
H6	HPE RESET#	Reset
B3	HPE RESOUT#	Reset
G19	HS DAT1-	High-speed LVDS Connector

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
G18	HS DAT1+	High-speed LVDS Connector
J22	HS DAT3-	High-speed LVDS Connector
J21	HS DAT3+	High-speed LVDS Connector
E21	HS DAT0-	High-speed LVDS Connector
D22	HS DAT0+	High-speed LVDS Connector
L4	I2C SCL1	I^2C
L5	I2C SDA1	I^2C
R20	JTAG DONE	Configuration
T21	JTAG INIT	Configuration
P5	LCD ENABLE	LCD
P3	LCD REGSEL	LCD
P4	LCD RW	LCD
E3	LED0#	LED
E4	LED1#	LED
E5	LED2#	LED
F4	LED3#	LED
F5	LED4#	LED
G4	LED5#	LED
G5	LED6#	LED
H5	LED7#	LED
B1	MACHXO CLK0	Configuration
C1	MACHXO IO0	Configuration
E2	MACHXO IO1	Configuration
F3	MACHXO IO2	Configuration
R6	MACHXO IO3	Configuration
U3	MACHXO IO4	Configuration
V3	MACHXO IO5	Configuration
V2	MACHXO IO6	Configuration
V1	CLK FPGA	Clock
AB20	MEMORY A0	FLASH/SRAM
AA20	MEMORY A1	FLASH/SRAM
AA17	MEMORY A10	FLASH/SRAM
Y17	MEMORY A11	FLASH/SRAM
W17	MEMORY A12	FLASH/SRAM
V17	MEMORY A13	FLASH/SRAM
U17	MEMORY A14	FLASH/SRAM
AB16	MEMORY A15	FLASH/SRAM
AA16	MEMORY A16	FLASH/SRAM
Y16	MEMORY A17	FLASH/SRAM
W16	MEMORY A18	FLASH/SRAM
V16	MEMORY A19	FLASH/SRAM
AB19	MEMORY A2	FLASH/SRAM
U16	MEMORY A20	FLASH/SRAM
AB15	MEMORY A21	FLASH/SRAM

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
AA15	MEMORY A22	FLASH/SRAM
AA19	MEMORY A3	FLASH/SRAM
Y19	MEMORY A4	FLASH/SRAM
AB18	MEMORY A5	FLASH/SRAM
AA18	MEMORY A6	FLASH/SRAM
Y18	MEMORY A7	FLASH/SRAM
W18	MEMORY A8	FLASH/SRAM
AB17	MEMORY A9	FLASH/SRAM
Y15	MEMORY DQ0	FLASH/SRAM
W15	MEMORY DQ1	FLASH/SRAM
AA11	MEMORY DQ10	FLASH/SRAM
Y11	MEMORY DQ11	FLASH/SRAM
W11	MEMORY DQ12	FLASH/SRAM
AA10	MEMORY DQ13	FLASH/SRAM
Y10	MEMORY DQ14	FLASH/SRAM
W10	MEMORY DQ15	FLASH/SRAM
V10	MEMORY DQ16	FLASH/SRAM
AB9	MEMORY DQ17	FLASH/SRAM
AA9	MEMORY DQ18	FLASH/SRAM
Y9	MEMORY DQ19	FLASH/SRAM
V15	MEMORY DQ2	FLASH/SRAM
W9	MEMORY DQ20	FLASH/SRAM
V9	MEMORY DQ21	FLASH/SRAM
AB8	MEMORY DQ22	FLASH/SRAM
AA8	MEMORY DQ23	FLASH/SRAM
Y8	MEMORY DQ24	FLASH/SRAM
W8	MEMORY DQ25	FLASH/SRAM
V8	MEMORY DQ26	FLASH/SRAM
AB7	MEMORY DQ27	FLASH/SRAM
AA7	MEMORY DQ28	FLASH/SRAM
Y7	MEMORY DQ29	FLASH/SRAM
U15	MEMORY DQ3	FLASH/SRAM
W7	MEMORY DQ30	FLASH/SRAM
V7	MEMORY DQ31	FLASH/SRAM
AB14	MEMORY DQ4	FLASH/SRAM
AA14	MEMORY DQ5	FLASH/SRAM
Y14	MEMORY DQ6	FLASH/SRAM
W14	MEMORY DQ7	FLASH/SRAM
AA13	MEMORY DQ8	FLASH/SRAM
Y13	MEMORY DQ9	FLASH/SRAM
AA6	MEMORY OE#	FLASH/SRAM
AB6	MEMORY WE#	FLASH/SRAM
V18	PROGRAM#	Configuration
M1	RS CTS LVTTL	RS232

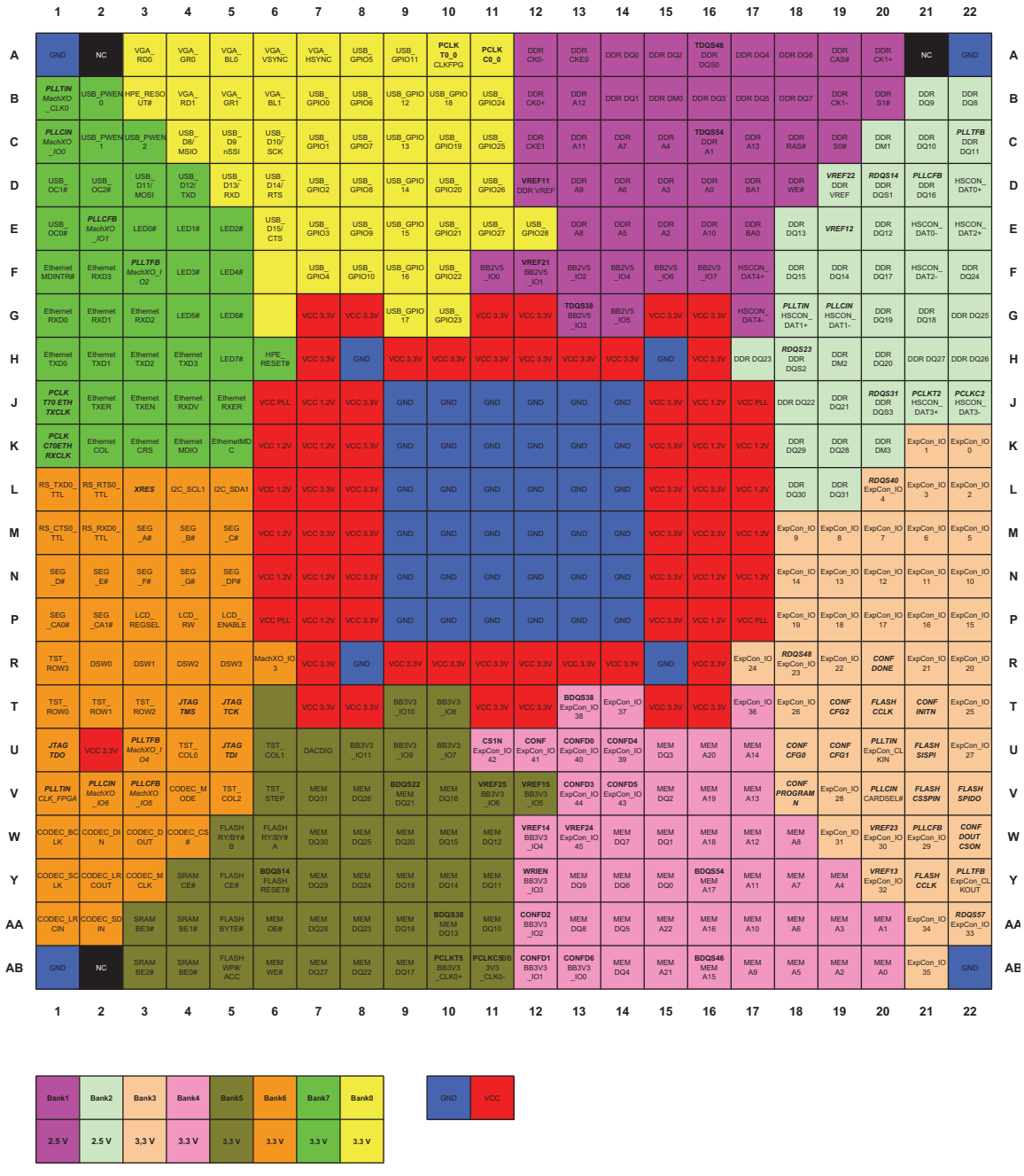
Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
L2	RS RTS LVTTL	RS233
M2	RS RXD LVTTL	RS234
L1	RS TXD LVTTL	RS235
M3	SEG A#	LCD, 7-Segment Display
M4	SEG B#	LCD, 7-Segment Display
M5	SEG C#	LCD, 7-Segment Display
P1	SEG CA0#	LCD, 7-Segment Display
P2	SEG CA1#	LCD, 7-Segment Display
N1	SEG D#	LCD, 7-Segment Display
N5	SEG DP#	LCD, 7-Segment Display
N2	SEG E#	LCD, 7-Segment Display
N3	SEG F#	LCD, 7-Segment Display
N4	SEG G#	LCD, 7-Segment Display
U21	SISPI	Configuration
V22	SPIDO	Configuration
AB4	SRAM BE0#	FLASH/SRAM
AA4	SRAM BE1#	FLASH/SRAM
AB3	SRAM BE2#	FLASH/SRAM
AA3	SRAM BE3#	FLASH/SRAM
Y4	SRAM CE#	FLASH/SRAM
U4	TST COL0	Key Matrix
U6	TST COL1	Key Matrix
V5	TST COL2	Key Matrix
T1	TST ROW0	Key Matrix
T2	TST ROW1	Key Matrix
T3	TST ROW2	Key Matrix
R1	TST ROW3	Key Matrix
V6	TST STEP	Key Matrix
E6	USB CTS	USB
B7	USB GPIO0	USB
C7	USB GPIO1	USB
F8	USB GPIO10	USB
A9	USB GPIO11	USB
B9	USB GPIO12	USB
C9	USB GPIO13	USB
D9	USB GPIO14	USB
E9	USB GPIO15	USB
F9	USB GPIO16	USB
G9	USB GPIO17	USB
B10	USB GPIO18	USB
C10	USB GPIO19	USB
D7	USB GPIO2	USB
D10	USB GPIO20	USB
E10	USB GPIO21	USB

Table 25. Pin Table (Continued)

Pin Name	Signal Name	Appliance
F10	USB GPIO22	USB
G10	USB GPIO23	USB
B11	USB GPIO24	USB
C11	USB GPIO25	USB
D11	USB GPIO26	USB
E11	USB GPIO27	USB
E12	USB GPIO28	USB
E7	USB GPIO3	USB
F7	USB GPIO4	USB
A8	USB GPIO5	USB
B8	USB GPIO6	USB
C8	USB GPIO7	USB
D8	USB GPIO8	USB
E8	USB GPIO9	USB
C4	USB MISO	USB
D3	USB MOSI	USB
E1	USB OC0#	USB
D1	USB OC1#	USB
D2	USB OC2#	USB
B2	USB PWEN0	USB
C2	USB PWEN1	USB
C3	USB PWEN2	USB
D6	USB RTS	USB
D5	USB RXD	USB
C6	USB SCK	USB
C5	USB SSI#	USB
D4	USB TXD	USB
A5	VGA BL0	VGA
B6	VGA BL1	VGA
A4	VGA GR0	VGA
B5	VGA GR1	VGA
A7	VGA HSYNC	VGA
A3	VGA RD0	VGA
B4	VGA RD1	VGA
A6	VGA VSYNC	VGA

Figure 11. LatticeECP33 BGA Pinout



Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeMico32/DSP Development Board	LFECP33E-D-EV	
ispLEVER Base with LatticeMico32/DSP Development Kit	LS-ECP33-BASE-PC-N	

Technical Support Assistance

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
July 2006	01.0	Initial release.
March 2007	01.1	Added Ordering Information section.
April 2007	01.2	Ordering information (EFUP) updated.
April 2007	01.3	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.
October 2007	01.4	Added note to DDR SODIMM Socket for DDR SDRAM Modules text section.
		Updated FPGA Pin column in the Serial Interface X1C Pin Definitions table.

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Appendix A. Schematics

Figure 12.

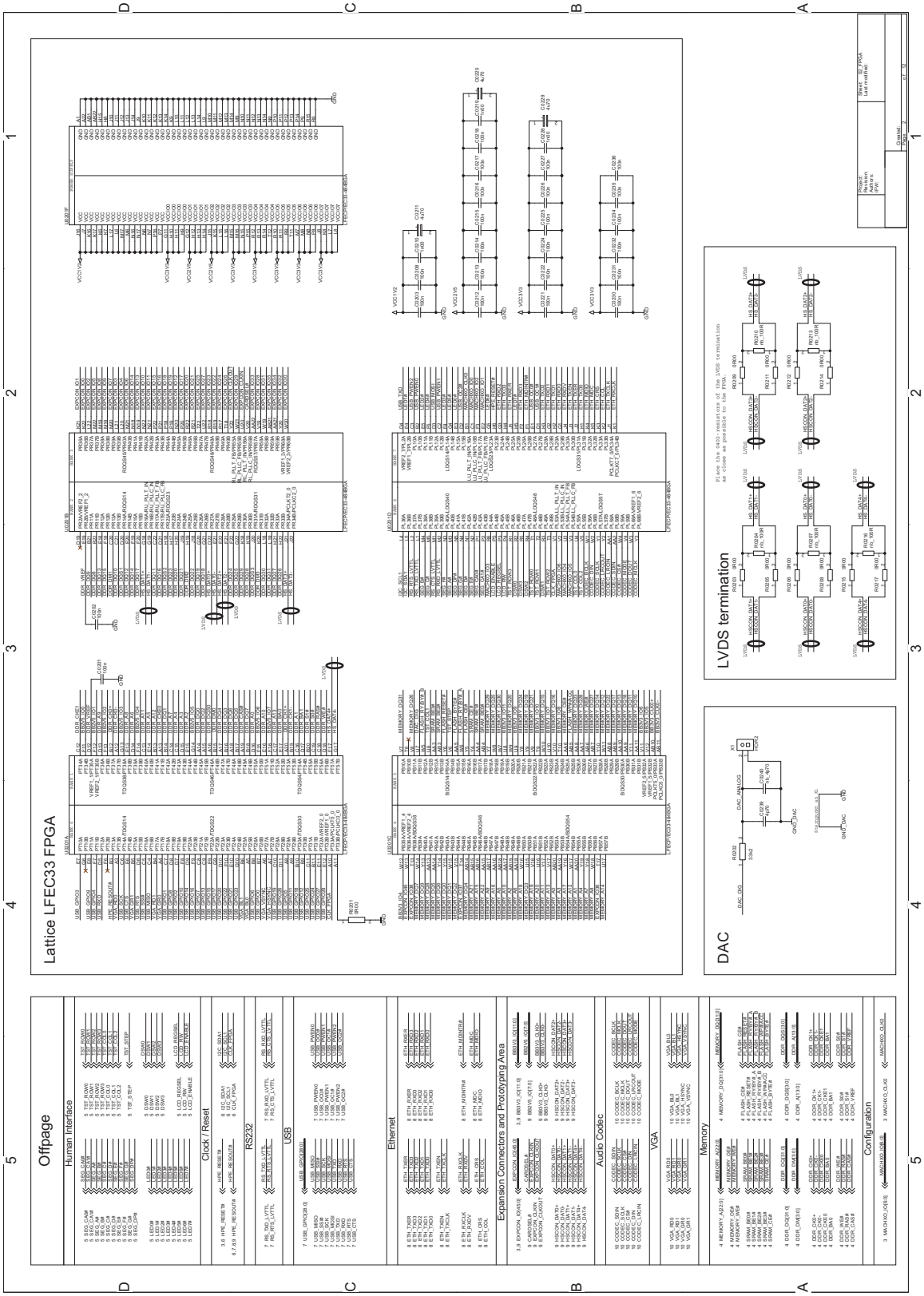


Figure 13.

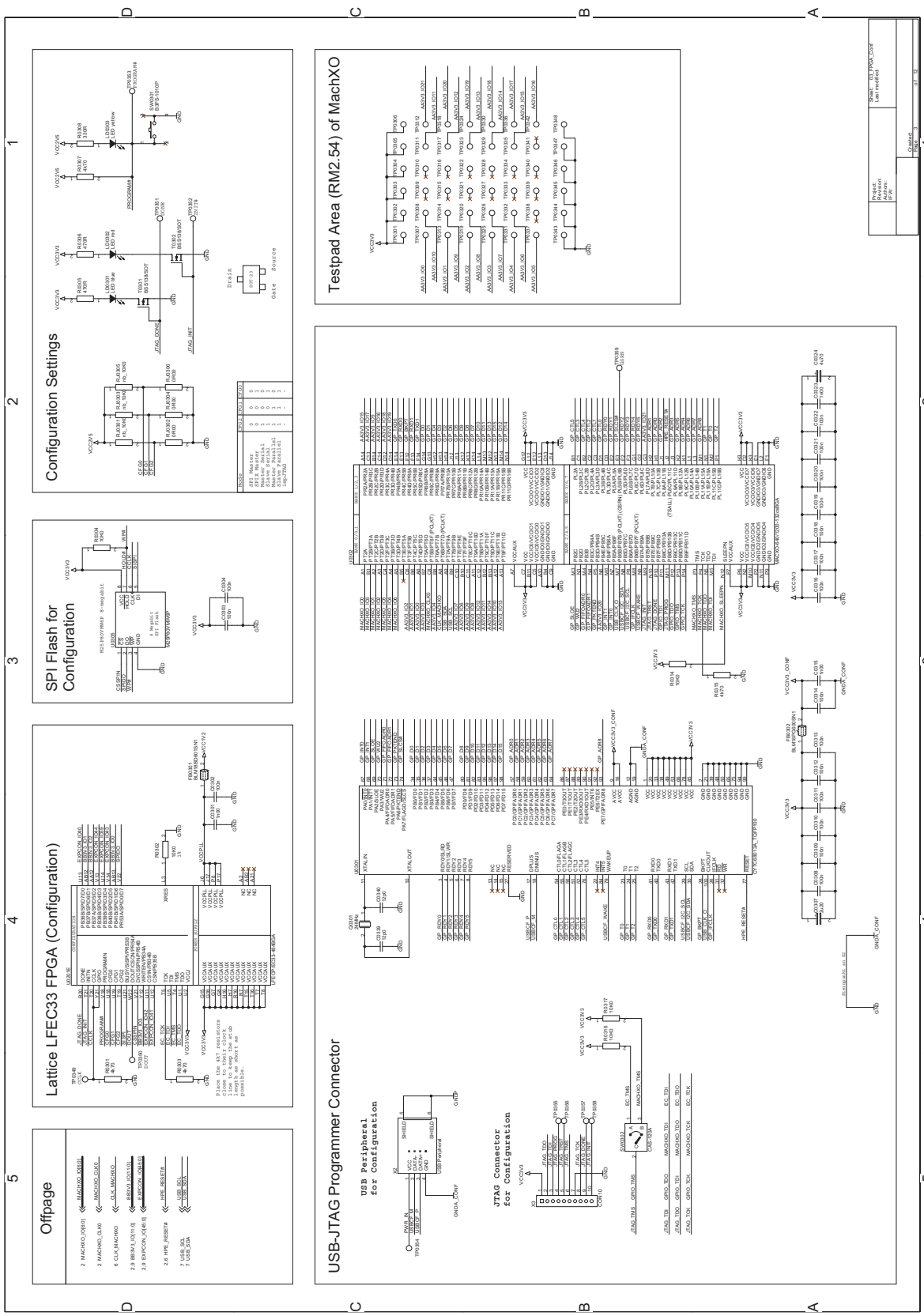

Offpage
Lattice LFEC33 FPGA (Configuration)
SPI Flash for Configuration
Configuration Settings
Testpad Area (RM2.54) of MachXO
USB-JTAG Programmer Connector
USB Peripheral for Configuration
JTAG Connector for Configuration

Figure 14.

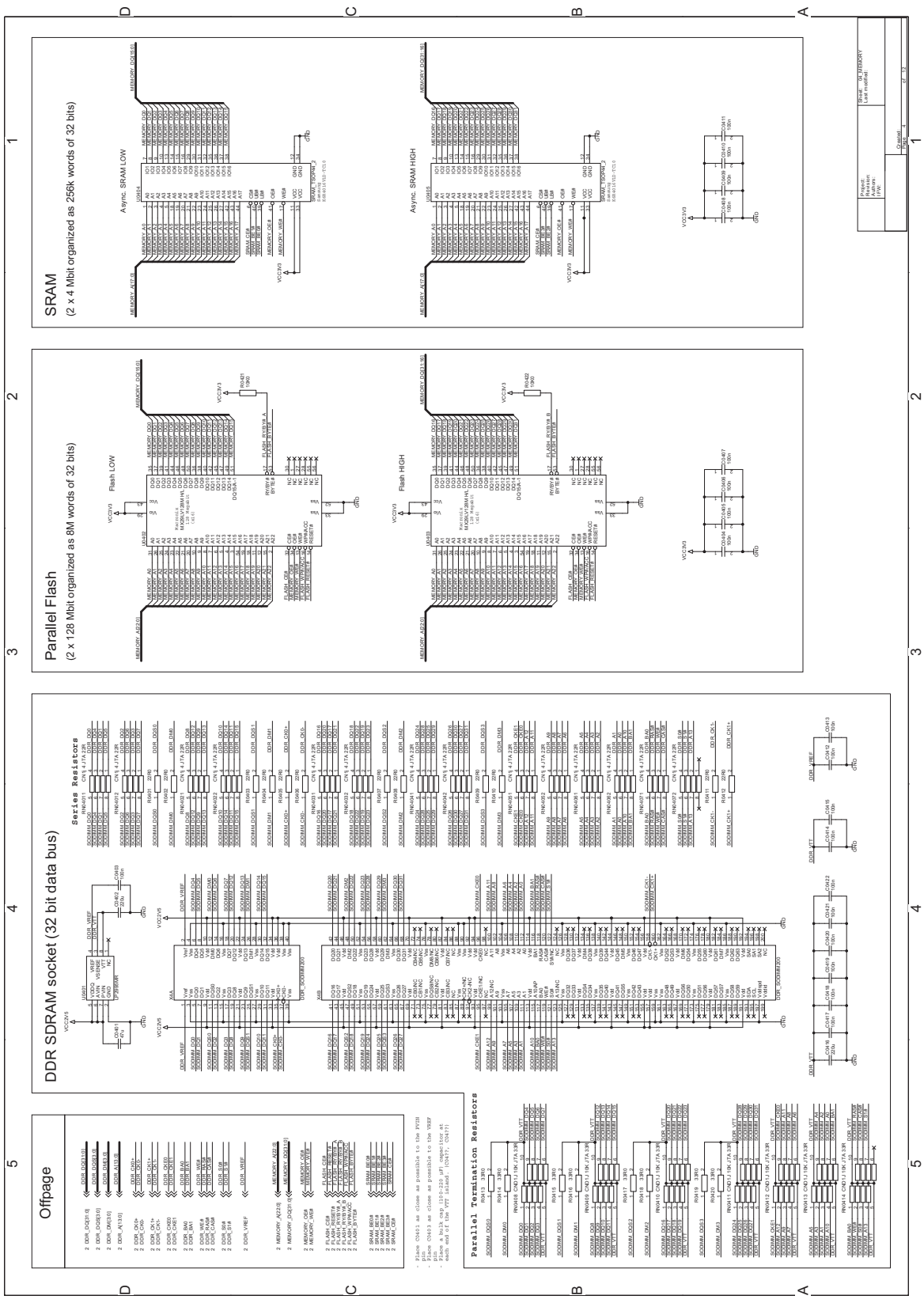

SRAM
(2 x 4 Mbit organized as 256k words of 32 bits)
Async. SRAM LOW
Async. SRAM HIGH
Parallel Flash
(2 x 128 Mbit organized as 8M words of 32 bits)
Flash LOW
Flash HIGH
DDR SDRAM socket (32 bit data bus)
Series Resistors
Parallel Termination Resistors
Offpage

Figure 15.

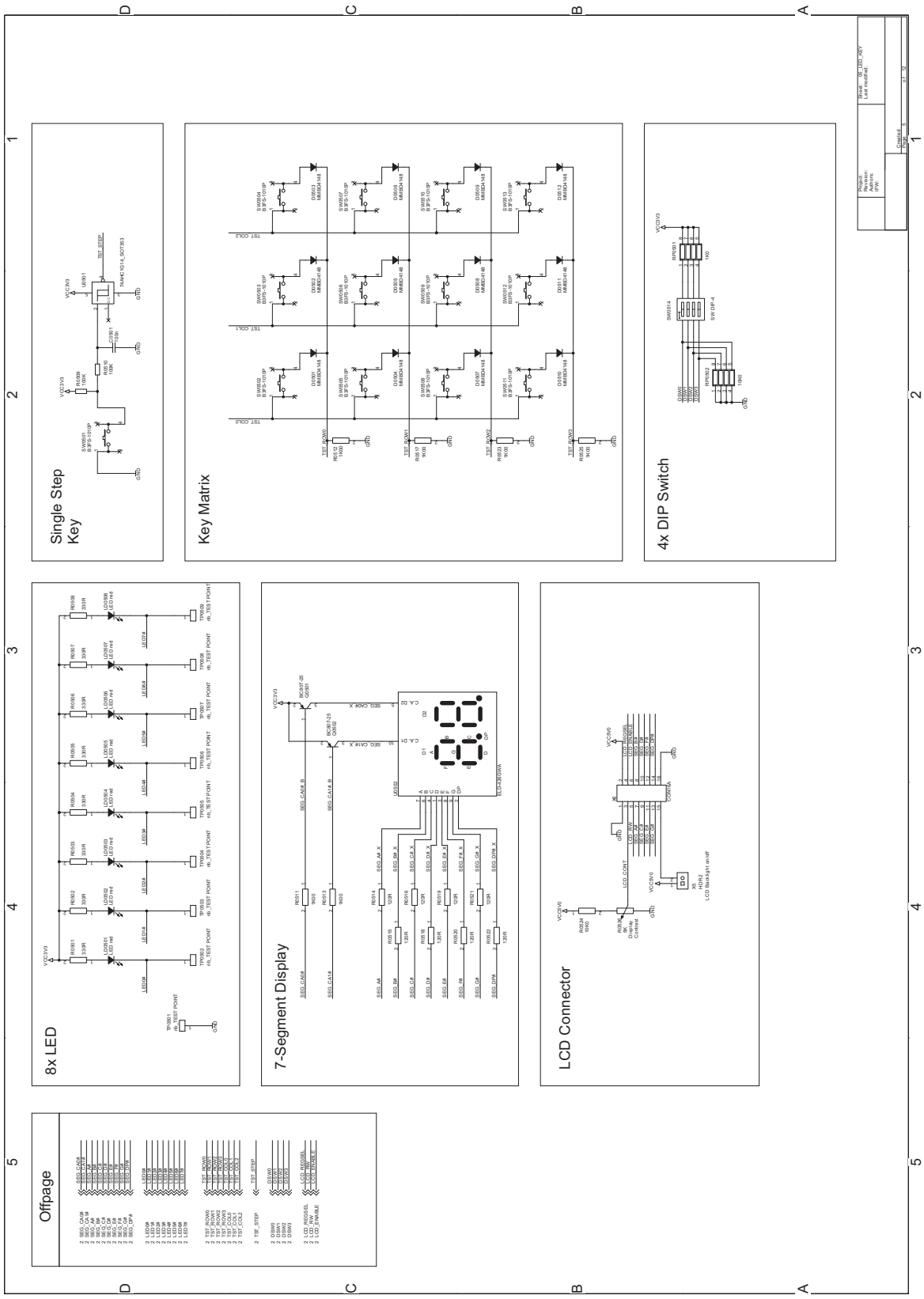

Single Step Key
Key Matrix
4x DIP Switch
8x LED
7-Segment Display
LCD Connector
Offpage

Figure 16.

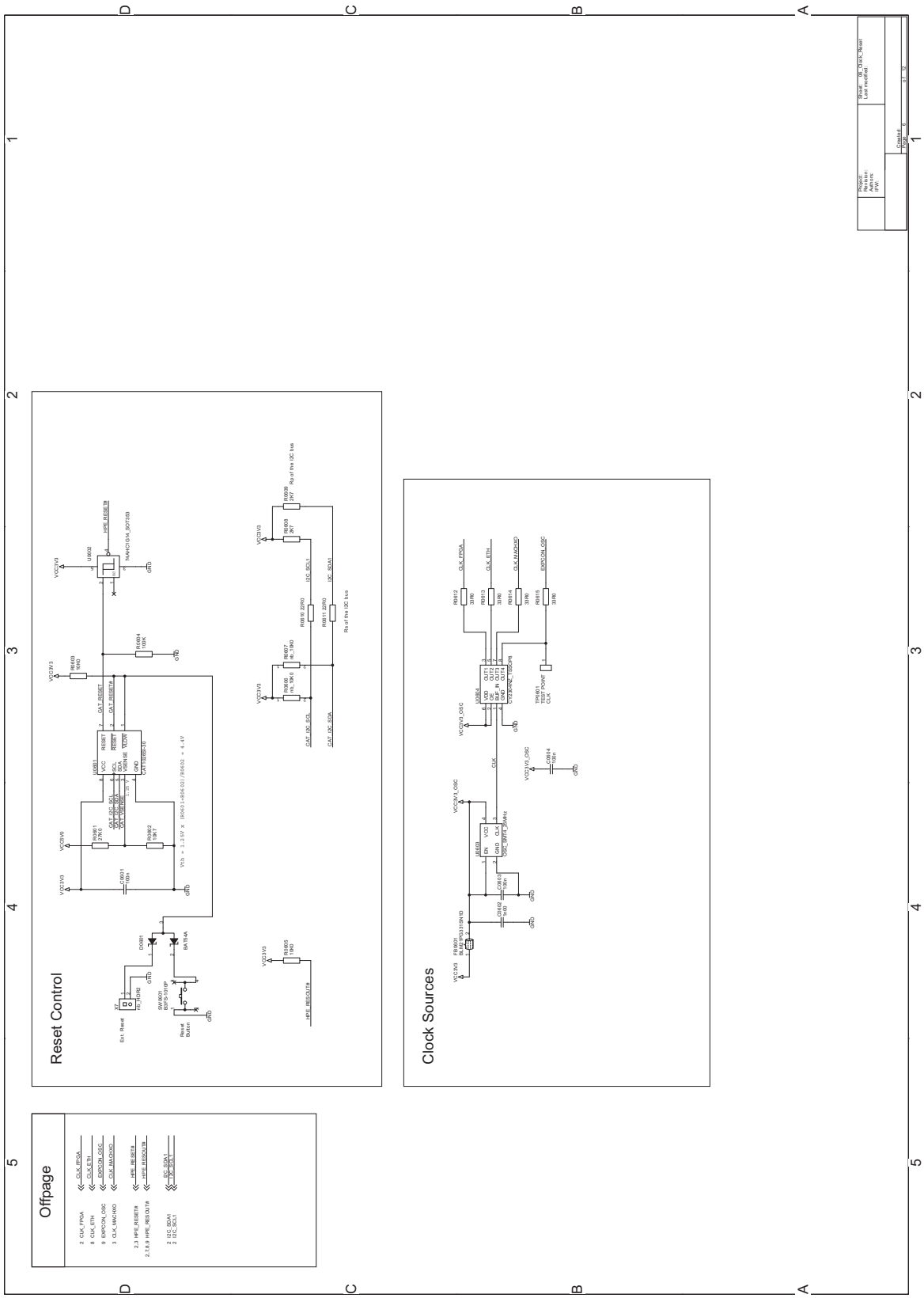

Reset Control
Clock Sources
Offpage
Project:
Revision:
Author:
IPX:
Sheet: 06_Clock_Reset
Last modified:
Created:
Page 6
of 9

Figure 17.

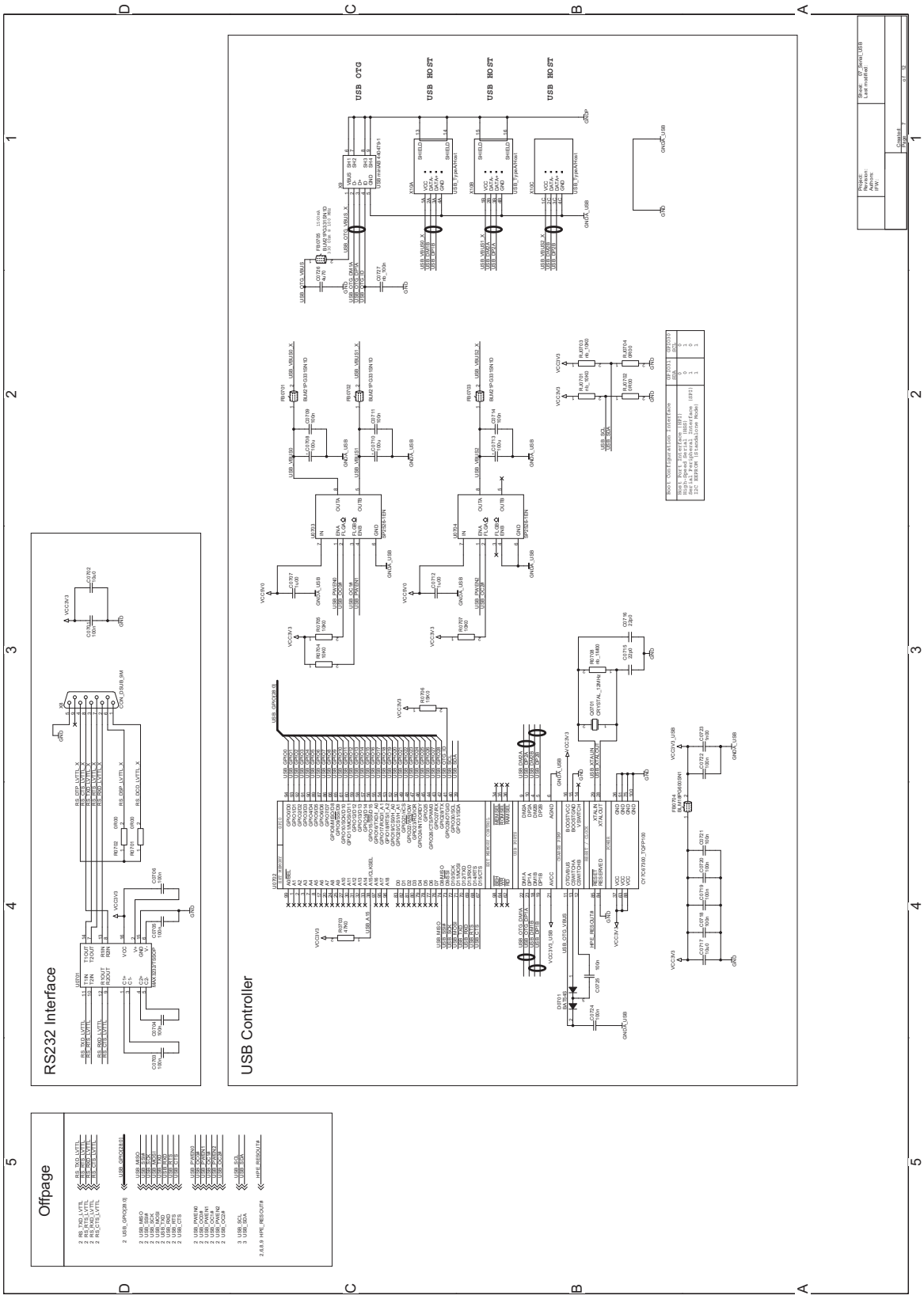

Offpage
RS232 Interface
USB Controller
USB OTG
USB HOST
USB HOST
USB HOST

Figure 18.

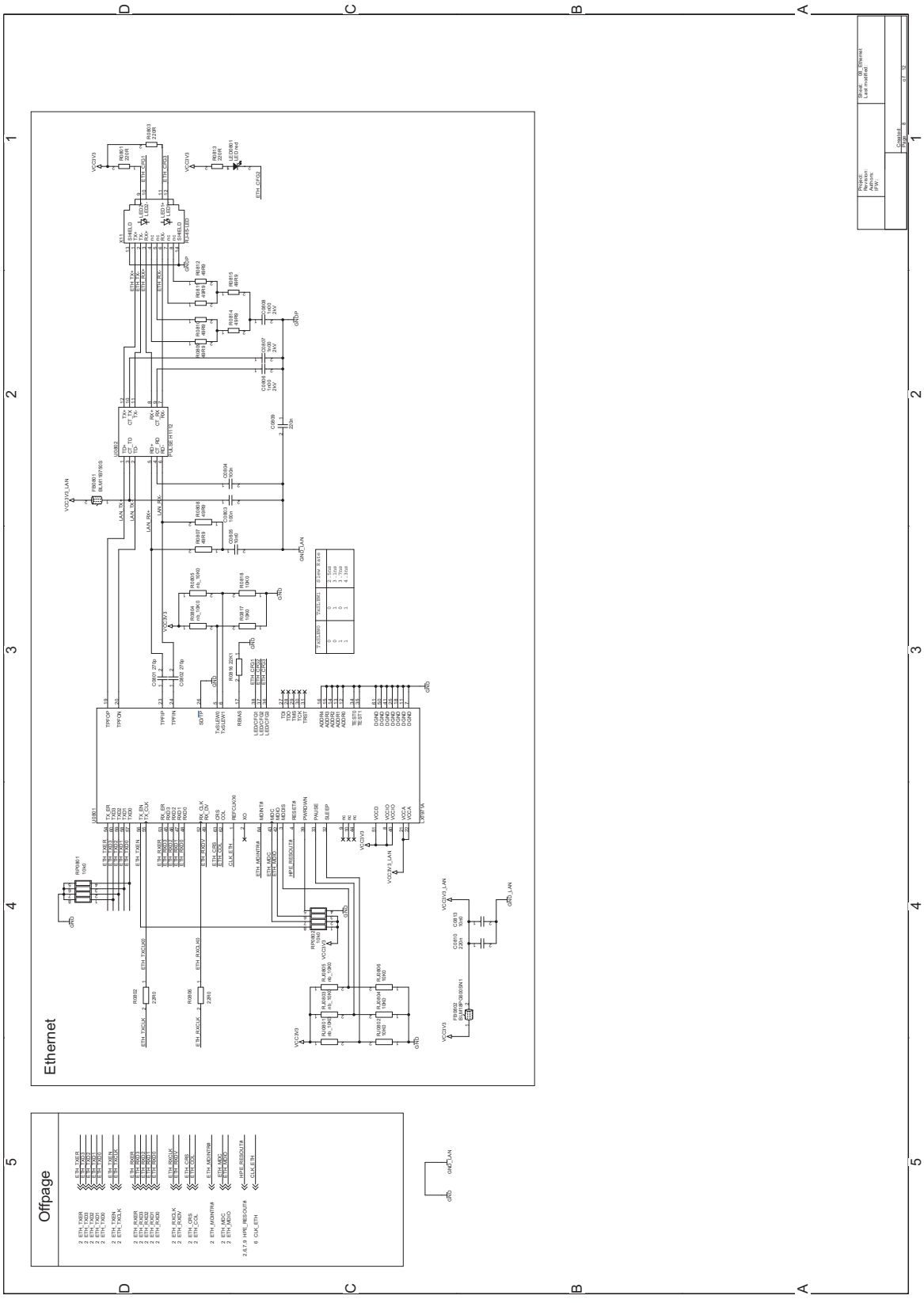


Figure 19.

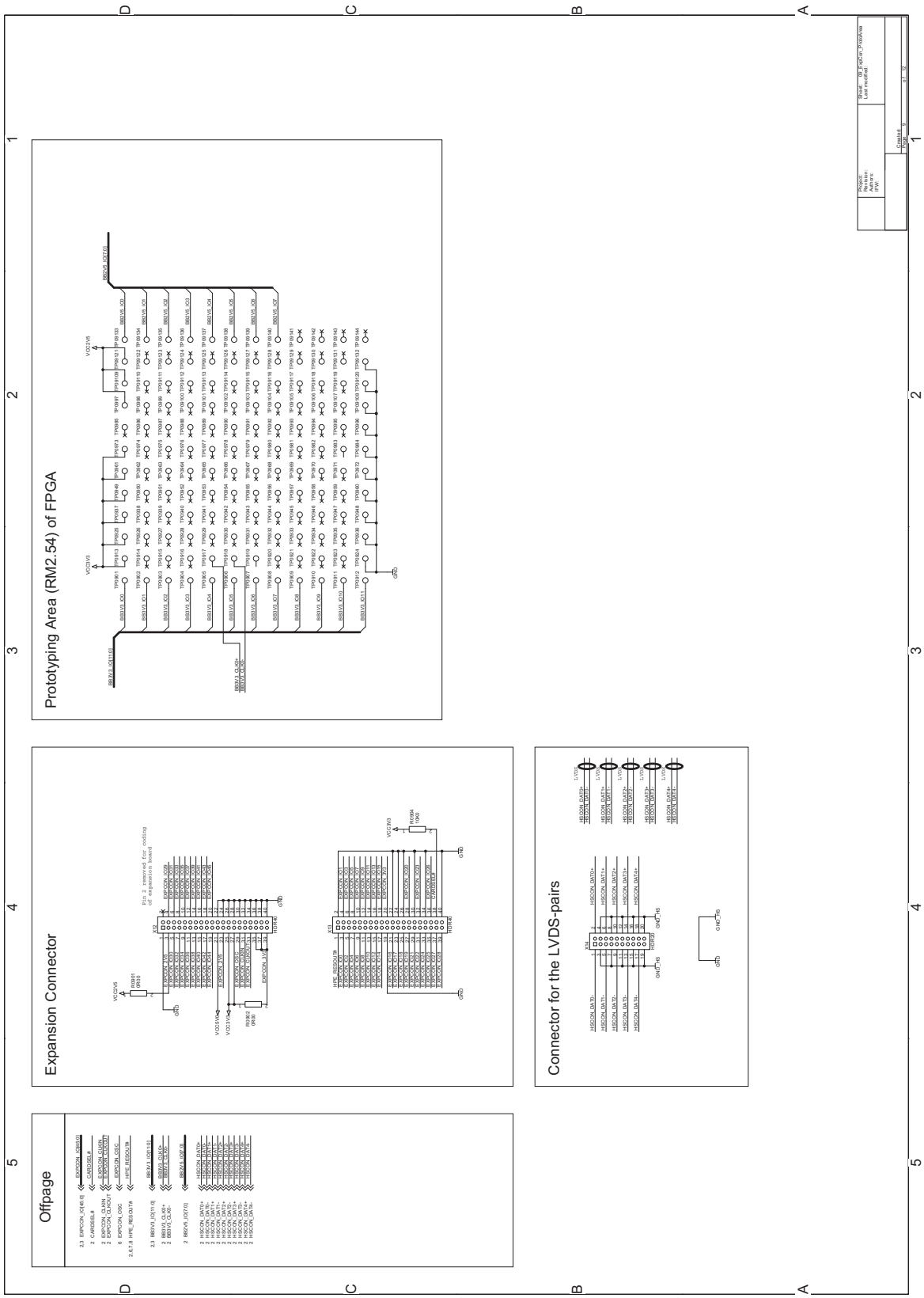

Offpage
Prototyping Area (RM2.54) of FPGA
Expansion Connector
Connector for the LVDS-pairs

Figure 20.

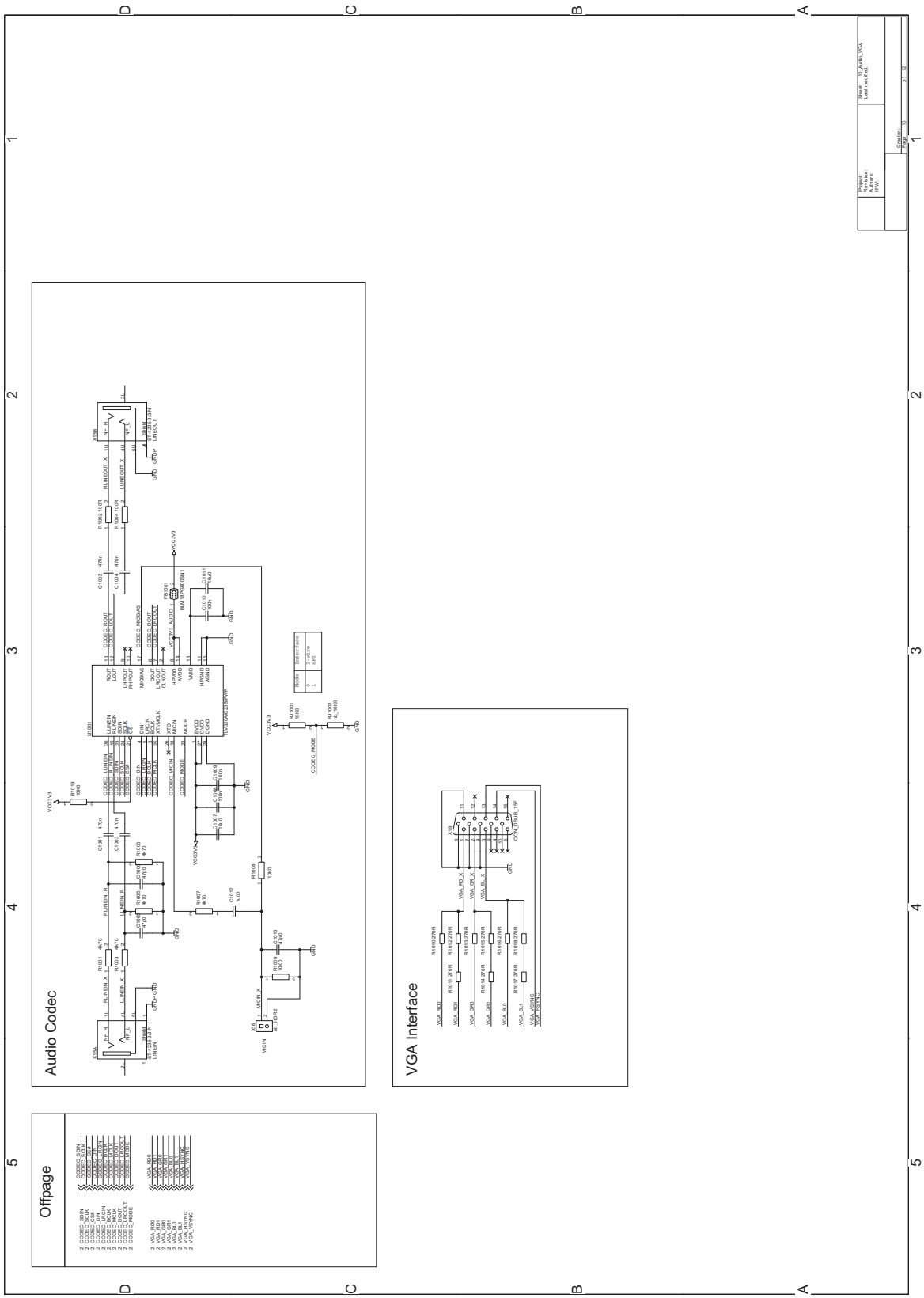
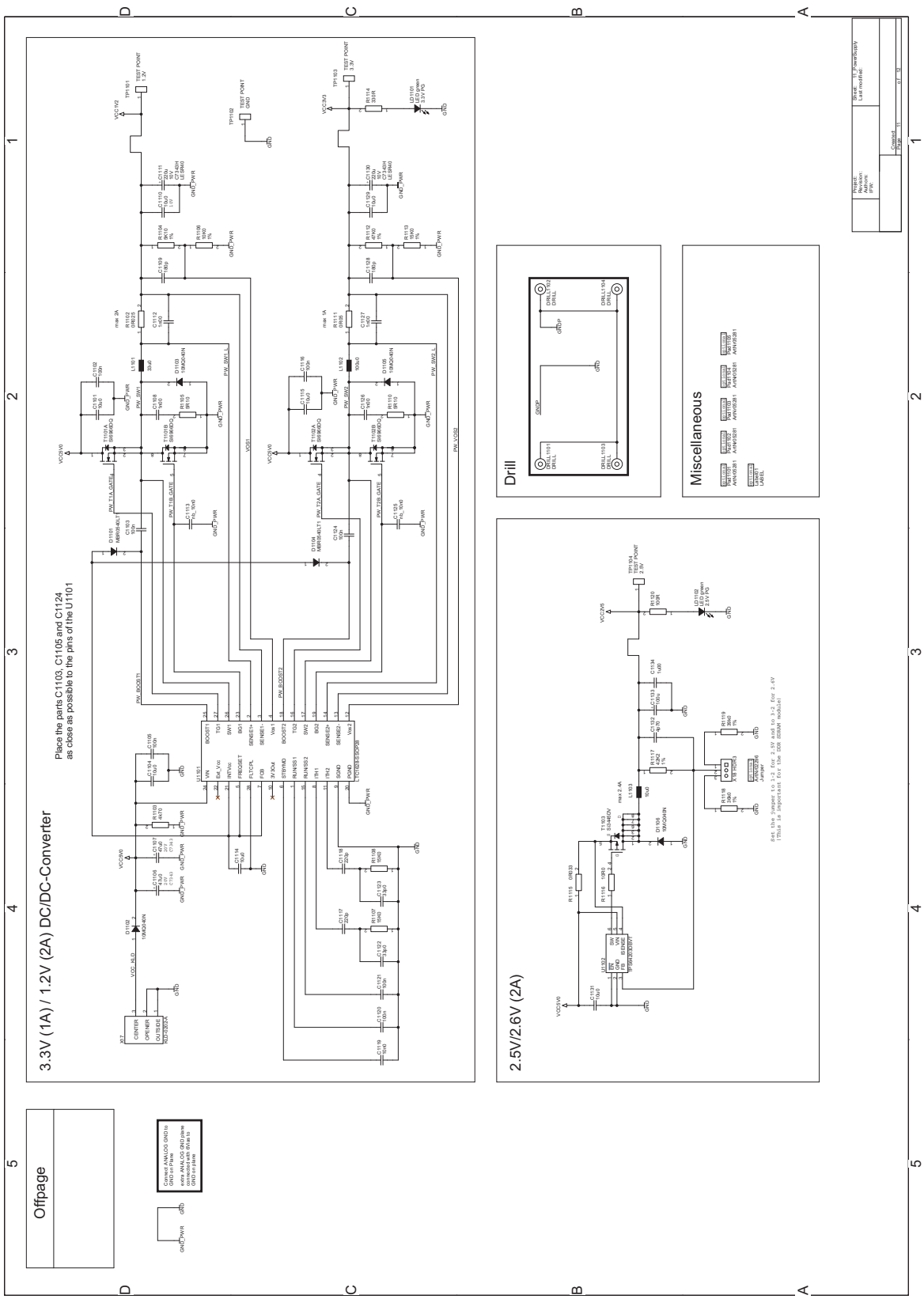


Figure 21.


3.3V (1A) / 1.2V (2A) DC/DC-Converter
Place the parts C1103, C1105 and C1124
as close as possible to the pins of the U1101
2.5V/2.6V (2A)
Drill
Miscellaneous
Offpage

Appendix B. Assembly Diagram

Note: Figures 23-26 provide an enlargement of each numbered section in Figure 22.

Figure 22. Assembly Diagram

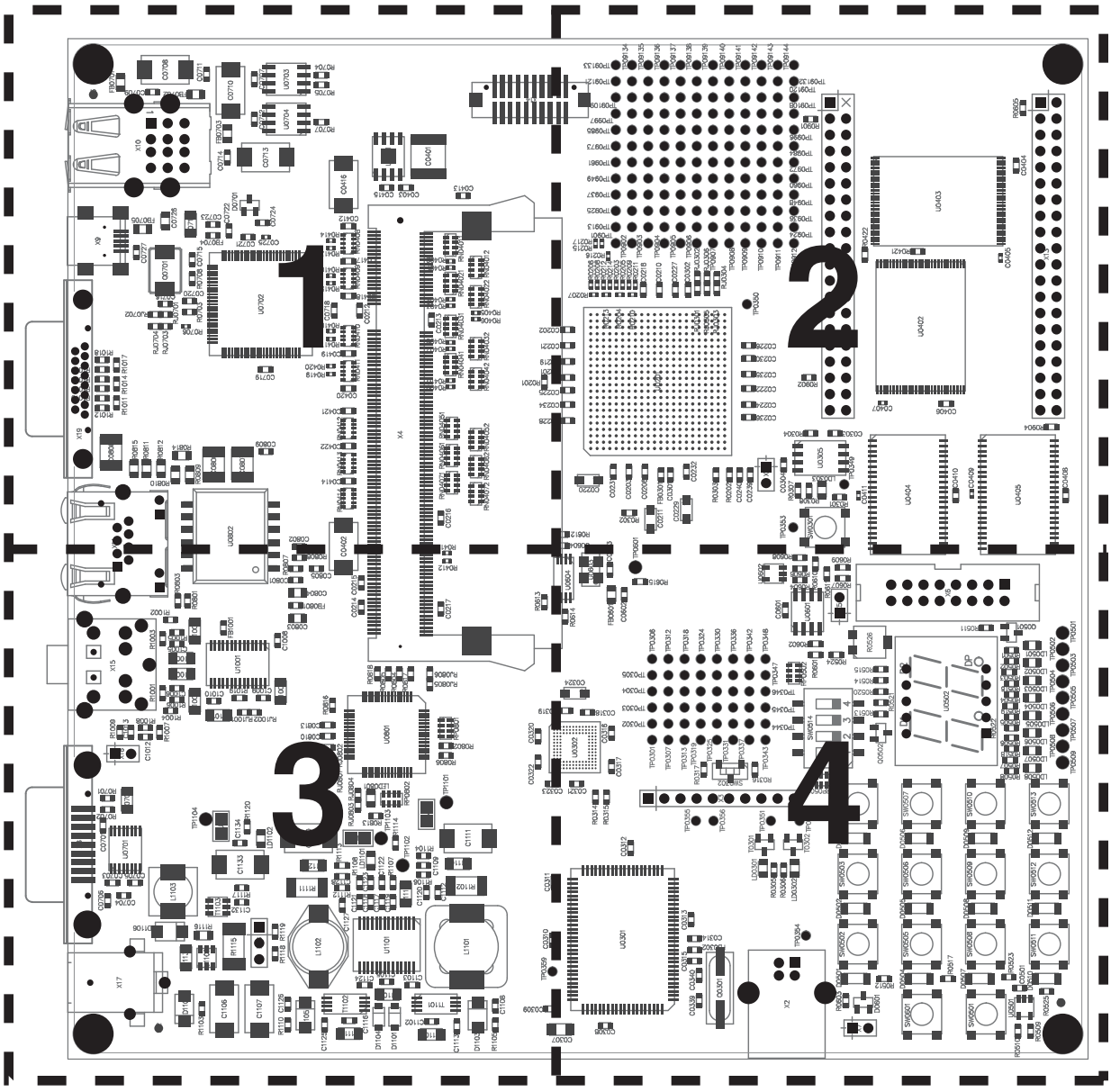


Figure 23. Assembly Diagram, Section 1 Detail

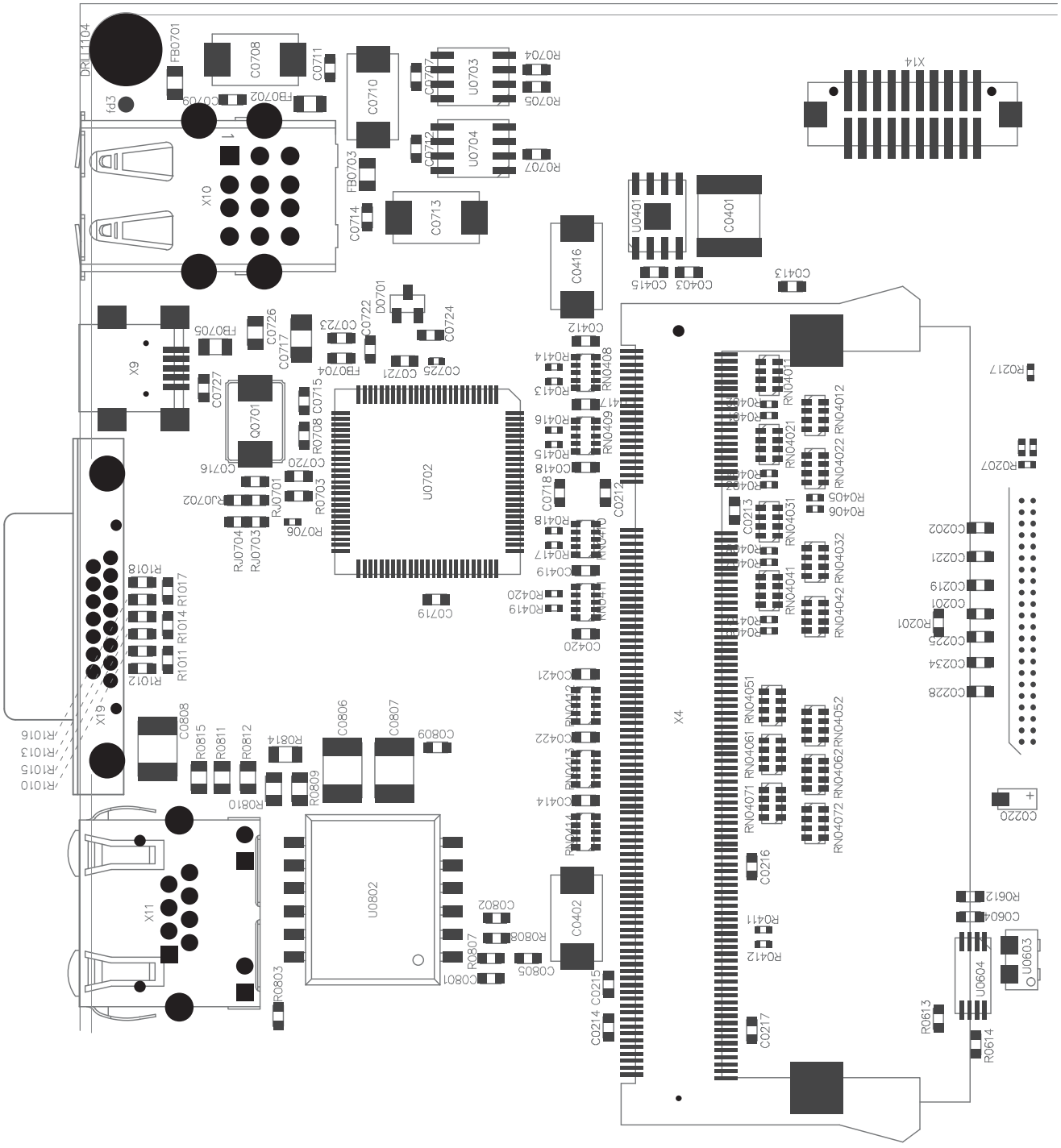


Figure 24. Assembly Diagram, Section 2 Detail

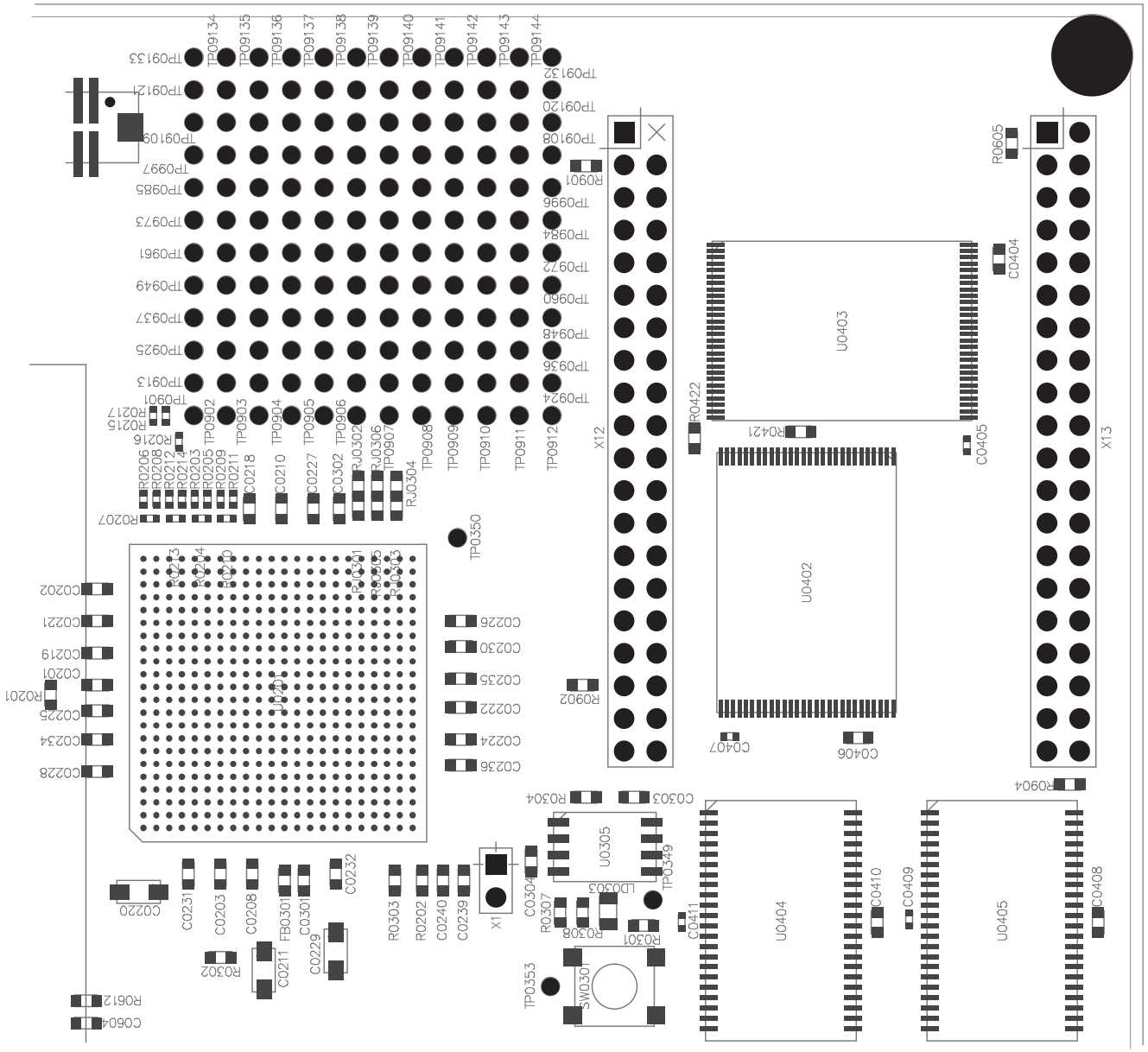


Figure 25. Assembly Diagram, Section 3 Detail

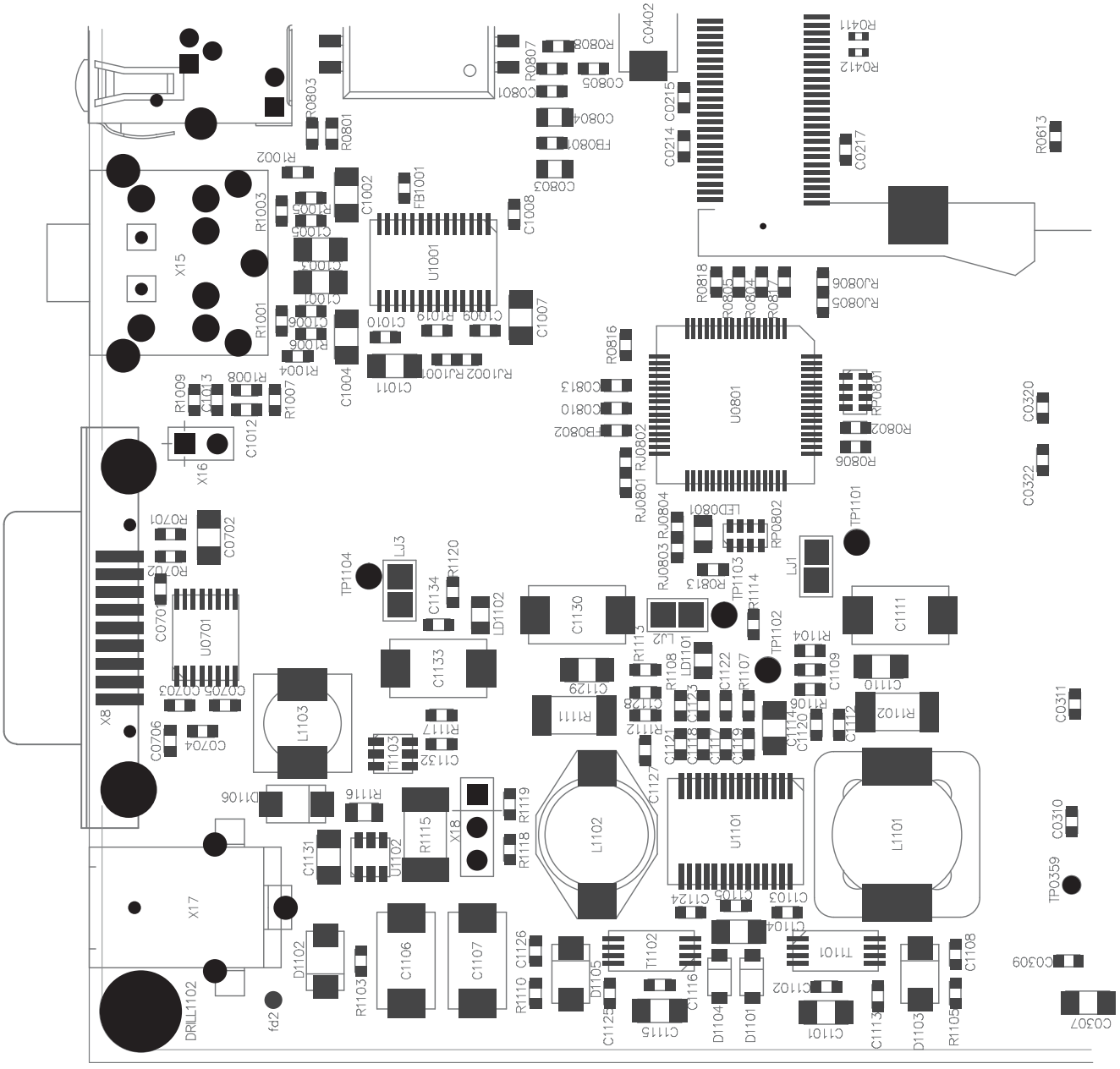
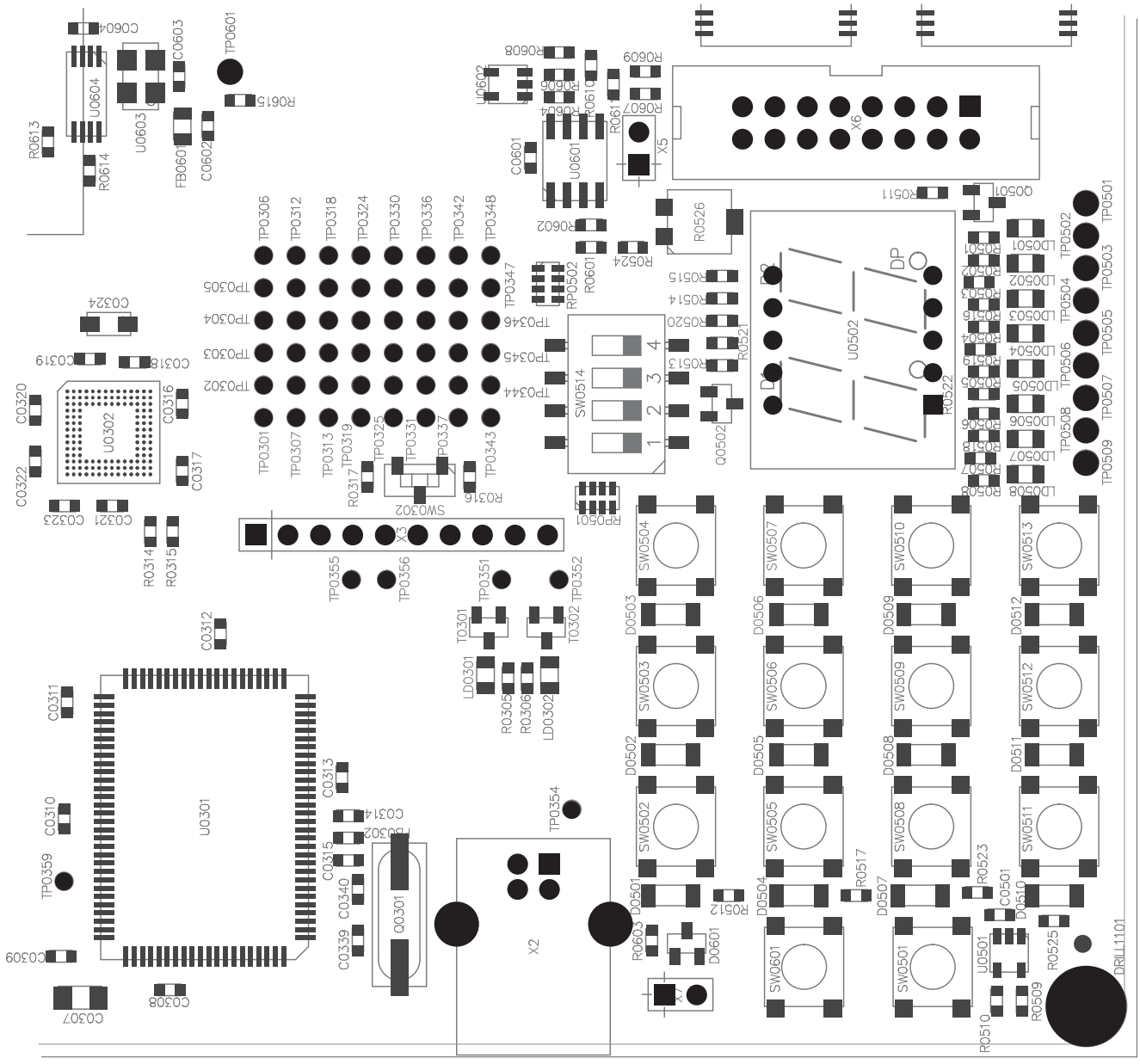


Figure 26. Assembly Diagram, Section 4 Detail



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