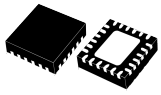
LNBH26S

Datasheet

Dual LNBS supply and control I²C with step-up and IC interface



QFN24 (4x4 mm)

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specification (15 programmable levels)
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- 22 kHz tone waveform integrity guaranteed at no-load condition as well
- Low drop post regulator and high efficiency step-up PWM with integrated power NMOS allowing low power losses
- LPM function (low power mode) to reduce dissipation
- Overload and overtemperature internal protection with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers

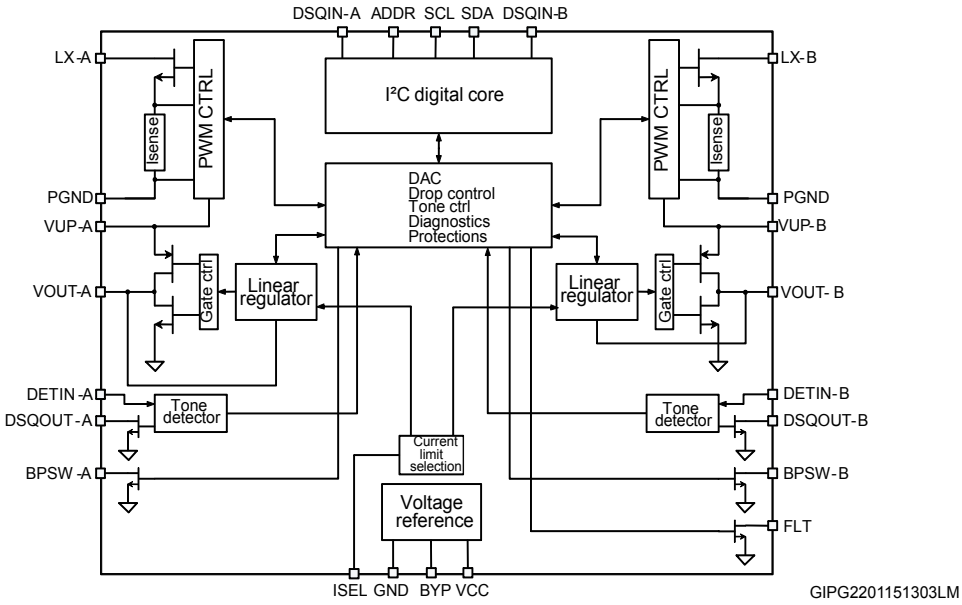
Maturity status link	
LNBH26S	
Device summary	
Order code	LNBH26SPQR
Package	QFN24 (4 x 4)
Packing	Tape and reel

Description

Intended for analog and digital dual satellite receivers/Sat-TV, and Sat-PC cards, the LNBH26S is a monolithic voltage regulator and interface IC, assembled in QFN24 4 x 4 specifically designed to provide the 13/18 V power supply and the 22 kHz tone signaling to the LNB down-converter in the antenna dishes or to the multi-switch box. In this application field, it offers a complete solution for dual tuner satellite receivers with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

1 Block diagram

Figure 1. **Block diagram**



2 Application information (valid for each section A/B)

The LNBH26S includes two completely independent sections. Except for ISEL, V_{CC} and I²C inputs, each circuit can be separately controlled and have their independent external components. All the specifications below must be considered equal for both sections (A/B).

This IC has a built-in DC-DC step-up converter that, from a single source (8 V to 16 V), generates the voltages (V_{UP}) that let the integrated LDO post-regulator (generating the 13 V / 18 V LNB output voltages plus the 22 kHz DiSEqC™ tone) work with a minimum dissipated power of 0.5 W typ. @ 500 mA load (the LDO drop voltage is internally kept at V_{UP} - V_{OUT} = 1 V typ.). The LDO power dissipation can be further reduced when 22 kHz tone output is disabled by setting the LPM bit to “1” (see LPM function description). The IC is also provided with an undervoltage lockout circuit that disables the whole circuit when the supplied V_{CC} drops below a fixed threshold (4.7 V typ.). The step-up converter soft-start function reduces the in-rush current during startup. The SS time is internally fixed at 4 ms typ. to switch from 0 to 13 V, and 6 ms typ. to switch from 0 to 18 V.

2.1 DISEQC™ data encoding (DSQIN pin)

The internal 22 kHz tone generator is factory trimmed in accordance with the DiSEqC™ standards, and can be activated in 3 different ways:

1. by an external 22 kHz source DiSEqC™ data connected to the DSQIN logic pin (TTL compatible). In this case the I²C tone control bits must be set: EXTM=TEN=1.
2. by an external DiSEqC™ data envelope source connected to the DSQIN logic pin. In this case the I²C tone control bits must be set: EXTM=0 and TEN=1.
3. through the TEN I²C bit if the 22 kHz presence is requested in continuous mode. In this case the DSQIN TTL pin must be pulled HIGH and the EXTM bit set to “0”.

Each of the above solutions requires that during the 22 kHz tone activation and/or DiSEqC™ data transmission, the LPM bit must be set to “0” see Section 2.4 LPM (low power mode).

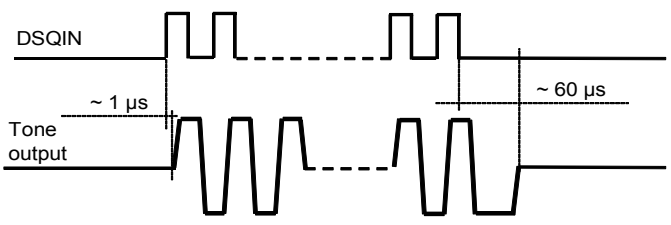
2.2 Data encoding by external 22 kHz tone TTL signal

In order to improve design flexibility an external tone signal can be input to the DSQIN pin by setting the EXTM bit to “1”.

The DSQIN is a logic input pin which activates the 22 kHz tone to the V_{OUT} pin, by using the LNBH26S integrated tone generator.

The output tone waveforms are internally controlled by the LNBH26S tone generator in terms of rise/fall time and tone amplitude, while, the external 22 kHz signal on the DSQIN pin is used to define the frequency and the duty cycle of the output tone. A TTL compatible 22 kHz signal is required for the proper control of the DSQIN pin function. Before sending the TTL signal on the DSQIN pin, the EXTM and TEN bits must be previously set to “1”. As soon as the DSQIN internal circuit detects the 22 kHz TTL external signal code, the LNBH26S activates the 22 kHz tone on the V_{OUT} output with about 1 µs delay from TTL signal activation, and it stops with about 60 µs delay after the 22 kHz TTL signal on DSQIN has expired, refer to Figure 2. Tone enable and disable timing (using external waveform).

Figure 2. Tone enable and disable timing (using external waveform)



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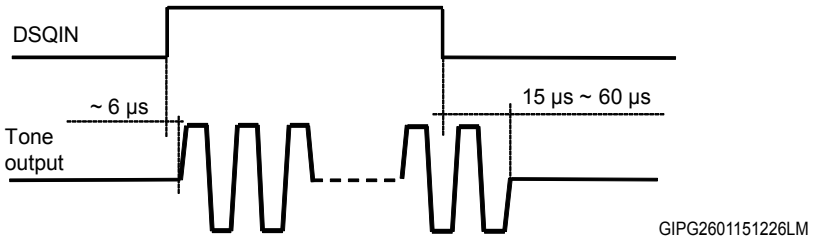
2.3 Data encoding by external DiSEqC envelope control through the DSQIN pin

If an external DiSEqC™ envelope source is available, it is possible to use the internal 22 kHz generator activated during the tone transmission by connecting the DiSEqC™ envelope source to the DSQIN pin. In this case the I²C tone control bits must be set: EXTM=0 and TEN=1. In this way the internal 22 kHz signal is superimposed on the V_{OUT} DC voltage to generate the LNB output 22 kHz tone. During the period in which the DSQIN is kept HIGH the internal control circuit activates the 22 kHz tone output.

The 22 kHz tone on the V_{OUT} pin is activated with a delay of about 6 µs from DSQIN TTL signal rising edge, and it stops with a delay time in the range of 15 µs to 60 µs after the 22 kHz TTL signal on DSQIN has expired, refer to Figure 3. Tone enable and disable timing (using envelope signal).

Figure 3. Tone enable and disable timing (using envelope signal)



2.4 LPM (low power mode)

In order to reduce total power loss, each section of the LNBH26S is provided with the LPM I²C bit that can be activated (LPM=1) in applications where the 22 kHz tone can be disabled for long time periods. The LPM bit can be set to “1” when the DiSEqC™ data transmission is not requested (no 22 kHz tone output is present); in this condition the drop voltage across the integrated LDO regulator (V_{UP} - V_{OUT}) is reduced to 0.6 V typ. and, consequently, the power loss inside the relative LNBH26S channel regulator is reduced too. For example, at 500 mA load, LPM=1, allowing a minimum LDO dissipated power of 0.3 W typ. It is recommended to set the LPM bit to “0” before starting the 22 kHz DiSEqC™ data transmission; in this condition the drop voltage across the LDO is kept to 1 V typ. Keep LPM=0 all times if LPM function is not used.

2.5 DISEQC™ 2.0 implementation

The built-in 22 kHz tone detector completes the fully bi-directional DiSEqC™ 2.0 interfacing. Each LNBH26S section DETIN pin must be AC coupled to the DiSEqC™ bus, and extracted PWK data is available on the corresponding DSQOUT pin. To comply with the bi-directional DiSEqC™ 2.0 bus hardware requirements, an output R-L filter is needed (per each voltage output pin). In order to avoid 22 kHz waveform distortion during tone transmission, each LNBH26S section is provided with a BPSW pin to be connected to an external transistor, which allows the bypassing of the corresponding output RL filter in DiSEqC 2.x applications while in transmission mode. Before starting tone transmission by means of the DSQIN pin, provide that the TEN bit is preventively set to “1” and after ending tone transmission, provide that the TEN bit is set to “0”.

2.6 Output current limit selection

The linear regulators current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit by the equation:

$$I_{MAX}\left(typ.\right) = \frac{16578}{RSEL^{1.206}} \quad (1)$$

with ISET = 0

$$I_{MAX}\left(typ.\right) = \frac{6452}{RSEL^{1.159}} \quad (2)$$

with ISET = 1

where RSEL is the resistor connected between ISEL and GND expressed in kΩ and I_{LIM}(typ.) is the typical current limit threshold expressed in mA. I_{LIM} can be set up to 1 A for each channel. However, it is recommended to not exceed, for a long period, a total amount of current of 1 A from both sections (I_{OUT_A} + I_{OUT_B} < 1 A) in order to avoid the overtemperature protection triggering and to thoroughly validate the PCB layout thermal management in real application environment conditions.

2.7 Output voltage selection

Each linear regulator channel output voltage level can be easily programmed in order to accomplish application specific requirements, using 4 + 4 bits of an internal DATA1 register see and Table 13. Output voltage selection (data1 register, write mode) for exact programmable values. Register writing is accessible via the I²C bus.

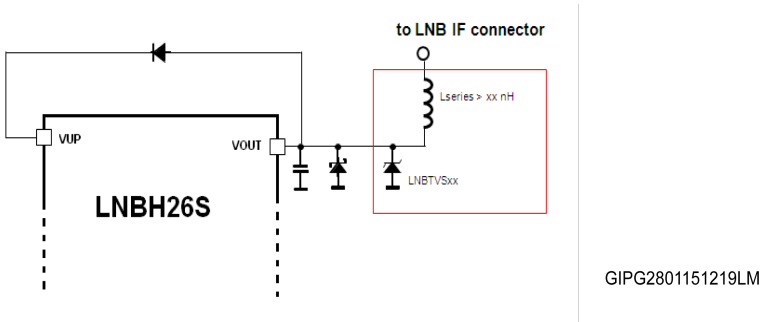
2.8 Diagnostic and protection functions

The LNBH26S has 14 diagnostic internal functions provided via the I²C bus, by reading 14 bits on two STATUS registers (in read mode). All the diagnostic bits are, in normal operation (that is, no failure detected), set to LOW. One diagnostic bit is dedicated to the overtemperature status (OTF), one bit is dedicated to the input voltage power not good function (PNG), while the remaining 12 bits (6 per channel) are dedicated to the overload protection status (OLF), to the output voltage level (VMON), to 22 kHz tone characteristics (TMON), to the minimum load current (IMON), to external voltage source presence on the V_{OUT} pin (PDO), and to 22 kHz tone presence on the DETIN pin (TDET). Once the OLF (or the OTF or PNG) bit has been activated (set to “1”), it is latched to “1” until the relevant cause is removed and a new register reading operation is done.

2.9 Surge protections and TVS diodes

Each LNBH26S device section is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. Transient voltage suppressor (TVS) devices are usually used, as shown in the following schematic Figure 4. Surge protection circuit to protect each section of STB output circuits where the LNBH26S and other devices are electrically connected to the antenna cable.

Figure 4. Surge protection circuit



For this purpose we recommend the use of LNBTVSxx surge protection diodes specifically designed by ST. The selection of the LNBTVS diode should be made based on the maximum peak power dissipation that the diode is capable of supporting (see the LNBTVS datasheet for further details).

2.10 FLT: fault FLAG

In order to get an immediate feedback on a diagnostic status, the LNBH26S is equipped with a dedicated fault flag pin (FLT). In the case an overload (OLF bit=1), overheating (OTF bit=1) or power not good (PNG bit=1) condition is detected, the FLT pin (open drain output) is set to low and is kept low until the relevant activating diagnostic bit is cleared. Be aware that diagnostic bits OLF, OTF and PNG, once activated, are kept latched to “1”

until the origin cause is removed and a new register reading operation is performed by the microprocessor. The FLT pin must be connected to a positive voltage (5 V max.) by a pull-up resistor.

2.11 VMON: output voltage diagnostic

When one device output voltage is activated (V_{OUT} pin), its value is internally monitored and, as long as the output voltage level is below the guaranteed limits, the relevant VMON I²C bit is set to “1”, see Table 16. Output voltage diagnostic (VMON-A/B bits, STATUS 1 register) characteristics for more details.

2.12 TMON: 22 kHz tone diagnostic

The 22 kHz tone can be internally detected and monitored if one (or both) DETIN pin are connected to the LNB output bus (see Figure 7. DiSEqC 2.x application circuit) through a decoupling capacitor.

The tone diagnostic function is provided with the corresponding TMON I²C bit. If the 22 kHz tone amplitude and/or the tone frequency is out of the guaranteed limits, see Table 18. 22 kHz tone diagnostic (TMON-A/B bit, STATUS 2 register) characteristics, the corresponding TMON I²C bit is set to “1”.

2.13 TDET: 22 kHz tone detection

When a 22 kHz tone presence is detected on one DETIN pin, the corresponding TDET I²C bit is set to “1”.

2.14 IMON: minimum output current diagnostic

In order to detect the output load absence (no LNB connected on the bus or cable not connected to the IRD) each LNBH26S section is provided with a minimum output current flag by the corresponding IMON I²C bit, accessible in read mode, which is set to “1” if the output current is lower than 12 mA (typ.). It is recommended to use the IMON function only with the 22 kHz tone transmission deactivated, otherwise the IMON bit could be set to “0” even if the output current is below the minimum current threshold. To activate the IMON diagnostic function, set to “1” the EN_IMON I²C bit in the DATA4 register. Be aware that as soon as the IMON function is activated by means of EN_IMON=1, the V_{OUT} is immediately increased to 21 V (typ.) independently on the VSEL bit setting. This operation is applied in order to be sure that the LNBH26S output has the higher voltage present in the LNB bus. Do not use this function in an application environment where a 21 V voltage level is not supported by other peripherals connected to the LNB bus.

2.15 PDO: overcurrent detection on output pull-down stage

When an overcurrent occurs on one section pull-down output stage due to an external voltage source greater than the LNBH26S nominal V_{OUT}, and for a time longer than $I_{SINK\_TIME\_OUT}$ (10 ms typ.), the corresponding PDO I²C bit is set to “1”. This may happen due to an external voltage source presence on the LNB output (V_{OUT} pin).

For current threshold and deglitch time details, see Table 12. A/B section electrical characteristics.

2.16 Power-on I²C interface reset and undervoltage lockout

The I²C interface built into the LNBH26S is automatically reset at power-on. As long as the V_{CC} stays below the undervoltage lockout (UVLO) threshold (4.7 V typ.), the interface does not respond to any I²C command and all DATA register bits are initialized to zeroes, therefore keeping the power blocks disabled. Once the VCC rises above 4.8 V typ., the I²C interface becomes operative and the DATA registers can be configured by the main microprocessor.

2.17 PNG: input voltage minimum detection

When input voltage (V_{CC} pin) is lower than LPD (low power diagnostic) minimum thresholds, the PNG I²C bit is set to “1” and the FLT pin is set LOW.

2.18 ISW: inductor switching current limit

In order to allow low saturation current inductors to be used, the maximum DC-DC inductor switching current limit threshold can be set by one I²C bit per section (ISW). Two values are available: 2.5 A typ. (with ISW = 1) and 4 A typ. (with ISW = 0).

2.19 COMP: boost capacitors and inductor

The DC-DC converter compensation loop can be optimized in order to properly work with both ceramic and electrolytic capacitors (V_{UP} pin). For this purpose, one I²C bit in the DATA 4 register (see COMP) can be set to “1” or “0” as follows:

COMP = 0 for electrolytic capacitors

COMP = 1 for ceramic capacitors

For recommended DC-DC capacitor and inductor values refer to Section 5 Typical application circuits and to the BOM in Table 4. LNBH26S DiSEqC 1.x bill of material.

2.20 OLF: overcurrent and short-circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short-circuit condition, each section of the device is provided with a dynamic short-circuit protection. It is possible to set the short-circuit current protection either statically (simple current clamp) or dynamically by the corresponding PCL bit of the I²C DATA3 register. When the PCL (pulsed current limiting) bit is set lo LOW, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for T_{ON} time (90 ms or 180 ms typ., according to the corresponding TIMER bit programmed in the DATA3 register) and after that, the output is set in shutdown for a T_{OFF} time of typically 900 ms. Simultaneously, the corresponding diagnostic OLF I²C bit of the STATUS1 register is set to “1” and the FLT pin is set to low level. After this time has elapsed, the involved output is resumed for a time T_{ON}. At the end of T_{ON}, if the overload is still detected, the protection circuit cycles again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW after register reading is done. Typical T_{ON} +T_{OFF} time is 990 ms (if TIMER=0) or 1080 ms (if TIMER=1) and is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short-circuit condition, still ensuring excellent power-on startup in most conditions. However, there may be some cases in which a highly capacitive load on the output can cause a difficult startup when the dynamic protection is chosen. This can be solved by initiating any power startup in static mode (PCL=1) and then, switching to dynamic mode (PCL=0) after a chosen amount of time, depending on the output capacitance. Also in static mode, the diagnostic OLF bit goes to “1” (and the FLT pin is set to low) when the current clamp limit is reached and returns LOW when the overload condition is cleared and register reading is done.

After the overload condition is removed, normal operation can be resumed in two ways, according to the OLR I²C bit on the DATA4 register.

If OLR=1, all VSEL bits corresponding to the involved section are reset to “0” and the LNB section output (V_{OUT} pin) is disabled. To re-enable the output stage, the VSEL bits must be set again by the microprocessor and the OLF bit is reset to “0” after a register reading operation.

If OLR=0, the involved output is automatically re-enabled as soon as the overload condition is removed, and the OLF bit is reset to “0” after a register reading operation.

2.21 OTF: thermal protection and diagnostic

The LNBH26S is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and both liner regulators are shut off, the diagnostic OTF bit in the STATUS1 register is set to “1” and the FLT pin is set to low level. After the overtemperature condition is removed, normal operation can be resumed in two ways, according to the THERM I²C bit on the DATA4 register.

If THERM=1, all VSEL bits are reset to “0” and both LNB outputs (V_{OUT} pins) are disabled. To re-enable output stages, the VSEL bits must be set again by the microprocessor, while the OTF bit is reset to “0” after a register reading operation.

If THERM=0, outputs are automatically re-enabled as soon as the overtemperature condition is removed, while the OTF bit is reset to “0” after a register reading operation.

3 Pin configuration

Figure 5. **Pin connections (top view)**

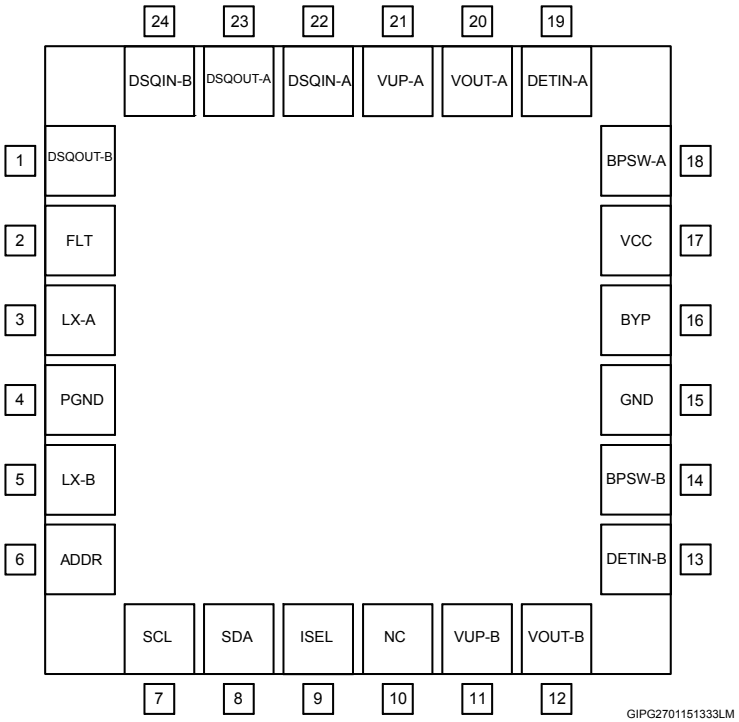


Table 1. **Pin description**

Pin	Symbol	Name	Pin function
1	DSQOUT-B	DiSEqC output	Open drain output of channel A tone detector to the main microcontroller for DiSEqC 2.0 data decoding. It is low when tone is detected on the DETIN-B input pin. Set to ground if not used.
2	FLT	FLT	Open drain output for IC fault conditions. It is set low in case of overload (OLF bit) or overheating status (OTF bit) or power not good (PNG bit) is detected. To be connected to pull-up resistor (5 V max.).
3	LX-A	NMOS drain	Channel A, integrated N-channel power MOSFET drain.
4	P-GND	Power ground	DC-DC converter power ground. To be connected directly to the exposed pad.
5	LX-B	NMOS drain	Channel B, integrated N-channel power MOSFET drain.
6	ADDR	Address setting	Two I^2C bus addresses available by setting the address pin level voltage. See Table 15. Address pin characteristics.
7	SCL	Serial clock	Clock from I²C bus.
8	SDA	Serial data	Bi-directional data from/to I²C bus.
9	ISEL	Current selection for both channel A and B	The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold. Refer to Section 2.5 DISEQC™ 2.0 implementation. The RSEL resistor defines the same current limit both for channels A and B.
10	N.C.	Not internally connected	Not internally connected pin. Set floating if not used.

Pin	Symbol	Name	Pin function
11	V_{UP-B}	Channel B step-up voltage	Input of channel B linear post-regulator. The voltage on this pin is monitored by the internal channel B step-up controller to keep a minimum dropout across the linear pass transistor.
12	V_{OUT-B}	Channel B LNB output port	Output of channel B integrated very low drop linear regulator. See Table 13. Output voltage selection (data1 register, write mode) for voltage selection and description.
13	DETIN-B	Tone detector input	Channel B, 22 kHz tone decoder input, must be AC coupled to the DiSEqC 2.0 bus. Set to ground if not used.
14	BPSW-B	Switch control	To be connected to an external transistor to be used to bypass the channel B output RL filter needed in DiSEqC 2.x applications during the DiSEqC transmitting mode (see Section 5 Typical application circuits). Set ground if not used. Open drain pin.
15	GND	Analog ground	Analog circuit ground. To be connected directly to the exposed pad.
16	BYP	Bypass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended to connect an external ceramic capacitor only. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.
17	V_{CC}	Supply input	8 to 16 V IC DC-DC power supply.
18	BPSW-A	Switch control	To be connected to an external transistor to be used to bypass the channel A output RL filter needed in DiSEqC 2.x applications during the DiSEqC transmitting mode (see Section 5 Typical application circuits). Set to ground if not used. Open drain pin.
19	DETIN-A	Tone detector input	Channel A, 22 kHz tone decoder input, must be AC coupled to the DiSEqC 2.0 bus. Set to ground if not used.
20	V_{OUT-A}	Channel A, LNB output port	Output of channel A integrated very low drop linear regulator. See Table 13. Output voltage selection (data1 register, write mode) for voltage selection and description.
21	V_{UP-A}	Channel A step-up voltage	Input of channel A linear post-regulator. The voltage on this pin is monitored by the internal channel A step-up controller to keep a minimum dropout across the linear pass transistor.
22	DSQIN-A	DSQIN for DiSEqC envelope input or external 22 kHz TTL input	It is intended for channel A 22 kHz tone control. It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on the EXTM-A I²C bit setting as follows: If EXTM-A=0, TEN-A=1: it accepts the DiSEqC envelope code from the main microcontroller. The LNBH26S uses this code to modulate the internally generated 22 kHz carrier. If EXTM-A=TEN-A=1: it accepts external 22 kHz logic signals which activate the 22 kHz tone output (refer to Section 2.2 Data encoding by external 22 kHz tone TTL signal). Pull up high if the tone output is activated by the TEN-A I²C bit only.
23	DSQOUT-A	DiSEqC output	Open drain output of channel A tone detector to the main microcontroller for DiSEqC 2.0 data decoding. It is low when tone is detected to the DETIN-A input pin. Set ground if not used.
24	DSQIN-B	DSQIN for DiSEqC envelope input or external 22 kHz TTL input	It is intended for channel B 22 kHz tone control. It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on the EXTM-B I²C bit setting as follows: if EXTM-B=0, TEN-B=1: it accepts the DiSEqC envelope code from the main microcontroller. The LNBH26S uses this code to modulate the internally generated 22 kHz carrier. If EXTM-A=TEN-A=1: it accepts external 22 kHz logic signals which activate the 22 kHz tone output (refer to Section 2.2 Data encoding by external 22 kHz tone TTL signal). Pull up high if the tone output is activated by the TEN-B I²C bit only.
Epad	Epad	Exposed pad	To be connected with power grounds and to ground layer through vias to dissipate the heat.

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	-0.3 to 20	V
V_{UP}	DC input voltage	-0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	-0.3 to 40	V
V_I	Logic input pin voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
V_O	Logic output pin voltage (FLT, DSQOUT)	-0.3 to 7	V
V_{BPSW}	BPSW pin voltage	-0.3 to 40	V
V_{DETIN}	Detector input signal amplitude	-0.6 to 2	V
I_O	Logic output pin current (FLT, DSQOUT, BPSW)	10	mA
LX	LX input voltage	-0.3 to 30	V
V_{BYP}	Internal reference pin voltage	-0.3 to 4.6	V
I_{SEL}	Current selection pin voltage	-0.3 to 3.5	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
T_{JMAX}	Maximum junction temperature	150	°C
ESD	ESD rating with human body model (HBM) for all pins, except power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

Table 3. Thermal data

Symbol	Parameter	Value	Unit
RthJC	Thermal resistance junction-case	2	°C/W
RthJA	Thermal resistance junction-ambient with device soldered on 2s2p 4-layer PCB provided with thermal vias below exposed pad	40	°C/W

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.

5 Typical application circuits

Figure 6. **DiSEqC 1.x application circuit**

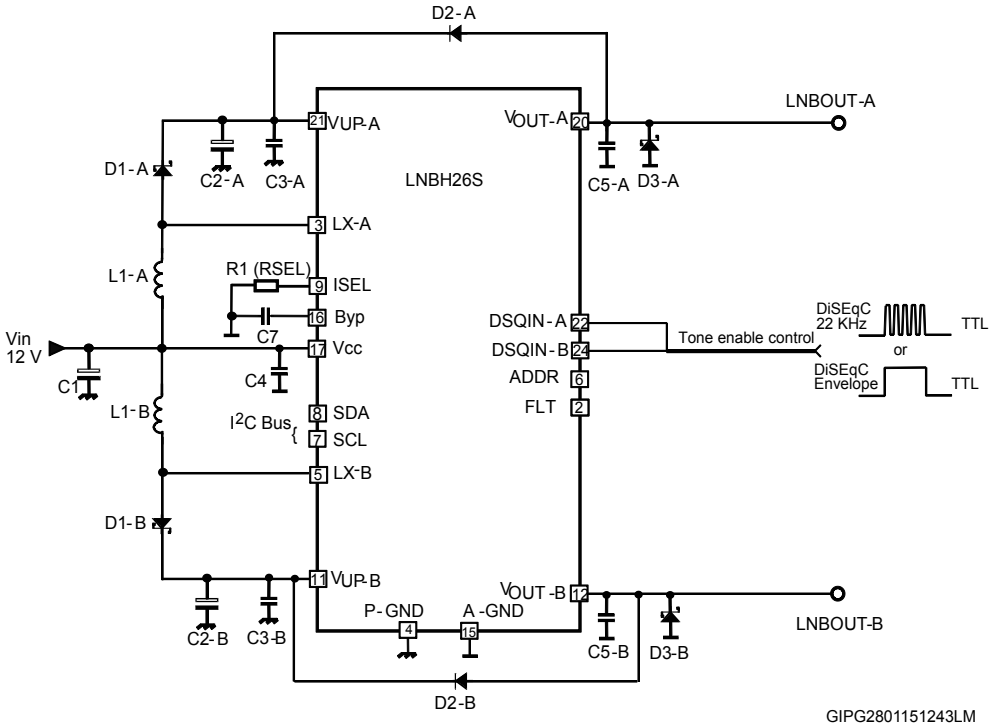


Table 4. **LNBH26S DiSEqC 1.x bill of material**

Component	Notes
R1 (RSEL)	Smd resistor. Refer to Table 12. A/B section electrical characteristics and ISEL pin description in Table 1. Pin description.
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable
C3	From 470 nF to 2.2 µF ceramic capacitor placed as close as possible to V_{UP} pins. Higher values allow lower DC-DC noise
C5	From 100 nF to 220 nF ceramic capacitor placed as close as possible to V_{OUT} pins. Higher values allow lower DC-DC noise
C4, C7	220 nF ceramic capacitors. To be placed as close as possible to V_{OUT} pin
D1	STPS130A or similar Schottky diode
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with $I_F(AV)$ > 0.2 A, V_{RRM} > 25 V, V_F < 0.5 V. To be placed as close as possible to V_{OUT} pin

Component	Notes
L1	With COMP=0, use 10 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current or with COMP=1 and C2 = 22 µF, use 6.8 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current

Figure 7. DiSEqC 2.x application circuit

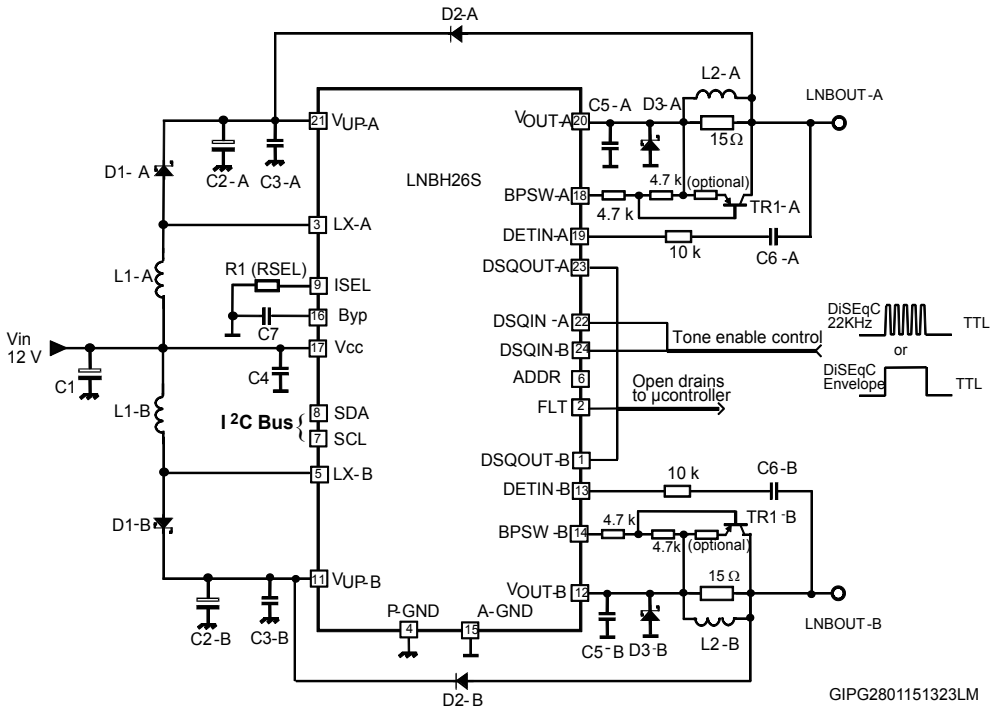


Table 5. LNBH26S DiSEqC 2.x bill of material

Component	Notes
R1 (RSEL)	SMD resistor. Refer to Table 12. A/B section electrical characteristics and ISEL pin description in Table 1. Pin description.
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable
C3	From 470 nF to 2.2 µF ceramic capacitor placed as close as possible to V_{UP} pins. Higher values allow lower DC-DC noise
C5	From 100 nF to 220 nF ceramic capacitor placed as close as possible to V_{OUT} pins. Higher values allow lower DC-DC noise
C4, C7	220 nF ceramic capacitors. To be placed as close as possible to V_{OUT} pin
D1	STPS130A or similar Schottky diode

Component	Notes
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with $I_F(AV)$ > 0.2 A, V_{RRM} > 25 V, V_F < 0.5 V. To be placed as close as possible to V_{OUT} pin
L1	With COMP=0, use 10 µH inductor with I_{SAT} > I_{PEAK} where I_{PEAK} is the boost converter peak current or with COMP=1 and C2 = 22 µF, use 6.8 µH inductor with I_{SAT} > I_{PEAK} where I_{PEAK} is the boost converter peak current
L2	220 µH - 270 µH inductor as per DiSEqC 2.x specification
TR1	MMBTA92, 2STR2160 or any low power PNP with I_C > 250 mA, V_{CE} > 30 V, can be used Also any small power PMOS with I_D > 250 mA, $R_{DS(on)}$ < 0.5 W, V_{DS} > 20 V, can be used

6 I²C bus interface

Data transmission from the main microprocessor to the LNBH26S and vice versa takes place through the 2-wire I²C bus interface, consisting of the 2-line SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

6.1 Data validity

As shown in Figure 8. Data validity on the I²C bus, the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

6.2 Start and stop condition

As shown in Figure 9. Timing diagram of I²C bus, a start condition is HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

6.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see Figure 10. Acknowledge on the I²C bus). The peripheral (LNBH26S) which acknowledges must pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed must generate acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninthclock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH26S does not generate acknowledge if the V_{CC} supply is below the undervoltage lockout threshold (4.7 V typ.).

6.5 Transmission without acknowledge

If detection of the acknowledge of the LNBH26S is not required, the microprocessor can use a simpler transmission: it simply waits for one clock without checking the slave acknowledging, and sends the new data. This approach is of course less protected from misworking and decreases noise immunity.

Figure 8. **Data validity on the I²C bus**

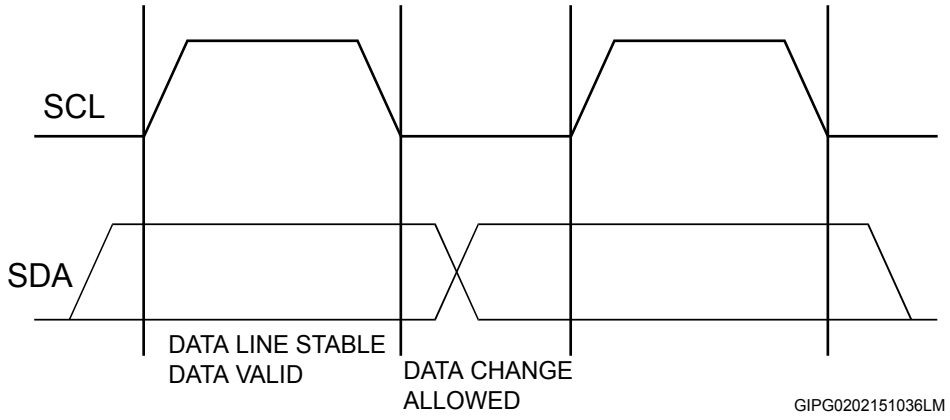


Figure 9. **Timing diagram of I²C bus**

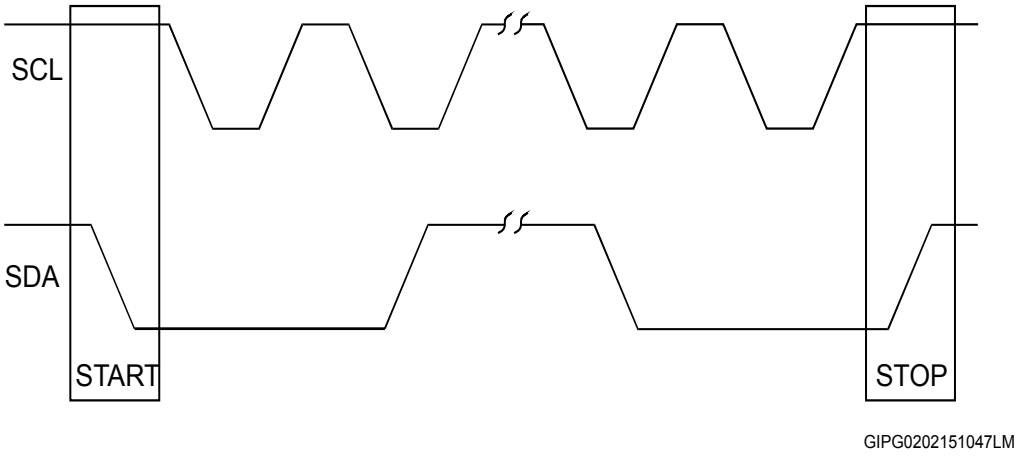
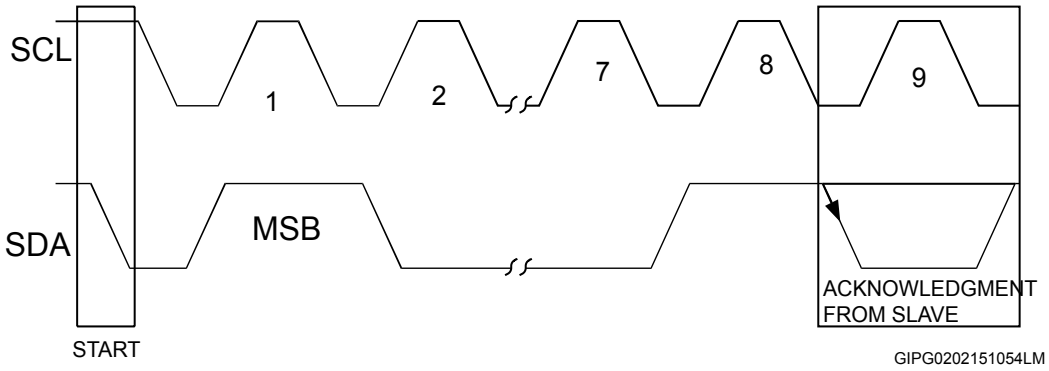


Figure 10. **Acknowledge on the I²C bus**



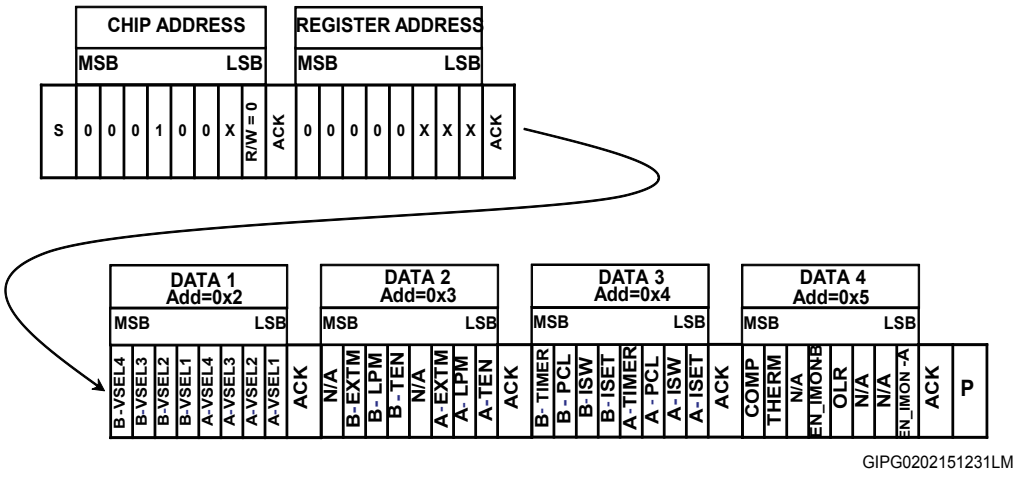
7 I²C interface protocol

7.1 Write mode transmission

The LNBH26S interface protocol is made up of:

- a start condition (S)
- a chip address byte with the LSB bit R/W = 0
- a register address (internal address of the first register to be accessed)
- a sequence of data (byte to write in the addressed internal register + acknowledge)
- the following bytes, if any, to be written in successive internal registers
- a stop condition (P). The transfer lasts until a stop bit is encountered
- the LNBH26S, as slave, acknowledges every byte transfer

Figure 11. Example of writing procedure starting with first data address 0x2



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ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address (see Table 15. Address pin characteristics for pin selection)

Note: The writing procedure can start from any register address by simply setting the X values in the register address byte (after the chip address). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

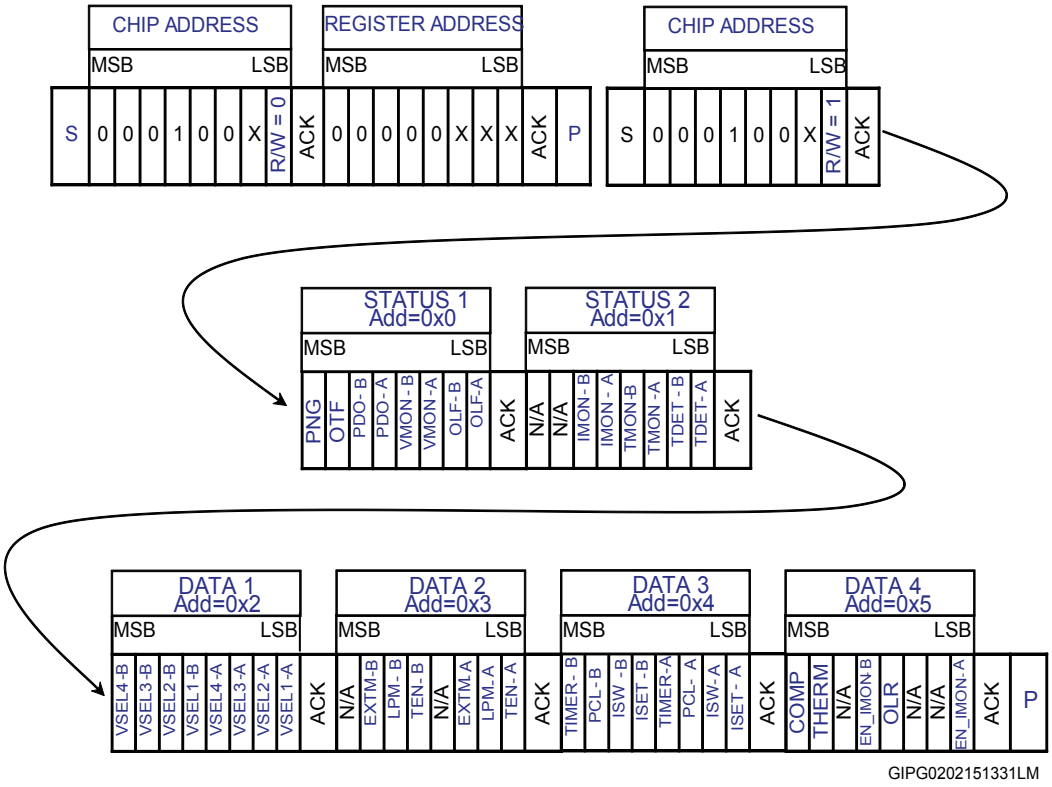
7.2 Read mode transmission

In read mode the byte sequence must be as follows:

- a start condition (S)
- a chip address byte with the LSB bit R/W=0
- the register address byte of the internal first register to be accessed
- a stop condition (P)
- a new master transmission with the chip address byte and the LSB bit R/W=1
- after the acknowledge the LNBH26S starts sending the addressed register content. As long as the master keeps the acknowledge LOW, the LNBH26S transmits the next address register byte content

- the transmission is terminated when the master sets the acknowledge HIGH with a following stop bit

Figure 12. Example of reading procedure starting with first status address 0X0



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ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address, see Table 15. Address pin characteristics for pin selection) and see Table 11. STATUS 2 (read register. Register address = 0X1).

Note: The reading procedure can start from any register address (status 1, 2 or Data1..4) by simply setting the X values in the register address byte (after the first chip address in the above figure). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

7.3 Data registers

The data 1..4 registers can be addressed both to write and read mode. In read mode they return the last writing byte status received in the previous write transmission.

The following tables provide the register address values of data 1..4 and a function description of each bit.

Note: The following tables provide the register address values of data 1..4 and a function description of each bit.

Table 6. DATA 1 (read/write register. Register address = 0X2)

Bit	Name	CH	Value	Description
Bit 0 (LSB)	VSEL1-A	A	0/1	Channel A Output voltage selection bits
Bit 1	VSEL2-A		0/1	
Bit 2	VSEL3-A		0/1	
Bit 3	VSEL4-A		0/1	
Bit 4	VSEL1-B	B	0/1	Channel B Output voltage selection bits
Bit 5	VSEL2-B		0/1	
Bit 6	VSEL3-B		0/1	
Bit 7	VSEL4-B		0/1	

Table 7. DATA 2 (read/write register. Register address = 0X3)

Bit	Name	CH	Value	Description
Bit 0 (LSB)	TEN-A	A	1	22 kHz tone enabled. Tone output controlled by the DSQIN pin
			0	22 kHz tone output disabled
Bit 1	LPM-A		1	Low power mode activated (used only with 22 kHz tone output disabled)
			0	Low power mode deactivated (keep always LPM=0 during 22 kHz tone transmission)
Bit 2	EXTM-A		1	DSQIN input pin is set to receive external 22 kHz TTL signal source
			0	DSQIN input pin is set to receive external DiSEqC envelope TTL signal
Bit 3	N/A		0	Reserved. Keep to “0”
Bit 4	TEN-B	B	1	22 kHz tone enabled. Tone output controlled by the DSQIN pin
			0	22 kHz tone output disabled
Bit 5	LPM-B		1	Low power mode activated (used only with 22 kHz tone output disabled)
			0	Low power mode deactivated (keep always LPM=0 during 22 kHz tone transmission)
Bit 6	EXTM-B		1	DSQIN input pin is set to receive external 22 kHz TTL signal source
			0	DSQIN input pin is set to receive external DiSEqC envelope TTL signal
Bit 7 (MSB)	N/A		0	Reserved. Keep to “0”

Table 8. DATA 3 (read/write register. Register address = 0X4)

Bit	Name	CH	Value	Description
Bit 0 (LSB)	ISET-A	A	1	Current limit of LNB output (VOUT pin) set to lower current range
			0	Current limit of LNB output (VOUT pin) set to default range
Bit 1	ISW-A		1	DC-DC, inductor switching current limit set to 2.5 A typ.
			0	DC-DC, inductor switching current limit set to 4 A typ.
Bit 2	PCL-A		1	Pulsed (dynamic) LNB output current limiting is deactivated
			0	Pulsed (dynamic) LNB output current limiting is activated
Bit 3	TIMER-A		1	Pulsed (dynamic) LNB output current T_{ON} time set to 180 ms typ.
			0	Pulsed (dynamic) LNB output current T_{ON} time set to 90 ms typ.
Bit 4	ISET-B	B	1	Current limit of LNB output (VOUT pin) set to lower current range
			0	Current limit of LNB output (VOUT pin) set to default range
Bit 5	ISW-B		1	DC-DC, inductor switching current limit set to 2.5 A typ.
			0	DC-DC, inductor switching current limit set to 4 A typ.
Bit 6	PCL-B		1	Pulsed (dynamic) LNB output current limiting is deactivated
			0	Pulsed (dynamic) LNB output current limiting is activated
Bit 7 (MSB)	TIMER-B		1	Pulsed (dynamic) LNB output current T_{ON} time set to 180 ms typ.
			0	Pulsed (dynamic) LNB output current T_{ON} time set to 180 ms typ.

Table 9. DATA 4 (read/write register. Register address = 0X5)

Bit	Name	CH	Value	Description
Bit 0 (LSB)	EN_IMON-A	A	1	IMON diagnostic function is enabled. (VOUT is set to 21 V typ.)
			0	IMON diagnostic function is disabled. Keep always at “0” if IMON is not used
Bit 1	N/A		0	Reserved. Keep to “0”
Bit 2			0	
Bit 3	OLR	A/B	1	In the case of overload protection activation (OLF=1), all VSEL bits are reset to “0” and LNB relevant output (VOUT pin) is disabled. The VSEL bits must be set again by the master after the overcurrent condition is removed (OLF=0)
			0	In the case of overload protection activation (OLF=1) the LNB output (VOUT pin) is automatically enabled as soon as the overload condition is removed (OLF=0) with the previous VSEL bit setting
Bit 4	EN_IMON-B	B	1	IMON diagnostic function is enabled
			0	IMON diagnostic function is disabled. Always keep “0” if IMON is not used
Bit 5	N/A		0	Reserved. Keep “0”

Bit	Name	CH	Value	Description
Bit 6	THERM	A/B	1	If thermal protection is active (OTF=1), all VSEL bits are reset to “0” and LNB output (VOUT pin) is disabled (both section A and B). VSEL bits must be set again by the master after the overtemperature condition is removed (OTF=0)
			0	In the case of thermal protection activation (OTF=1) the LNB output (VOUT pin) is automatically enabled as soon as the overtemperature condition is removed (OTF=0) with the previous VSEL bit setting
Bit 7 (MSB)	COMP		1	DC-DC converter compensation. Set to use very low E.S.R. capacitors or ceramic caps on VUP pin
			0	DC-DC converter compensation. Set to use standard electrolytic capacitors on VUP pin

7.4 Status registers

The STATUS 1, 2 registers can be addressed to read mode only and provide the diagnostic functions described in the following tables.

Table 10. STATUS 1 (read register. Register address = 0X0)

Bit	Name	CH	Value	Description
Bit 0 (LSB)	OLF-A	A	1	VOUT pin overload protection has been triggered (I_{OUT} > I_{LIM}).
			0	No overload protection has been triggered to VOUT pin (I_{OUT} < I_{LIM})
Bit 1	OLF-B	B	1	VOUT pin overload protection has been triggered (I_{OUT} > I_{LIM}).
			0	No overload protection has been triggered to VOUT pin (I_{OUT} < I_{LIM})
Bit 2	VMON-A	A	1	Output voltage (VOUT pin) is lower than VMON specification thresholds. Refer to Table 16. Output voltage diagnostic (VMON-A/B bits, STATUS 1 register) characteristics
			0	Output voltage (VOUT pin) is within the VMON specifications
Bit 3	VMON-B	B	1	Output voltage (VOUT pin) is lower than VMON specification thresholds. Refer to Table 16. Output voltage diagnostic (VMON-A/B bits, STATUS 1 register) characteristics
			0	Output voltage (VOUT pin) is within the VMON specifications
Bit 4	PDO-A	A	1	Overcurrent detected on output pull-down stage for a time longer than the deglitch period. This may happen due to an external voltage source present on the LNB output (VOUT pin)
			0	No overcurrent detected on output pull-down stage
Bit 5	PDO-B	B	1	Overcurrent detected on output pull-down stage for a time longer than the deglitch period. This may happen due to an external voltage source present on the LNB output (VOUT pin)
			0	No overcurrent detected on output pull-down stage

Bit	Name	CH	Value	Description
Bit 6	OTF	A/B	1	Junction overtemperature is detected, T_J > 150 °C (typ.). See also the THERM bit setting
			0	Junction overtemperature not detected, T_J <135 °C (typ.). T_J is below thermal protection threshold
Bit 7 (MSB)	PNG		1	Input voltage (VCC pin) is lower than LPD minimum thresholds. Refer to Table 12. A/B section electrical characteristics.
			0	Input voltage (VCC pin) is higher than LPD thresholds. Refer to Table 12. A/B section electrical characteristics.

N/A = reserved bit
All bits reset to 0 at power-on

Table 11. STATUS 2 (read register. Register address = 0X1)

Bit	Name	CH	Value	Description
Bit 0 (LSB)	TDET-A	A	1	22 kHz tone presence is detected on the DETIN pin
			0	No 22 kHz tone is detected on the DETIN pin
Bit 1	TDET-B	B	1	22 kHz tone presence is detected on the DETIN pin
			0	No 22 kHz tone is detected on the DETIN pin
Bit 2	TMON-A	A	1	22 kHz tone present on the DETIN pin is out of TMON specification thresholds. That is: the tone frequency or the A_{TONE} (tone amplitude) are out of the thresholds guaranteed in Table 18. 22 kHz tone diagnostic (TMON-A/B bit, STATUS 2 register) characteristics
			0	22 kHz tone present on the DETIN pin is within TMON specification thresholds. Refer to Table 18. 22 kHz tone diagnostic (TMON-A/B bit, STATUS 2 register) characteristics
Bit 3	TMON-B	B	1	22 kHz tone present on the DETIN pin is out of TMON specification thresholds. The tone frequency or the A_{TONE} (tone amplitude) is out of the thresholds guaranteed in Table 18. 22 kHz tone diagnostic (TMON-A/B bit, STATUS 2 register) characteristics
			0	22 kHz tone present on DETIN pin is within TMON specification thresholds. Refer to Table 18. 22 kHz tone diagnostic (TMON-A/B bit, STATUS 2 register) characteristics
Bit 4	IMON-A	A	1	Output current (from VOUT pin) is lower than IMON specification thresholds. Refer to Table 17. Output current diagnostic (IMON-A/B bits, STATUS 2 register) characteristics
			0	Output current (from VOUT pin) is higher than IMON specifications. Refer to Table 17. Output current diagnostic (IMON-A/B bits, STATUS 2 register) characteristics
Bit 5	IMON-B	B	1	Output current (from VOUT pin) is lower than IMON specification thresholds. Refer to Table 17. Output current diagnostic (IMON-A/B bits, STATUS 2 register) characteristics
			0	Output current (from VOUT pin) is higher than IMON specifications. Refer to Table 17. Output current diagnostic (IMON-A/B bits, STATUS 2 register) characteristics

Bit	Name	CH	Value	Description
Bit 6	N/A			Reserved
Bit 7 (MSB)				

N/A = reserved bit
All bits reset to 0 at power-on

8 Electrical characteristics

Refer to Section 5 Typical application circuits, T_J from 0 to 85 °C, all DATA 1..4 register bits set to 0 except VSEL1 = 1, RSEL = 11 kΩ, DSQIN = low, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = V_{OUT} pin voltage. See Section 6 I²C bus interface and Section 7 I²C interface protocol.

Table 12. A/B section electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage (1)		8	12	16	V
I_{IN}	Supply current	Both sections A and B enabled I_{OUT} = 0 mA		12		mA
		22 kHz tone enabled (TEN-A/B = 1, DSQIN-A/B = high), I_{OUT} = 0 mA		19		
		Both sections A and B set in standby: VSEL1=VSEL2=VSEL3=VSEL4=0		2		
V_{OUT}	Output voltage total accuracy	Valid at any V_{OUT} selected level	-3.5		+3.5	%
V_{OUT}	Line regulation	V_{IN} = 8 to 16 V			40	mV
V_{OUT}	Load regulation	I_{OUT} from 50 to 750 mA		100		
I_{LIM}	Output current limiting thresholds	RSEL = 11 kΩ, ISET = 0	750		1100	mA
		RSEL = 15 kΩ, ISET = 0	500		750	
		RSEL = 20 kΩ, ISET = 0	350		550	
I_{LIM}	Output current limiting thresholds	RSEL = 11 kΩ, ISET = 1		400		mA
		RSEL = 15 kΩ, ISET = 1		280		
		RSEL = 20 kΩ, ISET = 1		200		
I_{SC}	Output short-circuit current	RSEL = 11 kΩ, ISET = 0		500		mA
SS	Soft-start time	V_{OUT} from 0 to 13 V		4		ms
SS	Soft-start time	V_{OUT} from 0 to 18 V		6		ms
T13-18	Soft transition rise time	V_{OUT} from 13 V to 18 V		1.5		ms
T18-13	Soft transition fall time	V_{OUT} from 18 V to 13 V		1.5		ms
T_{OFF}	Dynamic overload protection off-time	PCL = 0, output shorted		900		ms
T_{ON}	Dynamic overload protection on-time	PCL = TIMER = 0, output shorted		T_{OFF}/10		
		PCL = 0, TIMER = 1, output shorted		T_{OFF}/5		
A_{TONE}	Tone amplitude	DSQIN=high, EXTM=0, TEN=1 I_{OUT} from 0 to 750 mA C_{BUS} from 0 to 750 nF	0.55	0.675	0.8	V_{PP}
F_{TONE}	Tone frequency	DSQIN=high, EXTM=0, TEN=1	20	22	24	kHz
D_{TONE}	Tone duty cycle		43	50	57	%
tr, tf	Tone rise or fall time (2)		5	8	15	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$Eff_{DC/DC}$	DC-DC converter efficiency	I_{OUT} = 500 mA		93		%
F_{SW}	DC-DC converter switching frequency			440		kHz
UVLO	Undervoltage lockout thresholds	UVLO threshold rising		4.8		V
		UVLO threshold falling		4.7		
V_{LP}	Low power diagnostic (LPD) thresholds	V_{LP} threshold rising		7.2		V
		V_{LP} threshold falling		6.7		
V_{IL}	DSQIN, pin logic low				0.8	V
V_{IH}	DSQIN, pin logic high		2			V
I_{IH}	DSQIN, pin input current	V_{IH} = 5 V		15		µA
F_{DETIN}	Tone detector frequency capture range	0.4 V_{PP} sine wave (3)	19	22	25	kHz
V_{DETIN}	Tone detector input amplitude	Sine wave signal, 22 kHz	0.3		1.5	V_{PP}
Z_{DETIN}	Tone detector input impedance			150		kΩ
V_{OL}	DSQOUT, FLT pin logic LOW	DETIN tone present, I_{OL} = 2 mA		0.3	0.5	V
V_{OL_BPSW}	BPSW pin low voltage	I_{OL_BPSW} = 5 mA DSQIN = high, EXTM = 0, TEN = 1		0.7		V
I_{OZ}	DSQOUT, FLT pin leakage current	DETIN tone absent, V_{OH} = 6 V			10	µA
I_{OBK}	Output backward current	All VSELx = 0, V_{OBK} = 30 V		-3	-6	mA
I_{SINK}	Output low-side sink current	V_{OUT} forced at V_{OUT_nom} +0.1 V		70		mA
$I_{SINK\_TIME-OUT}$	Low-side sink current time-out	V_{OUT} forced at V_{OUT_nom} +0.1 V PDO I²C bit is set to 1 after this time is elapsed		10		ms
I_{REV}	Max. reverse current	V_{OUT} forced at V_{OUT_nom} + 0.1 V, after PDO bit is set to 1 ($I_{SINK\_TIME-OUT}$ elapsed)		2		mA
T_{SHDN}	Thermal shutdown threshold			150		°C
DT_{SHDN}	Thermal shutdown hysteresis			15		°C

1. *In applications where (V_{CC} - V_{OUT}) > 1.3 V, the increased power dissipation inside the integrated LDO must be taken into account in the application thermal management design.*
2. *Guaranteed by design.*
3. *Frequency range in which the DETIN function is guaranteed. The V_{pp} level is intended on the LNB bus (before the C6 capacitor. See typical application circuit for DiSEqC 2.x) I_{OUT} from 0 to 750 mA, C_{BUS} from 0 to 750 nF.*

8.1 Output voltage selection

Each LNBH26S channel is provided with 15 output voltage levels (7 levels for 13 V range when VSEL4-A/B=0 and 8 levels for 18 V range when VSEL4-A/B=1) which can be selected through the register Data1. Table 13. Output voltage selection (data1 register, write mode) shows the output voltage values corresponding to VSELx bit combinations both for channel A and B. If all VSELx are set to “0” the device is set in standby mode and VOUT-A/B is disabled.

T_J from 0 to 85 °C, V_I = 12 V

Table 13. Output voltage selection (data1 register, write mode)

VSEL4-A/B	VSEL3-A/B	VSEL2-A/B	VSEL1-A/B	V_{OUT} min.	V_{OUT} -A/B pin voltage	V_{OUT} max.	Function
0	0	0	0		0		V_{OUT} -A/B disabled. The LNBH26S sets in standby mode
0	0	0	1	12.545	13.000	13.455	
0	0	1	0	12.867	13.333	13.800	
0	0	1	1	13.188	13.667	14.145	
0	1	0	0	13.51	14.000	14.490	
0	1	0	1	13.832	14.333	14.835	
0	1	1	0	14.153	14.667	15.180	
0	1	1	1	14.475	15.000	15.525	
1	0	0	0	17.515	18.150	18.785	
1	0	0	1	17.836	18.483	19.130	
1	0	1	0	18.158	18.817	19.475	
1	0	1	1	18.48	19.150	19.820	
1	1	0	0	18.801	19.483	20.165	
1	1	0	1	19.123	19.817	20.510	
1	1	1	0	19.445	20.150	20.855	
1	1	1	1	19.766	20.483	21.200	

T_J from 0 to 85 °C, V_I = 12 V

Table 14. I^2C electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	SDA, SCL			0.8	V
V_{IH}	High level input voltage	SDA, SCL	2			
I_{IN}	Input current	SDA, SCL V_{IN} = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage (1)	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL	400			kHz

1. *Guaranteed by design.*

T_J from 0 to 85 °C, V_I = 12 V

Table 15. Address pin characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ADDR-1}	"0001000(R/W)" address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
V_{ADDR-2}	"0001001(R/W)" address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

Refer to Section 5 Typical application circuits, T_J from 0 to 85 °C, all DATA 1..4 register bits set to "0", RSEL = 11 kΩ, DSQIN = low, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = V_{OUT} pin voltage.

Table 16. Output voltage diagnostic (VMON-A/B bits, STATUS 1 register) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 13.0 V	VSEL1 = 1, VSEL2 = VSEL3 = VSEL4 = 0	80	90	95	%
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 18.15 V	VSEL4=1, VSEL1 = VSEL2 = VSEL3 = 0	80	90	95	%

Note: If the output voltage is lower than the min. value the VMON I²C bit is set to 1.

If VMON=0 then V_{OUT} > 80% of V_{OUT} (typ.).

If VMON=1 then V_{OUT} < 95% of V_{OUT} (typ.).

Note: Refer to Section 5 Typical application circuits, T_J from 0 to 85 °C, RSEL = 11 kΩ, DSQIN = low, V_{IN} = 12 V, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = V_{OUT} pin voltage.

Table 17. Output current diagnostic (IMON-A/B bits, STATUS 2 register) characteristics

Symbol	*Parameter*	*Test conditions*	*Min.*	*Typ.*	*Max.*	*Unit*
I_{TH}	*Minimum current diagnostic threshold*	*EN_IMON = 1 (V_{OUT} is set to 21 V typ.)*	*5*	*12*	*20*	*mA*

If the output current is lower than the min. threshold limit, the IMON I²C bit is set to 1. If the output current is higher than the max. threshold limit, the IMON I²C bit is set to 0.

Refer to Section 5 Typical application circuits, T_J from 0 to 85 °C, all DATA 1..4 register bits set to "0" except VSEL1 = 1, TEN=1, RSEL = 11 kΩ, DSQIN = HIGH, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = V_{OUT} pin voltage.

Table 18. 22 kHz tone diagnostic (TMON-A/B bit, STATUS 2 register) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
A_{TH-L}	Amplitude diagnostic low threshold	DETIN pin AC coupled	200	300	400	mV
A_{TH-H}	Amplitude diagnostic high threshold	DETIN pin AC coupled	900	1100	1200	mV
F_{TH-L}	Frequency diagnostic low thresholds	DETIN pin AC coupled	13	16.5	20	kHz
F_{TH-H}	Frequency diagnostic high thresholds	DETIN pin AC coupled	24	29.5	38	kHz

Note: If 22 kHz tone parameters are lower or higher than the above limits, the TMON I²C bit is set to "1".

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.1 QFN24 (4x4 mm) package information

Figure 13. **QFN24 (4x4 mm) package outline**

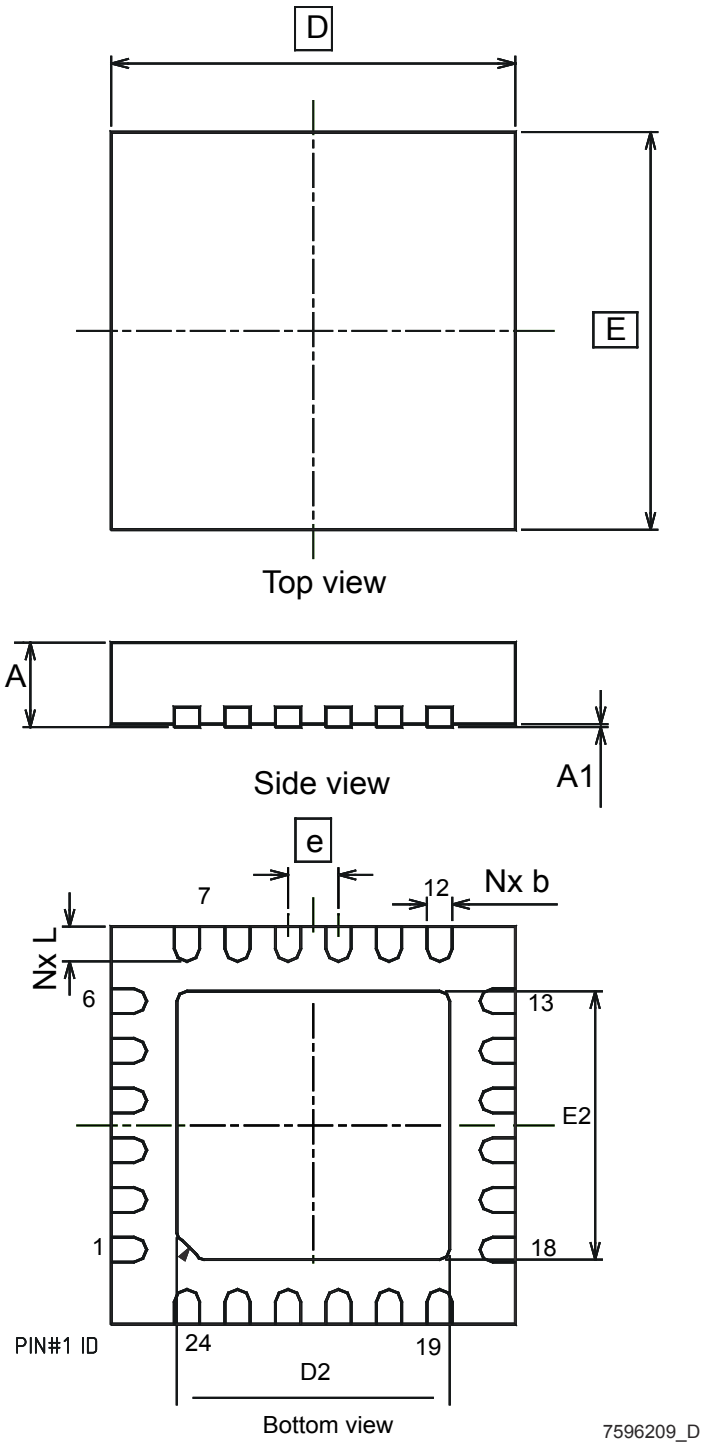
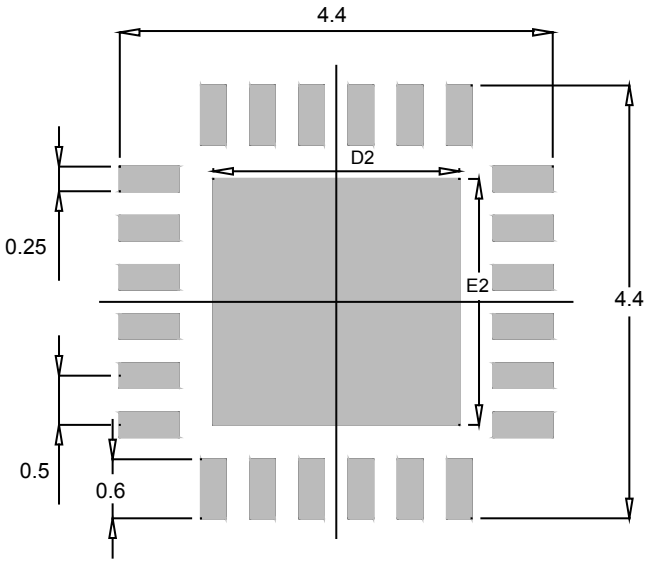


Table 19. **QFN24 (4x4 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
e	0.45	0.50	0.55
L	0.25	0.35	0.45

Figure 14. **QFN24 (4x4 mm) footprint recommended data**



Revision history

Table 20. **Document revision history**

Date	Revision	Changes
27-Mar-2012	1	Initial release.
01-Oct-2012	2	Added: Section 2.12: "TMON: 22 kHz tone diagnostic", Section 2.18: "ISW: inductor switching current limit", Section 2.19: "COMP: boost capacitors and inductor", Section 2.20: "OLF: overcurrent and short-circuit protection and diagnostic" and Section 2.21: "OTF: thermal protection and diagnostic".
12-Feb-2015	3	Modified: Section 2.19: "COMP: boost capacitors and inductor". Changed symbol I_{MAX} to I_{LIM} in Table 13: "A/B section electrical characteristics".
10-Apr-2018	4	Added: T_{JMAX} value Table 2. Absolute maximum ratings.
14-Jun-2018	5	Updated Eq. (1).

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