

# TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

## Plastic Medium-Power Complementary Silicon Transistors

Designed for general-purpose amplifier and low-speed switching applications.

### Features

- High DC Current Gain –  
 $h_{FE} = 2500$  (Typ) @  $I_C$   
= 1.0 Adc
- Collector–Emitter Sustaining Voltage – @ 30 mAdc  
 $V_{CEO(sus)} = 60$  Vdc (Min) – TIP110, TIP115  
= 80 Vdc (Min) – TIP111, TIP116  
= 100 Vdc (Min) – TIP112, TIP117
- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 2.5$  Vdc (Max) @  $I_C$   
= 2.0 Adc
- Monolithic Construction with Built-in Base–Emitter Shunt Resistors
- Pb–Free Packages are Available\*



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### DARLINGTON 2 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80–100 VOLTS, 50 WATTS



TO-220AB  
CASE 221A  
STYLE 1

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### MARKING DIAGRAM



TIP11x = Device Code  
x = 0, 1, 2, 5, 6, or 7  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb–Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

## MAXIMUM RATINGS

| Rating  | Symbol         | TIP110,<br>TIP115 | TIP111,<br>TIP116 | TIP112,<br>TIP117 | Unit                     |
|---|----------------|-------------------|-------------------|-------------------|--------------------------|
| Collector–Emitter Voltage   | $V_{CEO}$      | 60                | 80                | 100               | Vdc                      |
| Collector–Base Voltage  | $V_{CB}$       | 60                | 80                | 100               | Vdc                      |
| Emitter–Base Voltage  | $V_{EB}$       | 5.0               |                   |                   | Vdc                      |
| Collector Current – Continuous<br>– Peak  | $I_C$          | 2.0<br>4.0        |                   |                   | Adc                      |
| Base Current  | $I_B$          | 50                |                   |                   | mAdc                     |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 50<br>0.4         |                   |                   | W<br>W/ $^\circ\text{C}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 2.0<br>0.016      |                   |                   | W<br>W/ $^\circ\text{C}$ |
| Unclamped Inductive Load Energy – Figure 13   | E              | 25                |                   |                   | mJ                       |
| Operating and Storage Junction  | $T_J, T_{stg}$ | –65 to +150       |                   |                   | $^\circ\text{C}$         |

## THERMAL CHARACTERISTICS

| Characteristics                         | Symbol          | Max  | Unit                      |
|---|-----------------|------|---------------------------|
| Thermal Resistance, Junction–to–Case    | $R_{\theta JC}$ | 2.5  | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction–to–Ambient | $R_{\theta JA}$ | 62.5 | $^\circ\text{C}/\text{W}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

## OFF CHARACTERISTICS

|   |  |                |                 |                   |      |
|---|--|----------------|-----------------|-------------------|------|
| Collector–Emitter Sustaining Voltage (Note 1)<br>( $I_C = 30 \text{ mAdc}, I_B = 0$ )   | TIP110, TIP115<br>TIP111, TIP116<br>TIP112, TIP117 | $V_{CEO(sus)}$ | 60<br>80<br>100 | –<br>–<br>–       | Vdc  |
| Collector Cutoff Current<br>( $V_{CE} = 30 \text{ Vdc}, I_B = 0$ )<br>( $V_{CE} = 40 \text{ Vdc}, I_B = 0$ )<br>( $V_{CE} = 50 \text{ Vdc}, I_B = 0$ )  | TIP110, TIP115<br>TIP111, TIP116<br>TIP112, TIP117 | $I_{CEO}$      | –<br>–<br>–     | 2.0<br>2.0<br>2.0 | mAdc |
| Collector Cutoff Current<br>( $V_{CB} = 60 \text{ Vdc}, I_E = 0$ )<br>( $V_{CB} = 80 \text{ Vdc}, I_E = 0$ )<br>( $V_{CB} = 100 \text{ Vdc}, I_E = 0$ ) | TIP110, TIP115<br>TIP111, TIP116<br>TIP112, TIP117 | $I_{CBO}$      | –<br>–<br>–     | 1.0<br>1.0<br>1.0 | mAdc |
| Emitter Cutoff Current<br>( $V_{BE} = 5.0 \text{ Vdc}, I_C = 0$ )   |  | $I_{EBO}$      | –               | 2.0               | mAdc |

## ON CHARACTERISTICS (Note 1)

|   |  |               |             |        |     |
|---|--|---------------|-------------|--------|-----|
| DC Current Gain<br>( $I_C = 1.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$ )<br>( $I_C = 2.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$ ) |  | $h_{FE}$      | 1000<br>500 | –<br>– | –   |
| Collector–Emitter Saturation Voltage ( $I_C = 2.0 \text{ Adc}, I_B = 8.0 \text{ mAdc}$ )  |  | $V_{CE(sat)}$ | –           | 2.5    | Vdc |
| Base–Emitter On Voltage ( $I_C = 2.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$ )   |  | $V_{BE(on)}$  | –           | 2.8    | Vdc |

## DYNAMIC CHARACTERISTICS

|  |  |          |        |            |    |
|--|--|----------|--------|------------|----|
| Small–Signal Current Gain ( $I_C = 0.75 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ ) |  | $h_{fe}$ | 25     | –          | –  |
| Output Capacitance<br>( $V_{CB} = 10 \text{ Vdc}, I_E = 0, f = 0.1 \text{ MHz}$ )                    | TIP115, TIP116, TIP117<br>TIP110, TIP111, TIP112 | $C_{ob}$ | –<br>– | 200<br>100 | pF |

1. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

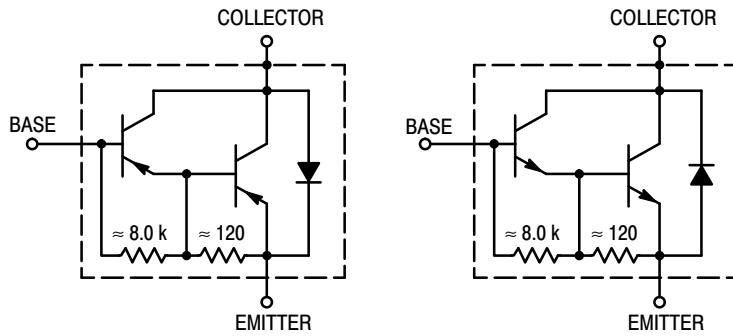


Figure 1. Darlington Circuit Schematic

## ORDERING INFORMATION

| Device  | Package             | Shipping        |
|---------|---------------------|-----------------|
| TIP110  | TO-220              | 50 Units / Rail |
| TIP110G | TO-220<br>(Pb-Free) | 50 Units / Rail |
| TIP111  | TO-220              | 50 Units / Rail |
| TIP111G | TO-220<br>(Pb-Free) | 50 Units / Rail |
| TIP112  | TO-220              | 50 Units / Rail |
| TIP112G | TO-220<br>(Pb-Free) | 50 Units / Rail |
| TIP115  | TO-220              | 50 Units / Rail |
| TIP115G | TO-220<br>(Pb-Free) | 50 Units / Rail |
| TIP116  | TO-220              | 50 Units / Rail |
| TIP116G | TO-220<br>(Pb-Free) | 50 Units / Rail |
| TIP117  | TO-220              | 50 Units / Rail |
| TIP117G | TO-220<br>(Pb-Free) | 50 Units / Rail |



Figure 2. Power Derating

# TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)



Figure 3. Switching Times Test Circuit

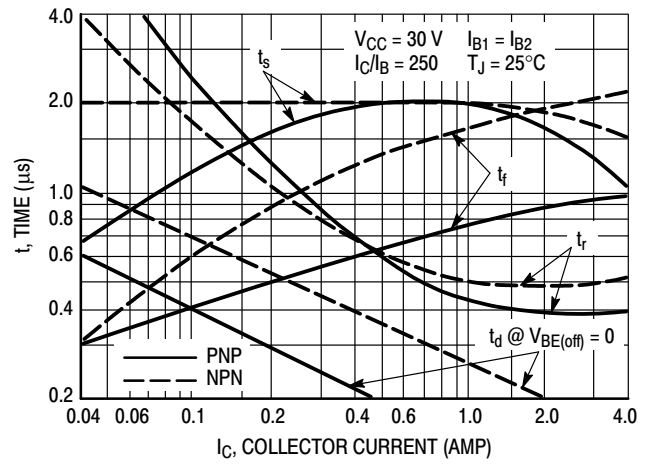


Figure 4. Switching Times



Figure 5. Thermal Response

# TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

## ACTIVE-REGION SAFE-OPERATING AREA



Figure 6. TIP115, 116, 117



Figure 7. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



Figure 8. Capacitance

TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

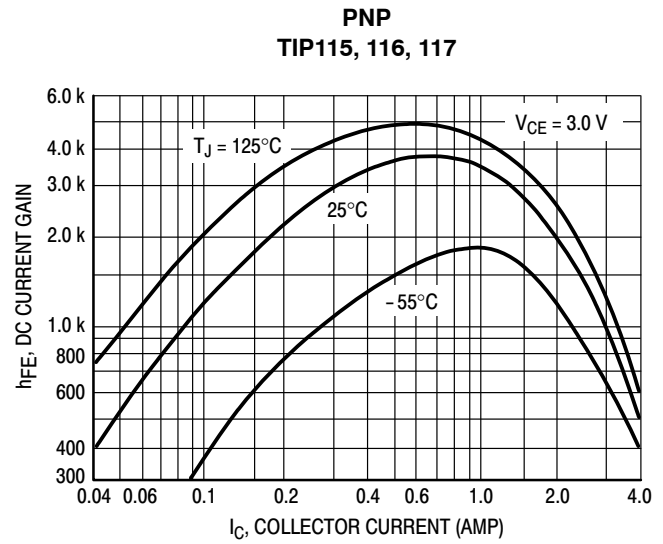
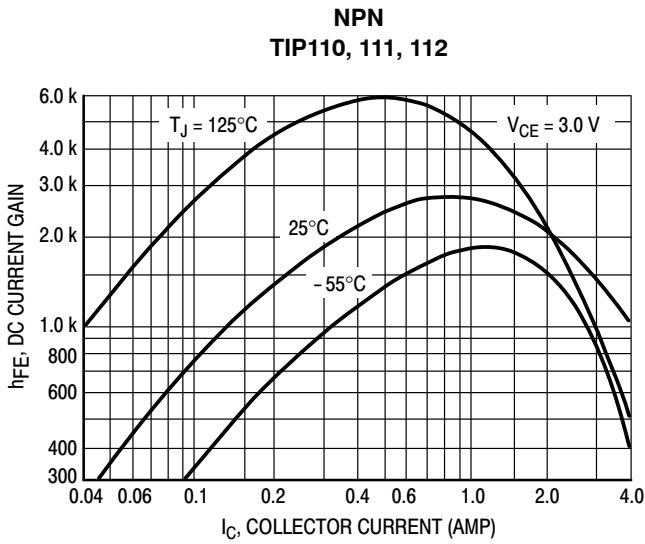


Figure 9. DC Current Gain

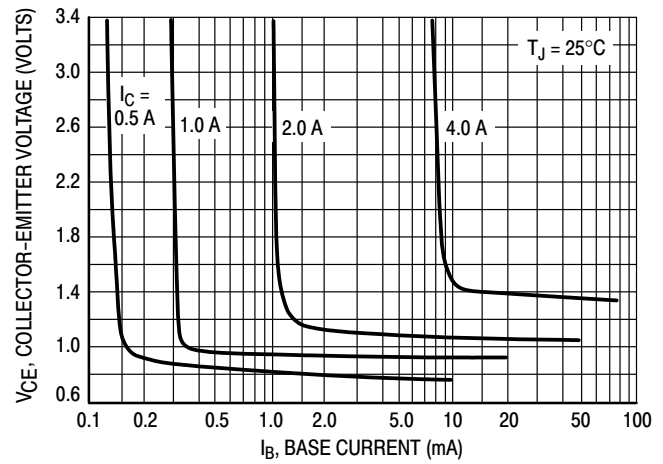
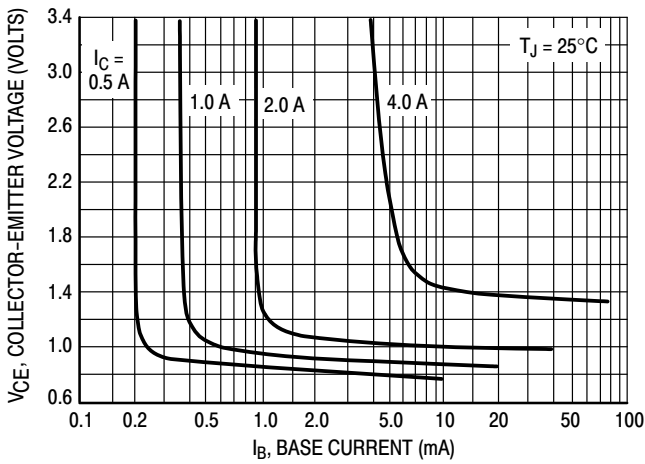


Figure 10. Collector Saturation Region

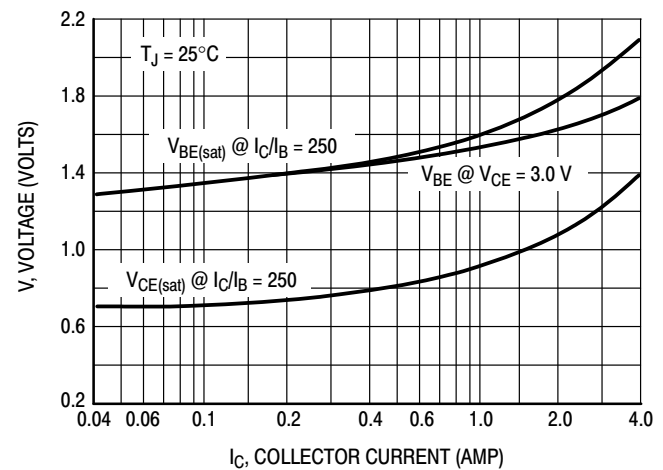
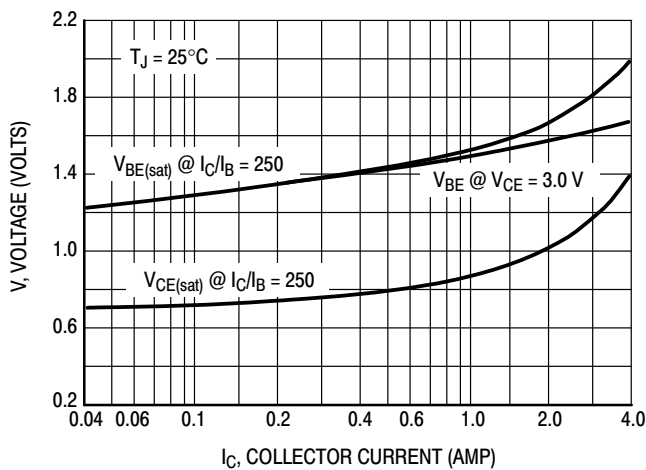


Figure 11. "On" Voltages

TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

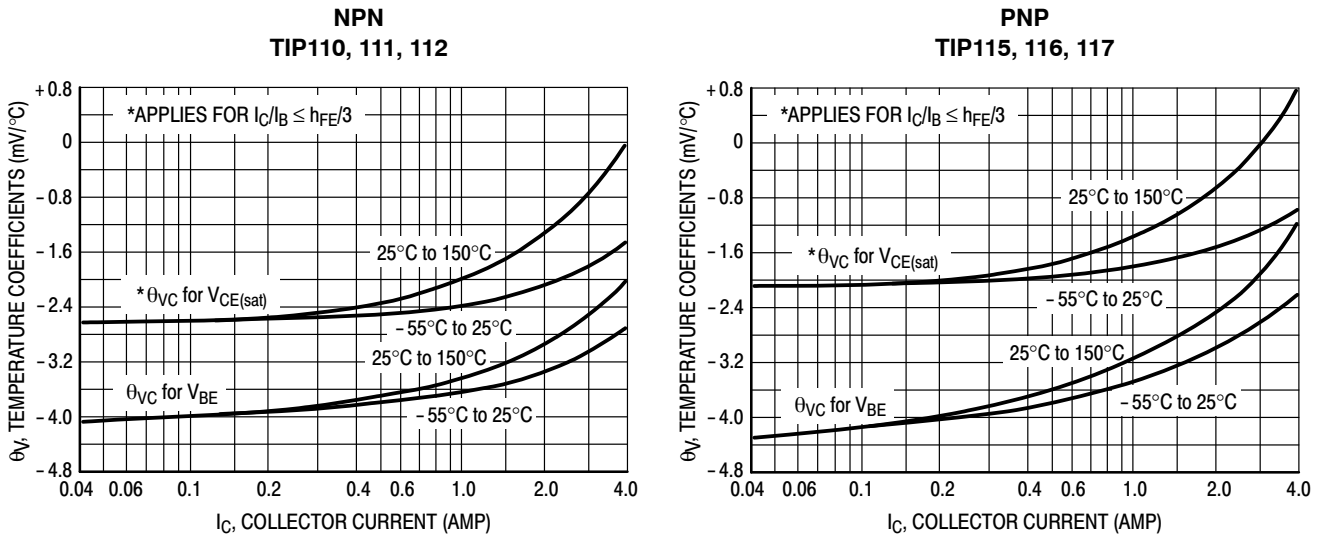


Figure 12. Temperature Coefficients

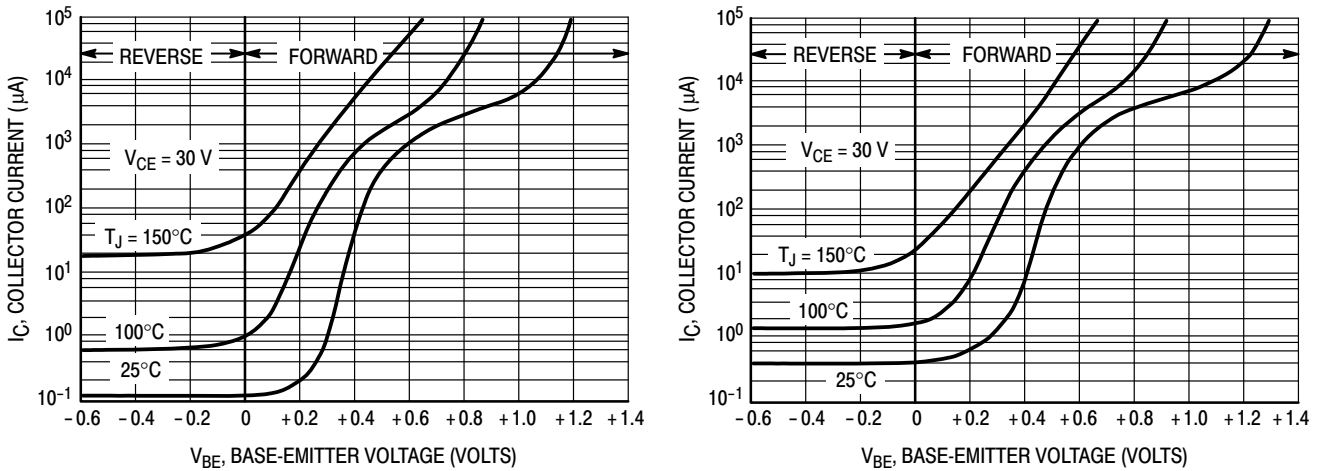
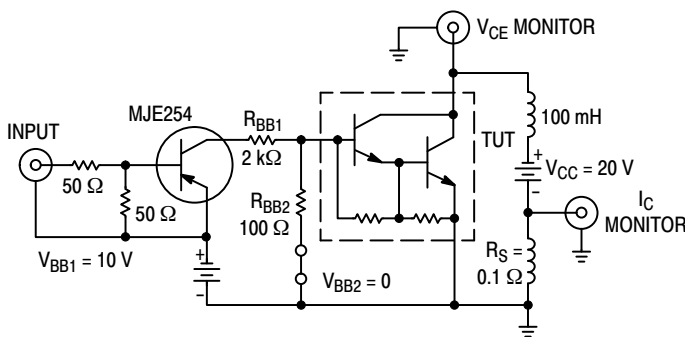
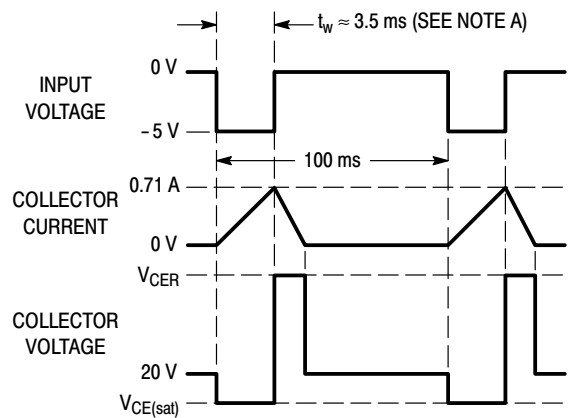


Figure 13. Collector Cut-Off Region

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



Note A: Input pulse width is increased until  $I_{CM} = 0.71$  A, NPN test shown; for PNP test reverse all polarity and use MJE224 driver.

Figure 14. Inductive Switching

# TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

## PACKAGE DIMENSIONS

### TO-220 CASE 221A-09 ISSUE AG



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN    | MAX   | MIN         | MAX   |
| A   | 0.570  | 0.620 | 14.48       | 15.75 |
| B   | 0.380  | 0.405 | 9.66        | 10.28 |
| C   | 0.160  | 0.190 | 4.07        | 4.82  |
| D   | 0.025  | 0.036 | 0.64        | 0.91  |
| F   | 0.142  | 0.161 | 3.61        | 4.09  |
| G   | 0.095  | 0.105 | 2.42        | 2.66  |
| H   | 0.110  | 0.161 | 2.80        | 4.10  |
| J   | 0.014  | 0.025 | 0.36        | 0.64  |
| K   | 0.500  | 0.562 | 12.70       | 14.27 |
| L   | 0.045  | 0.060 | 1.15        | 1.52  |
| N   | 0.190  | 0.210 | 4.83        | 5.33  |
| Q   | 0.100  | 0.120 | 2.54        | 3.04  |
| R   | 0.080  | 0.110 | 2.04        | 2.79  |
| S   | 0.045  | 0.055 | 1.15        | 1.39  |
| T   | 0.235  | 0.255 | 5.97        | 6.47  |
| U   | 0.000  | 0.050 | 0.00        | 1.27  |
| V   | 0.045  | ---   | 1.15        | ---   |
| Z   | ---    | 0.080 | ---         | 2.04  |

#### STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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Тел: +7 (812) 336 43 04 (многоканальный)

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