

# ISL29023

## Integrated Digital Light Sensor with Interrupt

FN6691  
Rev 4.00  
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The ISL29023 is an integrated ambient and infrared light to digital converter with I<sup>2</sup>C (SMBus Compatible) Interface. Its advanced self-calibrated photodiode array emulates human eye response with excellent IR rejection. The on-chip ADC is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. The lux range select feature allows users to program the lux range for optimized counts/lux.

For ambient light sensing, an internal 16-bit ADC has been designed based upon the charge-balancing technique. The ADC conversion time is nominally 90ms and is user adjustable from 11μs to 90ms, depending on oscillator frequency and ADC resolution. In normal operation, typical current consumption is 70μA. In order to further minimize power consumption, two power-down modes have been provided. If polling is chosen over continuous measurement of light, the auto-power-down function shuts down the whole chip after each ADC conversion for the measurement. The other power-down mode is controlled by software via the I<sup>2</sup>C interface. The power consumption can be reduced to less than 0.3μA when powered down.

The ISL29023 supports a software and hardware interrupt that remains asserted until the host clears it through I<sup>2</sup>C interface. Function of ADC conversion continues without stopping after interrupt is asserted.

Designed to operate on supplies from 2.25V to 3.63V with an I<sup>2</sup>C supply from 1.7V to 3.63V, the ISL29023 is specified for operation over the -40°C to +85°C ambient temperature range.

## Applications

- Mobile devices: smart phone, PDA, GPS
- Computing devices: Notebook PC, Webpad
- Consumer devices: LCD-TV, digital picture frame, digital camera
- Industrial and medical light sensing

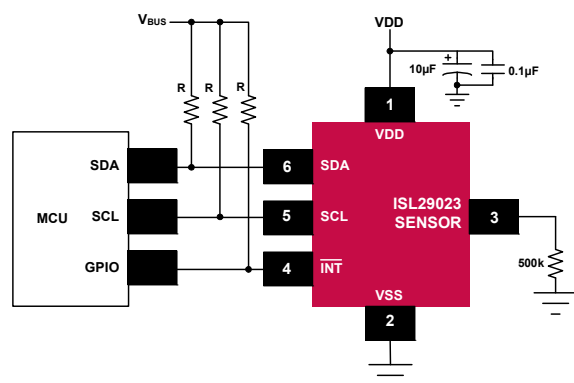


FIGURE 1. ISL29023 TYPICAL APPLICATION DIAGRAM

## Features

- Resolution . . . . .16-bits ADC
- Integrated noise reduction . . . . . 50/60Hz
- Light sensor close to human eye response
- Excellent light sensor IR and UV rejection
- Range selection via I<sup>2</sup>C
  - Range1 = 0.015 to 1,000 Lux
  - Range2 = 0.06 to 4,000 Lux
  - Range3 = 0.24 to 16,000 Lux
  - Range4 = 0.96 to 64,000 Lux
- Shutdown modes . . . . . Software and Automatic
- Supply current (Max) . . . . . 85μA
- Shutdown current (Max) . . . . . 0.3μA
- Control interface . . . . . I<sup>2</sup>C and SMB Compatible
- I<sup>2</sup>C power supply . . . . . 1.7V to 3.63V
- Sensor power supply . . . . . 2.25V to 3.63V
- Operating temperature range. . . . . -40°C to +85°C
- Small form factor package . . . . . 6 Ld 2.0x2.1x0.7 ODFN

## Related Literature

- [AN1534](#) "VDD Power-Up and Power Supply Considerations for Intersil Ambient Light Sensors"
- [AN1591](#) "Evaluation Hardware/Software Manual for ALS and Proximity Sensor"
- [AN1757](#) "I<sup>2</sup>C Fundamentals"
- [AN1782](#) "Ambient Light Sensor (ISL29023) Opto-Mechanical Reference Design"

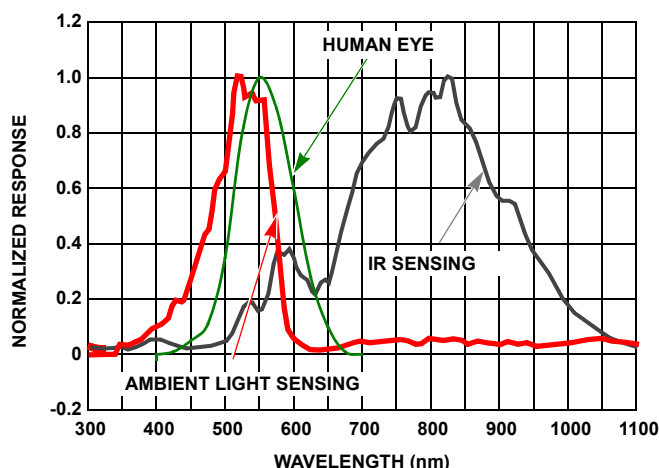
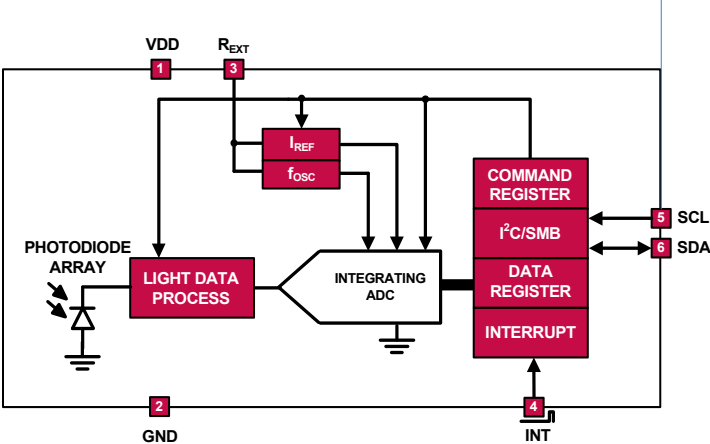


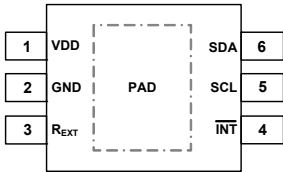
FIGURE 2. NORMALIZED SPECTRAL RESPONSE FOR AMBIENT LIGHT SENSING AND IR SENSING

Block Diagram



Pin Configuration

ISL29023  
(6 LD ODFN)  
TOP VIEW



\*EXPOSED PAD CAN BE CONNECTED TO GND OR ELECTRICALLY ISOLATED

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VDD	Positive supply; connect this pin to a 2.25V to 3.63V supply
2	GND	Ground pin
3	R <sub>EXT</sub>	External resistor pin for ADC reference; connect this pin to ground through a (nominal) 499kΩ resistor.
4	INT	Interrupt pin; low for interrupt alarming. INT pin is open drain. INT remains asserted until the interrupt flag status bit is reset.
5	SCL	I <sup>2</sup> C serial clock. This line can be pulled from 1.7V to above V <sub>DD</sub> , 3.63V max.
6	SDA	I <sup>2</sup> C serial data. This line can be pulled from 1.7V to above V <sub>DD</sub> , 3.63V max.
	PAD	Exposed pad connected to ground or electrically isolated

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL29023IROZ-T7	-40 to +85	6 Ld ODFN	L6.2x2.1
ISL29023IROZ-EVALZ	Evaluation Board (Pb-free)		

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL29023](#). For more information on MSL please see tech brief [TB477](#).

## Absolute Maximum Ratings

V <sub>DD</sub> to GND	+4.0V
I <sup>2</sup> C Bus (SCL, SDA) and $\overline{\text{INT}}$ Pin Voltage	-0.2V to 4.0V
I <sup>2</sup> C Bus (SCL, SDA) and $\overline{\text{INT}}$ Pin Current	<10mA
R <sub>EXT</sub> Pin Voltage	-0.2V to V <sub>DD</sub> +0.5V
ESD Ratings	
Human Body Model (HBM)	2kV
Charged Device Model (CDM)	1kV

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)
6 Ld ODFN Package (Note 4)	88
Maximum Junction Temperature (T <sub>JMAX</sub> )	+90°C
Storage Temperature Range	-40°C to +100°C
Operating Temperature	-40°C to +85°C
Pb-Free Reflow Profile (*)	see <a href="#">TB477</a>
*Peak temperature during solder reflow +235°C max	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).

## Electrical Specifications

V<sub>DD</sub> = 3V, T<sub>A</sub> = +25°C, R<sub>EXT</sub> = 499k $\Omega$  1% tolerance, 16-bit ADC operation, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V <sub>DD</sub>	Power Supply Range		2.25		3.63	V
I <sub>DD</sub>	Supply Current			70	85	$\mu$ A
I <sub>DD1</sub>	Supply Current when Powered Down	Software disabled or auto power-down		0.01	0.3	$\mu$ A
V <sub>I<sup>2</sup>C</sub>	Supply Voltage Range for I <sup>2</sup> C Interface		1.7		3.63	V
f <sub>OSC</sub>	Internal Oscillator Frequency		675	750	825	kHz
t <sub>int</sub>	ADC Integration/Conversion Time	16-bit ADC data		90		ms
F <sub>I<sup>2</sup>C</sub>	I <sup>2</sup> C Clock Rate Range			1 to 400		kHz
DATA_0	Count Output When Dark	E = 0 lux, Range 1 (1k lux)		1	5	Counts
DATA_F	Full Scale ADC Code				65535	Counts
DDATA DATA	Count Output Variation Over Three Light Sources: Fluorescent, Incandescent and Sunlight	Ambient light sensing		$\pm 10$		%
DATA_1	Light Count Output With LSB of 0.015 lux/count	E = 300 lux, Fluorescent light (Note 5), ALS Range 1 (1k lux)	15000	20000	25000	Counts
DATA_2	Light Count Output With LSB of 0.06 lux/count	E = 300 lux, Fluorescent light (Note 5), ALS Range 2 (4k lux)		5000		Counts
DATA_3	Light Count Output With LSB of 0.24 lux/count	E = 300 lux, Fluorescent light (Note 5), ALS Range 3 (16k lux)		1250		Counts
DATA_4	Light Count Output With LSB of 0.96 lux/count	E = 300 lux, Fluorescent light (Note 5), ALS Range 4 (64k lux)		312		Counts
DATA_IR1	Infrared Count Output	E = 210 lux, Sunlight (Note 6), IR sensing, Range 1	15000	20000	25000	
DATA_IR2	Infrared Count Output	E = 210 lux, Sunlight (Note 6), IR sensing, Range 2		5000		
DATA_IR3	Infrared Count Output	E = 210 lux, Sunlight (Note 6), IR sensing, Range 3		1250		
DATA_IR4	Infrared Count Output	E = 210 lux, Sunlight (Note 6), IR sensing, Range 4		312		
V <sub>REF</sub>	Voltage of R <sub>EXT</sub> Pin			0.52		V
V <sub>IL</sub>	SCL and SDA Input Low Voltage				0.55	V
V <sub>IH</sub>	SCL and SDA Input High Voltage		1.25			V
I <sub>SDA</sub>	SDA Current Sinking Capability		4	5		mA
I <sub>INT</sub>	$\overline{\text{INT}}$ Current Sinking Capability		4	5		mA

### NOTES:

- 550nm green LED is used in production test. The 550nm LED irradiance is calibrated to produce the same DATA count against an illuminance level of 300 lux fluorescent light.
- 850nm IR LED is used in production test. The 850nm LED irradiance is calibrated to produce the same DATA\_IR count against an illuminance level of 210 lux sunlight at sea level.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

## Typical Performance Curves

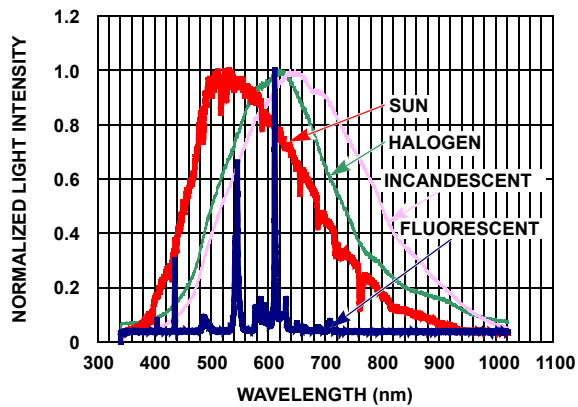


FIGURE 3. NORMALIZED SPECTRAL RESPONSE OF LIGHT SOURCES

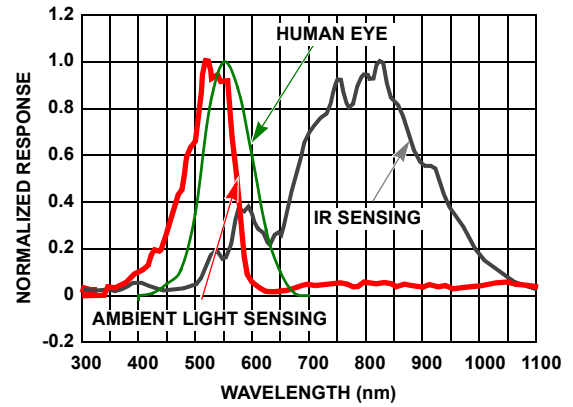


FIGURE 4. NORMALIZED SPECTRAL RESPONSE FOR AMBIENT LIGHT SENSING AND IR SENSING

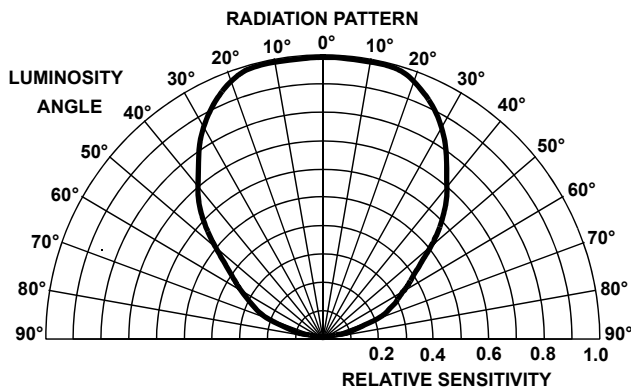


FIGURE 5. RADIATION PATTERN

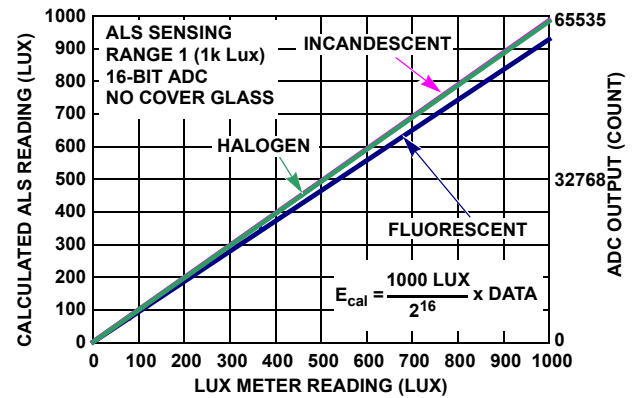


FIGURE 6. SENSITIVITY TO THREE LIGHT SOURCES

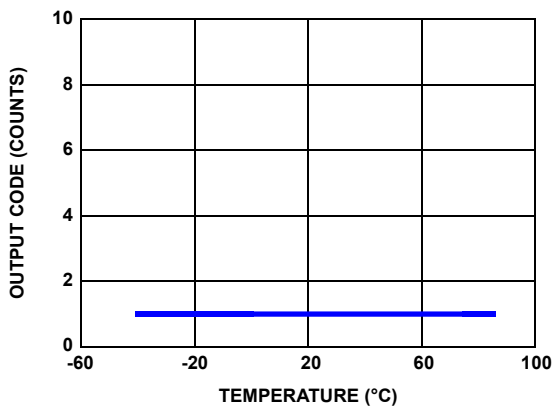


FIGURE 7. OUTPUT CODE FOR 0 LUX vs TEMPERATURE

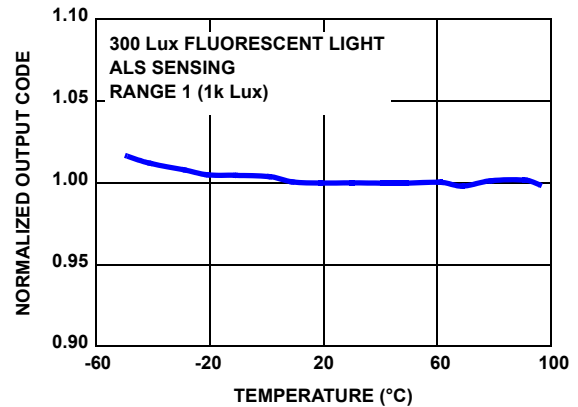


FIGURE 8. OUTPUT CODE vs TEMPERATURE

## Typical Performance Curves (Continued)

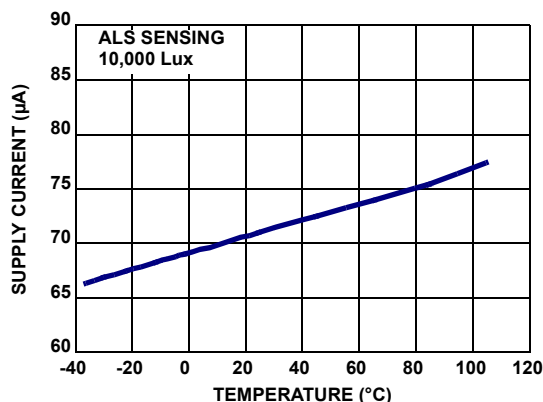


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE IN ALS SENSING

## Principles of Operation

### Photodiodes and ADC

The ISL29023 contains two photodiode arrays, which convert light into current. The spectral response for ambient light sensing and IR sensing is shown in Figure 4, on page 4. After light is converted to current during the light signal process, the current output is converted to digital by a built-in 16-bit Analog-to-Digital Converter (ADC). An I<sup>2</sup>C command reads the ambient light or IR intensity in counts.

The converter is a charge-balancing integrating type 16-bit ADC. The chosen method for conversion is best for converting small current signals in the presence of an AC periodic noise. A 100ms integration time, for instance, highly rejects 50Hz and 60Hz power line noise simultaneously.

The built-in ADC offers user flexibility in integration time or conversion time. There are two timing modes: Internal Timing Mode and External Timing Mode. In Internal Timing Mode, integration time is determined by an internal oscillator ( $f_{OSC}$ ), and the n-bit ( $n = 4, 8, 12, 16$ ) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive I<sup>2</sup>C External Timing Mode commands. A good balancing act of integration time and resolution (depending on the application) is required for optimal results.

The ADC has I<sup>2</sup>C programmable range select to dynamically accommodate various lighting conditions. For very dim conditions, the ADC can be configured at its lowest range (Range 1) in the ambient light sensing.

### Low-Power Operation

The ISL29023 initial operation is at the power-down mode after a supply voltage is provided. The data registers contain the default value of 0. When the ISL29023 receives an I<sup>2</sup>C command to do a one-time measurement from an I<sup>2</sup>C master, it will start the ADC conversion with light sensing. It will go into power-down mode automatically after one conversion is finished and keep the conversion data available for the master to fetch anytime afterwards. The ISL29023 will continuously do ADC conversion with light sensing if it receives an I<sup>2</sup>C command of continuous measurement. It will continuously update the data registers with

the latest conversion data. It will go into power-down mode after it receives the I<sup>2</sup>C command.

### Ambient Light and IR Sensing

There are four operational modes in ISL29023: Programmable ALS once with auto power-down, programmable IR sensing once with auto power-down, programmable continuous ALS sensing and programmable continuous IR sensing. These four modes can be programmed in series to fulfill the application needs. The detailed program configuration is listed in "Command-I Register (Address: 0x00)" on page 8.

When the part is programmed for ambient light sensing, the ambient light with wavelength within the "Ambient Light Sensing" spectral response curve in Figure 4 is converted into current. With ADC, the current is converted to an unsigned n-bit (up to 16 bits) digital output.

When the part is programmed for infrared (IR) sensing, the IR light with wavelength within the "IR Sensing" spectral response curve in Figure 4 is converted into current. With ADC, the current is converted to an unsigned n-bit (up to 16-bits) digital output.

### Interrupt Function

The active low interrupt pin is an open drain pull-down configuration. The interrupt pin serves as an alarm or monitoring function to determine whether the ambient light level exceeds the upper threshold or goes below the lower threshold. It should be noted that the function of ADC conversion continues without stopping after interrupt is asserted. If the user needs to read the ADC count that triggers the interrupt, the reading should be done before the data registers are refreshed by the following conversions. The user can also configure the persistency of the interrupt pin. This reduces the possibility of false triggers, such as noise or sudden spikes in ambient light conditions. An unexpected camera flash, for example, can be ignored by setting the persistency to 8 integration cycles.

## Serial Interface

The ISL29023 supports the Inter-Integrated Circuit (I<sup>2</sup>C) bus data transmission protocol. The I<sup>2</sup>C bus is a two-wire serial bidirectional interface consisting of SCL (clock) and SDA (data). Both the wires are connected to the device supply via pull-up resistors. The I<sup>2</sup>C protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The transmitting device pulls down the SDA line to transmit a “0” and releases it to transmit a “1”. The master always initiates the data transfer, only when the bus is not busy, and provides the clock for both transmit and receive operations. The ISL29023 operates as a slave device in all applications. The serial communication over the I<sup>2</sup>C interface is conducted by sending the most significant bit (MSB) of each byte of data first.

### Start Condition

During data transfer, the SDA line must remain stable while the SCL line is HIGH. All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH (see Figure 12, on page 7). The ISL29023 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 12). A START condition is ignored during the power-up sequence.

### Stop Condition

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH (see Figure 12). A STOP condition at the end of a read/write operation places the device in its standby mode. If a stop is issued in the middle of a Data byte, or before one full Data byte + ACK is sent, then the serial communication of ISL29023 resets itself without performing the read/write. The contents of the array are not affected.

### Acknowledge

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting 8-bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 12). The ISL29023 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL29023 also responds with an ACK after receiving a Data byte of a write operation. The master must respond with an ACK after receiving a Data byte of a read operation.

### Device Addressing

Following a START condition, the master must output a Device Address byte. The 7 MSBs of the Device Address byte are known as the device identifier. The device identifier bits of ISL29023 are internally hard-wired as “1000100”. The LSB of the Device Address byte is defined as a read or write (R/ $\overline{W}$ ) bit. When this R/ $\overline{W}$  bit is a “1”, a read operation is selected and when “0”, a write operation is selected (see Figure 10). The master generates a START condition followed by Device Address byte 1000100x (x as R/ $\overline{W}$ ) and the

ISL29023 compares it with the internal device identifier. Upon a correct comparison, the device outputs an acknowledge (LOW) on the SDA line (See Figure 12).

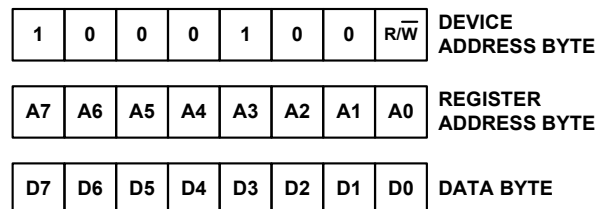


FIGURE 10. DEVICE ADDRESS, REGISTER ADDRESS, and DATA BYTE

## Write Operation

### BYTE WRITE

In a byte write operation, ISL29023 requires the Device Address byte, Register Address byte, and the Data byte. The master starts the communication with a START condition. Upon receipt of the Device Address byte, Register Address byte, and the Data byte, the ISL29023 responds with an acknowledge (ACK). Following the ISL29023 data acknowledge response, the master terminates the transfer by generating a STOP condition. ISL29023 then begins an internal write cycle of the data to the volatile memory. During the internal write cycle, the device inputs are disabled and the SDA line is in a high impedance state, so the device will not respond to any requests from the master (see Figure 11).

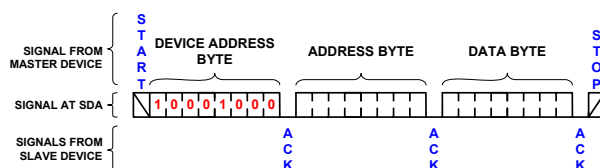


FIGURE 11. BYTE WRITE SEQUENCE

### BURST WRITE

The ISL29023 has a burst write operation, which allows the master to write multiple consecutive bytes from a specific address location. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first Data byte is transferred, the master can write to the whole register array. After the receipt of each byte, the ISL29023 responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the register address list, it “rolls over” and goes back to the first Register Address.



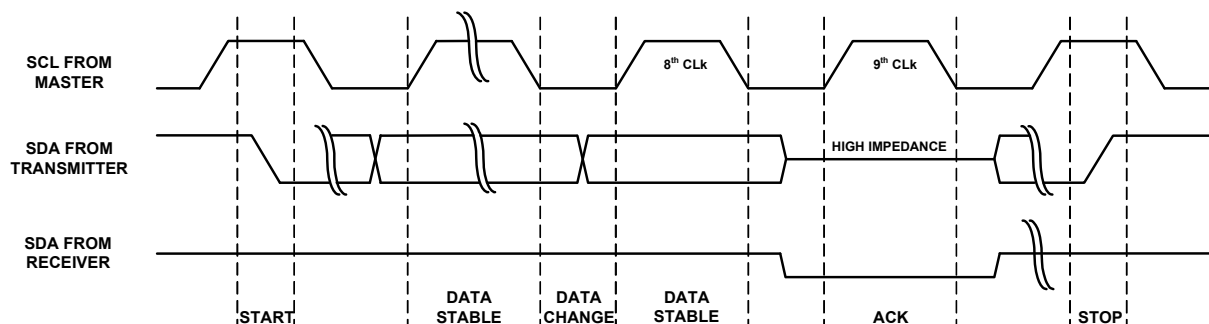


FIGURE 12. START, DATA STABLE, ACKNOWLEDGE, AND STOP CONDITION

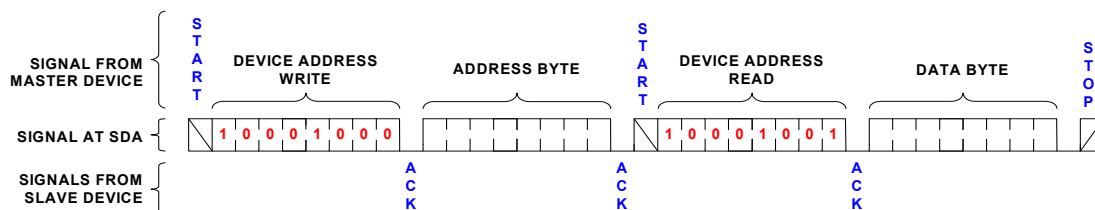


FIGURE 13. BYTE ADDRESS READ SEQUENCE

## Read Operation

ISL29023 has two basic read operations: Byte Read and Burst Read.

### BYTE READ

Byte read operations allow the master to access any register location in the ISL29023. The Byte read operation is a two step process. The master issues the START condition and the Device Address byte with the R/W bit set to "0", receives an acknowledge, then issues the Register Address byte. After acknowledging receipt of the register address byte, the master immediately issues another START condition and the Device Address byte with the R/W bit set to "1". This is followed by an acknowledge from the device and then by the 8-bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition (See Figure 13).

### BURST READ

Burst read operation is identical to the Byte Read operation. After the first Data byte is transmitted, the master now responds

with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge but issuing a STOP condition (See Figure 14).

For more information about the I<sup>2</sup>C standard, please consult the Phillips™ I<sup>2</sup>C specification documents.

## Power On Reset

The Power-On Reset (POR) circuitry protects the internal logic against powering up in the incorrect state. The ISL29023 will power-up into Standby mode after VDD exceeds the POR trigger level and will power-down into Reset mode when VDD drops below the POR trigger level. This bidirectional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

The POR is an important feature because it prevents the ISL29023 from starting to operate with insufficient voltage, prior to stabilization of the internal bandgap. The ISL29023 prevents communication to its registers and greatly reduces the likelihood of data corruption on power-up.

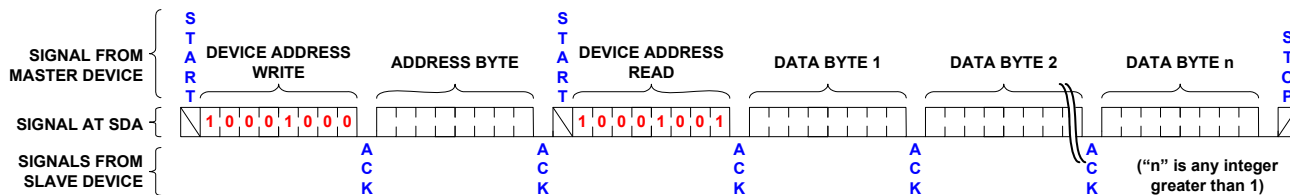


FIGURE 14. BURST READ SEQUENCE

TABLE 1. REGISTER MAP

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0	HEX
COMMAND-I	0	0x00	OP2	OP1	OP0	RESERVED		FLAG	PRST1	PRST0	00h
COMMAND-II	1	0x01	RESERVED				RES1	RES0	RANGE1	RANGE0	00h
DATA <sub>LSB</sub>	2	0x02	D7	D6	D5	D4	D3	D2	D1	D0	00h
DATA <sub>MSB</sub>	3	0x03	D15	D14	D13	D12	D11	D10	D9	D8	00h
INT_LT_LSB	4	0x04	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	00h
INT_LT_MSB	5	0x05	TL15	TL14	TL13	TL12	TL11	TL10	TL9	TL8	00h
INT_HT_LSB	6	0x06	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	FFh
INT_HT_MSB	7	0x07	TH15	TH14	TH13	TH12	TH11	TH10	TH9	TH8	FFh
TEST	8	0x08	0	0	0	0	0	0	0	0	00h

## Register Description

Following are detailed descriptions of the control registers related to the operation of the ISL29023 ambient light sensor device. These registers are accessed by the I<sup>2</sup>C serial interface. For details on the I<sup>2</sup>C interface, refer to “Serial Interface” on page 6.

All the functionalities of the device are controlled by the registers. The ADC data can also be read. The following sections explain the details of each register bit. **All RESERVED bits must be set to zero, unless otherwise specified.**

## Decimal to Hexadecimal Conversion

To convert decimal value to hexadecimal value, divide the decimal number by 16, and write the remainder on the side as the least significant digit. This process is continued by dividing the quotient by 16 and writing the remainder until the quotient is 0. When performing the division, the remainders, which will represent the hexadecimal equivalent of the decimal number, are written beginning at the least significant digit (right) and each new digit is written to the next more significant digit (the left) of the previous digit. Consider the number 175 decimal.

TABLE 2. DECIMAL TO HEXADECIMAL

DIVISION	QUOTIENT	REMAINDER	HEX NUMBER
175/16	10 = A	15 = F	0xAF

## Command-I Register (Address: 0x00)

TABLE 3. COMMAND-I REGISTER ADDRESS

NAME	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
COMMANDI	0x00	OP2	OP1	OP0	0	0	FLAG	PRST1	PRST0	0x00

The Command-I register consists of control and status bits. In this register, there are two interrupt persist bits, one interrupt status bit, and three operation mode bits. The operation mode bits and the interrupt persist bits are independent of each other. The default register value is 0x00 at power on.

## INTERRUPT PERSIST BITS (B0 - B1)

The interrupt persist bits provides control over when interrupts occur. There are four different selections for this feature. A value of  $n$  (where  $n$  is 1, 4, 8, and 16) results in an interrupt only if the value remains outside the threshold window for  $n$  consecutive integration cycles. For example, if  $n$  is equal to 16 and the ADC resolution is set to 16-bits then the integration time is 100ms. An interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing the COMMAND register with the CLEAR bit set. Table 4 lists the possible interrupt persist bits.

TABLE 4. INTERRUPT PERSIST BITS

B1	B0	NUMBER OF INTEGRATION CYCLES (n)
0	0	1
0	1	4
1	0	8
1	1	16

## INTERRUPT FLAG BIT (B2)

The interrupt flag bit is a status bit for light intensity detection. The bit is set to logic HIGH when the light intensity crosses the interrupt thresholds window (register address 0x04 - 0x07), and set to logic LOW when its within the interrupt thresholds window. Once the interrupt is triggered, the  $\overline{\text{INT}}$  pin goes low and the interrupt status bit goes HIGH until the status bit is polled through the I<sup>2</sup>C read command. Both the  $\overline{\text{INT}}$  pin and the interrupt status bit are automatically cleared at the end of the 8-bit Device Register byte (0x00) transfer. Table 5 shows interrupt flag states.

TABLE 5. INTERRUPT FLAG BIT

BIT 2	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered



## OPERATION MODE BITS (B5 - B7)

ISL29023 has different operating modes. These modes are selected by setting B5 - B7 bits on register address 0x00. The device powers up on a disable mode. Table 6 lists the possible operating modes.

TABLE 6. OPERATING MODES BITS

B7	B6	B5	OPERATION
0	0	0	Power-down the device (Default)
0	0	1	The IC measures ALS only once every integration cycle. This is the lowest operating mode.
0	1	0	IR once
0	1	1	Reserved (DO NOT USE)
1	0	0	Reserved (DO NOT USE)
1	0	1	The IC measures ALS continuously
1	1	0	The IC measures IR continuous
1	1	1	Reserved (DO NOT USE)

## Command-II Register (Address: 0x01)

TABLE 7. COMMAND-II REGISTER BITS

NAME	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
COMMANDII	0x01	0	0	0	0	RES1	RES0	RANGE1	RANGE0	0x00

The Command-II register consists of two dynamic range bits, and two DAC resolution bits. The default register value is 0x00 at power-on.

## FULL SCALE RANGE (B1-B0)

The Full Scale Range (FSR) has four different selectable ranges. Each range has a maximum allowable lux value. Higher range values offer wider ALS lux value. Table 8 lists the possible values of FSR for the 499kΩ R<sub>EXT</sub> resistor.

TABLE 8. RANGE REGISTER BITS

B0	B1	k	RANGE(k)	FSR (LUX) @ ALS SENSING	FSR @ IR SENSING
0	0	1	Range1	1,000	65535
0	1	2	Range2	4,000	65535
1	0	3	Range3	16,000	65535
1	1	4	Range4	64,000	65535

## ADC RESOLUTION (B3 - B2)

B3 and B2 determine the ADC's resolution and the number of clock cycles per conversion. Changing the number of clock cycles does more than just change the resolution of the device; it also changes the integration time, which is the period the device's analog-to-digital (A/D) converter samples the photodiode current signal for a measurement. The ONLY 16-bit ADC resolution is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. Table 9 lists the possible ADC resolution.

TABLE 9. ADC RESOLUTION DATA WIDTH

B3	B2	NUMBER OF CLOCK CYCLES	n-BIT ADC
0	0	2 <sup>16</sup> = 65,536	16
0	1	2 <sup>12</sup> = 4,096	12
1	0	2 <sup>8</sup> = 256	8
1	1	2 <sup>4</sup> = 16	4

## Data Registers (Addresses: 0x02 and 0x03)

TABLE 10. ADC REGISTER BITS

NAME	Reg. Addr (Hex)	Register Bits								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
DATA <sub>LSB</sub>	0x02	D7	D6	D5	D4	D3	D2	D1	D0	0x00
DATA <sub>MSB</sub>	0x03	D15	D14	D13	D12	D11	D10	D9	D8	0x00

The ISL29023 has two 8-bit read-only registers to hold the upper and lower byte of the ADC value. The upper byte is accessed at address 0x03 and the lower byte is accessed at address 0x02. For 16-bit resolution, the data is from D0 to D15; for 12-bit resolution, the data is from D0 to D11; for 8-bit resolution, the data is from D0 to D7 and 4-bit resolution, the data is from D0 to D3. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power-on.

TABLE 11. ADC DATA REGISTERS

ADDRESS (hex)	CONTENTS
0x02	D0 is LSB for 4, 8, 12 or 16-bit resolution; D3 is MSB for 4-bit resolution; D7 is MSB for 8-bit resolution
0x03	D15 is MSB for 16-bit resolution; D11 is MSB for 12-bit resolution

## Lower Interrupt Threshold Registers (Address: 0x04 and 0x05)

TABLE 12. INTERRUPT REGISTER BITS

NAME	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
INT_LT_LSB	0x04	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00
INT_LT_MSB	0x05	TL15	TL14	TL13	TL12	TL11	TL10	TL9	TL8	0x00

The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the ALS value crosses below or is equal to the lower threshold, an interrupt is asserted on the interrupt pin and the interrupt flag. Registers INT\_LT\_LSB (0x04) and INT\_LT\_MSB (0x05) provide the low and high bytes, respectively, of the lower interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 0x00 upon power-up.

## Upper Interrupt Threshold Registers (Address: 0x06 and 0x07)

TABLE 13. INTERRUPT REGISTER BITS

NAME	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
		B7	B6	B5	B4	B3	B2	B1	B0	
INT_HT_LSB	0x06	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF
INT_HT_MSB	0x07	TH15	TH14	TH13	TH12	TH11	TH10	TH9	TH8	0xFF

The upper interrupt threshold registers are used to set the upper trigger point for interrupt generation. If the ALS value crosses above or is equal to the upper threshold, an interrupt is asserted on the interrupt pin and the interrupt flag. Registers INT\_HT\_LSB (0x06) and INT\_HT\_MSB (0x07) provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 0xFF on power-up.

### Test Register (08 hex)

Register 8 is a reserved register that holds 00h during normal operation.

## Applications Information

### Calculating Lux

The ISL29023's ADC output codes, DATA, are directly proportional to lux in the ambient light sensing.

$$E_{\text{cal}} = \alpha \times \text{DATA} \quad (\text{EQ. 1})$$

Here,  $E_{\text{cal}}$  is the calculated lux reading. The constant  $\alpha$  is determined by the Full Scale Range and the ADC's maximum output counts. The constant is independent of the light sources (fluorescent, incandescent and sunlight) because the light sources' IR component is removed during the light signal process. The constant can also be viewed as the sensitivity (the smallest lux measurement the device can measure).

$$\alpha = \frac{\text{Range}(k)}{\text{Count}_{\text{max}}} \quad (\text{EQ. 2})$$

Here,  $\text{Range}(k)$  is defined in Table 8.  $\text{Count}_{\text{max}}$  is the maximum output counts from the ADC.

The transfer function used for n-bits ADC becomes:

$$E_{\text{cal}} = \frac{\text{Range}(k)}{2^n} \times \text{DATA} \quad (\text{EQ. 3})$$

Here,  $n = 4, 8, 12$  or  $16$ . This is the number of ADC bits programmed in the command register.  $2^n$  represents the maximum number of counts possible from the ADC output. Data is the ADC output stored in the data registers (02 hex and 03 hex).

### Integration and Conversion Time

The ADC resolution and  $f_{\text{OSC}}$  determine the integration time,  $t_{\text{int}}$ .

$$t_{\text{int}} = 2^n \times \frac{1}{f_{\text{OSC}}} = 2^n \times \frac{R_{\text{EXT}}}{725\text{kHz} \times 499\text{k}\Omega} \quad (\text{EQ. 4})$$

where  $n$  is the number of bits of resolution and  $n = 4, 8, 12$  or  $16$ . Therefore,  $2^n$  is the number of clock cycles.  $n$  can be programmed at the command register 01(hex) bits 3 and 2.

TABLE 14. INTEGRATION TIME OF n-BIT ADC

$R_{\text{EXT}}$ (k $\Omega$ )	n = 16-BIT	n = 12-BIT	n = 8-BIT	n = 4-BIT
499**	90ms	5.6ms	352 $\mu$ s	22 $\mu$ s

\*\*Recommended  $R_{\text{EXT}}$  resistor value

### External Scaling Resistor $R_{\text{EXT}}$ for $f_{\text{OSC}}$ and Range

The ISL29023 uses an external resistor  $R_{\text{EXT}}$  to fix its internal oscillator frequency  $f_{\text{OSC}}$  and the light sensing range, Range.  $f_{\text{OSC}}$  and Range are inversely proportional to  $R_{\text{EXT}}$ . For user simplicity, the proportionality constant is referenced to 499k $\Omega$ :

$$\text{Range} = \frac{499\text{k}\Omega}{R_{\text{EXT}}} \times \text{Range}(k) \quad (\text{EQ. 5})$$

$$f_{\text{OSC}} = \frac{499\text{k}\Omega}{R_{\text{EXT}}} \times 725\text{kHz} \quad (\text{EQ. 6})$$

### ADC Output in IR Sensing

The ISL29023's ADC output codes, DATA, are directly proportional to the IR intensity received in the IR sensing.

$$\text{DATA}_{\text{IR}} = \beta \times E_{\text{IR}} \quad (\text{EQ. 7})$$

Here,  $E_{\text{IR}}$  is the received IR intensity. The constant  $\beta$  changes with the spectrum of background IR noise, such as sunlight and incandescent light. The  $\beta$  also changes with the ADC's range and resolution selections.

### $V_{\text{DD}}$ Power-up and Power Supply Considerations

Upon power-up, please ensure a  $V_{\text{DD}}$  slew rate of 0.5V/ms or greater. For more information, see application note [AN1534](#).

### Noise Rejection

Electrical AC power worldwide is distributed at either 50Hz or 60Hz. Artificial light sources vary in intensity at the AC power frequencies. The undesired interference frequencies are infused on the electrical signals. This variation is one of the main sources of noise for the light sensors. Integrating type ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. By setting the sensor's integration time to an integer multiple of periodic noise signal, the performance of an ambient light sensor can be improved greatly in the presence of noise. In order to reject the AC noise, the integration time of the sensor must be adjusted to match the AC noise cycle. For instance, a 60Hz AC unwanted signal's sum from 0ms to  $k \times 16.66\text{ms}$  ( $k = 1, 2, \dots, k_i$ ) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise.

## Suggested PCB Footprint

It is important that users check the “Surface Mount Assembly Guidelines for Optical Dual Flat Pack No Lead (ODFN) Package” before starting ODFN product board mounting, see [TB477](#).

## Board Mounting Consideration

For applications requiring the light measurement, the board mounting location should be reviewed. The device uses an Optical Dual Flat Pack No Lead (ODFN) package, which subjects the die to mild stresses when the printed circuit (PC) board is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location.

## Layout Considerations

The ISL29023 is relatively insensitive to layout. Like other I<sup>2</sup>C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I<sup>2</sup>C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors, 1μF and 0.1μF, placed close to the device. R<sub>EXT</sub> must be placed as closely to the pin as possible to eliminate the stray capacitance, which will greatly affect the performance of the sensor.

## Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260 °C. A standard reflow soldering profile with a +260 °C maximum is recommended.

## Temperature Coefficient

The limits stated for temperature coefficient (TC) are governed by the method of measurement. The “Box” method is usually used for specifying the temperature coefficient. The overwhelming standard for specifying the temperature drift of a reference is to evaluate the maximum voltage change over the specified temperature range. This yields ppm/°C, and is calculated using Equation 8:

$$TC = \frac{V_{HIGH} - V_{LOW}}{V_{NOMINAL} \times (T_{HIGH} - T_{LOW})} \times 10^6 \quad (EQ. 8)$$

where:

V<sub>HIGH</sub> is the maximum reference voltage over the temperature range.

V<sub>LOW</sub> is the minimum reference voltage over the temperature range.

V<sub>NOMINAL</sub> is the nominal reference voltage at +25 °C.

T<sub>HIGH</sub> - T<sub>LOW</sub> is the specified temperature range (°C)

## Digital Inputs and Termination

The ISL29023 digital inputs are guaranteed to CMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are 50Ω lines, then 50Ω termination resistors should be placed as close to the sensor inputs as possible, connected to the digital ground plane (if separate grounds are used).

## Typical Circuit

A typical application for the ISL29023 is shown in Figure 1. The ISL29023's I<sup>2</sup>C address is internally hard-wired as 1000100. The device can be tied onto a system's I<sup>2</sup>C bus together with other I<sup>2</sup>C compliant devices.

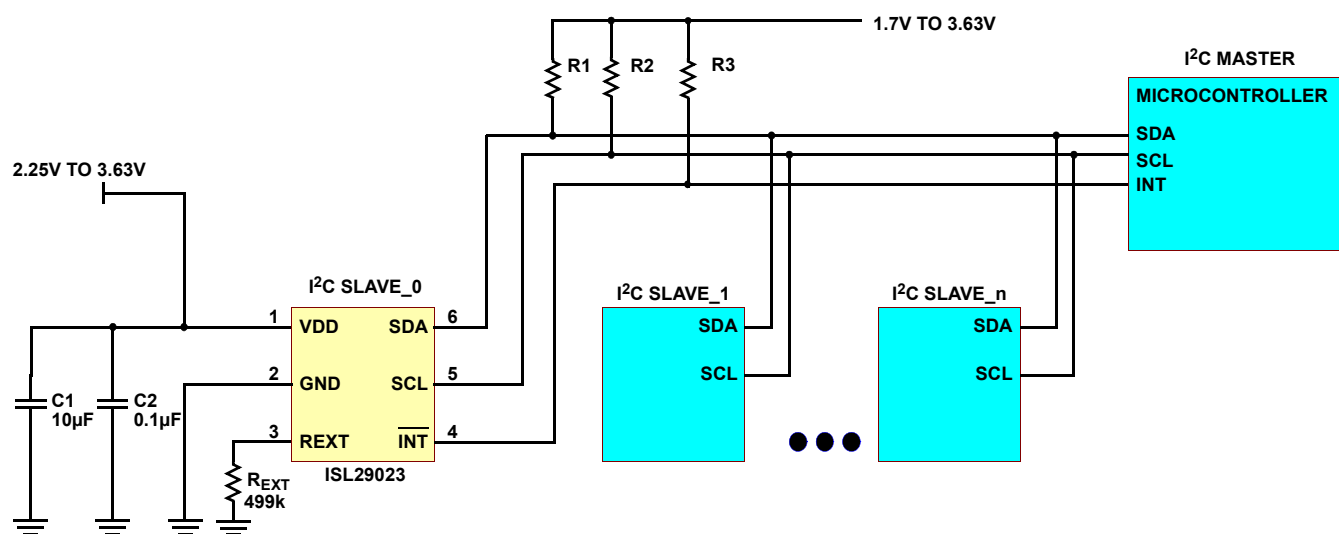


FIGURE 15. ISL29023 TYPICAL SYSTEM DIAGRAM

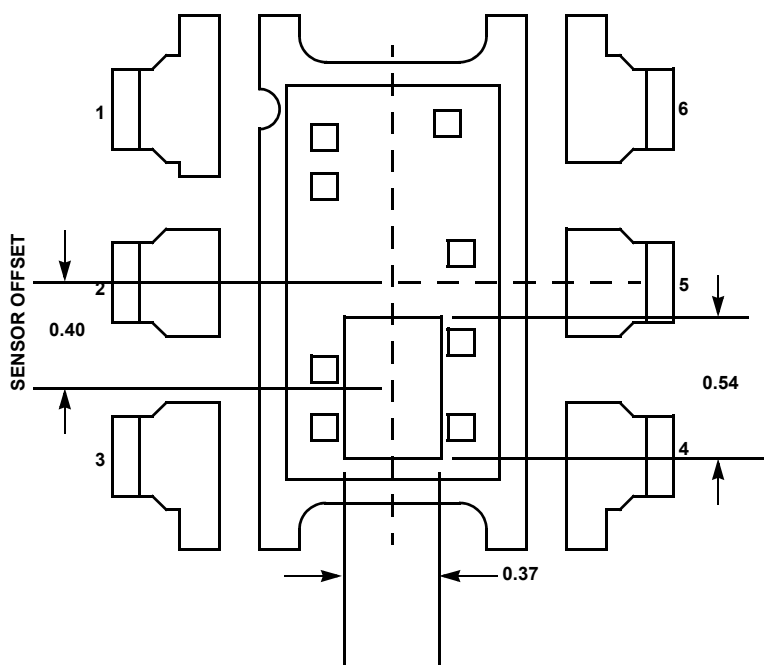


FIGURE 16. 6-LD ODFN SENSOR LOCATION OUTLINE

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 24, 2014	FN6691.4	Related Literature on page 1, "VDD Power-up and Power Supply Considerations" on page 10, and the explanation at Table 7 on page 9 were added. Updated "Temperature Coefficient" on page 11.
April 16, 2013	FN6691.3	ESD Specification Added
November 21, 2012	FN6691.2	Corrected part number in "Ordering Information" on page 2 from ISL29023IROZ-T7S2378 to ISL29023IROZ-T7 Updated TJA on page 3 from 90 to 88.
May 14, 2012	FN6691.1	I <sup>2</sup> C section and Register description explained in more detail.
March 3, 2009	FN6691.0	Initial Release

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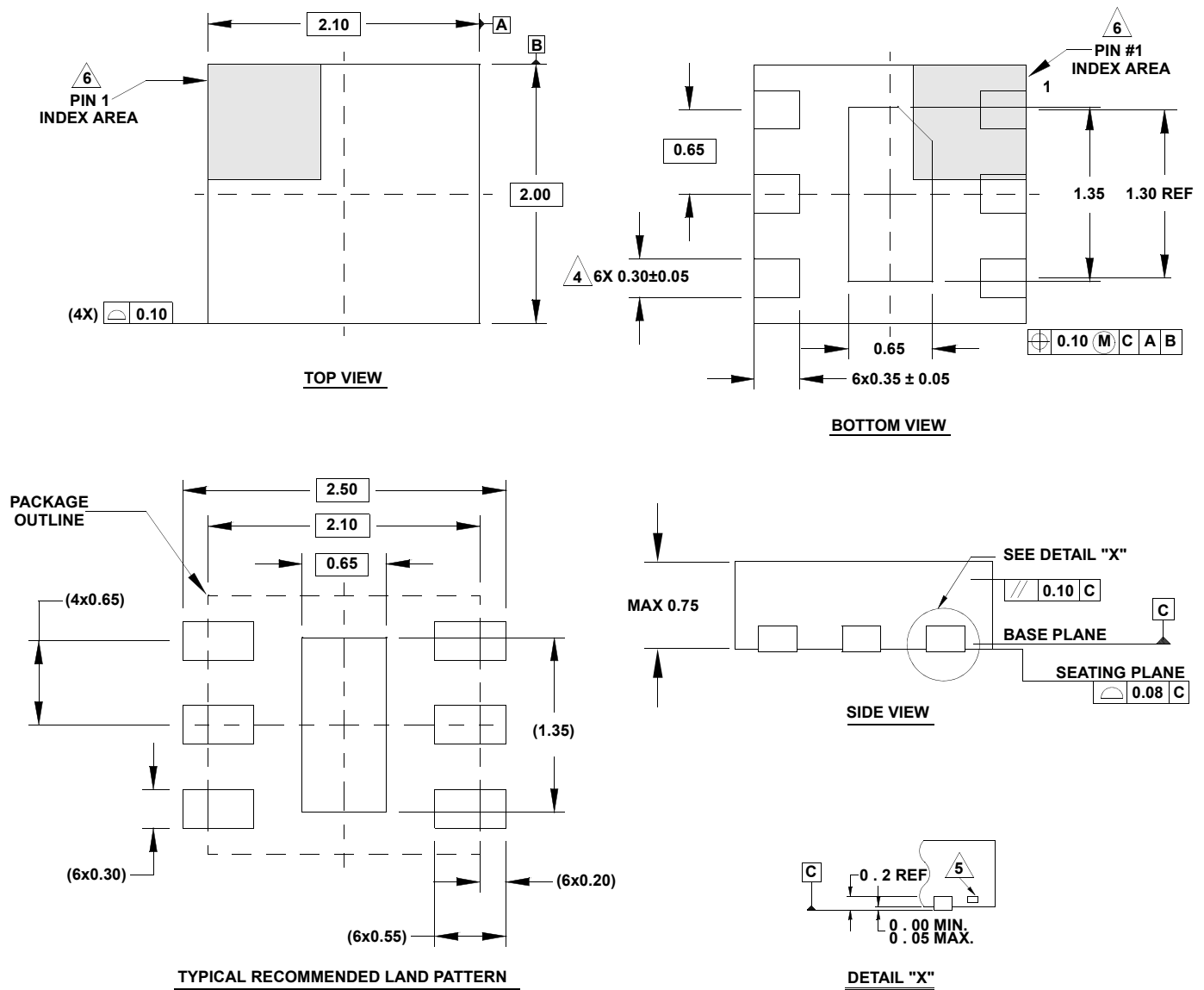
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# Package Outline Drawing

## L6.2x2.1

6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)

Rev 3, 5/11



### NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



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