

General Description

The 9DMU0131 is a member of IDT's SOC-Friendly 1.5V Ultra-Low-Power (ULP) PCIe Gen1-2-3 family. The output has an OE# pin for optimal system control and power management. The part provides asynchronous or glitch-free switching modes.

Recommended Application

2:1 1.5V PCIe Gen1-2-3 Clock Mux

Output Features

- 1 – Low-Power (LP) HCSL DIF pair

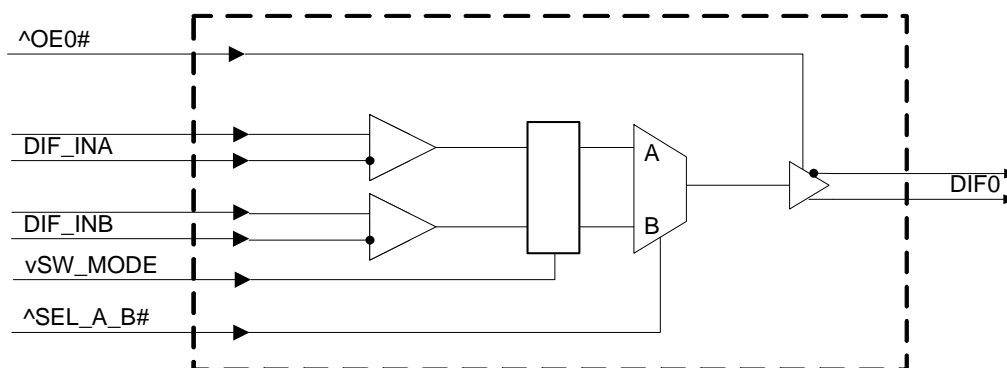
Key Specifications

- DIF *additive* cycle-to-cycle jitter <5ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- 125MHz additive phase jitter 535fs rms typical (12kHz to 20MHz)

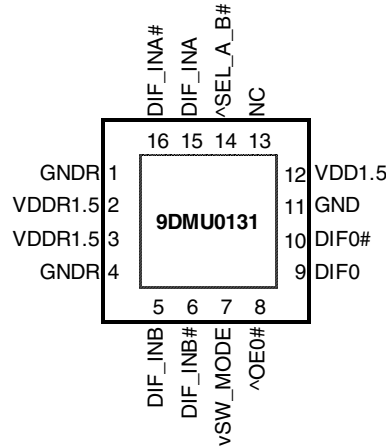
Features/Benefits

- LP-HCSL output; saves 2 resistors compared to standard HCSL output
- 1.5V operation; 11mW typical power consumption
- Selectable asynchronous or glitch-free switching; allows the mux to be selected at power up even if both inputs are not running, then transition to glitch-free switching mode
- Spread Spectrum Compatible; supports EMI reduction
- OE# pin; supports DIF power management
- HCSL differential inputs; can be driven by common clock sources
- 1MHz to 167MHz operating frequency
- Space saving 16-pin 3x3mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



16-pin VFQFPN, 3x3 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor
v prefix indicates internal 120KOhm pull down resistor

Note: Paddle may be connected to ground for thermal purposes. It is not required electrically.

Power Management Table

| OEx# Pin | DIF_IN | DIFx | |
|----------|---------|----------|-----------|
| | | True O/P | Comp. O/P |
| 0 | Running | Running | Running |
| 1 | Running | Low | Low |

Power Connections

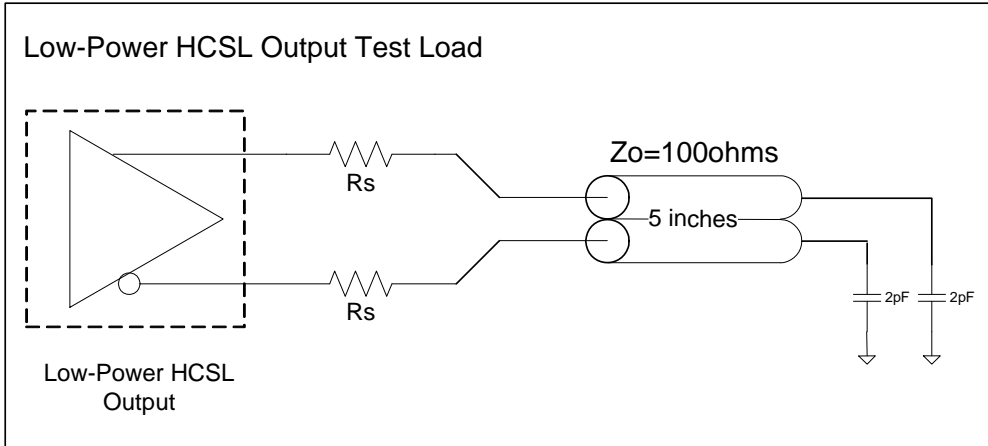
| Pin Number | | Description |
|------------|-----|-------------------------|
| VDD | GND | |
| 2 | 1 | Input A receiver analog |
| 3 | 4 | Input B receiver analog |
| 12 | 11 | DIF outputs |

Note: Pins 2 and 3 should be decoupled separately to pins 1 and 4 respectively.

Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|------|-----------|------|--|
| 1 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 2 | VDDR1.5 | PWR | 1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 3 | VDDR1.5 | PWR | 1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 4 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 5 | DIF_INB | IN | HCSL Differential True input |
| 6 | DIF_INB# | IN | HCSL Differential Complement Input |
| 7 | vSW_MODE | IN | Switch Mode. This pin selects either asynchronous or glitch-free switching of the mux. Use asynchronous mode if 0 or 1 of the input clocks is running. Use glitch-free mode if both input clocks are running. This pin has an internal pull down resistor of ~120kohms. 0 = asynchronous mode 1 = glitch-free mode |
| 8 | ^OE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 9 | DIF0 | OUT | Differential true clock output |
| 10 | DIF0# | OUT | Differential Complementary clock output |
| 11 | GND | GND | Ground pin. |
| 12 | VDD1.5 | PWR | Power supply, nominally 1.5V |
| 13 | NC | N/A | No Connection. |
| 14 | ^SEL_A_B# | IN | Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected. |
| 15 | DIF_INA | IN | HCSL Differential True input |
| 16 | DIF_INA# | IN | HCSL Differential Complement Input |

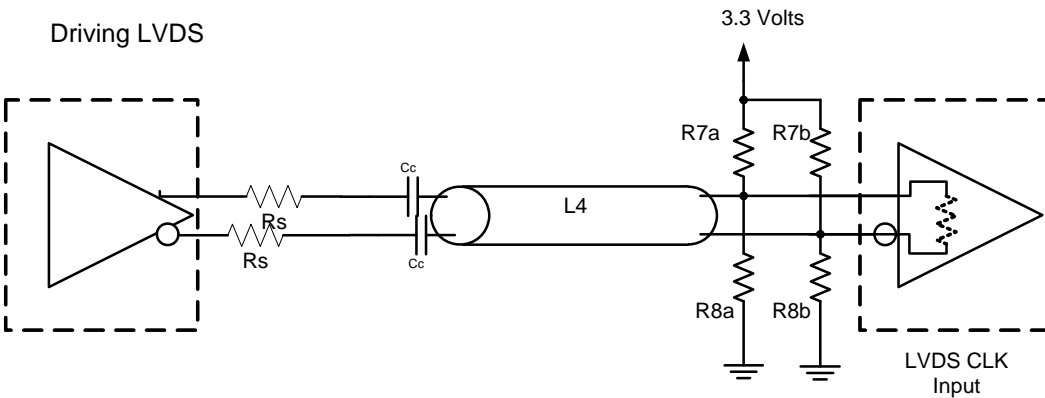
Test Loads



Alternate Differential Output Terminations

| Rs | Zo | Units |
|----|-----|-------|
| 33 | 100 | Ohms |
| 27 | 85 | |

Driving LVDS



Driving LVDS inputs

| Component | Value | | Note |
|-----------|--------------------------|------------------------------------|------|
| | Receiver has termination | Receiver does not have termination | |
| R7a, R7b | 10K ohm | 140 ohm | |
| R8a, R8b | 5.6K ohm | 75 ohm | |
| Cc | 0.1 uF | 0.1 uF | |
| Vcm | 1.2 volts | 1.2 volts | |

Electrical Characteristics–Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|---------------------------|------|-----|----------------------|-------|-------|
| Supply Voltage | VDDx | | -0.5 | | 2 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.5 | V | 1,3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins | | | 3.3 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

³Not to exceed 2.0V.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

T_A = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|------------------------|---|----------------------|-----|-----------------------|--------|-------|
| Supply Voltage | VDDx | Supply voltage for core and analog | 1.425 | 1.5 | 1.575 | V | |
| Ambient Operating Temperature | T _{AMB} | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus | 0.75 V _{DD} | | V _{DD} + 0.3 | V | |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus | -0.3 | | 0.25 V _{DD} | V | |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Input Frequency | F _{in} | | 1 | | 167 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | f _{MODINPCIe} | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | f _{MODIN} | Allowable Frequency for non-PCIe Applications (Triangular Modulation) | 0 | | 66 | kHz | |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| T _{fall} | t _F | Fall time of single-ended control inputs | | | 5 | ns | 1,2 |
| T _{rise} | t _R | Rise time of single-ended control inputs | | | 5 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

Electrical Characteristics–Clock Input Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | V _{IHDIF} | Differential inputs (single-ended measurement) | 300 | 750 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 200 | | 725 | mV | 1 |
| Input Amplitude - DIF_IN | V _{SWING} | Peak to Peak value (V _{IHDIF} - V _{ILDIF}) | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.35 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{in} | Measurement from differential waveform | 45 | 50 | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFin} | Differential Measurement | 0 | | 150 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|------|-------|-------|
| Slew rate | dv/dt | Scope averaging on, fast setting | 1.3 | 2.5 | 3.9 | V/ns | 1,2,3 |
| Slew rate matching | Δdv/dt | Slew rate matching, Scope averaging on | | 16 | 20 | % | 1,2,4 |
| Voltage High | V _{HIGH} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 550 | 766 | 850 | mV | |
| Voltage Low | V _{LOW} | | -150 | 22 | 150 | | |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | 774 | 1150 | mV | |
| Min Voltage | V _{min} | | -300 | -33 | | | |
| Vswing | V _{swing} | Scope averaging off | 300 | 1488 | | mV | 1,2 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 382 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-V _{cross} | Scope averaging off | | 11 | 140 | mV | 1,6 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ-V_{cross} to be smaller than V_{cross} absolute.

Electrical Characteristics–Current Consumption

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-------------------|---------------------------------|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD} | VDD, All outputs active @100MHz | | 7 | 11 | mA | 1 |
| Powerdown Current | I _{DDPD} | VDD, all outputs disabled | | 1.4 | 2.5 | mA | 1, 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-----------------------|-----------------------------------|------|------|------|-------|-------|
| Duty Cycle Distortion | t _{DCD} | Measured differentially @ 100MHz | -1 | -0.1 | 1 | % | 1,3 |
| Skew, Input to Output | t _{pdBYP} | Bypass Mode, V _T = 50% | 2166 | 2896 | 3952 | ps | 1 |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | N/A | N/A | ps | 1 |
| Jitter, Cycle to cycle | t _{jcyc-cyc} | Additive Jitter | | 0.1 | 8 | ps | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

Electrical Characteristics–Phase Jitter Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|------------------------------------|------------------------|---|-----|------|------|----------------|----------|-----------|
| Additive Phase Jitter, Bypass Mode | t _{jphPCIeG1} | PCIe Gen 1 | | 0.4 | 5 | N/A | ps (p-p) | 1,2,3,5 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.4 | 0.55 | N/A | ps (rms) | 1,2,3,4,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.1 | 0.2 | N/A | ps (rms) | 1,2,3,4 |
| | t _{jphPCIeG3} | PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.05 | 0.1 | N/A | ps (rms) | 1,2,3,4 |
| | t _{jph125M0} | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 365 | 380 | N/A | fs (rms) | 1,6 |
| | t _{jph125M1} | 125MHz, 12KHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 535 | 550 | N/A | fs (rms) | 1,6 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

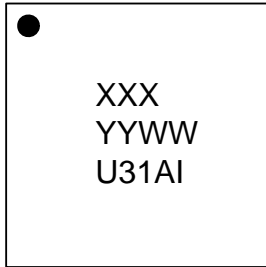
³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²]

⁵ Driven by 9FGU0831 or equivalent

⁶ Rohde&Schartz SMA100

Marking Diagram



Notes:

1. "XXX" is the last 3 characters of the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. Line 3: truncated part number
4. "I" denotes industrial temperature grade.

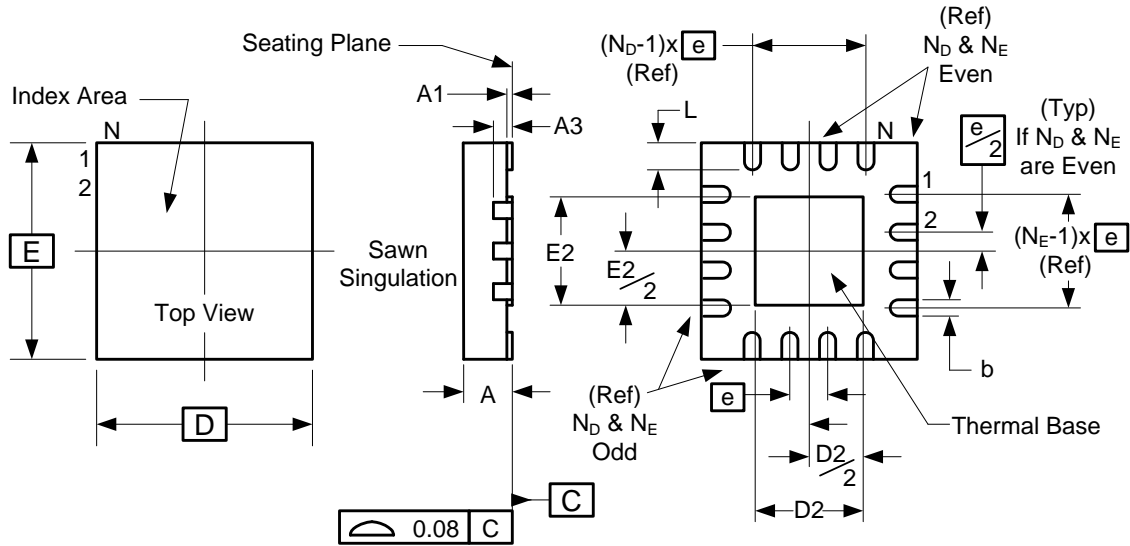
Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | θ_{JC} | Junction to Case | NLG16 | 66 | °C/W | 1 |
| | θ_{Jb} | Junction to Base | | 5 | °C/W | 1 |
| | θ_{JA0} | Junction to Air, still air | | 63 | °C/W | 1 |
| | θ_{JA1} | Junction to Air, 1 m/s air flow | | 56 | °C/W | 1 |
| | θ_{JA3} | Junction to Air, 3 m/s air flow | | 51 | °C/W | 1 |
| | θ_{JA5} | Junction to Air, 5 m/s air flow | | 49 | °C/W | 1 |

¹ePad soldered to board

Package Outline and Package Dimensions (NLG16)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | |
|-------------|----------------|------|
| | Min | Max |
| A | 0.80 | 1.00 |
| A1 | 0 | 0.05 |
| A3 | 0.20 Reference | |
| b | 0.18 | 0.30 |
| e | 0.50 BASIC | |
| N | 16 | |
| ND | 4 | |
| NE | 4 | |
| D x E BASIC | 3.00 x 3.00 | |
| D2 | 1.55 | 1.80 |
| E2 | 1.55 | 1.80 |
| L | 0.30 | 0.50 |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|---------------|---------------|
| 9DMU0131AKILF | Trays | 16-pin VFQFPN | -40 to +85° C |
| 9DMU0131AKILFT | Tape and Reel | 16-pin VFQFPN | -40 to +85° C |

“LF” to the suffix denotes Pb-Free configuration, RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|------|-----------|------------|--|---------|
| A | RDW | 9/29/2014 | 1. Update front page text and electrical tables with char data. 2. Update pinout diagram with note about package paddle. 3. Move to final. | Various |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

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Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru