

N-Channel Power MOSFET

600V, 8A, 0.6Ω

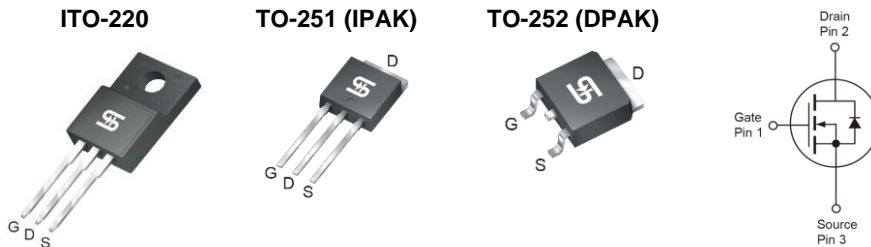
FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance

APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	0.6	Ω
Q_g	13	nC



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	ITO-220	IPAK/DPAK	UNIT
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	8	A
		$T_C = 100^\circ\text{C}$	4.8	
Pulsed Drain Current ^(Note 2)	I_{DM}	24		A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	32	83	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	100		mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	2		A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	ITO-220	IPAK/DPAK	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	3.9	1.5	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62		°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.0	3.0	4.0	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 4A$	$R_{DS(on)}$	--	0.49	0.6	Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 380V, I_D = 8A,$ $V_{GS} = 10V$	Q_g	--	13	--	nC
Gate-Source Charge		Q_{gs}	--	3	--	
Gate-Drain Charge		Q_{gd}	--	4	--	
Input Capacitance	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	743	--	pF
Output Capacitance		C_{oss}	--	66	--	
Gate Resistance	$F = 1\text{MHz}, \text{open drain}$	R_g	--	3.2	--	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 380V,$ $R_{GEN} = 25\Omega,$ $I_D = 8A, V_{GS} = 10V,$	$t_{d(on)}$	--	21	--	ns
Turn-On Rise Time		t_r	--	15	--	
Turn-Off Delay Time		$t_{d(off)}$	--	40	--	
Turn-Off Fall Time		t_f	--	9	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	$I_S = 8A, V_{GS} = 0V$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$V_R = 200V, I_S = 4A$ $di_f/dt = 100A/\mu s$	t_{rr}	--	185	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.4	--	μC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 50\text{mH}, I_{AS} = 2A, V_{DD} = 50V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM60N600CI C0G	ITO-220	50pcs / Tube
TSM60N600CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM60N600CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

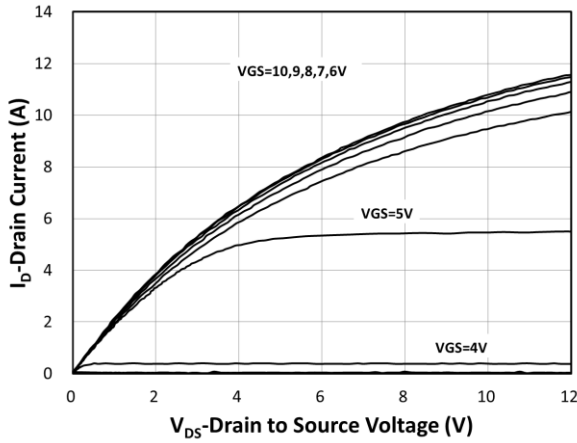
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

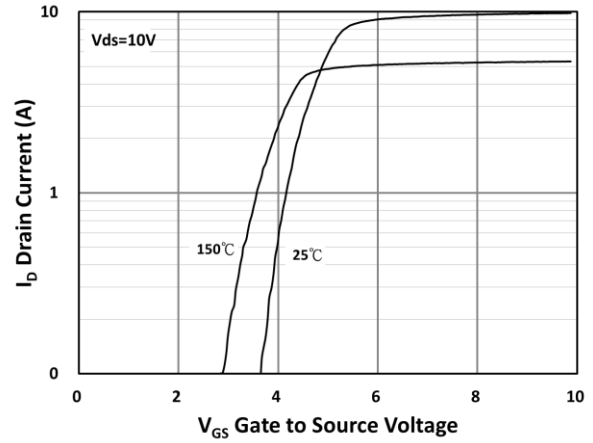
ELECTRICAL CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

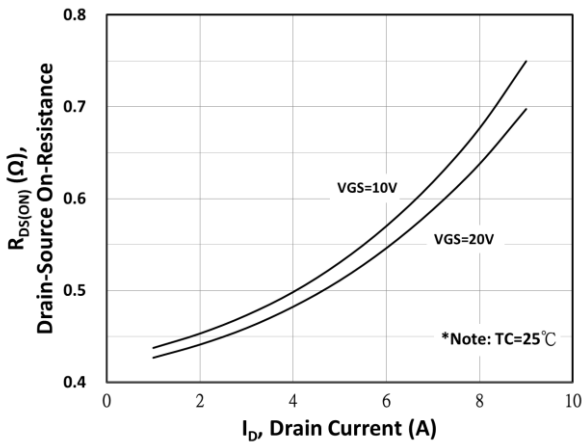
Output Characteristics



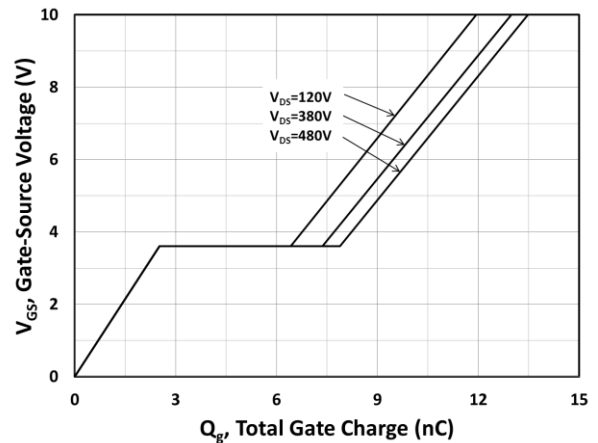
Transfer Characteristics



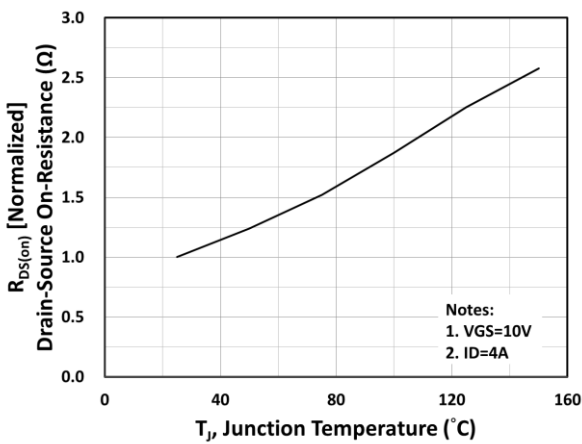
On-Resistance vs. Drain Current



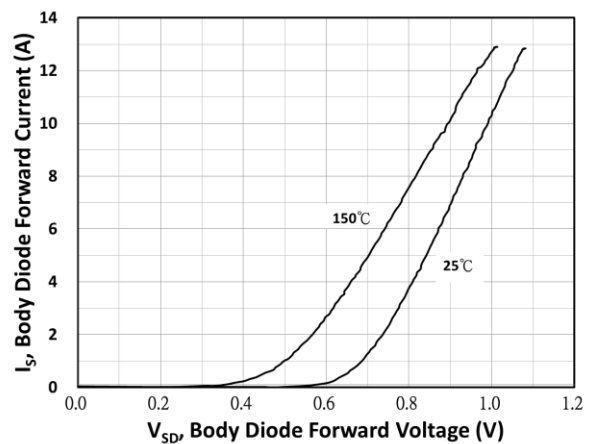
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



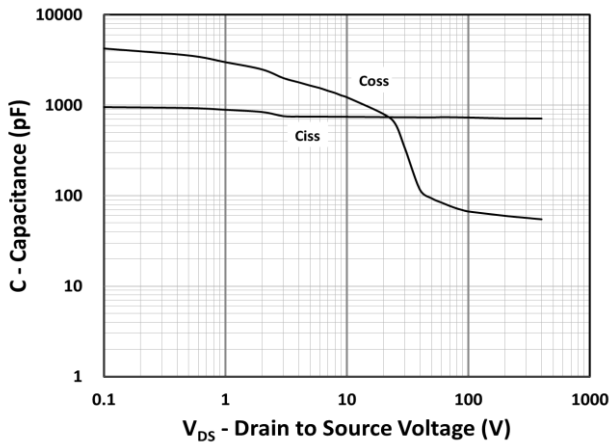
Source-Drain Diode Forward Current vs. Voltage



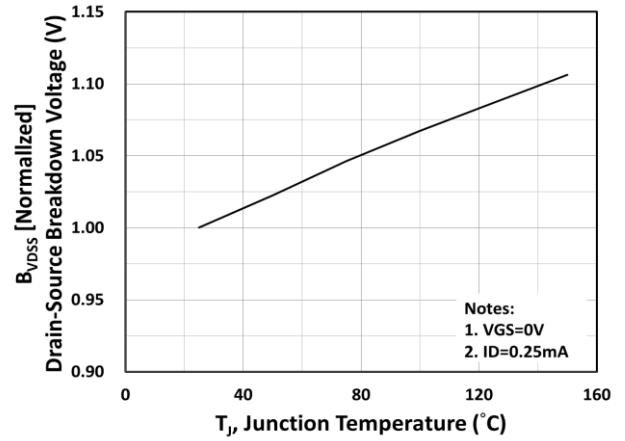
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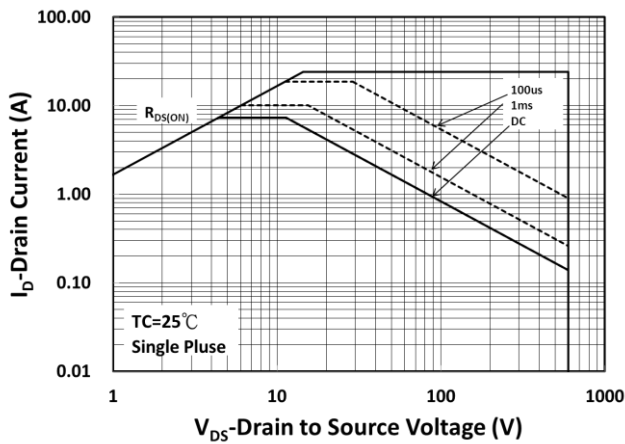
Capacitance vs. Drain-Source Voltage



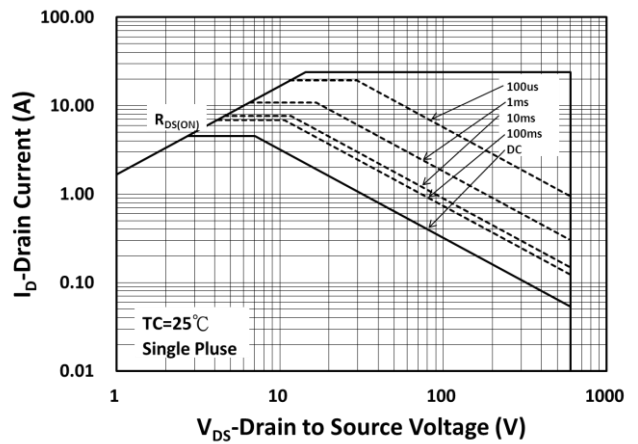
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area (DPAK/IPAK)



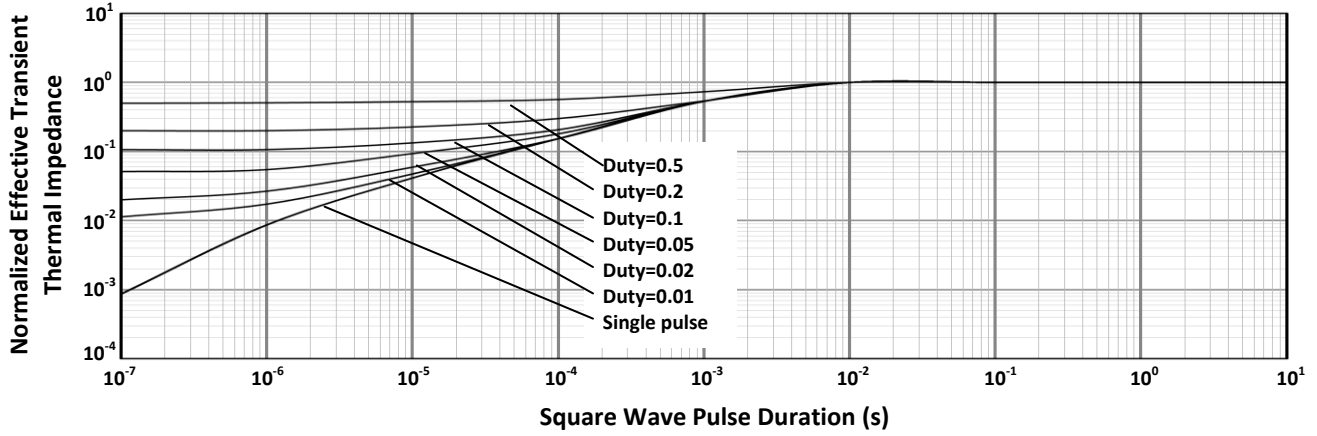
Maximum Safe Operating Area (ITO-220)



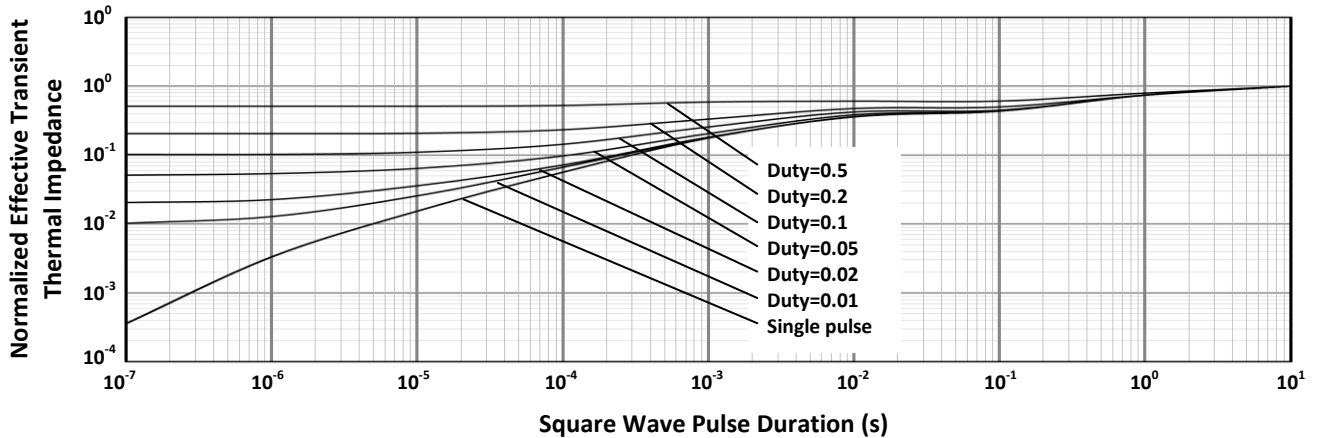
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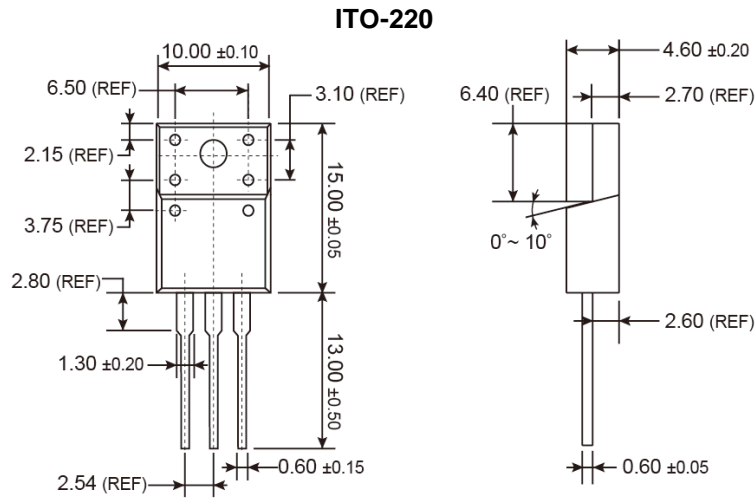
Normalized Thermal Transient Impedance, Junction-to-Case (DPAK/IPAK)



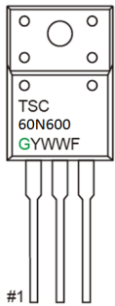
Normalized Thermal Transient Impedance, Junction-to-Case (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



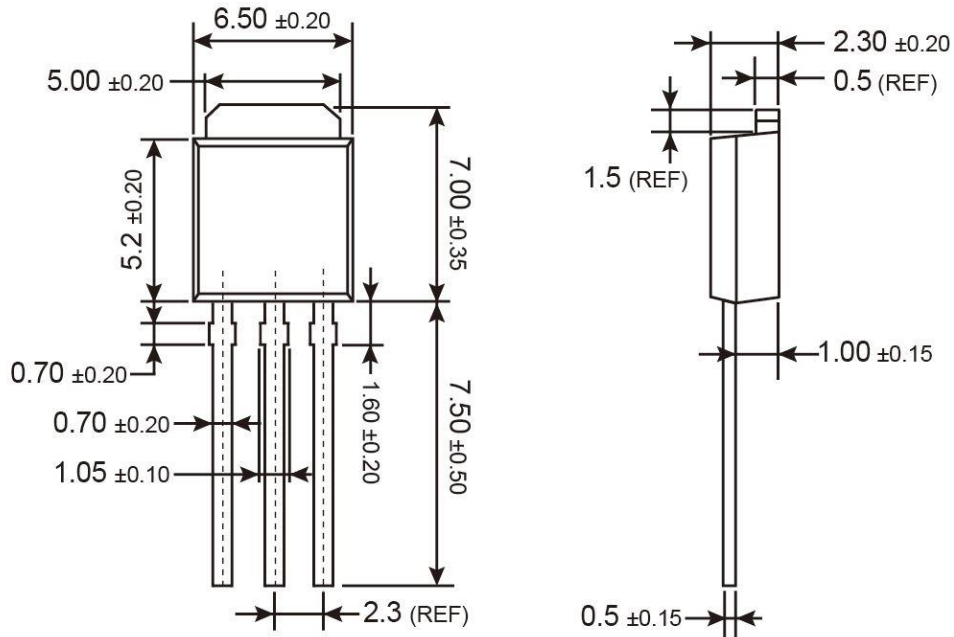
MARKING DIAGRAM



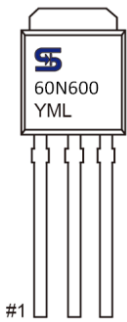
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251 (IPAK)

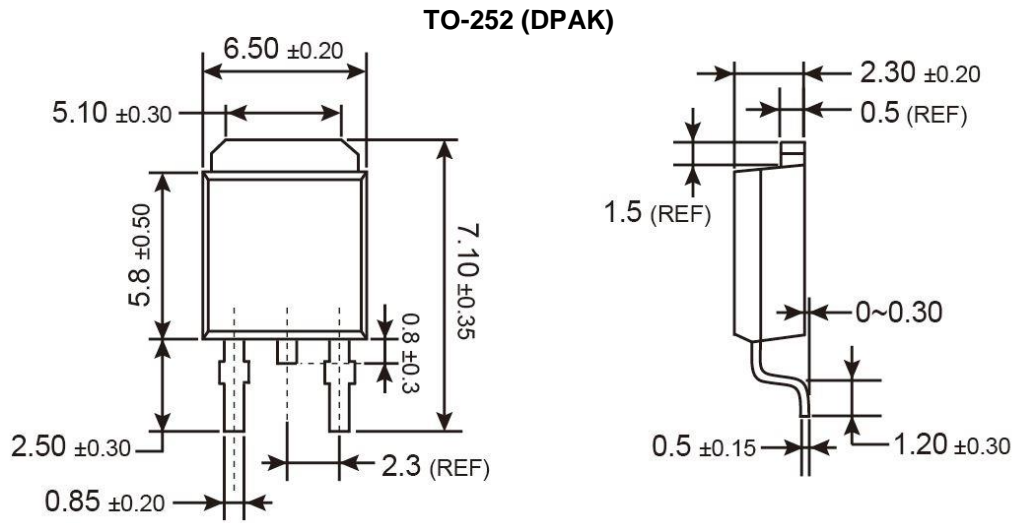


MARKING DIAGRAM

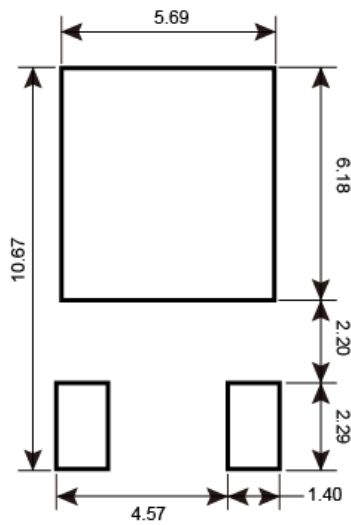


- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
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 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

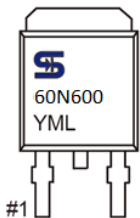
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM



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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
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