

# NCL30088LED1GEVB

## 18 W High Power Factor LED Driver Evaluation Board User's Manual



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### EVAL BOARD USER'S MANUAL

#### Overview

This manual covers the specification, theory of operation, testing and construction of the NCL30088LED1GEVB demonstration board. The NCL30088 board demonstrates a 18 W high PF buck boost LED driver in a typical T8 outline.

Table 1. SPECIFICATIONS

Parameter	Value	Comment
Input voltage (Class 2 Input, no ground)	100 – 277 V ac	
Line Frequency	50 Hz / 60 Hz	
Power Factor (100% Load)	0.9	Min
THD (Load > 30%)	20%	Max
Output Voltage Range	90 – 180 V dc	
Output Current	100 mA dc	±2%
Efficiency	92%	Typical
Start Up Time	< 500 msec	Typical
EMI (conducted)	Class B	FCC/CISPR

#### Key Features

As illustrated, the key features of this evaluation board include:

- Wide Mains
- Low THD across Line and Load
- High Power Factor across Wide Line and Load
- Integrated Auto Recovery Fault Protection (can be latched by Choice of Options)
  - ♦ Over Temperature on Board (a PCB mounted NTC)
  - ♦ Over Current
  - ♦ Output and Vcc Over Voltage



Figure 1. Evaluation Board Picture (Top View)

## THEORY OF OPERATION

**Power Stage**

The power stage for the demo board is a non-isolated buck-boost based. The controller has a built in control algorithm that is specific to the flyback transfer function. Specifically:

$$\frac{V_{out}}{V_{in}} = \frac{Duty}{(1 - Duty)}$$

This is applicable to flyback, buck-boost, and SEPIC converters. The control is very similar to the control of the NCL30080-83 with the addition of a power factor correction control loop. The controller has a built in hardware algorithm that relates the output current to a reference on the primary side.

$$I_{out} = \frac{V_{ref} \times N_{ps}}{2 \times R_{sense}}$$

$$N_{ps} = \frac{N_{pri}}{N_{sec}}$$

Where  $N_{pri}$  = Primary Turns and  $N_{sec}$  = Secondary Turns  
We can now find  $R_{sense}$  for a given output current.

$$R_{sense} = \frac{V_{ref} \times N_{ps}}{2 \times I_{out}}$$

**Line Feedforward**

The controller is designed to precisely regulate output current but variation input line voltage do have an impact. R3 sets the line feedforward and compensates for power stage delay times by reducing the current threshold as the line voltage increases. R3 is also used by the shorted pin detection. At start up the controller puts out a current to check for a shorted pin. If R3 is zero, the current sense resistor is too low a value and the controller will not start because it will detect a shorted pin. So R3 is required to make the controller operate properly. In practice, R3 should be greater than 250  $\Omega$ .

**Voltage Sense**

The voltage sense pin has several functions:

1. Basis for the reference of the PFC control loop
2. Line Range detection

The reference scaling is automatically controller inside the controller. While the voltage on  $V_s$  is not critical for the PFC loop control, it is important for the range detection. Generally the voltage on  $V_s$  should be 3.5 V peak at the highest input voltage of interest. The voltage on  $V_s$  determines which valley the power stage will operate in. At low line and maximum load, the power stage operates in the first valley (standard CrM operation). At the higher line range, the power stage moves to the second valley to lower the switching frequency while retaining the advantage of CrM soft switching.

**Auxiliary Winding**

The auxiliary winding has 3 functions:

1. CrM timing
2. Vcc Power
3. Output voltage sense

*CrM Timing*

In the off time, the voltage on the transformer/inductor forward biases  $D_{out}$  and  $D_9$ . When the current in the magnetic has reached zero, the voltage collapses to zero. This voltage collapse triggers a comparator on the ZCD pin to start a new switching cycle. The ZCD pin also counts rings on the auxiliary winding for higher order valley operation. A failure of the ZCD pin to reach a certain threshold also indicates a shorted output condition.

*Vcc Power*

The auxiliary winding forward biases  $D_9$  to provide power for the controller. This arrangement is called a "bootstrap". Initially the  $C_{vcc}$  is charged through R4 and R5. When the voltage on  $C_{vcc}$  reaches the startup threshold, the controller starts switching and providing power to the output circuit and the  $C_{vcc}$ .  $C_{vcc}$  discharges as the controller draws current. As the output voltage rises, the auxiliary winding starts to provide all the power to the controller. Ideally, this happens before  $C_{vcc}$  discharges to the under voltage threshold where the controller stops operating to allow  $C_{vcc}$  to recharge once again. The size of the output capacitor will have a large effect on the rise of the output voltage. Since the LED driver is a current source, the rise of output voltage is directly dependent on the size of the output capacitor.

There are tradeoffs in the selection of  $C_{out}$  and  $C_{vcc}$ . A low output ripple will require a large  $C_{out}$  value. This requires that  $C_{vcc}$  be large enough to support Vcc power to the controller while  $C_{out}$  is charging up. A large value of  $C_{vcc}$  requires that R4 and R5 be lower in value to allow a fast enough startup time. Smaller values of R4 and R5 have higher static power dissipation which lowers efficiency of the driver.

*Output Voltage Sense*

The auxiliary winding voltage is proportional to the output voltage by the turns ratio of the output winding and the auxiliary winding. The controller has an overvoltage limit on the Vcc pin at about 26 V minimum. Above that threshold, the controller will stop operation and enter overvoltage fault mode such as when an open LED string occurs.

In cases where the output has a lot of ripple current and the LED has high dynamic resistance, the peak output voltage can be much higher than the average output voltage. The auxiliary winding will charge the  $C_{vcc}$  to the peak of the output voltage which may trigger the OVP sooner than expected so in this case the peak voltage of the LED string is critical.

### SD Pin

The SD pin is a multi-function protection input.

1. Thermal Foldback Protection
2. Programmable OVP

#### *Thermal Protection*

There is an internal current source from the SD pin. Placing an NTC from the SD pin to ground will allow the designer to choose the level of current foldback protection from over temperature. Below 0.5 volts on SD, the controller stops. Series or parallel resistors on the NTC and shape the foldback curve. In the event that the pin is left open, there is a soft voltage clamp at 1.35 V (nominal). Output current is reduced when the voltage on the SD pin drops below 1 V.

#### *Programmable OVP*

While the SD pin has a current source for the OTP, it can be overcome raising the voltage on the SD pin. At about

2.5 V, the SD pin detects an OVP and shuts down the controller. Typically, a zener to Vcc is used for this. In this way, the designer can set the OVP to a lower value than the OVP threshold built into the Vcc pin.

### Circuit Modifications

#### *Output Current*

The output current is set by the value of Rsense as shown above. It's possible to adjust the output current by changing R7. Since the magnetic is designed for 18 W, it is possible to increase the current while reducing the maximum LED forward voltage within limits. Changes of current of  $\pm 10\%$  are within the existing EMI filter design and magnetic, changes of more than 10% may require further adjustments to the transformer or EMI filter.

# NCL30088LED1GEVB

## SCHEMATIC

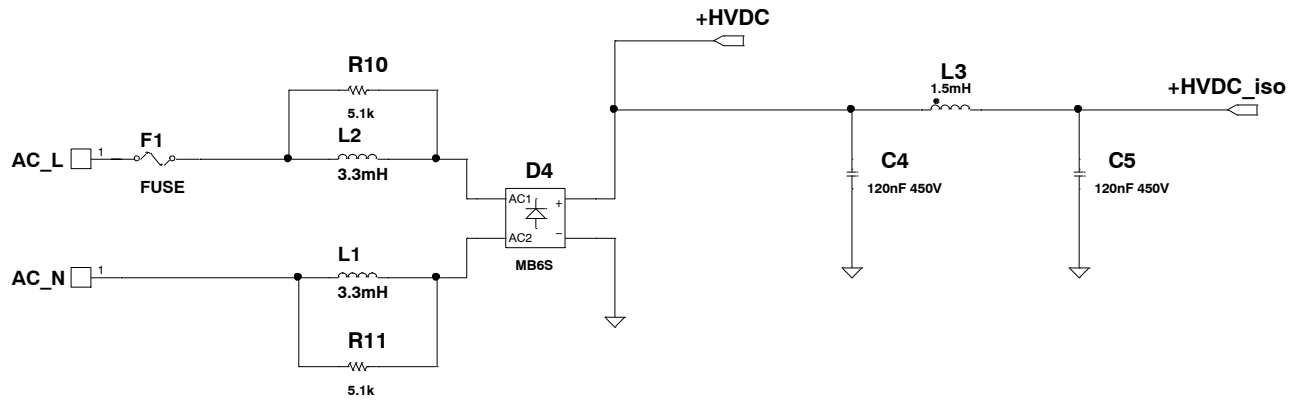


Figure 2. Input Circuit

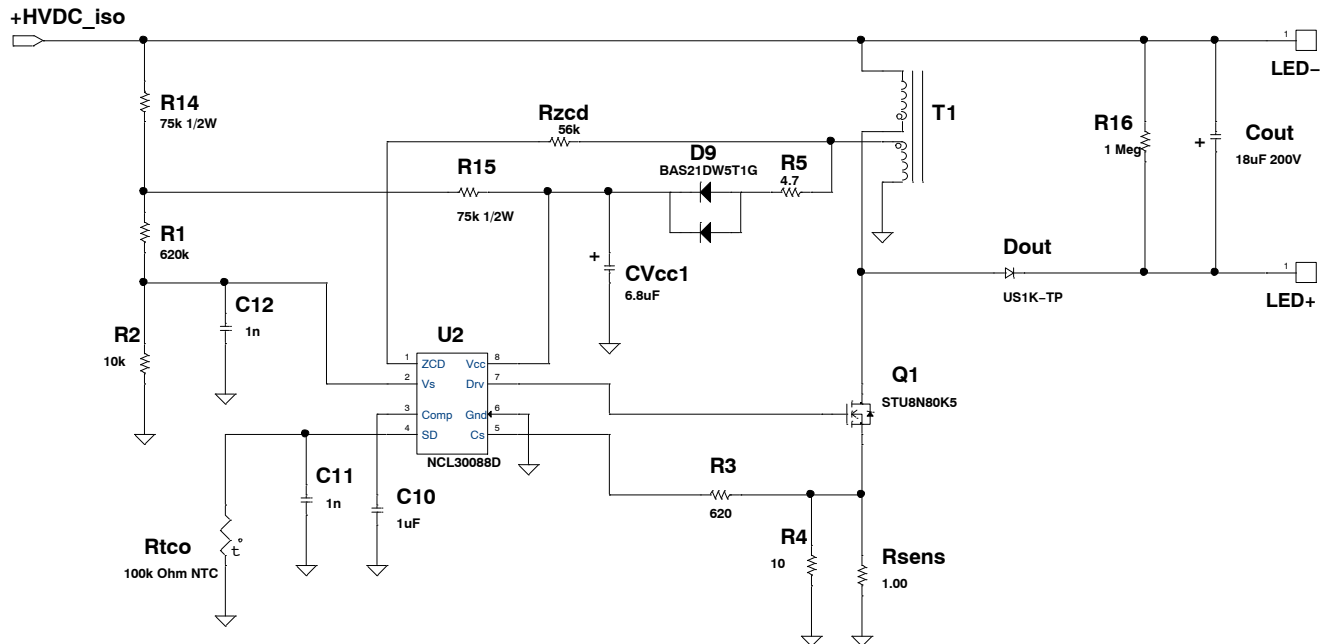


Figure 3. Main Schematic

# NCL30088LED1GEVB

## BILL OF MATERIAL

Table 2. BILL OF MATERIAL\*

Qty	Reference	Part	Manufacturer	Mfr_PN	PCB Footprint	Substitution Allowed
1	Cvcc1	6.8 $\mu$ F	TDK	C3216X7R1V685K160AC	1206	Yes
1	Cout	18 $\mu$ F 200 V	Rubycon	200LLE18MEFC10X12.5	ALEL_10X12M5_VERT	Yes
2	C4, C5	120 nF 450 V	Panasonic	ECW-FD2W124KQ	CAP_BOX_12M6X4M6_LS10	Yes
1	C10	1 $\mu$ F	Taiyo Yuden	TMK105BJ105MV-F	402	Yes
2	C11, C12	1 n	Kemet	C0402C102K3GACTU	402	Yes
1	Dout	US1K-TP	MCC	US1K-TP	SMA	Yes
1	D4	MB6S	MCC	MB6S	MB6S	Yes
1	D9	BAS21DW5T1G	ON Semiconductor	BAS21DW5T1G	SC-88A	No
1	F1	FUSE	Littelfuse	0263.500WRT1L	FUSE-HAIRPIN-L S250	Yes
2	L1, L2	3.3 mH	Wurth	744772332	RAD_IND_LS5	Yes
1	L3	1.5 mH	Wurth	744772152	RAD_IND_LS5	Yes
1	Q1	STU8N80KS	ST	STU8N80K5	IPAK	Yes
1	Rtco	100 k $\Omega$ NTC	Epcos	B57331V2104J60	603	Yes
1	Rzcd	56k	Yaego	RC1206FR-0756KL	1206	Yes
1	R1	620k	Yaego	RC1206FR-07620KL	1206	Yes
1	R2	10k	Yaego	RC0402FR-0710KL	402	Yes
1	R3	620	Yaego	RC0402FR-07620RL	402	Yes
1	R5	4.7	Yaego	RC1206FR-074R7L	1206	Yes
2	R10, R11	5.1k	Yaego	RC1206FR-075K1L	1206	Yes
2	R14, R15	75k $\frac{1}{2}$ W	Stackpole	RNCP1206FTD75K0	1206	Yes
1	R16	1 Meg	Yaego	RC1206JR-071ML	1206	Yes
1	T1	XFRM_LINEAR	Wurth	750314731	RM6_4P	Yes
6"	W1	Wire, Red, 24AWG	McMaster Carr	7587K922	UL1569	Yes
6"	W2	Wire, Blk, 24AWG	McMaster Carr	7587K921	UL1569	Yes
12"	W3, W4	Wire, Wht, 24AWG	McMaster Carr	7587K924	UL1569	Yes

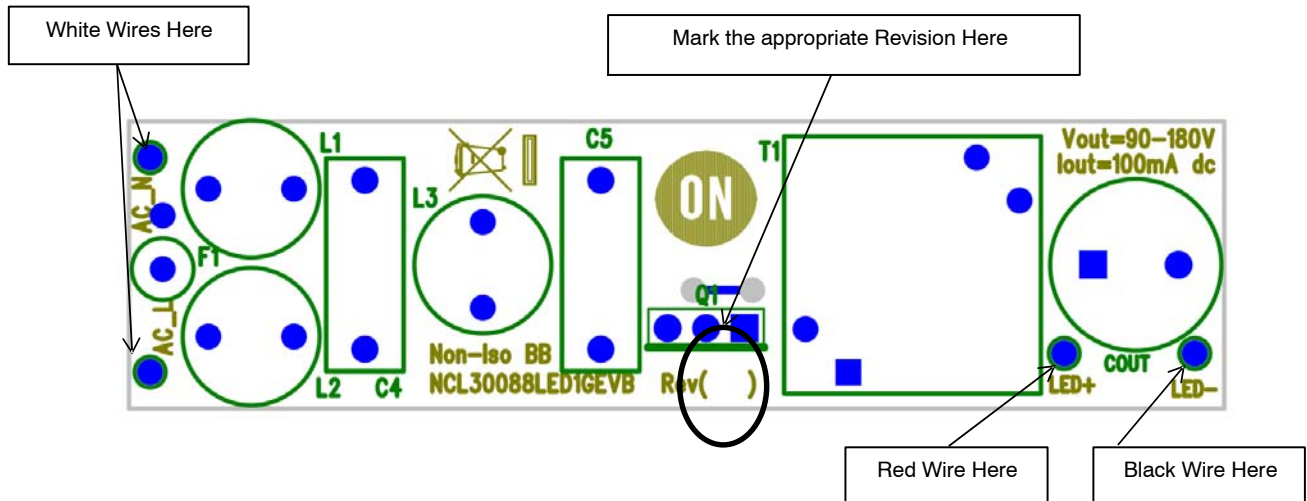
\*All Components to comply with RoHS 2002/95/EC

### Construction Options

NCL30088B Revision 00						
1	U2	NCL30088B	ON Semiconductor	NCL30088B	SO8	No
1	Rsens	1.13	Yaego	RC1206FR-071R13L	1206	Yes
1	R4	No Stuff	Yaego	RC0805JR-0710RL	805	Yes
NCL30088D Revision 01						
1	U2	NCL30088D	ON Semiconductor	NCL30088D	SO8	No
1	Rsens	1	Yaego	RC1206FR-071RL	1206	Yes
1	R4	10	Yaego	RC0805JR-0710RL	805	Yes



# NCL30088LED1GEVB



1. Strip and tin lead wires to  $6'' \pm 0.5''$  4 Places.



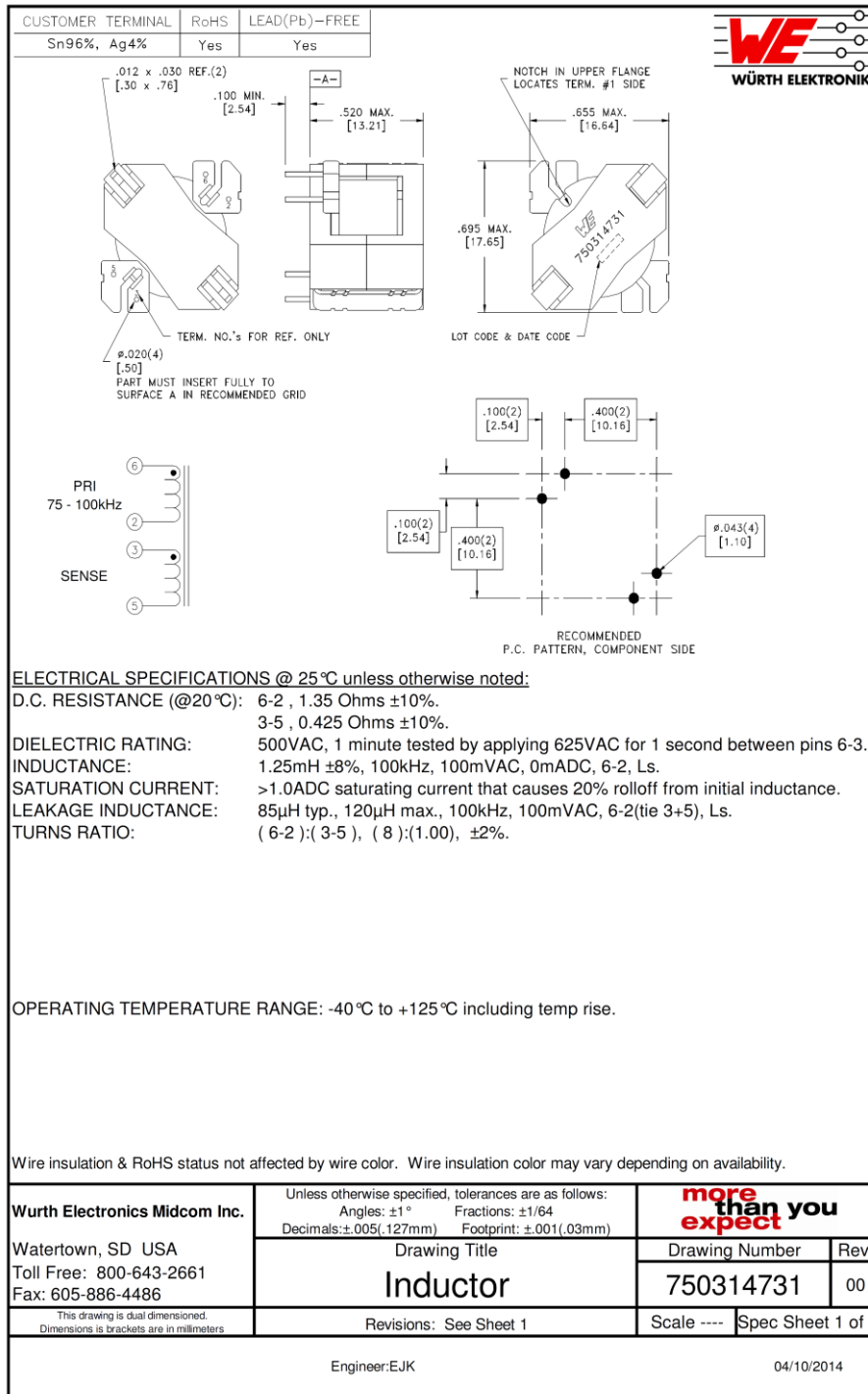
Figure 7. Assembly Notes

**CIRCUIT BOARD FABRICATION NOTES**

1. Fabricate per IPC-6011 and IPC6012. Inspect to IPA-A-600 Class 2 or updated standard.
2. Printed Circuit Board is defined by files listed in fileset.
3. Modification to copper within the PCB outline is not allowed without permission, except where noted otherwise. The manufacturer may make adjustments to compensate for manufacturing process, but the final PCB is required to reflect the associated gerber file design  $\pm 0.001$  in. for etched features within the PCB outline.
4. Material in accordance with IPC-4101/21, FR4, Tg 125°C min.
5. Layer to layer registration shall not exceed  $\pm 0.004$  in.
6. External finished copper conductor thickness shall be 0.0026 in. min. (ie 2oz)
7. Copper plating thickness for through holes shall be 0.0013 in. min. (ie 1oz)
8. All holes sizes are finished hole size.
9. Finished PCB thickness 0.031 in.
10. All un-dimensioned holes to be drilled using the NC drill data.
11. Size tolerance of plated holes:  $\pm 0.003$  in. : non-plated holes  $\pm 0.002$  in.
12. All holes shall be  $\pm 0.003$  in. of their true position U.D.S.
13. Construction to be SMOBC, using liquid photo image (LPI) solder mask in accordance with IPC-SM-B40C, Type B, Class 2, and be green in color.
14. Solder mask mis-registration  $\pm 0.004$  in. max.
15. Silkscreen shall be permanent non-conductive white ink.
16. The fabrication process shall be UL approved and the PCB shall have a flammability rating of UL94V0 to be marked on the solder side in silkscreen with date, manufactures approved logo, and type designation.
17. Warp and twist of the PCB shall not exceed 0.0075 in. per in.
18. 100% electrical verification required.
19. Surface finish: electroless nickel immersion gold (ENIG)
20. RoHS 2002/95/EC compliance required.

# NCL30088LED1GEVB

## BUCK BOOST INDUCTOR SPECIFICATION





## NCL30088LED1GEVB

### Functional Test Procedure

1. Set the LED Load for 26 V output.
2. Set the input power to 120 V 60 Hz.

**CAUTION:** Do not touch the ECA once it is energized because there are hazardous voltages present.

### LINE AND LOAD REGULATION

**Table 3. 120 V / MAX LOAD**

	Output Current 100 mA $\pm$ 3 mA	Output Power	Power Factor	THD < 20%
90 V				
135 V				
180 V				

**Table 4. 230 V / MAX LOAD**

	Output Current 100 mA $\pm$ 3 mA	Output Power	Power Factor	THD < 20%
90 V				
135 V				
180 V				

$$\text{Efficiency} = \frac{V_{\text{out}} \times I_{\text{out}}}{P_{\text{in}}} \times 100\%$$

# NCL30088LED1GEVB

## TEST DATA

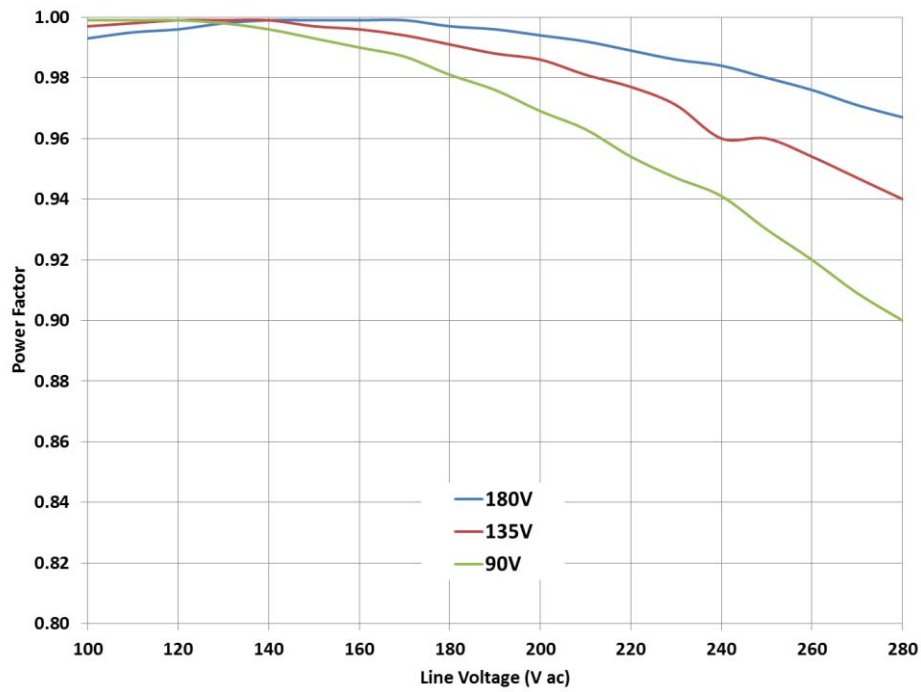


Figure 11. Power Factor over Line and Load

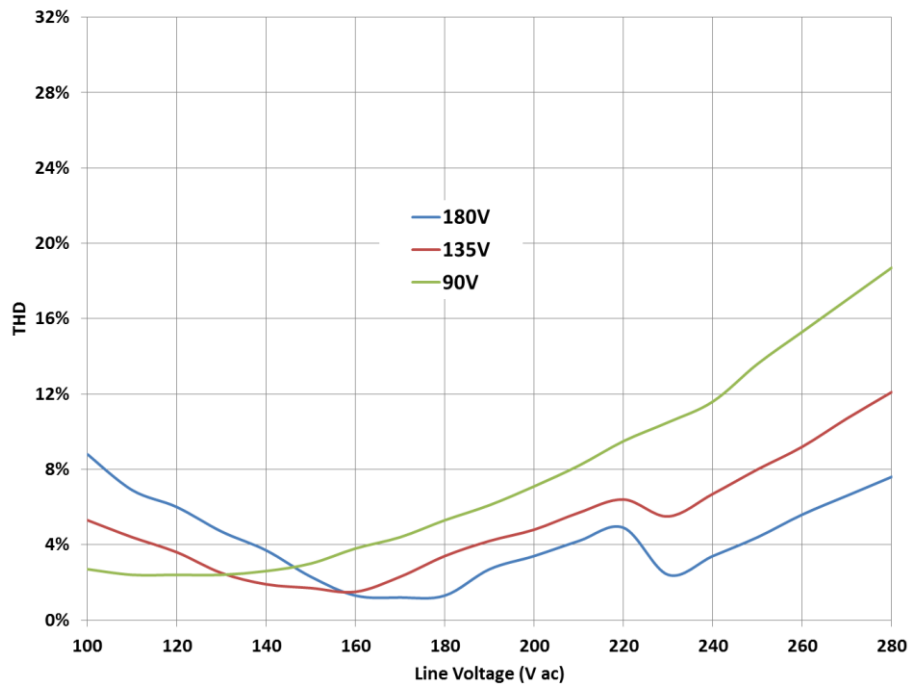


Figure 12. THD over Line and Load

## NCL30088LED1GEVB

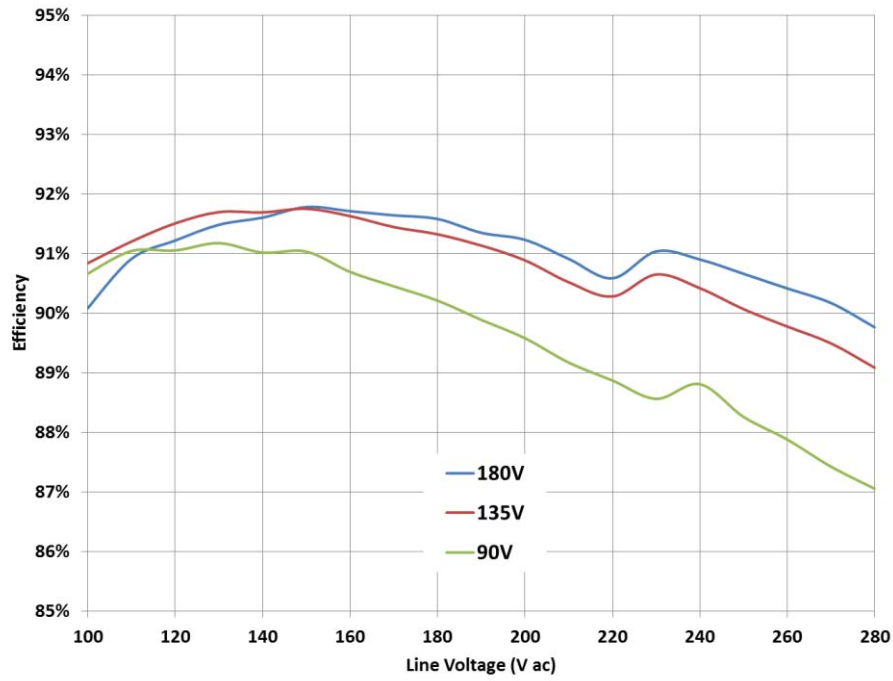


Figure 13. Efficiency over Line and Load

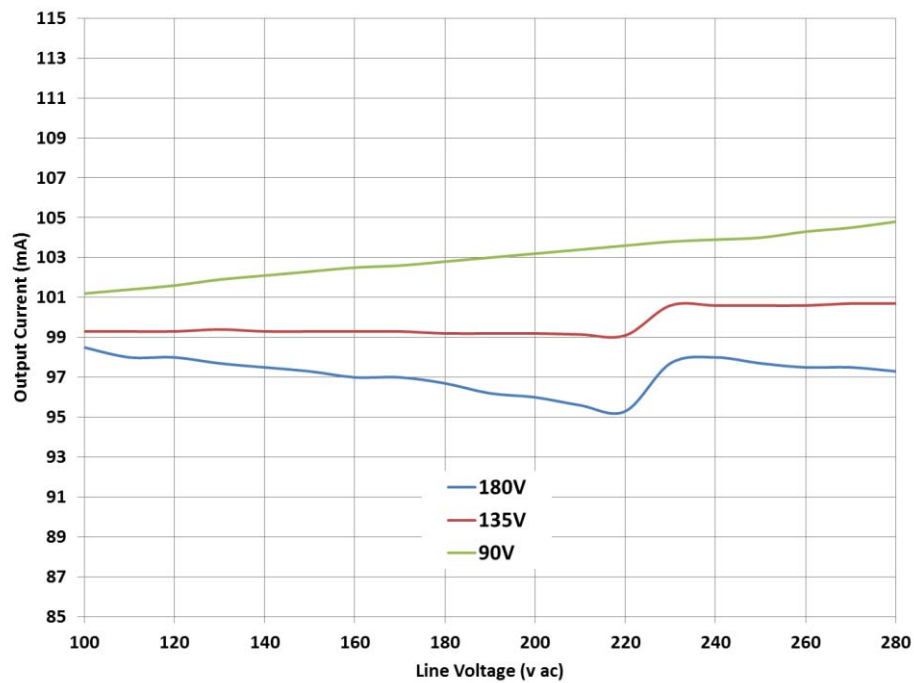


Figure 14. Regulation over Line

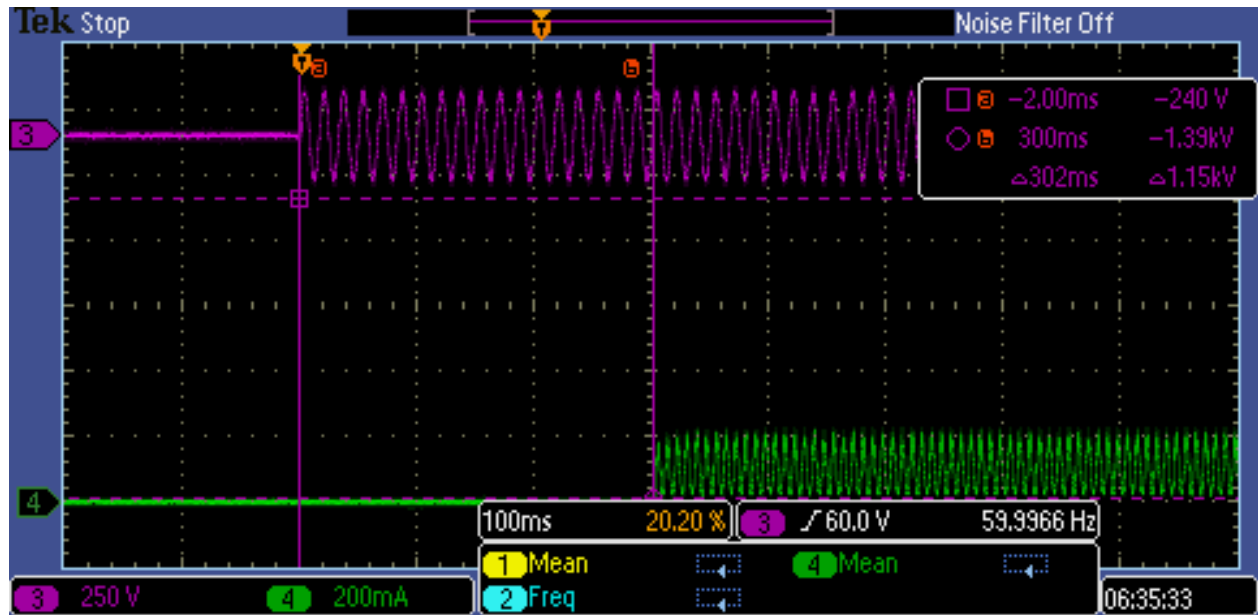


Figure 15. Start Up with AC Applied 120 V Maximum Load

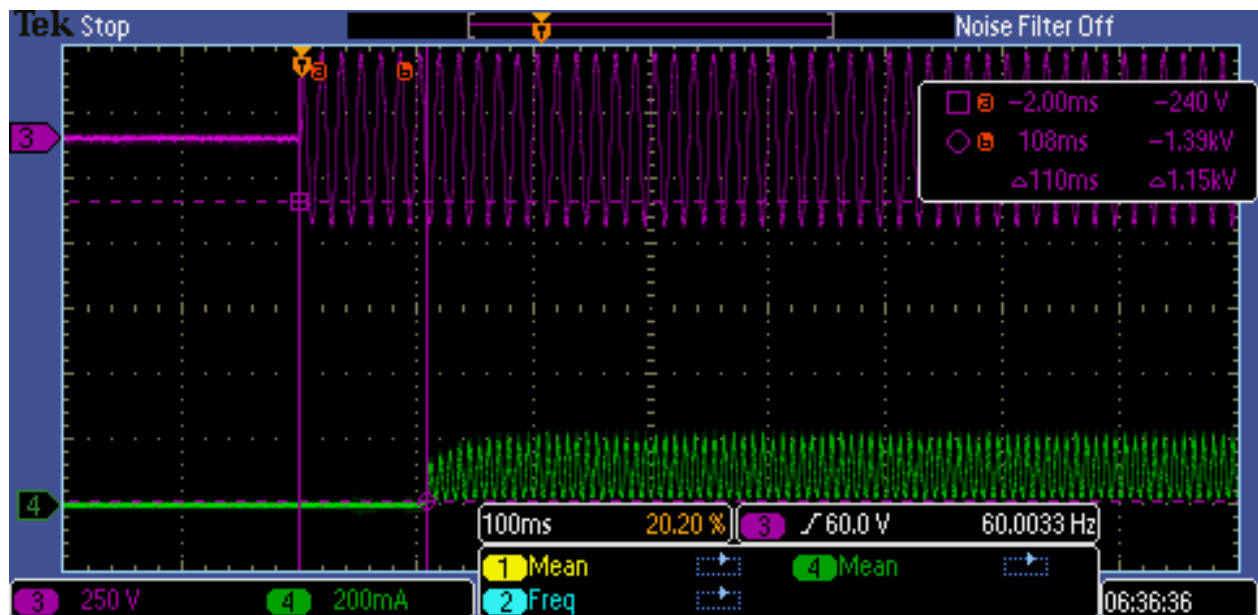


Figure 16. Start Up with AC Applied 230 V Maximum Load

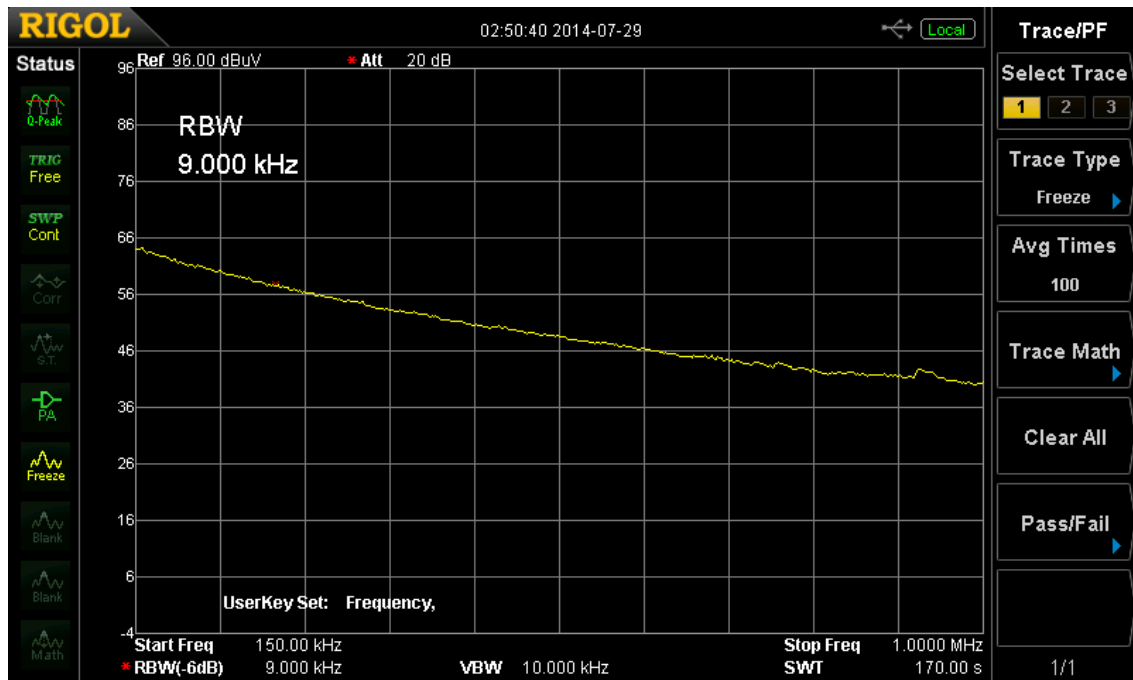


Figure 17. Conducted EMI Pre-compliance QP Data 150 kHz – 1 MHz

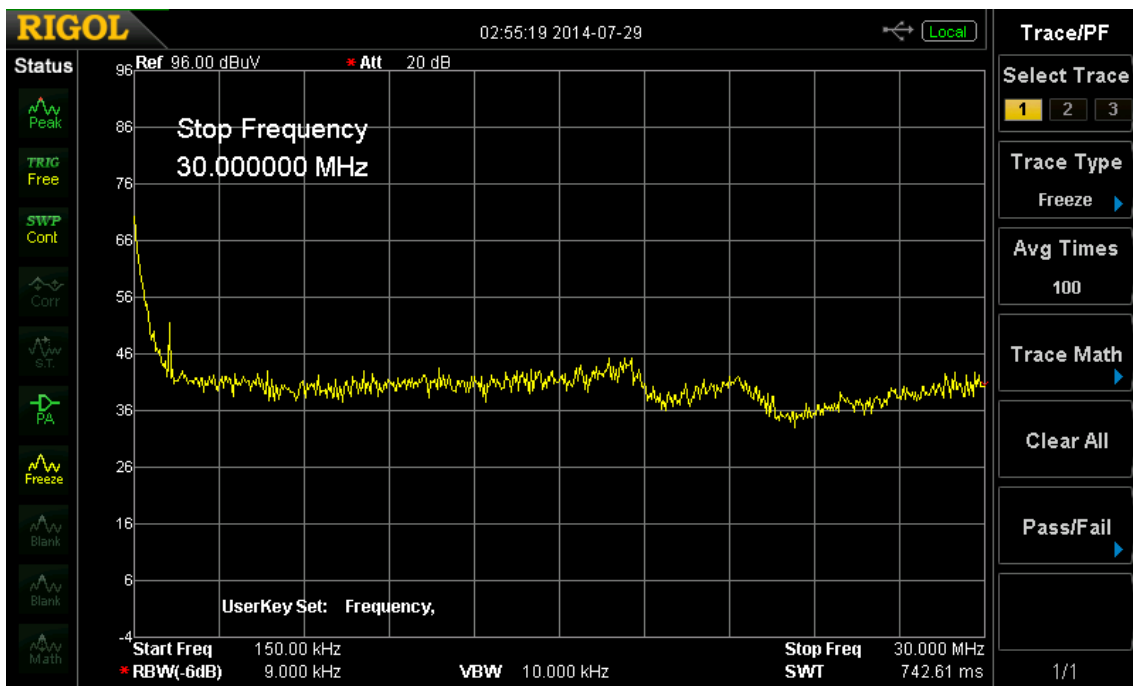



Figure 18. Conducted EMI Pre-compliance Peak Data 150 kHz – 30 MHz

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