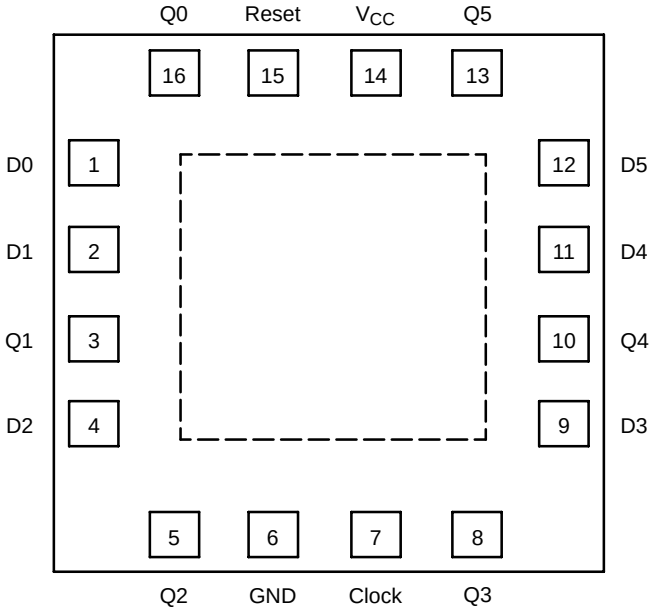
NLSF1174

Hex D Flip-Flop with Common Clock and Reset

This device consists of six D flip−flops with common Clock and Reset inputs. Each flip−flop is loaded with a low−to−high transition of the Clock input. Reset is asynchronous and active low. All inputs/outputs are standard CMOS compatible.

Features

- Output Drive Compatibility: 10 LSTTL Loads
- Outputs Directly Interface to CMOS
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- MSL Level 1
- Chip Complexity: 162 FET
- Pb−Free Package is Available*



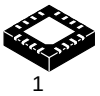
Center pad on bottom may be connected to V_{CC} of device. This pad must be isolated or connected to V_{CC}.

Figure 1. PIN ASSIGNMENT (Top View)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

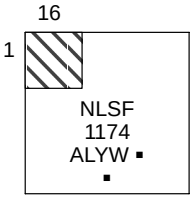
http://onsemi.com



1

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM



NLSF1174	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs			Output
Reset	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change
H	↓	X	No Change

ORDERING INFORMATION

Device	Package	Shipping†
NLSF1174MNR2	QFN−16	3000 / Tape & Reel
NLSF1174MNR2G	QFN−16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2006

May, 2006 − Rev. 5

Publication Order Number:
NLSF1174/D

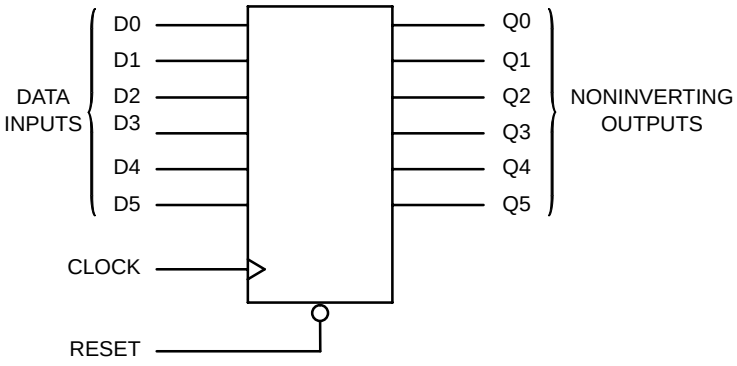


Figure 2. LOGIC DIAGRAM

DESIGN/VALUE TABLE

Design Criteria	Value	Unit
Internal Gate Count*	40.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two−input NAND gate.

MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
DC Supply Voltage	(Referenced to GND)	V_{CC}	−0.5 to +7.0	V
DC Input Voltage	(Referenced to GND)	V_{IN}	−1.5 to V_{CC} +1.5	V
DC Output Voltage	(Referenced to GND) (Note 1)	V_{OUT}	−0.5 to V_{CC} +0.5	V
DC Input Current, per Pin		I_{IN}	±20	mA
DC Output Current, per Pin		I_{OUT}	±25	mA
DC Supply Current, V_{CC} and GND Pins		I_{CC}	±50	mA
Storage Temperature Range		T_{STG}	−65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds	PDIP, SOIC, TSSOP	T_L	260	°C
Junction Temperature Under Bias		T_J	+150	°C
Thermal Resistance	QFN	θ_{JA}	80	°C/W
Power Dissipation in Still Air at 85°C	QFN	P_D	800	mW
Moisture Sensitivity		MSL	Level 1	
Flammability Rating	Oxygen Index: 30 to 35	F_R	UL 94 V−0 @ 0.125 in	
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V_{ESD}	>2000 >100 >500	V
Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	$I_{LATCHUP}$	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.
6. For high frequency or heavy load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Max	Unit
DC Supply Voltage	(Referenced to GND)	V_{CC}	2.0	6.0	V
DC Input Voltage, Output Voltage	(Referenced to GND) (Note 7)	V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature, All Package Types		T_A	−55	+125	°C
Input Rise and Fall Time (Figure 4)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	t_r, t_f	0 0 0	1000 500 400	ns

7. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Parameter	Test Conditions	Symbol	V_{CC} V	Guaranteed Limit −55°C to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
Minimum High−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\| \le 20\ \mu A$	V_{IH}	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
Maximum Low−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\| \le 20\ \mu A$	V_{IL}	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
Minimum High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	V_{OH}	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA		4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	V_{OL}	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA		4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	I_{IN}	6.0	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current (per Package)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	I_{CC}	6.0	4.0	40	160	μA

8. Information on typical parametric values, along with high frequency or heavy load considerations, can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Parameter	Symbol	V_{CC} V	Guaranteed Limit −55°C to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
Maximum Clock Frequency (50% Duty Cycle) (Figures 4 and 7)	f_{max}	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
Maximum Propagation Delay, Clock to Q (Figures 5 and 7)	t_{PLH} t_{PHL}	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
Maximum Propagation Delay, Reset to Q (Figures 2 and 7)	t_{PLH} t_{PHL}	2.0 4.5 6.0	110 21 19	140 28 24	160 32 27	ns
Maximum Output Transition Time, Any Output (Figures 4 and 7)	t_{TLH} t_{THL}	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Maximum Input Capacitance	C_{in}		10	10	10	pF
			Typical @ 25°C, V_{CC} = 5.0 V			
Power Dissipation Capacitance, per Enabled Output (Note 10)	C_{PD}		62			pF

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).
10. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Parameter	Figure	Symbol	V_{CC} V	Guaranteed Limit −55°C to 25°C Min	−55°C to 25°C Max	≤85°C Min	≤85°C Max	≤125°C Min	≤125°C Max	Unit
Minimum Setup Time, Data to Clock	6	t_{su}	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
Minimum Hold Time, Clock to Data	6	t_h	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
Minimum Recovery Time, Reset Inactive to Clock	5	t_{rec}	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
Minimum Pulse Width, Clock	4	t_w	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
Minimum Pulse Width, Reset	5	t_w	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
Maximum Input Rise and Fall Times	4	t_r, t_f	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

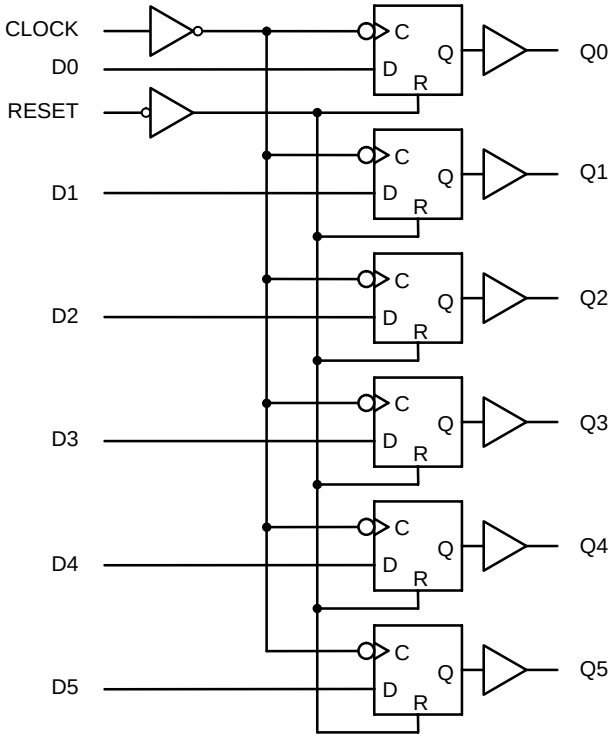


Figure 3. Expanded Logic Diagram

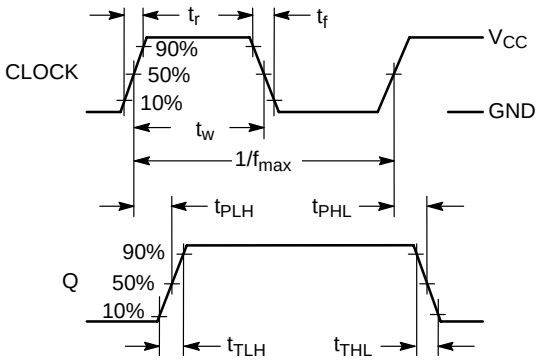


Figure 4. Switching Waveform

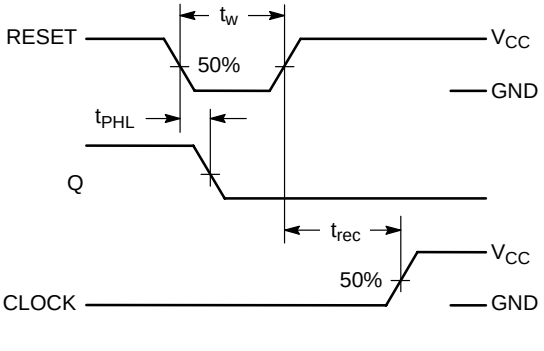


Figure 5. Switching Waveform

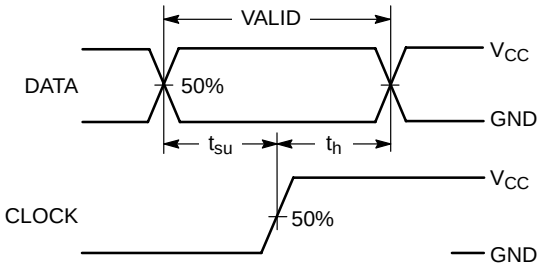
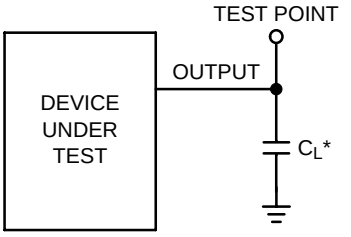


Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit

PIN1/PRODUCT ORIENTATION CARRIER TAPE

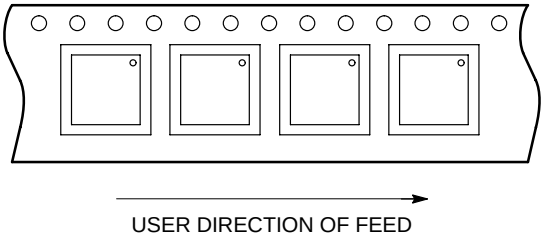
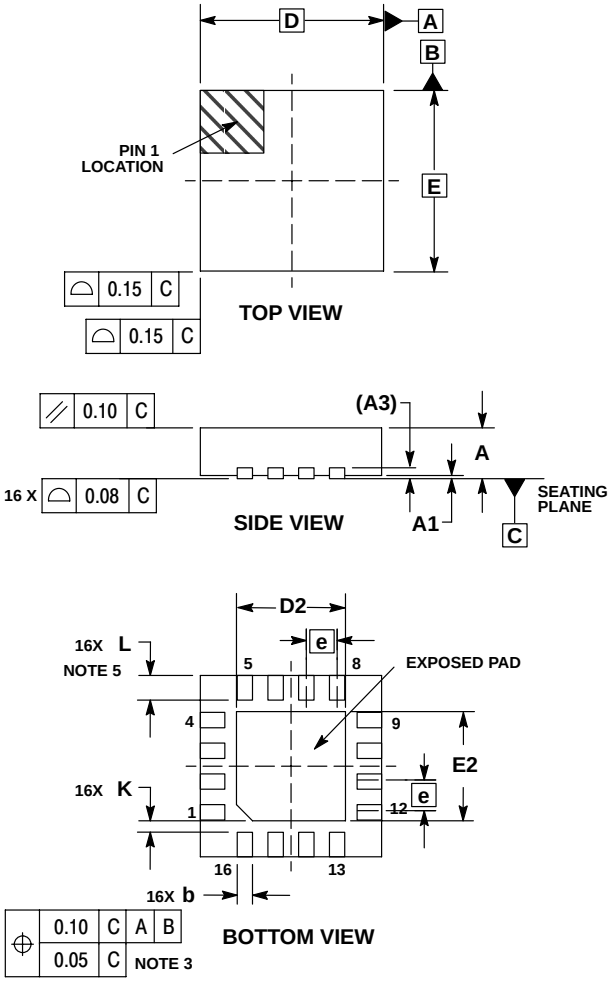


Figure 8.

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru