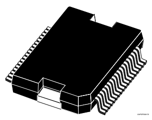
L9375TRLF

Eight channel valve driver

Datasheet - production data



PowerSO-36

Features

- Eight protected low-side drivers with diagnostics
  - Four 0.16 Ω (typ) low side outputs (Q1 - Q4)
  - Four 0.2 Ω (typ) PWM controlled outputs (Q5 - Q8)
- All outputs with 35 V (min) zener clamp
- Programmable output timer
- Clock monitor
- Integrated recirculation diodes (Q5-Q8 only)
- 16 bit serial peripheral interface (SPI), up to 5 MHz with diagnostics
- Battery compatible supply voltage
- Detailed load diagnostics
  - Over load protection
  - Open load (off-state)
  - Under current
  - Under voltage
  - Temperature warning and shutdown
  - Power or signal GND loss
  - Recirculation diode loss
  - Silent valve driver test

Description

The L9375TRLF is a SPI controlled octal channel low side driver with integrated recirculation diodes.

The output duty cycle (Q5 - Q8) can be programmed individually. It is possible to program two consecutive output duty cycles per channel as well as an individual duration time for each channel actuation (all channels).

Table 1. Device summary

Order code	Package	Packing
L9375TRLF	PowerSO-36 (slug down)	Tube

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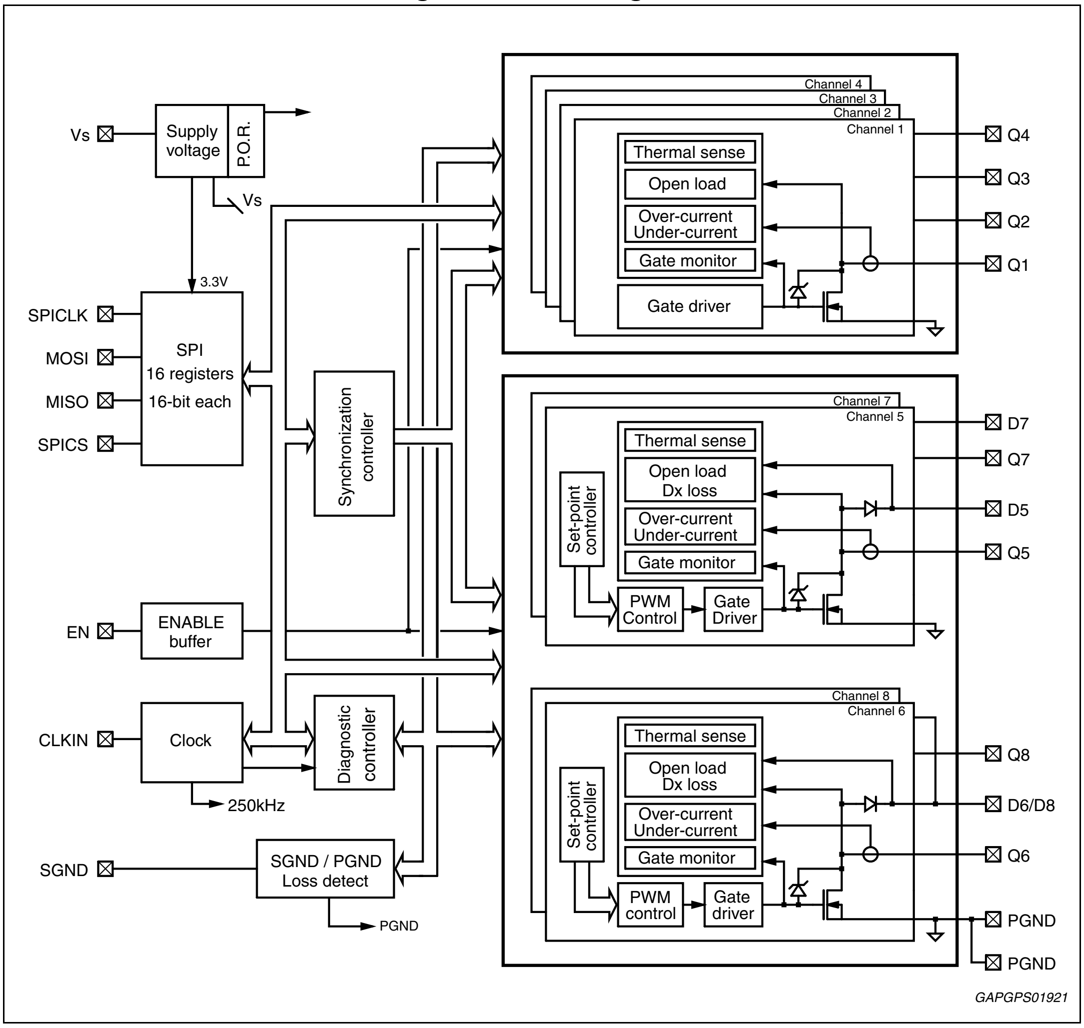
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

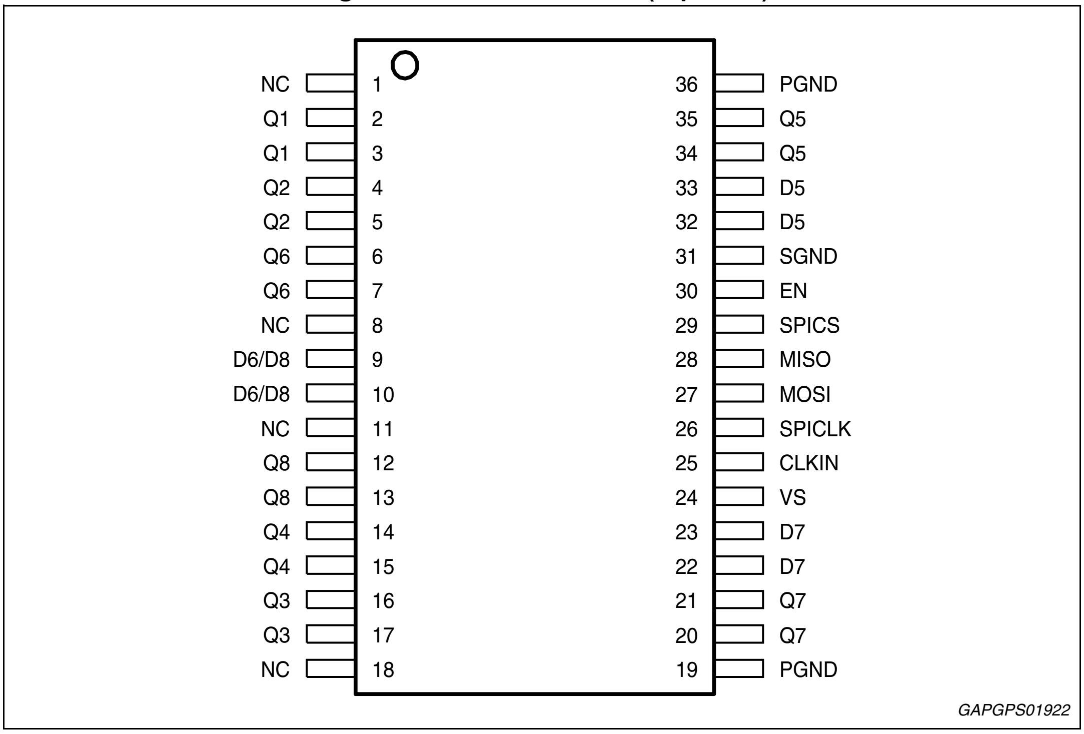


Table 2. Pins description

Pin #	Name	Description
1	N.C.	Not connected
2	Q1	Low side driver output 1
3	Q1	Low side driver output 1
4	Q2	Low side driver output 2
5	Q2	Low side driver output 2
6	Q6	Low side driver output 6
7	Q6	Low side driver output 6
8	N.C.	Not connected
9	D6/D8	Output 6 and 8 recirculation diode
10	D6/D8	Output 6 and 8 recirculation diode
11	N.C.	Not connected
12	Q8	Low side driver output 8
13	Q8	Low side driver output 8
14	Q4	Low side driver output 4
15	Q4	Low side driver output 4
16	Q3	Low side driver output 3

Table 2. Pins description (continued)

Pin #	Name	Description
17	Q3	Low side driver output 3
18	N.C.	Not connected
19	PGND	Power ground
20	Q7	Low side driver output 7
21	Q7	Low side driver output 7
22	D7	Output 7 recirculation diode
23	D7	Output 7 recirculation diode
24	VS	IC supply
25	CLKIN	Precision clock input
26	SPICLK	SPI communication clocK
27	MOSI	Master out slave in for SPI communication
28	MISO	Master in slave out for SPI communication
29	SPICS	SPI chip select
30	EN	Device Enable
31	SGND	Signal ground
32	D5	Output 5 recirculation diode
33	D5	Output 5 recirculation diode
34	Q5	Low side driver output 5
35	Q5	Low side driver output 5
36	PGND	Power ground

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_s	Supply voltage	-0.3	38	V
V_{Dx}	Recirculation diode voltage Continuous t<2 ms	 -0.3 -0.3	 35 38	 V V
V_{Qx}	Output Voltage	-0.3	Internally Clamped	V
V_{EN} V_{SPICLK} V_{SPICS} V_{MOSI} V_{MISO} V_{CLKIN}	Enable voltage SPI clock voltage SPI chip select voltage SPI MOSI voltage SPI MISO voltage SPI clock input voltage	-0.3	6	V
I_Q	Output current at reversal voltage		-2	A
I_{EN_CL} I_{SPICLK_CL} I_{SPICS_CL} I_{MOSI_CL} I_{CLKIN_CL}	Input clamping currents (static) Input clamping currents (dynamic)	- 3 -10	+ 3 +10	mA
T_{amb}	Ambient operating temperature	-40	+125	°C

Definition: Current flowing into the L9375TRLF are considered positive -> " + "
Current flowing out of the L9375TRLF are considered negative -> " - "

Warning: Transients beyond this limit will cause currents into ESD structures which must be limited externally to ±10 mA (maximum energy to be dissipated: 2 mJ).

3.2 ESD susceptibility

3.2.1 HBM

ESD susceptibility HBM according to EIA/JESD 22-A 114B:

Table 4. HBM

Pin	Condition	Min	Max	Unit
All pins	-	± 2	-	kV
Output pins D_X; Q_X;	All PGND and SGND pins are connected together.	± 4	-	kV

3.2.2 MM

ESD susceptibility according to EIA/JESD 22-A 115A:

Table 5. MM

Parameter	Condition	Min	Max	Unit
Machine model (MM)	All pins	± 250	-	V

3.3 Electrical characteristics

V_S = 5.2 to 20 V; -40 °C ≤ T_j1 ≤ 175 °C, unless other-wise specified.

Function is guaranteed until thermal shutdown threshold, T_{SD};

3.3.1 Supply current

Table 6. Supply current

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VS}	Supply current	V_s = 13.5 V @+175 °C @+25 °C @-40 °C	 4.0 - -	 - 7.5 -	 - - 10	mA
V_s	Supply voltage operating range	-	5.2	-	20	V

3.3.2 Output power stages

All output power stages consist of a MOSFET with accompanying protection/diagnostic circuitry. Outputs Q5 - Q8 have a recirculation diode as well for PWMming inductive loads.

Figure 3. Output power stages Q1-Q4

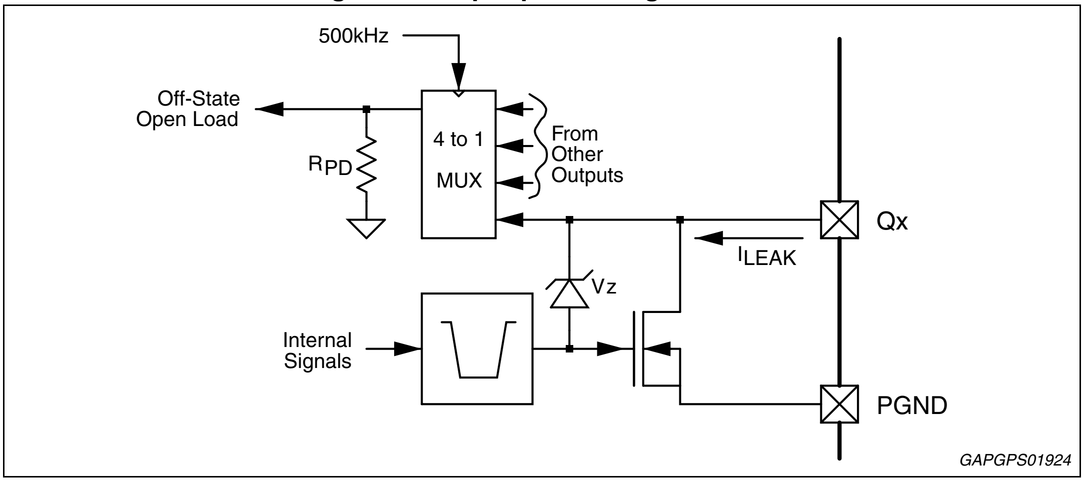
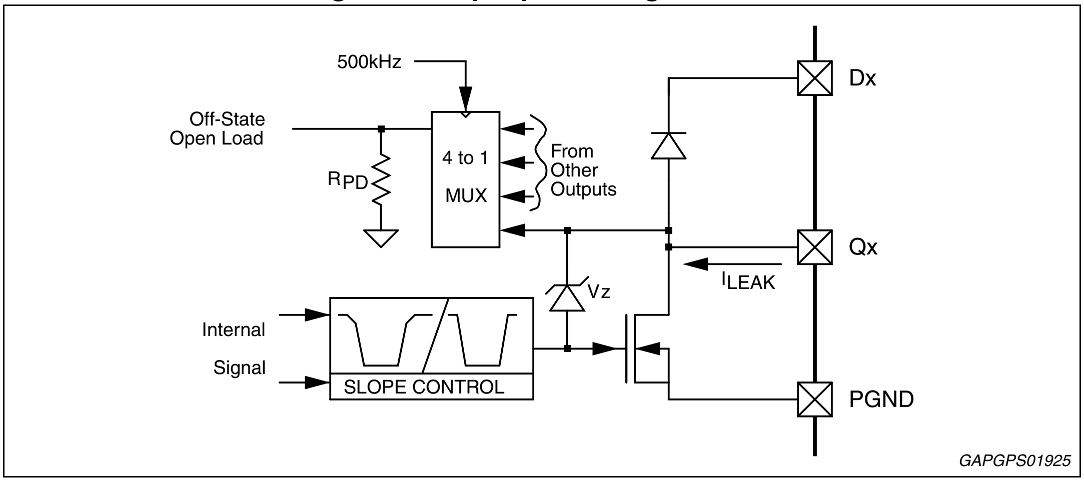


Table 7. Output power stages

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{ON}(Q_1\text{-}Q_4)$	Static drain-source on-resistance Q_1 - Q4	I_Q = 1 A (TC: 0.58 %/K; Typ @ RT)	60	160	390	mΩ
$R_{ON}(Q_5\text{-}Q_8)$	Static drain-source on-resistance Q_5 - Q_8	I_Q = 1 A (TC: 0.58 %/K; Typ @ RT)	100	200	520	mΩ
V_Z	Z-diode clamping voltage	I_Q = current limitation	35	-	40	V
R_{PD}	Output pull down resistor (multiplexed to 4 outputs sequentially)(1)	EN = 1	20	40	100	kΩ
I_{LEAK}	Output leakage current	V_Q = 20 V; EN = 0 V T_j = 140 °C T_j = 25 °C	-	-	3 1.5	µA µA

1. R_{PD} is sequentially connected to each output for 2 µs (8 µs period) for the purpose of detecting off-state open load. There are two R_{PDs} and two 4:1 multiplexers, one for outputs Q1 -Q4 and another for outputs Q5 - Q8.

Figure 4. Output power stages Q5-Q8



3.3.3 Recirculation diode

Table 8. Recirculation diode electrical characteristics (Q5-Q8)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{FD(5-8)}$	Recirculation diode forward voltage	I_{FD}< -3 A	0.5	0.75	1.75	V
R_{D5-8}	Resistor D_X-Pin to ground	V_Q< V_D < 18 V (Typ @ Tj = 25 °C)	100	240	650	kΩ
$I_{leak\_Dx\_0}$	Leakage current into Dx-Pin D5, D7, D6/D8	-	6	90	170	µA
I_{sub}	Dx substrate current	% of Recirculation current	-	-	2	%

3.3.4 Output timing characteristics

The DMOS outputs have controlled slopes to minimize EME. The Edge Shaping option is programmed via SPI (See *: Edge shaping (EDGE_SH):*). Edge shaping is optional for outputs Q5-Q8 only.

Figure 5. Output timing (Q1 - Q4)

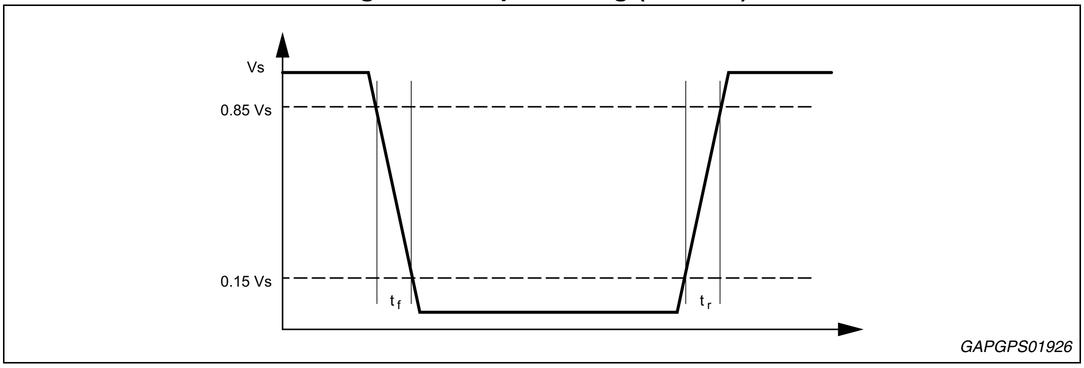
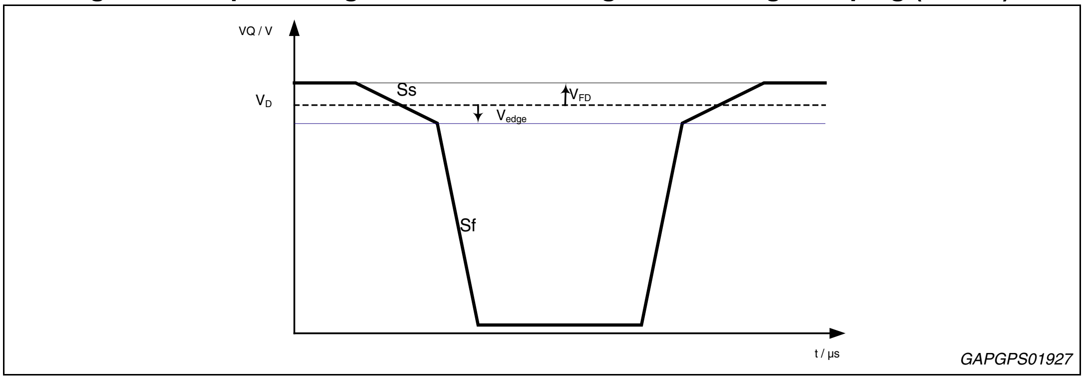


Table 9. Timing for outputs Q1 - Q4 (no edge shaping)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_r	Output slope rising edge (15 % to 85 %)	0.5 A < IQ < 1.5 A	4	8	12	V/µs
t_f	Output slope falling edge (85 % to 15 %)	0.5 A < IQ < 1.5 A	4	8	12	V/µs

Figure 6. Output timing characteristics diagram with edge shaping (Q5-Q8)l



Where:

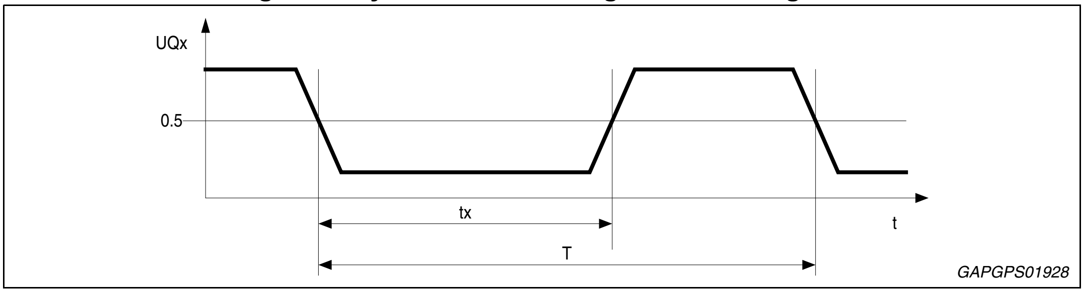
- V_D: Valve supply voltage
- V_{FD}: Forward voltage drop across the recirculation diode
- V_{EDGE}: Voltage Sf to Ss slope transition
- Ss: Slow slope
- Sf: Fast slope

Table 10. Output timing electrical characteristics (Q5-Q8)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{edge}	Edge shaping threshold	0.5 A < I_Q < 1.5 A 8 V< V_D < 20 V measured from V_D	-2.2		-1	V
Sf_Q_1-Q_4	Sf output on/off slope fast Q_1-Q_4	8 V< V_D < 20 V 0.5 A < I_{load} < 1.5 A resistive load 15 % to 85 %	3	10	17	V/µs
Ss_Q_1-Q_4	Ss output on/off slope slow Q_1-Q_4		2	4	6	V/µs
Sf_Q_5-Q_8	Sf output on/off slope fast Q_5-Q_8		6	13	20	V/µs
Ss_Q_5-Q_8	Ss output on/off slope slow Q_5-Q_8		2.5	5	7.5	V/µs

Symmetric switching of DMOS

Figure 7. Symmetric switching of DMOS diagram



A Symmetric switching is present to assure a reliable PWM at the output.

Table 11. Symmetric switching of DMOS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{sym1}	Symmetry 1 with edge shaping	|tx. dc x T| < 1.5 µs dc = {0..1} 0.5 A < I_Q < 1.5 A	0	-	1.5	µs
t_{sym2}	Symmetry 2 without edge shaping	|tx. dc x T| < 2.7 µs dc = {0..1} 0.5 A < I_Q < 1.5 A	0	-	2.7	µs

3.3.5 Output configuration Q1 - Q4

Table 12. Q3 / Q4 (current controller) electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{D(min)}$	Minimum duration		250	-	-	µs
$t_{D(res)}$	Duration resolution (per bit) Address 0 bit 9 = 0 Address 0 bit 9 = 1		-	250 500	-	µs
n	Number of bits		-	5	-	-
$t_{D(max)}$	Maximum duration Address 0 bit 9 = 0 Address 0 bit 9 = 1	$(2^5 - 1) \times 250\ \mu s$ $(2^5 - 1) \times 250\ \mu s$	-	-	7.75 15.5	ms

3.3.6 Output configuration Q5 - Q8

(refer to *Section 4.4: Set-point controller* for details)

Table 13. PWM output behavior characteristics (Q5 - Q8)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_Q_x	Output frequency	-	-2 %	4	+2 %	kHz
DC	Duty range	-	0	-	100	%
DC_{RES}	Duty resolution of f_A	-	-	0.2	-	%
N_{RES}	Number of bits for duty resolution	-	-	9	-	-
$t(n)_{RES}$	Resolution of duration Add. 0 bit D9 = 0 Add. 0 bit D9 = 1	1/f_A	-	250 500	-	µs µs
N_{Bit}	Number of bits for duration	-	-	5	-	-
$t(n)_{MAX}$	Max. duration Add. 0 bit D9 = 0 Add. 0 bit D9 = 1	$(2^5-1) \times 250\ \mu s$ $(2^5-1) \times 500\ \mu s$	-	-	7.75 15.5	ms ms

3.3.7 Logic inputs / outputs

Figure 8. Logic inputs

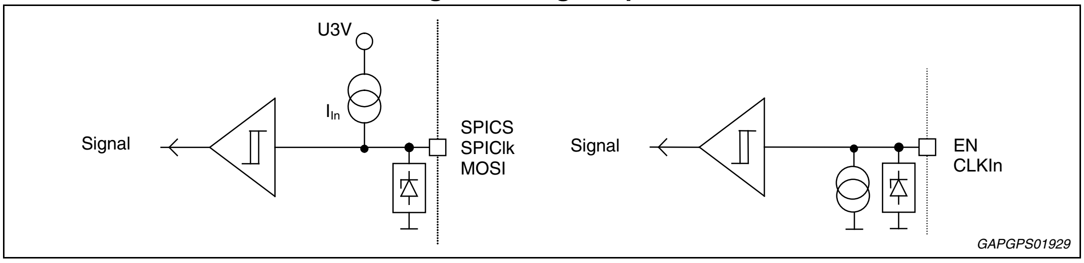


Table 14. Logic inputs electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{In_low}	Input threshold	-	-0.3	-	1.0	V
V_{In_high}	Input threshold	-	2.0	-	3.5	V
$V_{In\text{-}hys}$	Input threshold hysteresis	-	50	100	350	mV
$I_{P\text{-}U}$	Internal pull-up current source for SPICS, SPICLK, MOSI	$0V \le V_{In\text{-}xy} \le 2$ V	-12	-30	-60	µA
$I_{P\text{-}D}$	Internal pull-down current source for EN, CLKIN	$1V \le V_{In\text{-}xy} \le 3.45$ V	+12	+30	+60	µA
C_{in}	Input capacitance	designed but not tested	3.5	-	7.5	pF

3.3.8 Logic outputs (MISO)

Figure 9. Logic outputs (MISO) circuit

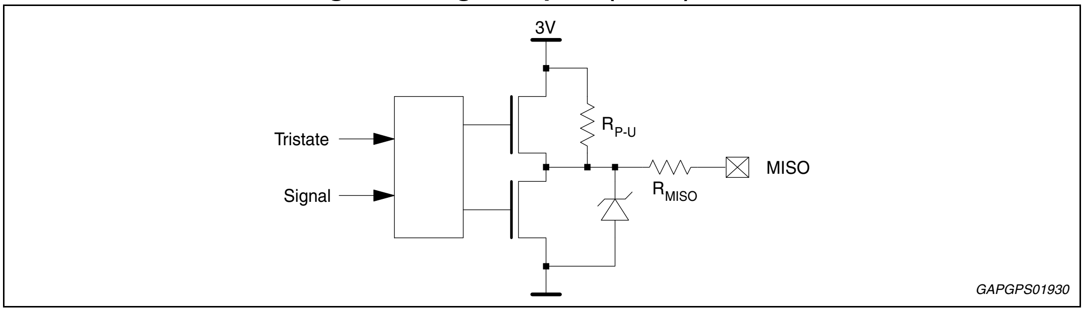


Table 15. Logic outputs (MISO) electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{MISO_L}	MISO low voltage	$I_{Out\text{-}xy} \le 25$ µA; $C_L \le 30$ pF	0	-	0.4	V
V_{MISO_H}	MISO high voltage	$I_{Out\text{-}xy} \le -25$ µA;	2.5	3.3	3.45	V
$R_{MISO\text{-}ON}$	MISO ON resistance	$R_{ON}+R_{MISO}$	40	100	400	Ω
$R_{P\text{-}U}$	MISO pull up resistor	SPICS = high → MISO in tristate mode	50	120	300	kΩ
C_{in}	Input capacitance	designed but not tested	3.5	-	7.5	pF

3.3.9 Output stage diagnostic functions

(refer to *Section 4.7: Diagnostics* for details)

Table 16. Diagnostic functions at output stage electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL}	Open load threshold	output off	0.3	0.33	0.39	x VS
I_{UC}	Undercurrent threshold	output on	50	100	140	mA
T_{SD}	Temperature shut down threshold(1)	-	180	200	225	°C
T_W	Temperature warning	-	160	180	200	°C
ΔT_{SD}	T_{SD} Hysteresis	T_{SD}	5	-	35	°C
$D_{x\ loss}$	D_x supply loss threshold and zener clamp	Output is clamping	32	-	39	V
I_{OC}	Overcurrent threshold	Qx switched off after t_{OC}	3	5	8	A
V_{G_ON}	Gate monitoring threshold	Internal node, not tested	5	-	-	V
V_{G_OFF}	Gate monitoring threshold	Max allowable I_{DS} See: *Gate monitoring*	-	-	15	mA

1. Monitoring is only active if the output is on.

3.3.10 General diagnostic functions

(refer to *Section 4.7: Diagnostics* for details)

Table 17. General diagnostic functions electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UV}	Under voltage threshold	(VS-pin)	3.0	-	5.2	V
V_{SG_L}	Signal GND loss threshold	-	0.2	0.4	0.6	V
V_{PG_L}	Power GND loss threshold	-	0.7	1.45	2.2	V
V_{PG_Lh}	Power GND loss hysteresis	-	-	1.0	-	V

Table 18. CLKIN-monitoring characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLKIN_H250}	CLKIN monitoring @ 250 kHz-mode set SPI bit	frequency too high	290	-	760	kHz
f_{CLKIN_L250}	CLKIN monitoring @ 250 kHz-mode set SPI bit	frequency too low	90	-	190	kHz
f_{CLKIN_H1M}	CLKIN monitoring @ 1 MHz-mode set SPI bit	frequency too high	1.16	-	3.04	MHz
f_{CLKIN_L1M}	CLKIN monitoring @ 1 MHz-mode set SPI bit	frequency too low	0.36	-	0.76	MHz
f_{CLKIN_OK}	CLKIN monitoring clear SPI bit	CLKIN frequency ok	-	250 1	-	kHz MHz

3.3.11 Filtering times

Table 19. Failure filtering times characteristics

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
t_{OL}	Open load filtering time	outputs off	20	44	70	µs
t_{UC}	Under current filtering time	-	10	20	40	µs
t_{OC}	Over current switch-off delay time	-	10	20	40	µs
t_{SD}	Thermal shutdown delay time	-	10	40	80	µs
t_{TW}	Thermal Warning filtering time	-	10	20	40	µs
t_{DX_L}	Dx loss filtering time	-	1	2	5	µs
t_{PGND_L}	Power GND loss filtering time	-	10	20	40	µs
t_{SGND_L}	Signal GND loss filtering time	-	10	20	40	µs
$t_{\_EN\_F}$	EN filtering time[2]	-	1.5	2	3	µs
t_{CLK_F}	CLKIN-failure detection time	-	140	200	310	µs

1. All parameters based on valid CLKIN (250 kHz/1 MHz) signal.
2. Digital filter only for falling edges and analog filter for both edges.

Table 20. SVDT test timing (refer to *4.7.11: Silent valve driver test (SVDT)*)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_x	Minimum passing test time	SVDT Enabled $I\_Qx < I_{UC}$	90	100	110	µs
t_y	Maximum failing test time, Outputs Q1 - Q7 only	SVDT Enabled $I\_Qx < I_{UC}$	900	1000	1100	µs
t_y	Maximum failing test time Output Q8 Only	SVDT Enabled $I\_Q8 < I_{UC}$	675	750	825	µs

3.3.12 Internal oscillator

Table 21. Internal oscillator electrical characteristics

Symbol	Parameter	Condition	min	typ	max	Unit
f_{osc}	Oscillator frequency	-	1.4	2.0	2.6	MHz

3.3.13 SPI timing characteristics SPICLK, MISO, MOSI, SPICS

Figure 10. SPI timing characteristics SPICLK, MISO, MOSI, SPICS

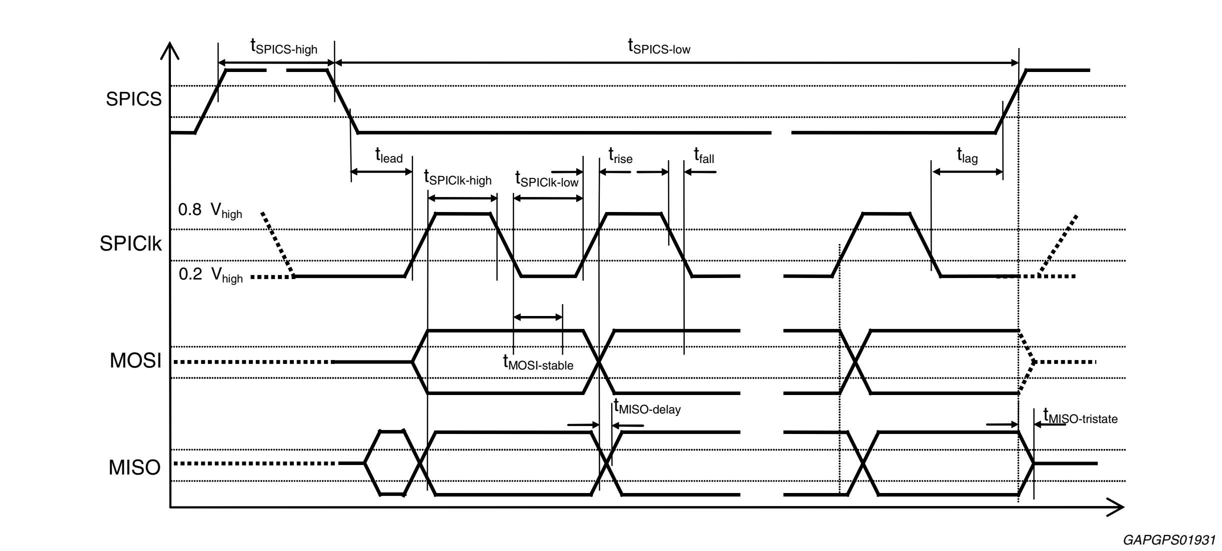


Table 22. SPI timing characteristics

No.	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPICLK}	SPICLK frequency	$C_{load} \leq 30$ pF	0	-	5	MHz
$t_{SPICLK-high}$, $t_{SPICLK-low}$	SPICLK high time / low time	-	68	-	-	ns
t_{lead}	SPICS -> SPICLK delay	-	50	-	-	ns
t_{lag}	SPICLK -> SPICS delay	-	60	-	-	ns
$t_{MOSI-stable}$	MOSI stable	-	68	-	-	ns
t_{rise}/t_{fall}	SPICLK, MOSI rise time / fall time	$C_{load} \leq 50$ pF $C_{load} \leq 100$ pF $C_{load} \leq 150$ pF	0 0 0	-	14 23 32	ns
$t_{MISO-delay}$	SPICLK -> MISO delay	$C_{load} \leq 150$ pF	-	-	65	ns
$t_{MISO-rise}$, $t_{MISO-fall}$	MISO rise time / fall time(1)	$C_{load} \leq 15$ pF $C_{load} \leq 50$ pF $C_{load} \leq 65$ pF	0.8 2.5 3.5	2 7 9	7 21 28	ns ns ns
$t_{SPICS-high}$	SPICS high time / low time	$C_{load} \leq 150$ pF	150	-	-	ns
t_{MISO_tri}	MISO tri-state	$C_{load} \leq 150$ pF	-	-	100	ns

1. guaranteed by design

Note: The MISO pin is tri-stated with a weak pull-up when SPICS is high.

4 Circuit description

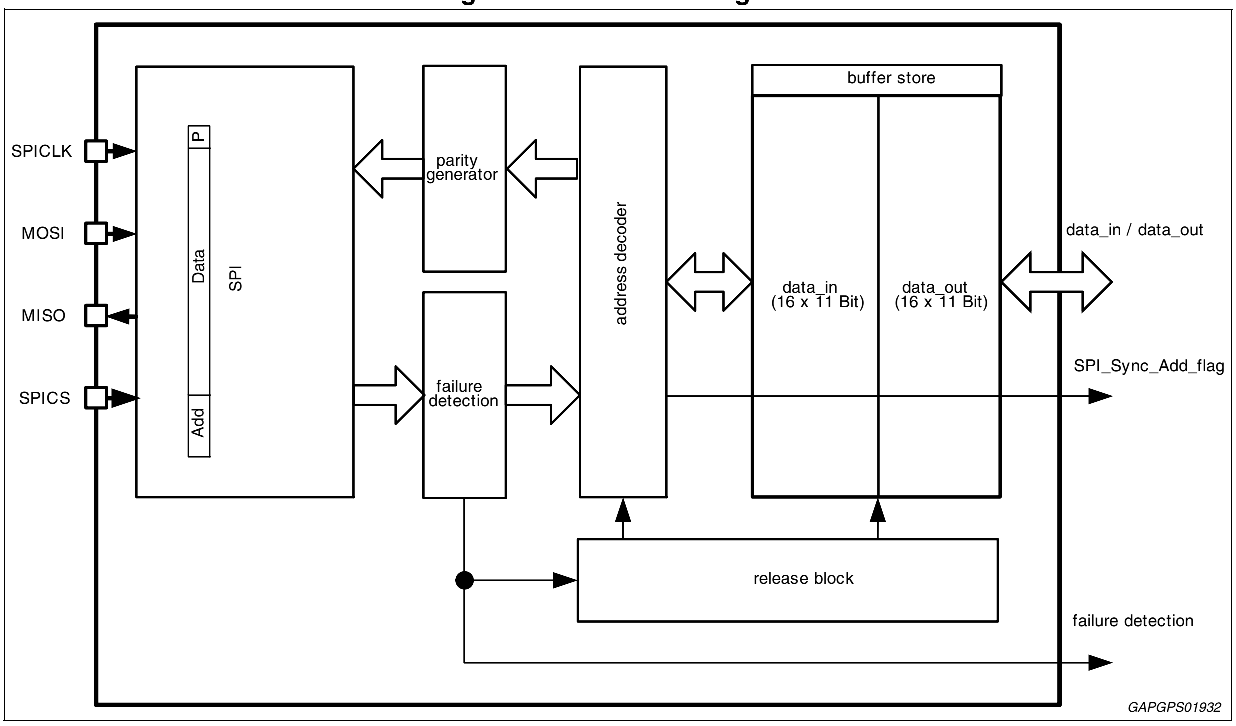
The L9375TRLF is an eight channel low side driver intended for ABS applications. The device communicates entirely by individual SPI commands. All of the outputs can be switched on or off for defined periods with four of the outputs having PWM capability. It is possible to program two consecutive on-time durations or PWM duty cycles at one time.

All outputs have high level diagnostic capabilities. These include off state open load, under current, shorted load, gate monitoring, thermal warning, and thermal shutdown flags. Higher level diagnostics include a Silent-Valve-Detection-Test (SVDT) to verify load and driver integrity as well as detection and reporting of a missing recirculation diode (Q5-Q8), Ground loss, Clock failure, and SPI synchronization failure.

4.1 SPI serial peripheral interface

The L9375TRLF SPI is a fully bidirectional serial interface configured as a SLAVE for communication between a µC (the MASTER) and the L9375TRLF. All of the data management is handled in 16 sets of SPI registers of 16 bits each. There are 16 input or command registers and 8 status registers. All output control including on-time and PWM / switching timing is realized internally. The control parameters (Duty Cycle and Duration) are programmed via serial communication. The 16 status registers (only 8 are used) provide a high level of diagnostic capability from output status to internal control parameter confirmation.

Figure 11. SPI block diagram



Messages from the master (µC) to the L9375TRLF are sent over the MOSI (Master out Slave In) pin. Messages from the L9375TRLF to the master will be sent over the MISO (Master in Slave Out) pin.

The master starts the communication with a '1' → '0' transition on the SPICS pin. After t_{LEAD}, (*Table 22*) the master sends a clock signal to the SPICLK and data to the MOSI pin. The SPICLK pin must be low at the falling edge of SPICS and remain low for t_{LEAD} for correct communication to occur. The SPICS pin must rise after every 16 bits sent.

The MISO pin is tri-stated with a high ohmic pull-up resistor when the SPI chip select (SPICS) pin is held high.

The SPI has the following features:

- 4 wire SPI (SPICS, SPICLK, MOSI, MISO)
- Word length of 16-Bits (0..15)
- 4 address and 11 data bits and one parity bit
- 16 receive-buffers (11 bit wide)
- 8 send-buffers (11 bit wide)

4.1.1 General protocol

The protocol has the following structure:

- A parity-bit at the LSB and eleven data bits (bits 1 to 11).
- The four address bits are at the highest position at the transfer (bits 12 - 15).
- SPI communication begins with the MSB.
- High level = '1'
- Low level = '0'

General SPI protocol

MSB															LSB
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

- Ax: address bits
- Dx: data bits
- P: parity bit

A message from the L9375TRLF to the master µC (MISO) contains 4 address bits. These bits are not a copy of the received address from the previous transmission, but are addresses that were decoded from the address decoder. This is done so that the master (µC) has the ability to discern the integrity of the L9375TRLF address decoder.

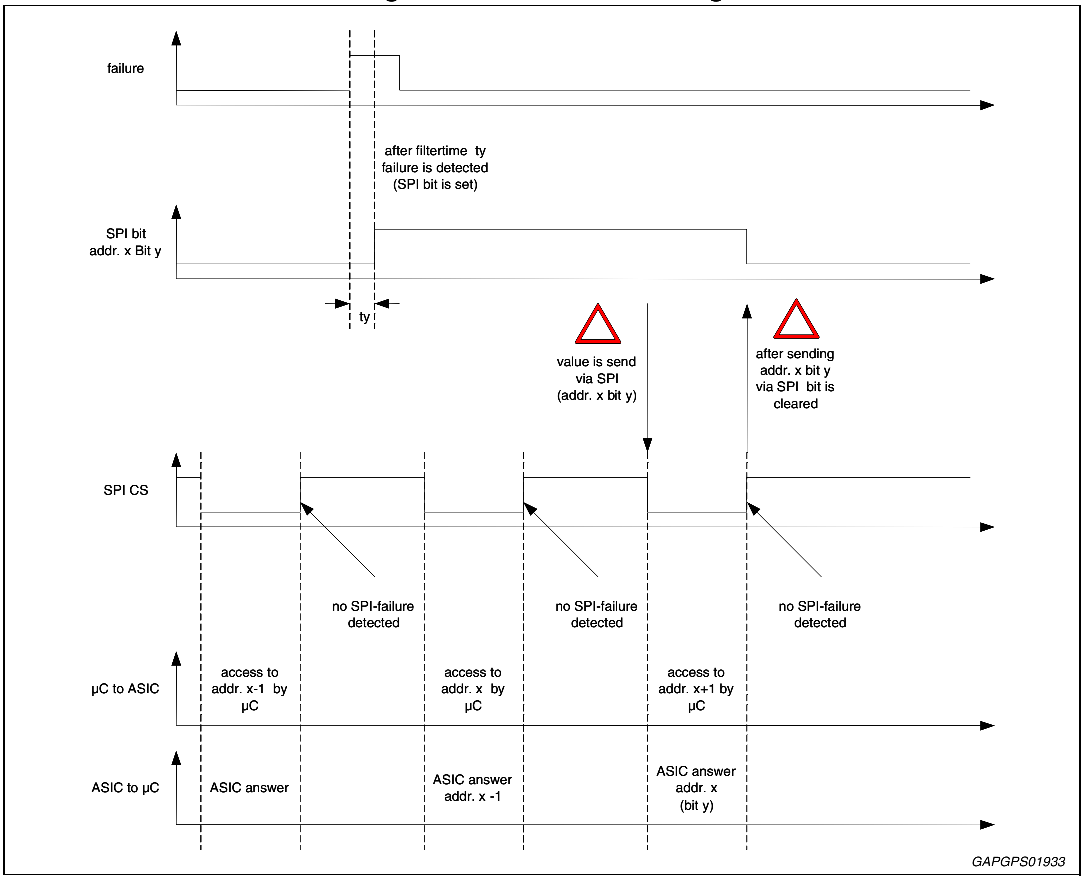
Every time an error bit in one of the SPI registers is set by the L9375TRLF it will remain set until the corresponding register has been read out via SPI. Once a status register has been read the corresponding register will be reset upon the rising edge of SPICS.

Every SPI communication writes data into a register (read only not possible). Every SPI response is associated with the address of the message sent one communication before.

4.1.2 SPI failure detection

SPI communications sent to the L9375TRLF that contain errors are ignored. This inaction includes both the commands given and the data retrieved. That is, commands are ignored and the initial state of the output is not changed. Also data registers referenced by the erroneous SPI communication will not be reset.

Figure 12. SPI error handling



Three functions are monitored to discern a correct SPI communication from the master:

1. Correct number of Clock pulses in SPICLK per transfer.
   During each SPICS-low-phase the L9375TRLF counts the number of positive edges of SPICLK. If this number is unequal to 16 a SPICLK-error is detected.
2. Parity check (odd)
   The L9375TRLF detects a parity error if the number of ‘1’s within a transfer is even.
3. Data-failure monitoring:
   This bit is set if the master writes inappropriate data to any of the config-registers (2/14/15).

4.1.3 Data transfer

Upon the completion of each 16 bit SPI command (rising edge of SPICS), data is transferred from the SPI block to the appropriate internal registers. Some internal SPI registers are reset (such as fault bits) once they are accessed.

4.1.4 Address decoder

The address decoder routes incoming data into the appropriate receive buffer and sets up the appropriate send buffer register to transmit information back to the master (MISO) for the subsequent SPI communication.

4.1.5 Parity generator

The parity generator completes the output messages with a parity bit. The number of ‘1’s within an output-transfer has to be odd. Parity is verified prior to the SPICS going high.

4.1.6 Initial MISO information

After initial power on, the first SPI-answer from the L9375TRLF reflects the Chip-ID information. Typically, the information will appear as follows:

A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
1	0	1	0	0	0	1	x	x	x	x	x	x	x	x	x

This information is unique to this device and reflects specific device information relevant only to ST.

4.1.7 Register map

This is a brief reference to the register locations within the L9375TRLF (for more detailed information please see Section *5: Programmers guide*).

Command buffer (data in)

Table 23. Command buffer (data_in)

Address$_{(HEX)}$	Content	Buffer name
0	Sync-trigger, Reset, and Sync values	SYNC_REG
1	STW min and max values	STW_V
2	Configuration register	CONFIG
3	Fast Switch ON gate commands	FSON
4	Duration Registers for Q1 /Q2	Duration Q1/Q2
5	Duration Registers for Q5 /Q6	Duration Q5/Q6
6	Duty cycle 1 Q5	DUTY1_Q5
7	Duty cycle 2 Q5	DUTY2_Q5
8	Duty cycle 1 Q6	DUTY1_Q6
9	Duty cycle 2 Q6	DUTY2_Q6
10	Duty cycle 1 Q7	DUTY1_Q7
11	Duty cycle 2 Q7	DUTY2_Q7
12	Duty cycle 1 Q8	DUTY1_Q8
13	Duty cycle 2 Q8	DUTY2_Q8
14	Duration Registers for Q7 /Q8	Duration Q7/Q8
15	Duration Registers for Q3 /Q4	Duration Q3/Q4

Status buffer (data out)

Table 24. Status buffer (data_out)

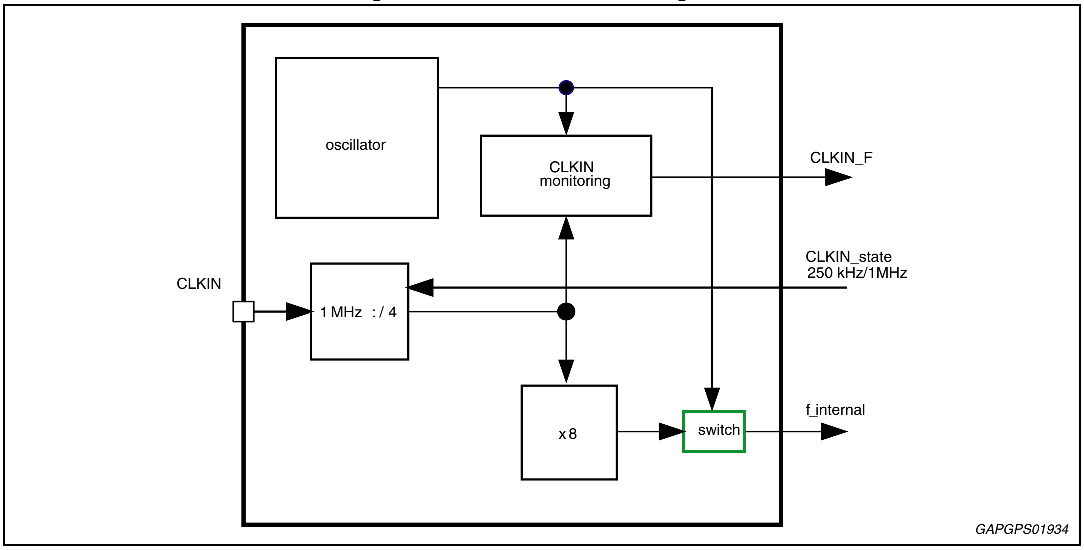
Address$_{(HEX)}$	Content	Buffer name
0	General status	G_STATUS
1	Q1 Output Status Register	STATUS_Q1
2	Q2 Output Status Register	STATUS_Q2
3	Q5 Output Status Register	STATUS_Q5
4	Q6 Output Status Register	STATUS_Q6
5	Q3 Output Status Register	STATUS_Q3
6	Q4 Output Status Register	STATUS_Q4
7	Q7 Output Status Register	STATUS_Q7
8	Q8 Output Status Register	STATUS_Q8
9	Reserved → data ‚000 0000 0000‘	RESERVED
10	Reserved → data ‚000 0000 0000‘	RESERVED
11	Reserved → data ‚000 0000 0000‘	RESERVED
12	Reserved → data ‚000 0000 0000‘	RESERVED
13	Reserved → data ‚000 0000 0000‘	RESERVED
14	Reserved → data ‚000 0000 0000‘	RESERVED
15	Reserved → data ‚000 0000 0000‘	RESERVED

A more detailed explanation about the register settings can be found in *Section 5: Programmers guide*.

4.2 Clock

The clock controller contains a CLKIN-monitoring function to validate the CLKIN frequency, a clock multiplier to produce an internal 2 MHz clock, and an internal oscillator for monitoring purposes and backup.

Figure 13. Clock block diagram



4.2.1 Clock multiplier

The Clock Multiplier provides a steady 2 MHz signal (f_{CLK}) for the internal logic based on the CLKIN signal. The multiplier factor is determined by setting the CLKIN_S bits in the SPI Command register *Configuration register (address 2)*. It is possible to have the wrong CLKIN_S bits set for a specific CLKIN frequency. When this occurs a CLKIN failure (CLKIN_F) is registered.

4.2.2 Internal oscillator

The 2 MHz internal oscillator ($f_{osc,}$ *Table 21*) provides a comparison signal used to validate the incoming CLKIN signal. If the CLKIN signal is determined to be out of range then the internal oscillator is used to provide clock signals internal to the L9375TRLF. The internal oscillator does not have the accuracy of a proper CLKIN signal. Therefore the diagnostic filter times will reflect the accuracy of this clock for that case.

4.2.3 CLKIN signal monitoring

The CLKIN signal is an external 250 kHz or 1 MHz signal from the µC to the L9375TRLF. This signal is monitored to be within a specified range ($f_{CLKIN\_L} < f_{CLKIN} < f_{CLKIN\_H}$, *Table 18*). If the value is out of range, then the CLKIN_F (CLKIN failure) bit is set to ‘1’. If a CLKIN failure (f_{CLK} out of range) is detected, the outputs are disabled and the internal 2 MHz oscillator is used as the clock for the internal logic.

Table 25. Clock validation

CLKIN	CLKIN_S 250 kHz / 1 MHz	f_{CLK}	CLKIN_F
250 kHz	250 kHz	2 MHz	0 (no failure)
1 MHz	1 MHz	2 MHz	0 (no failure)
250 kHz	1 MHz	1 MHz	1 (failure)
1 MHz	250 kHz	8 MHz	1 (failure)

4.3 Synchronization controller

Due to natural SPI communication task time jitter, proper actuation of the outputs requires some level of synchronization. The Synchronization Controller provides for synchronized output actuation eliminating SPI task time jitter issues.

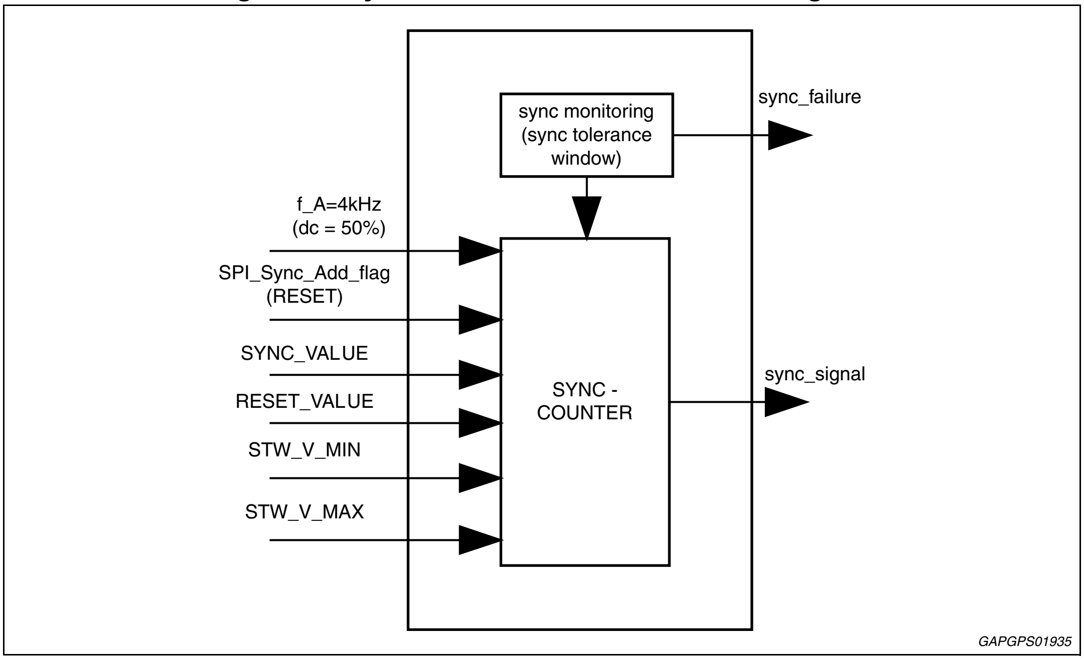
This function forces the outputs to change to their commanded state at a specified point in time outside of the SPI communication window. This also ensures a more stable SPI communication by minimizing ground fluctuation due to output switching during periods of SPI communications. This delay between the SPI commands and the output actuation is programmed by setting the RESET_VALUE and SYNC_VALUE parameters located in the *Section 5.1.1: Sync + Sync-trigger register (address 0)*.

4.3.1 Output synchronization

The RESET_VALUE time value is determined by using the typical time between SPI cycles. When programmed properly, the SPI communications occur at or around the RESET_VALUE timing. The Sync Tolerance Window (STW) is an interval of time between RESET_VALUE times where accessing the Sync (*Section 5.1.1: Sync + Sync-trigger* register (address 0)) during this interval generates a sync failure (SYNC_F). This window is defined by the parameters STW_V_MIN and STW_V_MAX.

The SYNC_VALUE is a programmed delay after the RESET_VALUE when the output transitions occur. This delay is typically set as half of the RESET_VALUE. This sets the output transitions furthest from each SPI cycle and during the STW.

Figure 14. Synchronization controller block diagram



Inputs

The synchronization controller receives the following input signals:

– f_A = 4 kHz for internal clocking.
– SYNC_TRIG =”1” initiates the synchronization timing with that SPI event.
– SPI synchronization values (SYNC_VALUE, RESET_VALUE, STW_V_MIN; STW_V_MAX) provide the parameters that allow for output synchronization.

Outputs

The synchronization controller provides the following output signals:

– The STW signal is used in conjunction with accessing address 0 to notify the master that the SPI cycles are within the programmed exclusionary window (SYNC_F=1).
– The SYNC_SIG initiates the actuation of the new output commands.

The synchronization counter increases its value with every period of f_A. When the value of the counter equals the SYNC_VALUE a synchronization signal (SYNC_SIG) is generated (SYNC_SIG=’1’).

The synchronization counter continually counts to the RESET_VALUE and resets unless a SYNC_TRIG command is sent. If a SYNC_TRIG command is sent then the counter resets immediately. Upon resetting the SYNC_TRIG and STW signals are reset (SYNC_SIG = STW =’0’).

Normal sequence

When stepping through a normal sequence of events the following occurs:

– At a SYNC_TRIG (SYNC_TRIG='1') command the synchronization counter, STW and SYNC_SIG flags are reset (STW='0', SYNC_SIG='0')
– The counter counts up at a rate defined by f_A (=4kHz).
– When the counter value reaches STW_V_MIN the STW flag is set (STW='1')
– When the counter value reaches SYNC_VALUE the SYNC_SIG flag is set (SYNC_SIG='1') which activates the most recent output commands.
– When the counter value reaches the STW_V_MAX value the STW flag is reset (STW='0')
– When the counter value 4 MSBs are equal to the RESET_VALUE the counter is reset and the output signal sync_signal is reset (SYNC_SIG='0')

Disallowed programming states

Erroneous programming results in the STW flag being set '1'

– If the STW_V_MIN value is higher than or equal to STW_V_MAX value the STW flag is set (STW = 1)
– If the STW_V_MAX value is higher or equal to the RESET_VALUE value the STW flag is set (STW = 1)

Synchronization failure

Sync failure detects a timing error in the output command synchronization. The master µC programs a timing window (STW) where accessing to the Status Register address 0 is not allowed.If there is an access to the Status Register address 0 when the STW flag is set then a sync-failure is generated (SYNC_F = 1). Also, a SYNC_F will be detected if there is no SPI traffic at all between two SYNC_SIG events. This status will be read out on the subsequent SPI transfer.

Without a SYNC_SIG or at sync-failure there is no effect for the actuation and set points.

Synchronization controller programming

It is necessary to write into two registers (Command Register addresses 0 and 1, *Section 5.1.1* and *5.1.2*) to program the Synchronization Controller. The SYNC_VALUE, the RESET_VALUE and the SYNC_TRIG values are programmed through address 0. The SYNC_TRIG is written to once to initialize the counter. Once initialized the SYNC_TRIG bit is reset by the controller. For subsequent SPI transfers the SYNC_TRIG bit should not be set to avoid re-initializing the sync counter. There is no influence on the sync counter if the SYNC_TRIG is not set. Occasionally, the sync counter may need re-initializing depending on the timing between the RESET_VALUE and the µC loop time. The RESET_VALUE is incremented by 1ms intervals. The SYNC_VALUE is incremented by 250 µs intervals.

The STW_V_MIN and STW_V_MAX values are programmed via register 1 (*Section 5.1.2*). Their interval length is dependant on the RESET_VALUE MSB (address '0', bit D9):

Table 26. Sync. tolerance window interval length

RESET_VALUE (add.0, bit D9)	RESET_VALUE duration	Sync tolerance window interval
0	<8ms	250 µs/bit
1	$\geq$8ms	500 µs/bit

Example

Example for a 5 ms cycle time, 2.5 ms SYNC_VALUE-, STW of +1.75 ms/-1.25 ms:

- Cycle time:
- For programming the cycle time the master has to write the RESET_VALUE (4 bit) via SPI. One bit has the resolution of 4/f_A = 1 ms.
- RESET_VALUE: 5 ms / 1 ms = 5 → $0101_{(2)}$
- SYNC_VALUE:
- For programming the sync-signal the master has to write the SYNC_VALUE (6 bit). The LSB has the resolution of 250 µs.
- SYNC_VALUE: 2.5 ms / 250 µs = 10 → 00 $1010_{(2)}$
- Sync tolerance window:
- For programming the STW the master must write min and max values (2 x 5 bit).

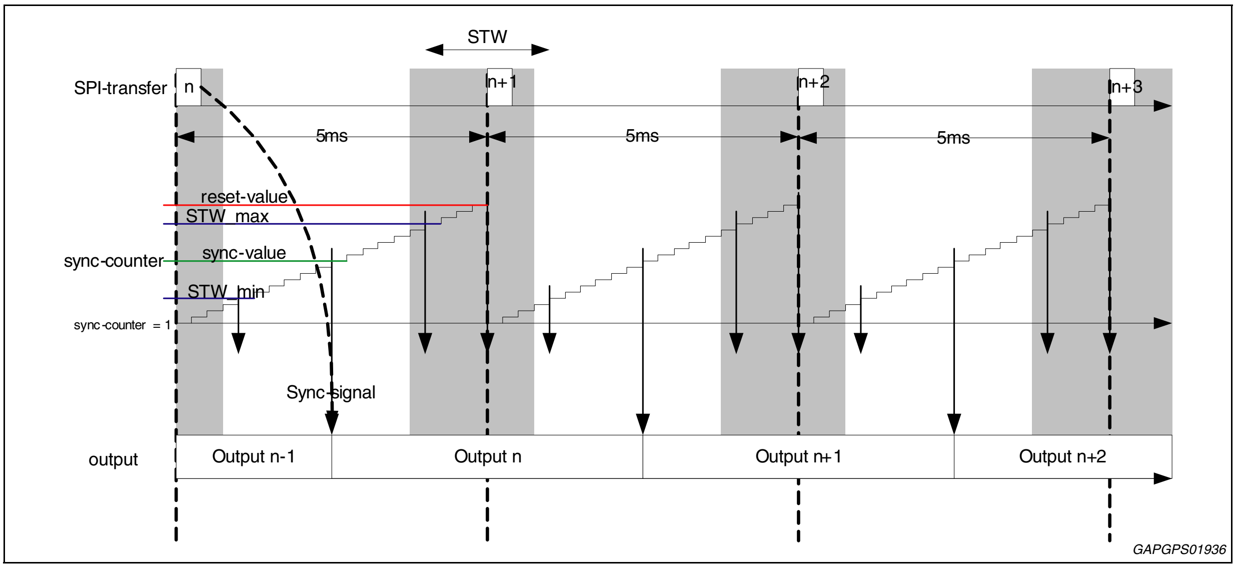
  STW_V_MIN: 0.75 ms

  STW_V_MAX: 3.75 ms

  STW_V_MIN: 0.75 ms / 250 µs + 1 = 4 → 0 $0100_{(2)}$

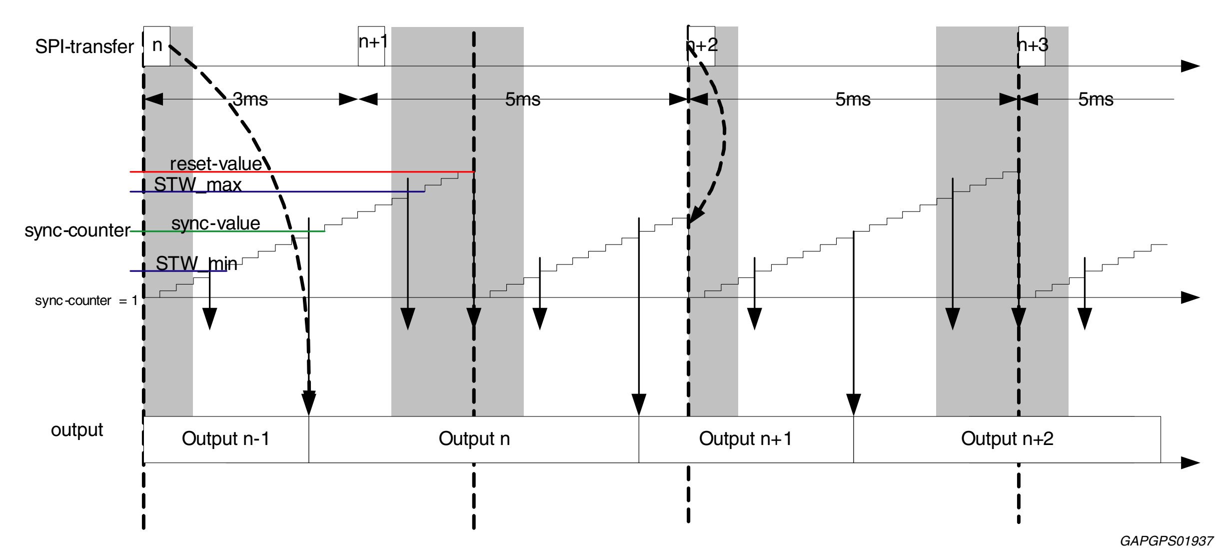
  STW_V_MAX: 3.75 ms / 250 µs + 1 = 16 → 1 $0000_{(2)}$

Figure 15. Normal mode



SPI transfer means transfer of all send and receive registers (0 through 15).

Figure 16. Sync-failure + re-synchronization

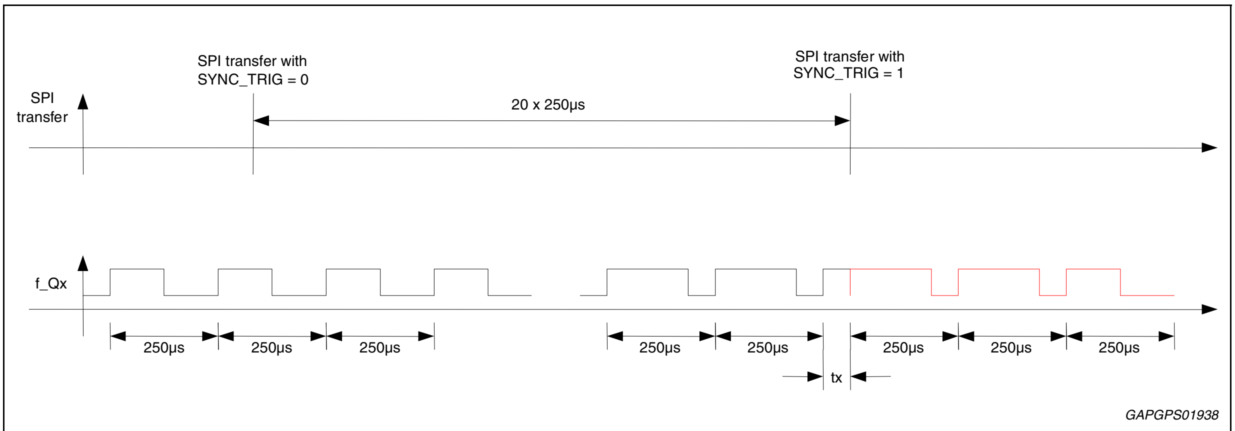


Re-synchronizing

The master sets the SYNC_TRIG bit to '1' (*Section 5.1.1*) to re-initialize the sync counter. This re-synchronizes the L9375TRLF synchronization controller to the master. When this bit is set three counters are reset: the PWM counter (output frequency and duty cycle), the synchronization counter and the duration counter. The SYNC_TRIG bit is reset (set to '0') by the L9375TRLF upon re-synchronization.

Figure 17 shows the behavior of the output when the synchronization is done. The time tx is anything lower than 250 µs.

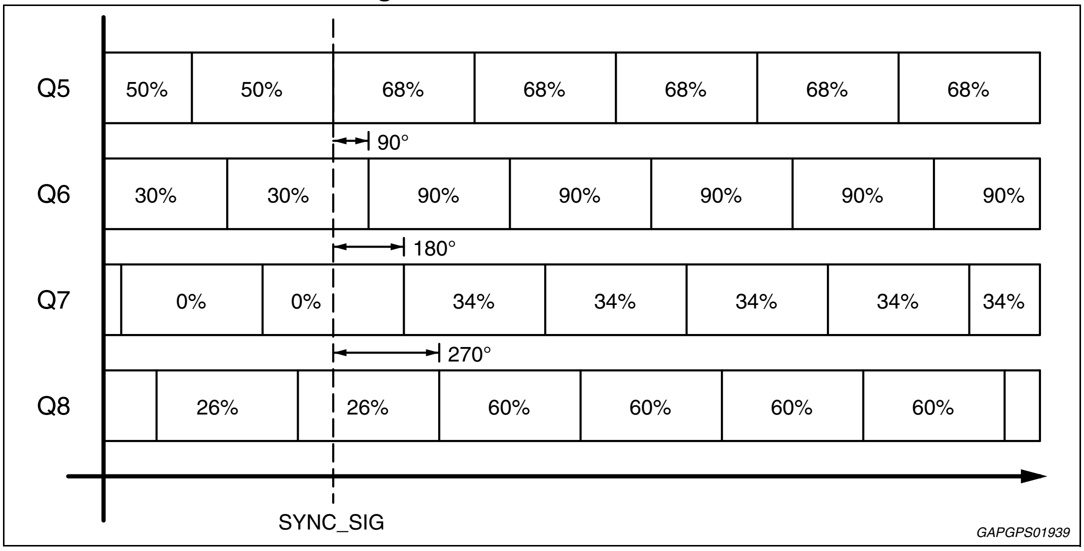
Figure 17. Behavior of the output when the synchronization is done



4.3.2 Time shift between output actuation (Q5-Q8 only)

The actuations of the outputs are time shifted by 90° (typ 62.5 µs) to offset their effect on the supply during switching. This balances the incremental switching current and reduces the EME generated by the switching of these channels. The new duty cycle or target current also becomes valid with this 90 degree time shift after the SYNC_SIG.

Figure 18. Channels time shift

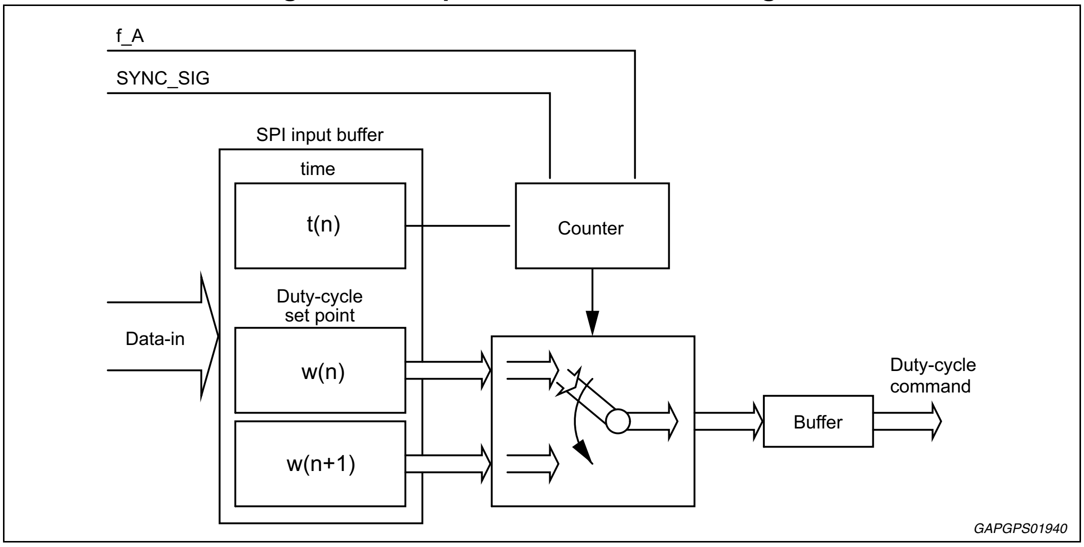


4.4 Set-point controller

The set point controller commands an on time duration (all outputs) and a PWM duty cycle (Q5-Q8 only) based on a duration command and duty cycle values from the SPI command registers for each output.

For outputs Q5 through Q8 this circuit is designed to generate two different PWM duty cycle values for each output per SPI cycle. This translates to a duty cycle [w(n)] for a duration [t(n)] and then a second duty cycle [w(n+1)] until otherwise commanded for each output per SPI cycle.

Figure 19. Set-point controller block diagram



The set point controller receives the following input information:

– Synchronization-signal (SYNC_SIG)
– Frequency of the PWM-generator (f_A; duty 50%)
– Set Point 1 (Duty cycle) = w(n) (9 bits)
– Set Point 2 (Duty cycle) = w(n+1) (9 bits)
– Duration (duration of Duty cycle = t(n) (5 bits)

The Duty cycle set point value is the only output signal.

The timer commands the change between w(n) and w(n+1) to the Duty cycle set point according to the programmed timing value t(n). If the value of the counter is lower than t(n) the Duty Cycle set point is set to w(n). If the value is equal or higher the Duty Cycle set point is set to w(n+1).

Table 27. Example of PWM duration timing, t(n)

Duration value (5 Bit)	Add. 0, bit D9	on-time (ms)
$00000_{(2)}$	X	0 ms (off)
$11111_{(2)}$	0	7.75 ms
$01101_{(2)}$	0	3.25 ms
$11111_{(2)}$	1	15.5 ms
$01101_{(2)}$	1	6.5 ms

Note that the RESET_VALUE MSB (bit 9 of address 0) affects the timer duration. With the MSB set the timer values double. This means if the SPI cycle time is equal or higher than 8 ms (>$100_{(H)}$) the resolution of the duration t(n) is 500 µs per LSB instead of 250 µs.

Table 28. Timer t(n) resolution versus RESET_VALUE MSB

RESET_VALUE (add.0, bit D9)	RESET_VALUE duration	Resolution of timer duration
0	<8 ms	250 µs
1	≥8 ms	500 µs

All buffers and the timer counter are reset by:

– A CLKIN failure detection (CLKIN_F = ‘1’)
– A re-synchronization command (SYNC_TRIG = ‘1’)

The Q5 - Q8 PWM value range (externally programmed):

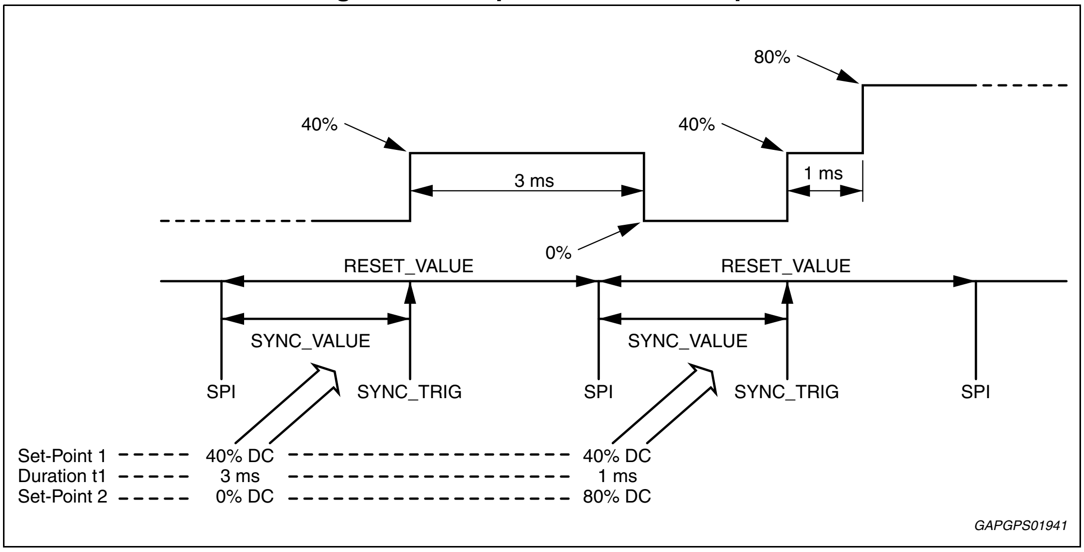
w(n): 9 Bit
w(n+1): 9 Bit
t(n): 5 Bit

Example of set-point control (Q5 - Q8 only)

Below is an example of programming two sets of Set-Points sequentially for outputs Q5 through Q8. After programming the parameters that govern the synchronization (RESET_VALUE, SYNC_VALUE and the SWT values) the parameters Set-Point 1 (DUTY1), Set-Point 2 (DUTY2) and duration t1 (D_Qx) are programmed (for programming instructions see *Section 5.1.5: Duration registers (address 4, 5, 14, and 15)*).

Generically, after the SYNC_TRIG the Set-Point 1 is valid for t1 ms. After t1 ms the set-point controller switches to Set-Point 2 until the next SYNC_TRIG event.

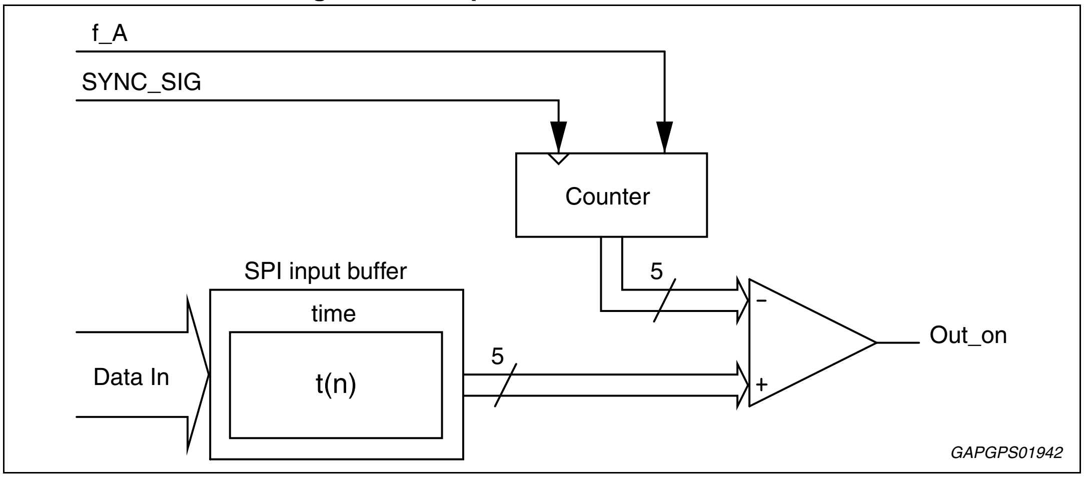
Figure 20. Set-point control example



In this example the RESET_VALUE (and therefore the SPI transfer loop time) is set to 5ms and the SYNC_VALUE is set to 2.5 ms. This sets the SYNC_TRIG at 2.5ms after each SPI transfer. At SYNC_TRIG, the new information received at the previous SPI transfer is incorporated into the Set-Point Controller.

All that is required for outputs Q1 through Q4 is a commanded on-time based on data in the SPI input command registers (see *Section 5.1.5: Duration registers (address 4, 5, 14, and 15)*). Since there is no duty cycle information to decode there is no need to generate duty cycle commands or go through a PWM generator. The resulting circuit is shown in *Figure 21* below.

Figure 21. Set point controller for Q1-Q4

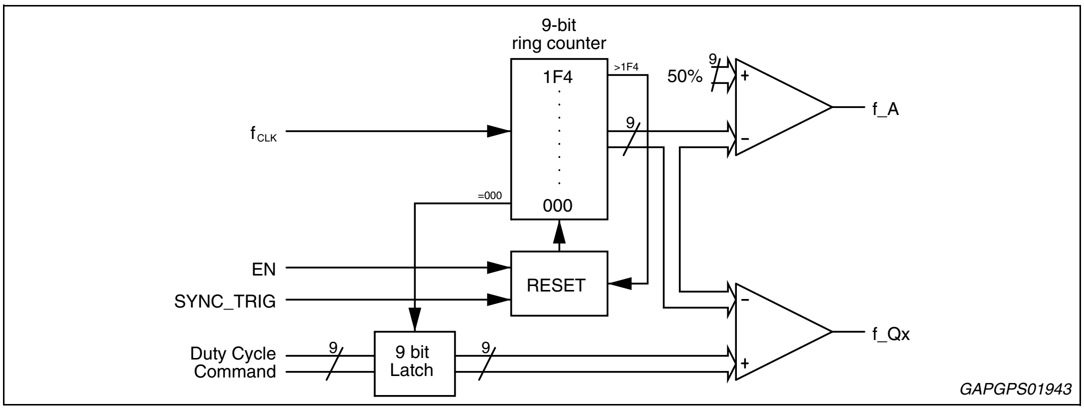


4.5 PWM generator(Q5-Q8 only)

The PWM Generator converts the commanded Duty Cycle from the Set Point controller into a PWM signal for Output Driver Q5 - Q8. The PWM-generator provides a 4 kHz PWM duty cycle (f_Qx) depending on the value of the 9 bit control variable. A 9-Bit ring counter counts with a frequency of f_{CLK} (2 MHz). The ring counter output is compared to the control variable. If the value of the counter is lower than the control variable the output, f_Qx is high turning on the output Qx. If the value of the counter is equal or higher to the output, f_Qx is low turning off the output Qx.

The counter can be reset by either a counter overflow at '$1F4_{(Hex)}$' (→ $500_{(10)}$), or by a SYNC_TRIG command. The control variable value is changed only when the counter passes through zero.

Figure 22. PWM control block diagram (Q5 - Q8 only)



4.6 Output driver

The output driver controls the gate of the low side power DMOS as well as provides specific diagnostic information to the SPI diagnostic registers. There are several signals that control the actuation of the output power DMOS. In normal operation the typical input is the f_Qx from the PWM generator (Q5-Q8) or Out_on for the Set Point controller (Q1 -Q4). Other inputs that can turn on the output are the silent valve driver test (SVDT) and the Fast Switch on circuitry. Inputs that can disable the outputs are the fast switch off command, device enable, and certain failure detections that can potentially cause catastrophic damage if the output is left on.

Figure 23. Gate drive block diagram with power (Q5-Q8)

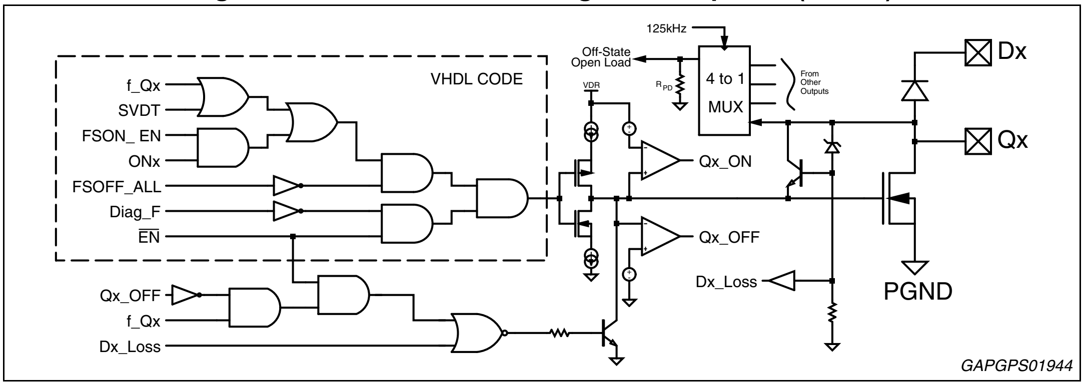
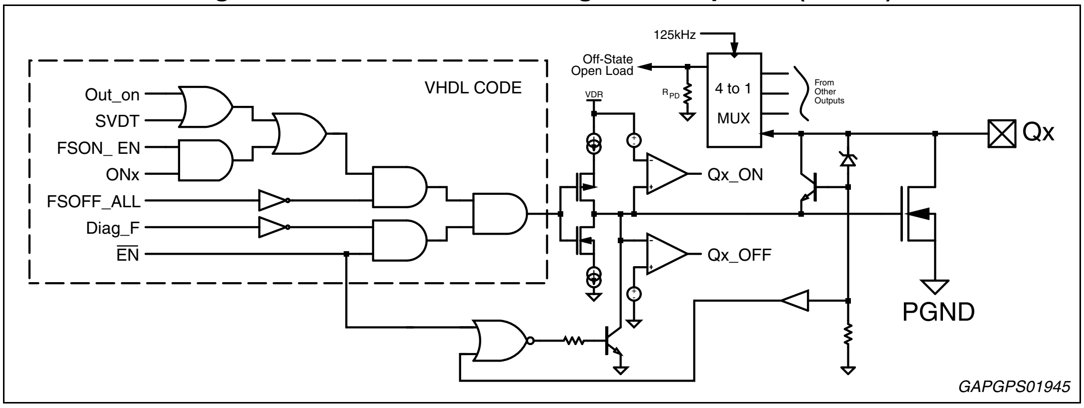


Figure 24. Gate drive block diagram with power (Q1-Q4)



4.6.1 Output driver controls

The output driver control circuit includes the logical combination of the following signals:

- PWM generator (*Figure 22*) (Q5-Q8):(f_Qx)/ Set Point controller (*Figure 21*) (Q1-Q4): (Out_on)
- Silent valve driver test signal (SVDT)
- Device enable (EN)
- Specific diagnostic failure indications such as PGND loss, overload, over temperature (Diag_F).
- Fast switch off for all outputs: (FSOFF_ALL)
- Fast switch on enable: (FSON_EN)
- Direct SPI driven output switching through the fast switch on command (ON_X)

In normal operation, the signals EN = ‘1’, FSOFF_ALL = ‘0’, Diag_F = ‘0’, allow the gate to be driven by the PWM generator/set point controller signal (f_Qx). The signal f_Qx can override the SVDT input if actuation is commanded during an SVDT.

The signals Diag_F=’0’, EN=’0’ and FSOFF_ALL=’1’ by-pass all other inputs and turn off the output immediately. The Diag_F flag is set to ‘1’ at the detection of PGND loss, overload and over-temperature disabling the affected output. Hardware Enable (EN) is an external pin and is controlled by the µC directly. FSOFF_ALL is a SPI command that provides a method to shut down all outputs in one SPI command.

4.6.2 Diagnostics

Output stage diagnostics provide fault feedback information for the SPI status registers.

Gate monitoring

The Qx_ON and Qx_OFF SPI diagnostic bits provide Gate status history information. If the output DMOS Gate voltage is above the Qx_ON threshold at any point between two SPI cycles the Qx_ON output will latch on (‘1’) the SPI bit associated with that signal (bit 6 of status registers 1 - 8). If the output DMOS gate is below the Qx_OFF threshold at any point between two SPI cycles the Qx_OFF output will latch on (‘1’) the SPI bit associated with that signal (bit 7 of status of status registers 1 - 8). If an output is PWMmed both Qx_ON and Qx_OFF will return a ‘1’ when read by the SPI. Upon reading status registers 1 through 8 the Qx_ON and Qx_OFF bits are reset to ‘0’.

This parameter cannot be tested directly as the Output MOSFET Gates are not exposed to measure their voltage. These parameters can only be tested by secondary means. and are guaranteed by design.

To verify that Qx_ON is functional it is checked when the output is commanded on. At this point the output transistor is fully enhanced and the Rds(on) is within specification. The Qx_on bit should be set.

To verify the Qx_OFF condition the output is commanded off and a 15 mA current is forced into the Qx pin. This forces the output voltage to rise to the clamped voltage and raise the gate voltage so that the output MOSFET can sink the 15 mA. This will then reset the Qx_OFF bit. This guarantees that the Qx_OFF threshold is below the gate voltage value required for the output MOSFET to sink 15 mA.

Conversely if the Gate voltage remains above or below the thresholds mentioned the status bits Qx_ON or Qx_OFF will indicate only one state was present. At no time during normal operation will both bits not be set.

Table 29. Qx_ON and Qx_OFF provide gate voltage status history information

Condition	QX_ON	QX_OFF
duty: 100%	1	0
duty: 0%	0	1
duty: 0% < dc <100%	1	1
Fault condition	0	0

Recirculation diode loss detection (Q5-Q8)

Dx_Loss transmits to the SPI register latch a ‘1’ whenever the output protection clamping structure is used. This notifies the SPI that the recirculation diode, Dx, was not in the circuit.

According *Figure 23* the device ENABLE has a direct link to a separate discharge path on the power gate. Only the high voltage clamp (Dx_loss) gets a higher priority. This is done to protect the DMOS from high voltage damage if the recirculation diode is “lost”.

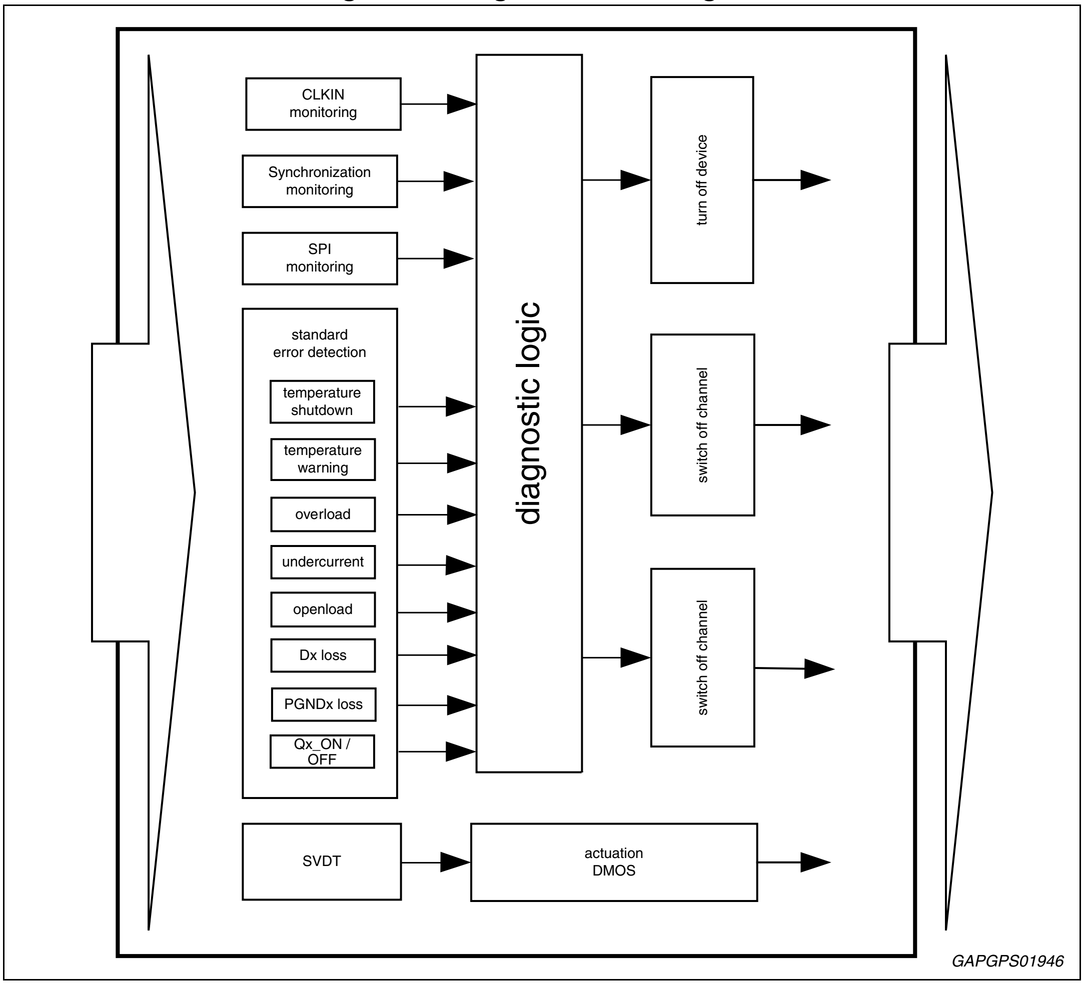
Table 30. Output driver possible input configuration

FSOFF_ALL	FSON_EN	ON_X	Setpoints	Output Qx (0=off, 1=on)	Remark
10	x	x	Q = on / PWM	0	like EN pin
10	x	x	Q = off	0	like EN pin
01	0	x	Q = on / PWM	1 or PWM	-
01	0	x	Q = off	0	-
01	x	0	Q = on / PWM	1 or PWM	-
01	x	0	Q = off	0	-
01	1	1	Q = on / PWM	1	Channel switched on without a SYNC_SIG
01	1	1	Q = off	1	Channel switched on without a SYNC_SIG

4.7 Diagnostics

There is a large amount of diagnostic functions in the L9375TRLF. These functions are designed to verify internal as well as external conditions. In so doing virtually every function is checked for proper operation. All of the diagnostic results are read by the master µC via SPI commands.

Figure 25. Diagnosis block diagram



4.7.1 Undercurrent / openload

Undercurrent can be detected if the current through the load in on-state is below the undercurrent threshold (I_{UC}, *Table 16*) for longer than the filter time (t_{UC}, *Table 19*). The filter is active in that a counter counts up when the undercurrent is detected (the device is on AND load current below I_{UC}) and counts down when undercurrent is not detected (either the device is off OR the current is above I_{UC}). Once undercurrent is detected for the duration of the undercurrent counter (see *Figure 26*) the SPI fault bit is set. The SPI fault bit is reset when the undercurrent has not been detected long enough for the counter to reach 0.

This bit is not latched unless undercurrent is detected during the SVDT test.

Figure 26. Diagram under current

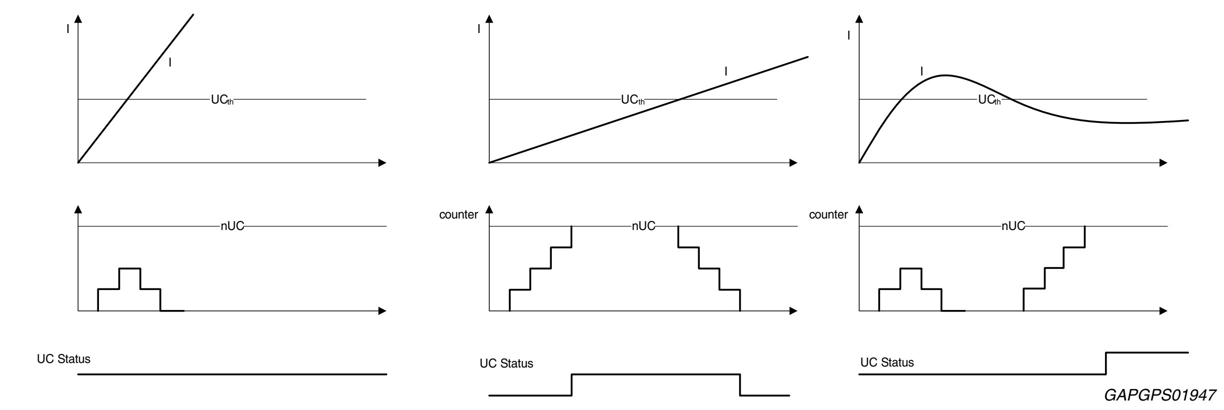
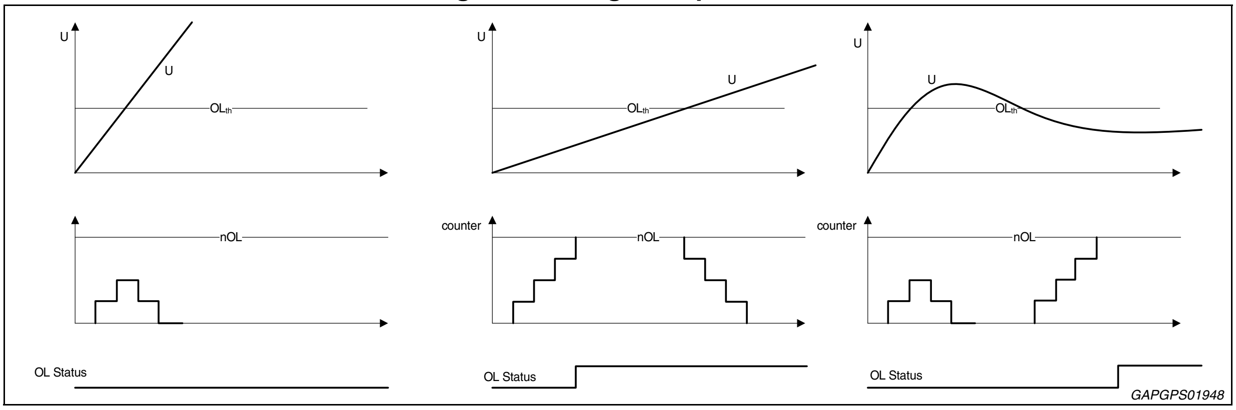


Figure 27. Diagram open load



4.7.2 Openload

Openload detection is done in the off-state through a multiplexed pull-down resistor, R_{PD} (see *Figure 3 and 4*). R_{PD} is multiplexed onto each output node sequentially at a fixed 125kHz rate. The output voltage is measured while R_{PD} is connected to the output. Voltages below V_{OL} (*Table 16*) indicate an off-state Open load condition. Multiplexing R_{PD} reduces the overall “leakage” current while providing a substantial pull-down current to verify open load status. There is a counter that “debounces” the open load detection similar to the undercurrent filter counter (See *Figure 27*). Open load is latched in the SPI status registers (bit D0 of registers 1 - 8, *Section 5.2.2*) and is cleared once read.

4.7.3 Over current

If the measured load current is higher than the overcurrent threshold ($I_{OCx,}$ *Table 16*) a failure is detected. The overcurrent detection is measured in on state only. This failure is filtered for t_{OC} (20 µs typ., *Table 19*). After t_{OC} the output is shut down immediately and all of the set point and control variables are set to zero. This disables the output from further actuation until the appropriate status registers are read and cleared (refer to *Section 5.2.2*). Once the appropriate SPI status registers are read the offending output(s) are released to be driven again. This failure detection is used for all outputs.

The overcurrent bit is latched upon an overcurrent detection and reset after reading the corresponding SPI register.

This failure detection is also used during SVDT (see *4.7.11: Silent valve driver test (SVDT)*).

4.7.4 Thermal warning and thermal shutdown

The L9375TRLF is equipped with a two stage thermal protection system. This system provides for an early thermal warning and a thermal overload shutdown protection. With thermal warning some countermeasures can be realized by the Master µC to potentially prevent thermal shutdown. The temperature for each output is only measured when the output is on. Temperature warning has the same functionality as over temperature. The only differences are:

– The threshold is 20 °C below over temperature.

– The Output is not shut down.

– The SPI-Bit shows the actual status at the time it is accessed.

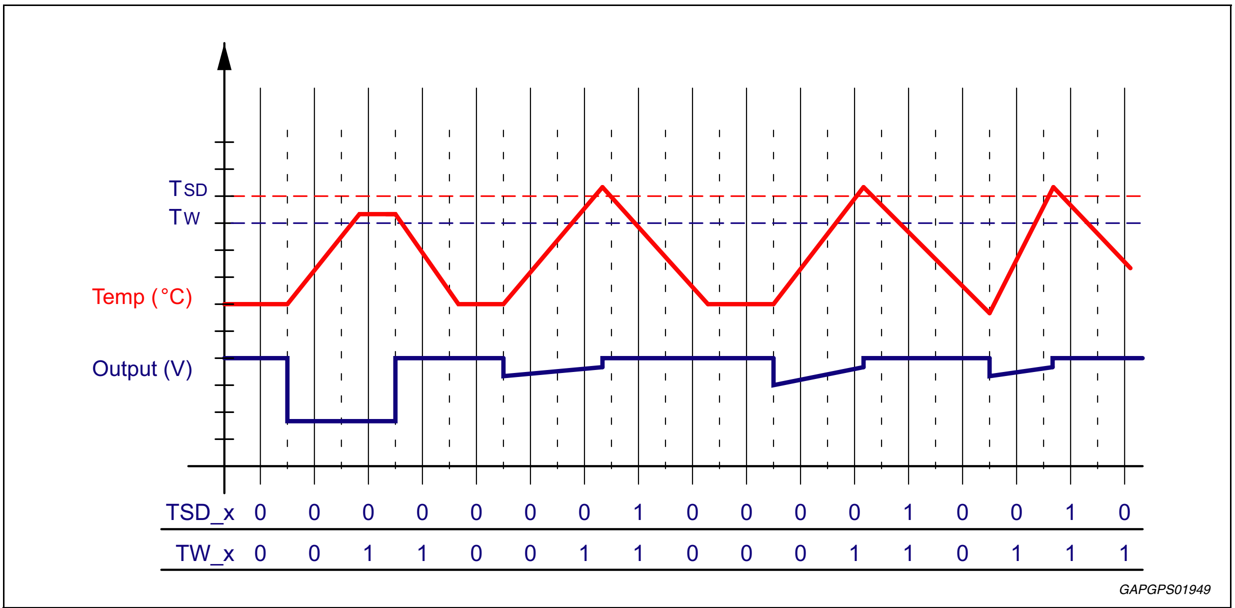
Thermal warning

If the measured value is higher than the thermal warning threshold, T_W (*Table 16*), for t_{TW} (*Table 19*) the appropriate thermal warning bit for that output is set in the SPI Status register (bit D8 of status registers 1 through 8, *Section 5.2.2*). No other action is taken. Reading the status registers clears the TW bit(s) once the device is cooled sufficiently. This failure detection is used for all outputs.

Thermal shutdown

The L9375TRLF is equipped with a thermal shutdown protection system. There is one thermal sensor shared for every two outputs. When the measured temperature exceeds the thermal shutdown threshold, T_{SD} (*Table 16*), a failure is detected. This failure detection is filtered for t_{OT} (40 µs typ., *Table 19*). After t_{OT} the affected outputs are shut down immediately and all of the set point and control variables are set to zero. This disables both of the shared outputs from further actuation until the over temperature condition is removed and appropriate status register(s) (bit D2 of status registers 1 through 8, *Section 5.2.2*) are read. Reading the status registers clears the T_{SD} bits once the device is cooled sufficiently.

Figure 28. Thermal detection / protection behavior



4.7.5 Power ground loss (PGND-loss)

PGND-loss continuously monitors the voltage between SGND and PGND. If the measured value is higher than V_{PG_L} (*Table 17*) for longer than t_{PGND_L} (*Table 19*) a failure is detected. This sets the PGNDL_Qx bit (*Section 5.2.2*) and sets all of the set point and control variables to zero disabling the offending output. There is a power ground loss bit for each output even though in the packaged part the power grounds are shared.

Once the power ground loss condition is removed the outputs are re-enabled by reading the appropriate status register (SPI Status registers 1 - 8). This clears the failure bit in the status register and re-enables the output for use. This failure detection is used for all outputs.

The status of the failure is shown via SPI. PGND-loss is latched and can be reset only by accessing this register when the failure is no longer present.

4.7.6 Signal ground loss (SGND-loss)

The SGND-loss monitors the voltage between SGND and PGND. If the measured value is higher than V_{SG_L} (*Table 17*) for t_{SGND_L} (*Table 19*) a failure is detected. After this time ALL outputs are switched off immediately and the driver is shut down. The SPI communication is possible but there is a threshold shift at the logic I/O due to an additional substrate diode in the ground path between PGND and SGND (see *Section 5.2.1*).

4.7.7 Recirculation diode loss detection (Dx-loss)(Q5 - Q8 only)

Recirculation diode loss is detected by measuring the current through the output clamping structure. If the clamping structure is used for more than t_{DX_L}(*Table 19*) a Dx_Loss is detected and the appropriate Status register bit (bit D5 of status registers 3,4,7,8, *Section 5.2.2*) is latched on. This bit can only be cleared once the failure is removed and the status register is read.

4.7.8 SPI-failure

There are 3 possible SPI-failures:

– parity failure (PARITY_F)
– clock failure (SPICLK_F)
– data failure (DATA_F)

In case of any SPI-Failure the next transmission to the master contains the following data:

Table 31. SPI failure Response data

MSB															LSB
received address				1	1	1	1	1	1	1	1	1	1	1	Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Parity failure

A parity failure is detected if the total number of '1's in the message is not odd. The PARITY_F bit of status register 0 is set and master message is ignored (no change of the data). The corresponding status message returned to the master after a parity failure contains the received address and only ‘1’s for the data bits. The PARITY_F bit can be cleared by accessing address 0.

SPI clock failure

TheL9375TRLF counts the number of SPICLK positive edges during SPICS actuations (SPICS='0'). If this number is unequal to 16 an error is detected and the message is not used (no change of the data) and the SPICLK_F bit in the status address 0 is set. The corresponding status message returned to the master after a Clock failure contains the received address and only '1's for the data bits (see *Table 31*). The SPICLK_F bit can be cleared by accessing address 0.

Data failure

A SPI command with data content that is not allowed produces a data failure (DATA_F).

The Data_F bit in the SPI status register 0 is set if the master writes invalid data to the config-registers (address 2, 14 and 15). When this failure occurs all data in these addresses are not modified (no change in the content at these registers).The Data_F bit can be cleared by accessing address 0.

4.7.9 CLKIN-failure

CLKIN-failure (CLKIN_F) is detected if the input frequency (*Table 18*) at the CLKIN pin is out of the specified range for t_{CLK_F}.(*Table 19*). Once this failure is detected all outputs are switched off immediately, all set points, control variables, and counters are reset to zero and the sync_counter is set to one. This frequency is monitored by an internal oscillator. This oscillator is used to clock all internal nodes otherwise driven by CLKIN.

All failures which occur due to a CLKIN-failure are not reflected in any SPI-register. Only a sync failure will be reflected. Failures which occurred prior to a CLKIN failure are not deleted or overwritten.

The CLKIN_F bit can be cleared by accessing address 0 once the failure is removed.

4.7.10 Sync-failure

Sync failure detects a timing error in the output command synchronization. The master µC programs a timing window (STW, *Section 4.3*) where accessing to status address 0 is not allowed. If there is an access to Status address 0 when the STW flag is set then a sync-failure is generated (SYNC_F = 1). Also, a SYNC_F will be detected if there is no SPI traffic at all between two SYNC_SIG events. This status will be read out on the subsequent SPI transfer.

Without a SYNC_SIG or at sync-failure there is no effect for the actuation and set points.

A sync-failure detection results in two consecutive error flags (SYNC_F = 1).

To re-synchronize the L9375TRLF a SYNC_TRIG signal must be sent.

Table 32. Fault diagnostic summary

Failure	Output state	Effect	Reset behavior
Openload	off	– bit is set (latched)	Access SPI-register
Undercurrent	on	– bit is set (filtered) see *4.7.1*	Access SPI-register

Table 32. Fault diagnostic summary (continued)

Failure	Output state	Effect	Reset behavior
Overload	on	– bit is set (latched) – output is switched off – all set points / duty cycle / durations are kept at zero	Access SPI-register
Over temperature	on	– bit is set (latched) – output is switched off – all set points / duty cycle / durations are kept at zero	Access SPI-register
Thermal Warning	on	– bit is set (latched)	Access SPI-register
PGND-loss	on + off	– bit is set (latched) – output is switched off – all set points / duty cycle / durations are kept at zero	Access SPI-register
SGND-loss	on + off	– No constraints at all functions – SPI-communication has to be possible – The SPI-bit SGND_L is set after the filter time (t_{SGND_L}) – All channels are switched off after t_{SGND_L} and all set points are reset. – The sync-parameters are not cleared; sync-counter is not reset	Access SPI-register
Dx-loss	on	– bit is set (latched)	Access SPI-register
SPI: Parity failure odd	on + off	– bit is set (latched) – data are not used	Access SPI-register
SPI: SPICLK-failure n <> 16	on + off	– bit is set (latched) – data are not used	Access SPI-register
SPI: Data-failure	on + off	– bit is set (latched) – data are not used (within a register)	Access SPI-register
CLKIN-failure	on + off	– bit is set (latched) – all outputs switched off immediately – all set points / current / duty cycle / durations are kept at zero – all counters are kept at zero – all synchronization values are kept at zero (reset, sync, STW) – there is no change in the status register	Access SPI-register

Table 32. Fault diagnostic summary (continued)

Failure	Output state	Effect	Reset behavior
Sync-failure STW_V_MIN < X < STW_V_MAX	on + off	– bit is set (latched)	Access SPI-register
Under voltage @ VS	on + off	– all outputs switched off immediately – all set points / current / duty cycle /durations are kept zero – all counters are kept at zero – all synchronization values are kept at zero (reset, sync, STW) – all status register are kept at zero – all input, outputs and data buffer are kept at default	-

4.7.11 Silent valve driver test (SVDT)

The silent valve driver test (SVDT) checks the DMOS Output and valve load integrity. Because the valve is switched on for a very short time during the test, the current in the loads remains very low. Subsequently the valves are not actuated and there is no observable valve noise.

The SVDT is initiated via a SPI command and automatically tests all outputs sequentially. It is not possible to restart the SVDT while it is in the middle of a test. However the SVDT can be interrupted by setting the SYNC_TRIG bit (Command register 0, bit D10).

The following status monitors are used during an SVDT:

Table 33. Status monitored during SVDT

Status	Bit description	Bit(s)
Off- State Open Load	OL_Qx	D0
Under Current	UC_Qx	D1
Over current	OC_Qx	D2
Over Temperature	OT_Qx	D3
Loss of recirculation diode	Dx_Loss	D5

The SVDT SPI command is a 2 bit command where only one combination is acceptable to begin the test

Table 34. SVDT command

SVDT command (Address 2)	Bit 1	Bit 0
Not Possible	0	0
Normal Operation / No test	0	1
SVDT Active (in test mode)	1	0
Not Possible	1	1

When the SVDT has completed testing all of the outputs, the SVDT command bits are reset '01' and the test is halted. To restart the test the SVDT command bits must be rewritten as '10'. All of the results are stored within the SPI output status registers (SPI status addresses 1 - 8, *Section 5.2.2*). Accessing the output status registers after the SVDT is completed clears these registers. It is important to note that reading these addresses during an SVDT test also clears the status bits.

The SVDT sequence begins at the next SYNC_SIG after initiating the SVDT command. It is important to disable edge shaping (Command Address 2, bits D8 & D7 = '10', *Section 5.1.3*) during the SVDT test for accurate results. This can be done in the same command.

The SVDT will run in a loop until completed even if the programmed sync register cycle time (RESET_VALUE) is shorter than the SVDT actuation time.

Figure 29. Timing between each output tests

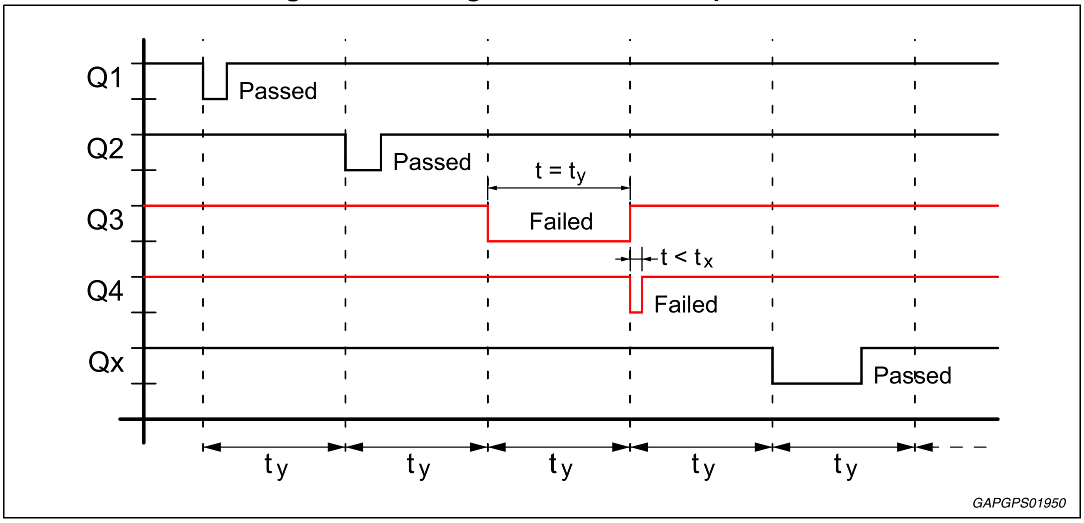
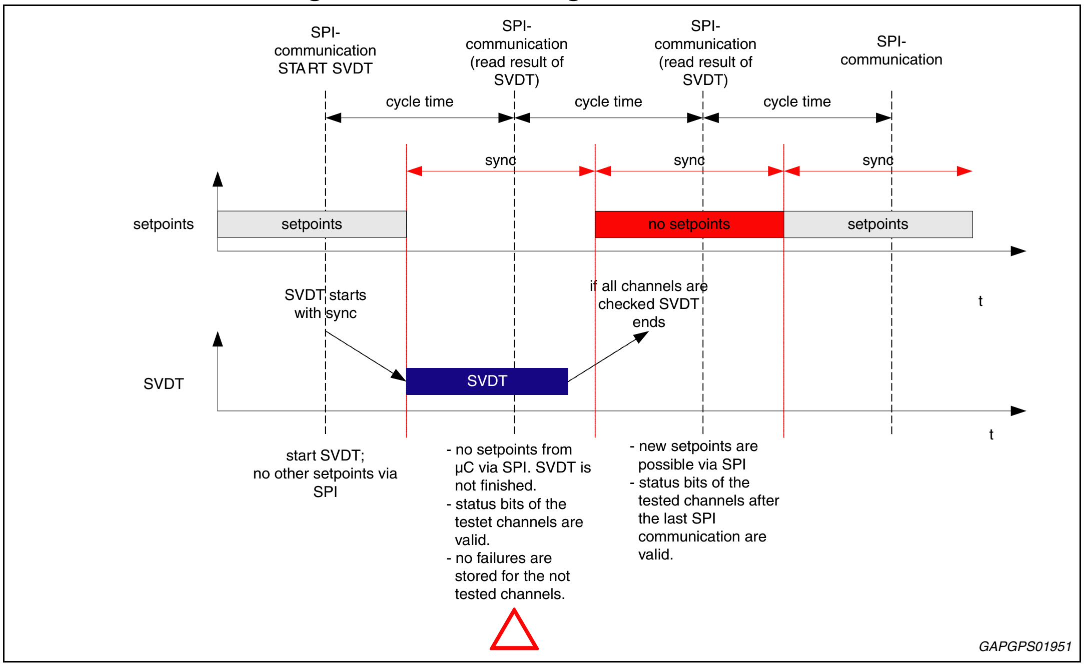


Figure 30. SVDT-Timing with SPI-transfer



SVDT test sequence

1. Disable Edge Shaping (Command address 2, bits D8 & D7 = ‘10’)
2. Initiate SVDT (Command address 2; bits D1 & D0 = ‘10’)
3. Qx switches on at the next sync-signal (sequence of actuation: Q1..Q8)
4. Because the output is actuated the output current increases.
5. At time tx, if the output current has exceeded the under current value, I_{UC}, the output is switched off.
6. If the over current threshold (I_{OC}) is achieved prior to tx then the output is immediately disabled and an over current condition is detected.
7. The output will switch off any time prior to exceeding time, ty, if the undercurrent threshold, I_{UC}, has been met.
8. After the output is disabled if the output clamps the voltage to V_Z (35V) a Dx_Loss is detected.
9. If an Over temperature is not detected then the SDVT test is passed
10. The SVDT will then test at Qx+1 until all 8 outputs have been tested.

Criterion for passing:

- no overcurrent
- Current value increases and reached undercurrent value within time ty (I_{Qx}>I_{UC}) & (tx < t < ty).
- Channels with a recirculation diode does not have a clamping thus do not report a Dx_Loss condition

SPI:

- no failure at all Output status registers (Status Addresses 1 - 8).
- Qx_ON = 1

Figure 31. Passing test diagram

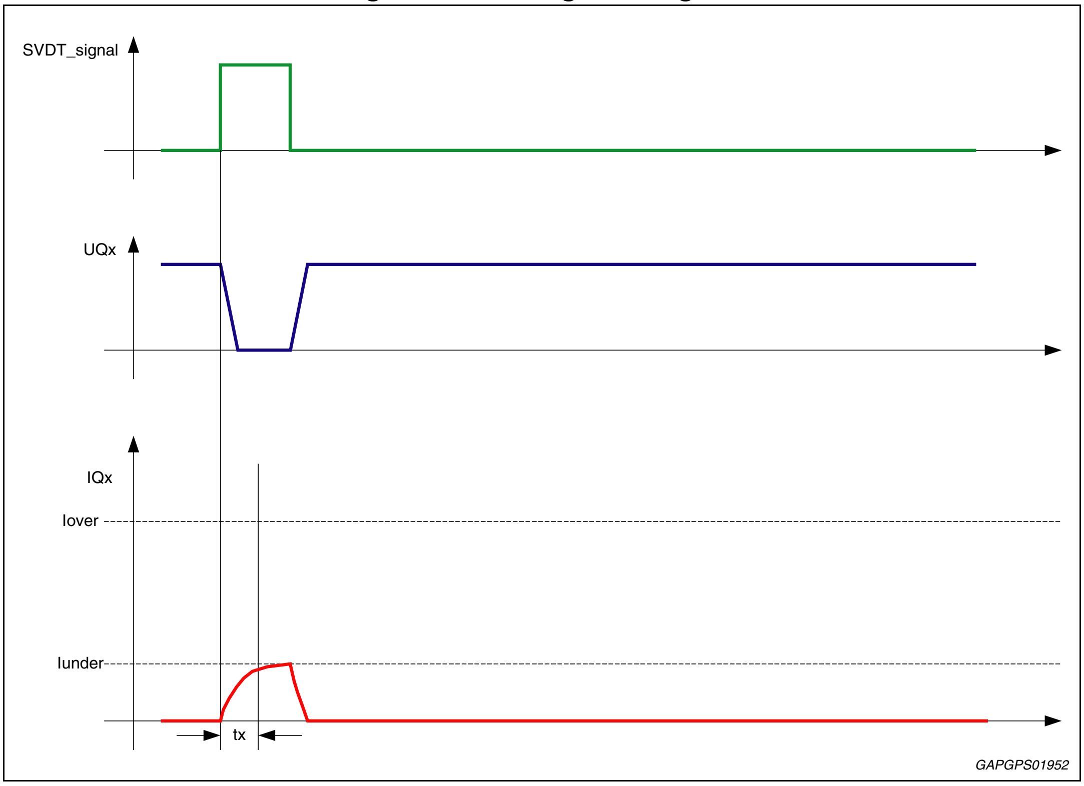
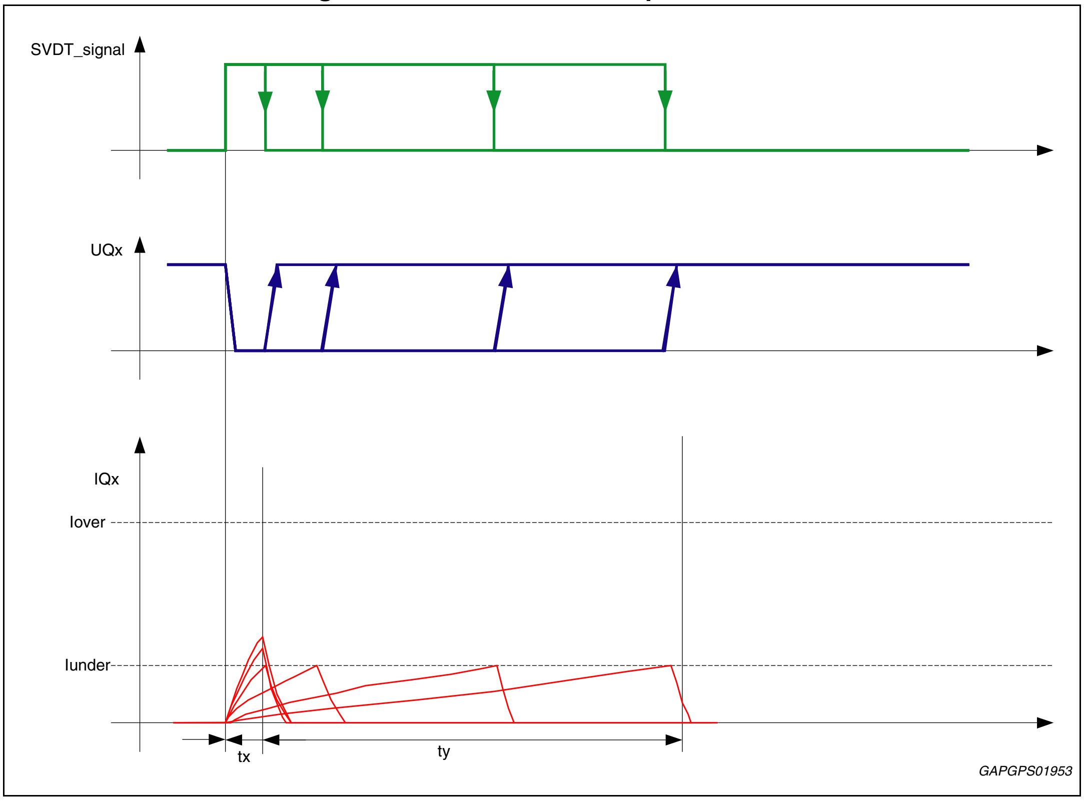
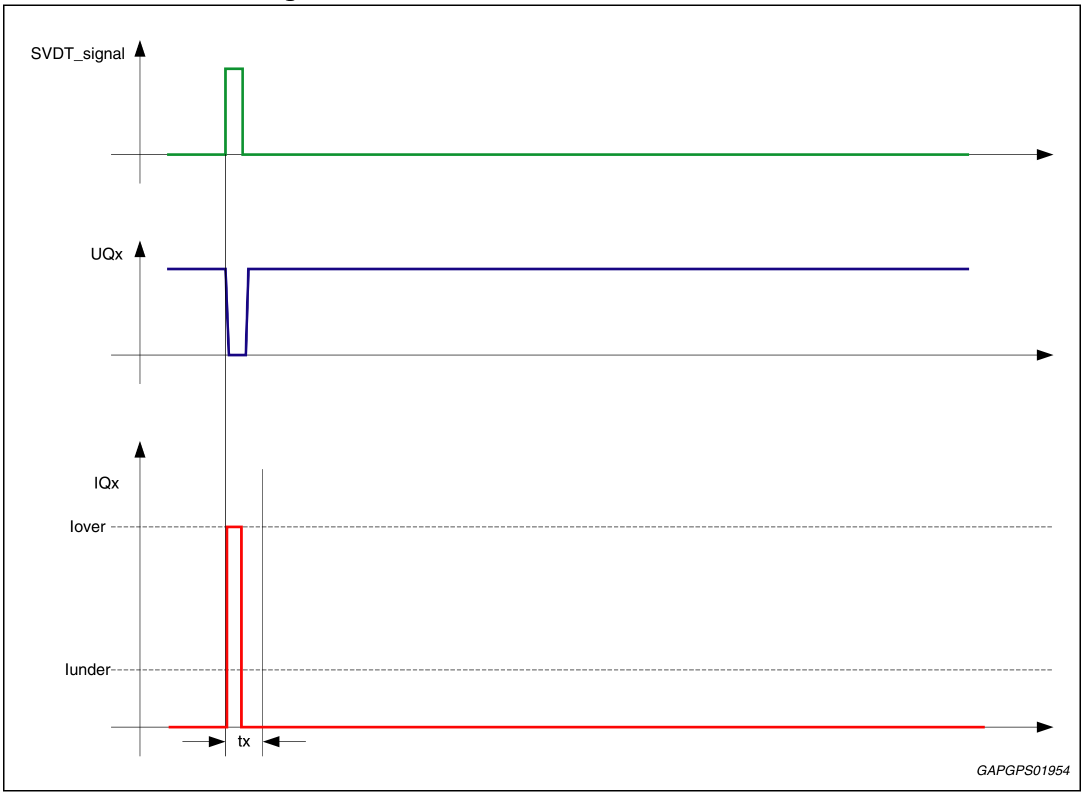


Figure 32. Possibilities of a passed test



The SVDT test examples

Figure 33. Test failed: short circuit / overload



A failed test sequence for overload condition:

1. Disable Edge Shaping (Command address 2, bits D8 & D7 = ‘10’)
2. Initiate SVDT (Command address 2; bits D1 & D0 = ‘10’)
3. Qx switches on at the next sync-signal (sequence of actuation: Q1..Q8)
4. The output current increases and reaches I_{OL} before tx is reached
5. Output Qx is switched off for overload protection and the overload bit (bit D0 of the status registers 1 - 8).
6. After the output is disabled if the output clamps the voltage to V_Z (35V) a Dx_Loss is detected.
7. If an Over temperature is not detected then the TEMP_Qx bit is not set.
8. The SVDT will then test at Qx+1 until all 8 outputs have been tested.

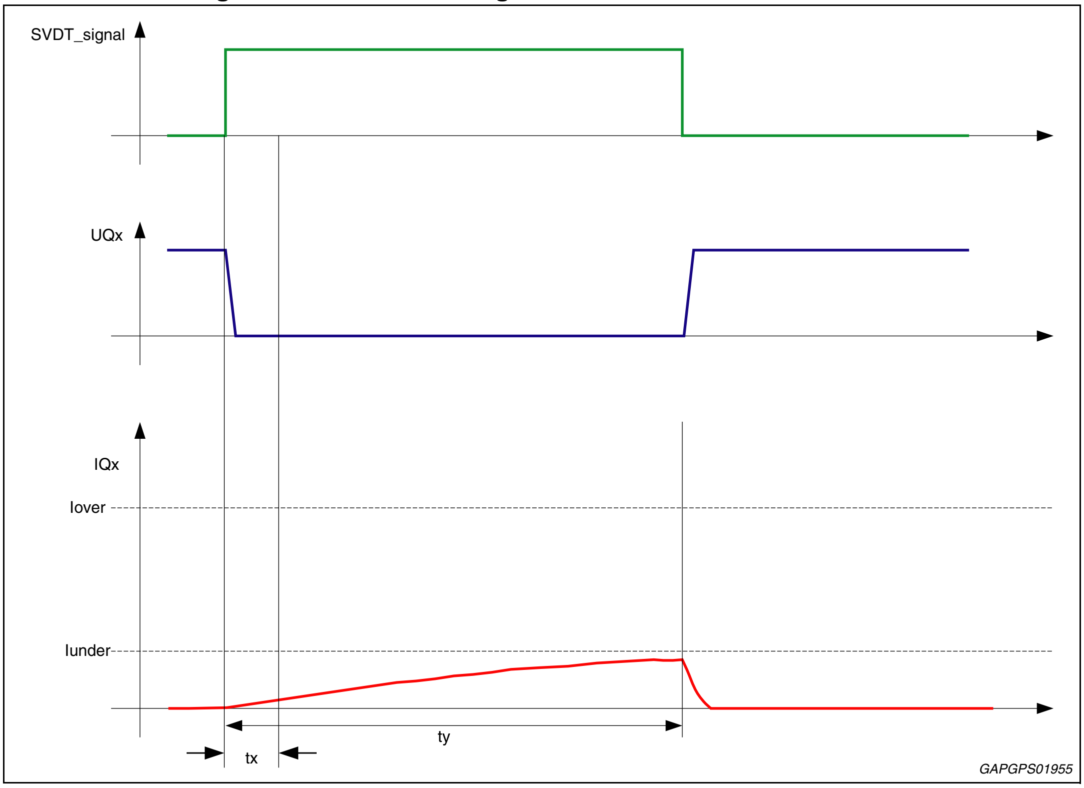
Criterion:

– The output current increases and reaches overcurrent value within the test time tx

SPI:

– Status registers 1 - 8, OL_Qx bit is set.

Figure 34. Test failed: high resistive load / undercurrent



A failed test sequence for under current condition

The test sequence:

1. Disable Edge Shaping (Command address 2, bits D8 & D7 = ‘10’)
2. Initiate SVDT (Command address 2; bits D1 & D0 = ‘10’)
3. Qx switches on at the next sync-signal (sequence of actuation: Q1..Q4)
4. The output current increases but does not reach the undercurrent value, I_{UC}.
5. After ty the output is switched off.
6. After the output is disabled if the output clamps the voltage to V_Z (35V) a Dx_Loss is detected.
7. If an Over temperature is not detected then the TEMP_Qx bit is not set.
8. The SVDT will then test at Qx+1 until all 4 outputs have been tested.

Criterion:

– the current value does not reach the undercurrent value within time ty

SPI:

– Status registers 1 - 4, UC_Qx bit is set.

Table 35. SVDT status

Dx_loss	Over current OC_Qx	Under current UC_Qx	Description
0	0	0	Test is passed
0	0	1	High resistive load or high inductive load
0	1	0	Overcurrent: short circuit to supply voltage or short circuit of the load
0	1	1	Not possible
1	0	0	Dx-loss
1	0	1	Dx-loss+ high resistive load or high inductive load
1	1	0	Dx-loss + short circuit to supply voltage or short circuit of the load
1	1	1	Not possible

5 Programmers guide

This programmers guide is a reference section intended to aid in the L9375TRLF interface software development. The L9375TRLF uses SPI messaging for all of its communication into or out of the device. The Command registers are written to and the Status registers are read.

5.1 Command registers

The Command Registers are registers written to by the MASTER µC to actuate the L9375TRLF,s various functions. Each command consists of an address, data, and a parity bit (refer to *Section 4.1: SPI serial peripheral interface* for more details).

5.1.1 Sync + Sync-trigger register (address 0)

MSB																**LSB**
0	0	0	0	SYNC_TRIG	RESET_VALUE				SYNC_VALUE							Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		P

Table 36. Sync + sync-trigger register

Sync + sync-trigger	Name	Bit location	Number of bits	bit time
Synchronization value	SYNC_VALUE	D0-D5	6	250 µs
Reset value (highest 4 Bits)	RESET_VALUE	D6-D9	4	1 ms
Sync-trigger	SYNC_TRIG	D10	1	-

For this section see *Section 4.3: Synchronization controller* for more details.

Synchronization value

This 6-bit-value represents a time value. At this time the new set points are processed.
Resolution of LSB: 250 µs.

Reset value

With this value the time base of the synchronization can be modified.
Resolution of LSB: 1 ms.

The MSB of the RESET_VALUE (D9) affects the bit times for the Sync Trigger Window, the Duration x, and the Duration y parameters.

Sync-trigger

The synchronization is re-triggered by setting this bit to ‘1’. After a re-synchronization the internal logic will clear this bit automatically.

If the SVDT is active and still running, it will be interrupted by setting the SYNC_TRIG bit (See also section *Synchronization controller programming*).

5.1.2 Sync tolerance window (STW) register (address 1)

MSB															LSB
0	0	0	1	0	STW_V_MAX					STW_V_MIN					Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

STW value:

These two sets of 5 bits each define a window (between min and max) where accessing address ‘0’ within this window will cause a sync failure indication (SYNC_F).

To keep the resolution meaningful for the entire range of Sync Triggering the resolution is dependant on the RESET_VALUE MSB. For programming the two values to the STW the master has to write both values (2 x 5 bit).

Table 37. STW value

STW value	Name	Bit location	Number of bits	bit time RESET_VALUE $\leq 0111_{(2)}$	bit time RESET_VALUE $\geq 1000_{(2)}$
STW value min.	STW_V_MIN	D0 - D4	5	250 µs	500 µs
STW value max.	STW_V_MAX	D5 - D9	5	250 µs	500 µs

For this section see *4.3: Synchronization controller* for more details

5.1.3 Configuration register (address 2)

MSB															LSB
0	0	1	0	x	x	EDGE_SH		FSON_EN	FSOFF_ALL		CLKIN_S		SVDT		Parity
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Table 38. Configuration register 1

Config register	Name	Bit location	Number of bits
Silent valve driver test	SVDT	D0 - D1	2 Bit
CLKIN frequency 1MHz / 250kHz	CLKIN_S	D2 - D3	2 Bit
Fast switch off all	FSOFF_ALL	D4 - D5	2 Bit
Fast switch on enable (general)	FSON_EN	D6	1 Bit
Edge shaping on / off	EDGE_SH	D7 - D8	2 Bit

Silent valve driver test (SVDT):

These two bits (D0 & D1) are normally set to ‘01’. Writing '10' to these two bits starts the silent valve driver test (for more details see *4.7.11: Silent valve driver test (SVDT)*).

Table 39. Silent valve driver test (SVDT)

Bit 1	Bit 0	Combination
0	0	Not valid
0	1	Normal condition / no test
1	0	Active
1	1	Not valid

Writing not valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all ‘1’s.

CLKIN input frequency 1 MHz / 250 kHz (CLKIN_S):

These two bits set the ratio between internal and external clock (see *4.2: Clock*).

Table 40. CLKIN_S

Bit 1	Bit 0	External clock value
0	0	Not valid
0	1	250 kHz
1	0	1 MHz
1	1	Not valid

Writing not valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all ‘1’s.

Fast switch off (FSOFF_ALL):

These two bits (D4 & D5) are normally set to ‘01’. With these two bits set to ‘10’ all outputs are switched off immediately (without regard to the synchronization). When set to active these bits clear the fast switch on enable (FSON_EN) bit at address 3 and all set points. It is not possible to activate any output with status FSOFF_ALL = ‘10’ (active).

Table 41. Fast switch off

Bit 1	Bit 0	Combination
0	0	Not valid
0	1	Normal condition
1	0	Active → all outputs are off
1	1	Not valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all ‘1’s.

Fast switch on enable (FSON_EN):

This bit (D6) is normally set to ‘0’. Setting this bit (‘1’) enables the SPI ability to drive outputs directly. With this bit set, writing to address 3 (bits D0 -D7) turns on or off outputs Q1 - Q8. All of the bits in Command Register 3 are reset when FSON_EN is reset (‘0’).

Edge shaping (EDGE_SH):

Edge Shaping option allows the user to incorporate a slower more EMI sensitive slope to the output waveform. By setting these bits the user is able to turn on / off edge shaping for all outputs (see *Section 3.3.4: Output timing characteristics*). There is no option to select individual outputs for edge shaping. When performing the SVDT it is recommended that Edge Shaping be turned OFF.

Table 42. Edge shaping

Bit 1	Bit 0	Combination
0	0	Not Valid
0	1	Edge Shaping **ON** for all outputs
1	0	Edge Shaping **OFF** for all outputs
1	1	Not Valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all ‘1’s.

5.1.4 Fast switch-on (FSON) register (address 3)

MSB															LSB
0	0	1	1	x	x	x	ON_8	ON_7	ON_6	ON_5	ON_4	ON_3	ON_2	ON_1	Parity
A3	A2	A1	A0	free	free	free	D7	D6	D5	D4	D3	D2	D1	D0	P

Table 43. Fast switch-on

Configuration register	Bit Location	Name
Switch on Q1	D0	ON_1
Switch on Q2	D1	ON_2
Switch on Q3	D2	ON_3
Switch on Q4	D3	ON_4
Switch on Q5	D4	ON_5
Switch on Q6	D5	ON_6
Switch on Q7	D6	ON_7
Switch on Q8	D7	ON_8

If the fast switch on enable bit (FSON_EN) is set, writing 1 to the bit ON_X switches the output on 100%. A ‘0’ written to the fast switch on enable pin will disable this function. Any outputs on as a result of an ONx bit being high will be turned off.

The fast switch off all bits (FSOFF_ALL) turns off all channels immediately and does not depend on the synchronization controller, and clears all bits at this address. The fast switch off (FSOFF_ALL) all command has the highest priority.

5.1.5 Duration registers (address 4, 5, 14, and 15)

MSB															LSB
0	1	0	0	x	D_Q2					D_Q1					Parity
0	1	0	1	x	D_Q6					D_Q5					Parity
1	1	1	0	x	D_Q8					D_Q7					Parity
1	1	1	1	x	D_Q4					D_Q3					Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Outputs Q1 - Q4 are driven for the duration specified in Registers 4 and 15. Once the duration has expired they are turned off. Outputs Q5 - Q8 can be driven in two stages by one SPI transfer, a duty cycle for a duration and then a second duty cycle. These registers provide the initial duration information.

Table 44. Register duration value

Register address	Duration parameter	Number of bits	Bit location	Output
4	D_Q1	5 Bit	D4 - D0	Q1
4	D_Q2	5 Bit	D9 - D5	Q2
5	D_Q5	5 Bit	D4 - D0	Q5
5	D_Q6	5 Bit	D9 - D5	Q6
14	D_Q7	5 Bit	D4 - D0	Q7
14	D_Q8	5 Bit	D9 - D5	Q8
15	D_Q3	5 Bit	D4 - D0	Q3
15	D_Q4	5 Bit	D9 - D5	Q4

The duration bit resolution depends on the synchronization timer RESET_VALUE MSB:

Table 45. Duration bit resolution

RESET_VALUE MSB (add.0, bit D9)	Resolution of duration
0	250 µs
1	500 µs

5.1.6 Duty cycle register (address 6 to 13)

MSB															LSB
0	1	1	0	x	x	DUTY1_Q5									Parity
0	1	1	1	x	x	DUTY2_Q5									Parity
1	0	0	0	x	x	DUTY1_Q6									Parity
1	0	0	1	x	x	DUTY2_Q6									Parity
1	0	1	0	x	x	DUTY1_Q7									Parity
1	0	1	1	x	x	DUTY2_Q7									Parity
1	1	0	0	x	x	DUTY1_Q8									Parity
1	1	0	1	x	x	DUTY2_Q8									Parity
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

The value of these registers represent the outputs Q5 through Q8 set point duty cycles. Addresses 6, 8, 10 and 12 provide the initial duty cycle used during the durations specified in the duration registers (addresses 5 and 14). Addresses 7, 9, 11, and 13 provide the duty cycles used after the durations specified in addresses 5 and 14 have expired.

Table 46. Duty cycle register (address 6 to 9)

Register address	Duty cycle register	Number of bits	Bit location	Name
6	Output 5 Duty cycle 1	9	D0 - D8	DUTY1_Q5
7	Output 5 Duty cycle 2	9	D0 - D8	DUTY2_Q5
8	Output6 Duty cycle 1	9	D0 - D8	DUTY1_Q6
9	Output 6 Duty cycle 2	9	D0 - D8	DUTY2_Q6
10	Output 7 Duty cycle 1	9	D0 - D8	DUTY1_Q7
11	Output 7 Duty cycle 2	9	D0 - D8	DUTY2_Q7
12	Output 8 Duty cycle 1	9	D0 - D8	DUTY1_Q8
13	Output 8 Duty cycle 2	9	D0 - D8	DUTY2_Q8

The resolution is 0.2% per LSB.

$000_{(H)}$ = 0% Duty Cycle

$1F4_{(H)}$ = 100% Duty cycle.

To achieve the full diagnostic capability do not use a duty cycle of less than 5%(or $19_{(H)}$).

5.2 Status registers

5.2.1 General status (address 0)

MSB															LSB
0	0	0	0	0	SGND_L	FSON_S	CLKIN_State		EN	CLKIN_F	SYNC_F	DATA_F	SPICLK_F	PARITY_F	Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Table 47. Status registers

General status	Number of bits	Bit location	Name
Parity-failure	1 Bit	D0	PARITY_F
SPI-Clock-failure	1 Bit	D1	SPICLK_F
Data-failure	1 Bit	D2	DATA_F
Sync-Failure	1 Bit	D3	SYNC_F
CLKIN-failure	1 Bit	D4	CLKIN_F
EN Status	1 Bit	D5	EN
1MHz / 250kHz Status	2 Bits	D7 - D6	CLKIN_S
Fast Switch On Enable Status	1 Bit	D8	FSON_S
SGND loss	1 Bit	D9	SGND_L

Parity-failure:

If a parity-failure occurs during any command write this bit is set. It is cleared by accessing address 0.

SPI-Clock-failure:

This bit is set by a clock-failure (number of positive edges of SPICLK within SPICS = low is unequal 16) and is cleared by accessing address 0.

Data-failure:

This bit is set if the master writes invalid data to the configuration-register (Data: SVDT, CLKIN_S and FSOFF_ALL / CCPWM_Qx / OV_THx, EDGE_SH_OFF). Reset of this bit is done by accessing address 0. If the master tries to write invalid data to one of the input registers its content will not be changed (invalid write access is ignored, SPI data failure is set).

Sync-failure:

This bit is set by a Sync-failure and is cleared when the failure does not exist anymore (shows the actual status). For more details see*: Synchronization failure*.

CLKIN-failure:

If the frequency of CLKIN-signal is not in a specified range a CLKIN-failure occurs (CLKIN_F = 1). The specification range can be changed via SPI (CLKIN_STATE). This bit (CLKIN_F) can be cleared by accessing this address.

Hardware EN status:

The EN Status bit reflects the level of the Enable (EN) pin. If the value of the Enable pin was low since the last access to this register the status EN is low (low sensitive signal). This bit is cleared by accessing this address.

1 MHz / 250 kHz status:

These bits reflect the two CLKIN_S bits from the Command register 2 (bits D3 and D2). This is done to verify that the L9375TRLF has received the CLKIN_S command.

Table 48. CLKIN_S command

Bit 1	Bit 0	Combination
0	0	Not possible
0	1	250kHz
1	0	1MHz
1	1	Not possible

Fast switch on enable (FSON_EN) status

This bit shows the actual status of Fast switch on enable (FSON_EN) bit found in Command register 2, bit D6.

SGND loss:

After sensing a signal ground loss for t_{SGND_filt} the SPI-bit SGND_L is set, all channels are switched off, and all current set points are reset. The sync-parameters and the sync_counter are not cleared. With SGND-loss a SPI-communication is still possible by using PGND as a ground reference. When the loss of SGND no longer exists the SGND_L bit is reset after an access to address 0 (refer to *Section 4.7.6: Signal ground loss (SGND-loss)*).

5.2.2 Output status Q1 to Q8 (address 1 to 8)

MSB															**LSB**
0	0	0	1	0	0	TW_1	Q1_OFF	Q1_ON	free	PGNDL_1	TSD_1	OC_1	UC_1	OL_1	Parity
0	0	1	0	0	0	TW_2	Q2_OFF	Q2_ON	free	PGNDL_2	TSD_1	OC_2	UC_2	OL_2	Parity
0	0	1	1	0	0	TW_5	Q5_OFF	Q5_ON	DL_5	PGNDL_5	TSD_1	OC_5	UC_5	OL_5	Parity
0	1	0	0	0	0	TW_6	Q6_OFF	Q6_ON	DL_6	PGNDL_6	TSD_1	OC_6	UC_6	OL_6	Parity
0	1	0	1	0	0	TW_3	Q3_OFF	Q3_ON	free	PGNDL_3	TSD_1	OC_3	UC_3	OL_3	Parity
0	1	1	0	0	0	TW_4	Q4_OFF	Q4_ON	free	PGNDL_4	TSD_1	OC_4	UC_4	OL_4	Parity
0	1	1	1	0	0	TW_7	Q7_OFF	Q7_ON	DL_7	PGNDL_7	TSD_1	OC_7	UC_7	OL_7	Parity
1	0	0	0	0	0	TW_8	Q8_OFF	Q8_ON	DL_8	PGNDL_8	TSD_1	OC_8	UC_8	OL_8	Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

Channel

Table 49. Output status Q1 to Q8

Channel status	Number of bits	Bit Location	Name
Open load	1 Bit	D0	OL_x
Under current	1 Bit	D1	UC_x
Over current	1 Bit	D2	OC_x
Thermal shutdown	1 Bit	D3	TSD_x
PGND-loss	1 Bit	D4	PGNDL
Dx-loss (Q5-Q8 only)	1 Bit	D5	DL_x
Output ON	1 Bit	D6	Qx_ON
Output OFF	1 Bit	D7	Qx_OFF
Thermal warning	1 Bit	D8	TW_x

Note: See section 4.7: Diagnostics for details for most of the parameters in this section.

Open load

The open load bit is set if the voltage at output Qx in off-state is lower than the failure-threshold V_{OL} (*Table 16*). This bit is cleared by accessing this address (refer to *Section 4.7.1* for more details).

Under current

The undercurrent bit shows the status of the undercurrent detection (I_{UC},*Table 16*). This bit is cleared by accessing this address (refer to *Section 4.7.1* for more details).

Over current

When the on-state current through output Qx is higher than the failure-threshold (I_{OC}, *Table 16*) the overload bit is set and all set point and control variables for the offending output are set to zero. This bit can be cleared by accessing this address (refer to *Section 4.7.3* for more details).

Thermal shutdown

Thermal shutdown is detected if the temperature of the DMOS is above T_{SD}, (*Table 16*) for t_{OVL} (*Table 19*); for more details refer to *Thermal shutdown*.

PGND-loss

This bit is set by a power ground loss and is cleared by accessing this address (refer to *Section 4.7.5* for more details).

Loss of recirculation diode (Dx-loss) (Q5 - Q8 only)

This bit is set by loss of the recirculation diode and is cleared by accessing this address (refer to *Section 4.7.7* for more details).

Gate voltage on status (Qx_ON)

This bit shows the status of the output driver gate. A comparator monitors the voltage of the gate and reports the status of the gate. The status of the gate is latched. If the Gate voltage is above the Qx_ON threshold for any length of time the Qx_ON bit is set. The bit is cleared by accessing this address (refer to *Gate monitoring* for more information).

Gate voltage off status (Qx_OFF)

This bit shows the status of the output driver gate. A comparator monitors the voltage of the gate and reports the status of the gate. The status of the gate is latched.

If the Gate voltage is below the Qx_OFF threshold for any length of time the Qx_OFF bit is set. The bit is cleared by accessing this address (refer to *Gate monitoring* for more information).

If an output has been both “off” and “on” prior to reading the appropriate status register both Qx_OFF and Qx_ON bits will be set.

Thermal Warning

If the measured value is higher than the thermal warning threshold, T_W (*Table 16*), for t_{TW} (*Table 19*) the TW_x bit is set. No other action is taken. Reading the status registers clears the TW bit(s) once the device is cooled sufficiently (refer to *Thermal warning* for more details)

5.2.3 Reserved (addresses 9 - 15)

These registers are not used. The response will always be 0x(addr)001.

MSB															**LSB**
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

6 Register block functional overview

6.1 Input command register block overview (MOSI data)

Note: Without address-bits and parity

Table 50. Overview input register block

address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0 SYNC_REG	**sync_trig**	**RESET_VALUE**				**SYNC_VALUE**					
		RESET_VAL_3	RESET_VAL_2	RESET_VAL_1	RESET_VAL_0	SYNC_VAL_5	SYNC_VAL_4	SYNC_VAL_3	SYNC_VAL_2	SYNC_VAL_1	SYNC_VAL_0
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
1 STW_V	**free**	**STW_V_MAX**					**STW_V_MIN**				
		STW_max_4	STW_max_3	STW_max_2	STW_max_1	STW_max_0	STW_min_4	STW_min_3	STW_min_2	STW_min_1	STW_min_0
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
2 CONFIG 1	**free**	**free**	**EDGE_SH**		FSON_EN	**FSOFF_ALL**		**CLKIN_S**		**SVDT**	
			EDGE_SH_OFF_1	EDGE_SH_OFF_0		F_{SOFF_1}	F_{SOFF_0}	CLKIN_S_1	CLKIN_S_0	SVDT_1	SVDT_0
P.O.R. State	0	0	0	1	0	0	1	0	1	0	1
3 FSON	**free**	**free**	Q8_ON	Q7_ON	Q5_ON	Q6_ON	Q5_ON	Q4_ON	Q3_ON	Q2_ON	Q1_ON
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
4 Duration Q1/Q2	**free**	**D_Q2**					**D_Q1**				
		D_{Q2_4}	D_{Q2_3}	D_{Q2_2}	D_{Q2_1}	D_{Q2_0}	D_{Q1_4}	D_{Q1_3}	D_{Q1_2}	D_{Q1_1}	D_{Q1_0}
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
5 Duration Q5/Q6	**free**	**D_Q6**					**D_Q5**				
		D_{Q6_4}	D_{Q6_3}	D_{Q6_2}	D_{Q6_1}	D_{Q6_0}	D_{Q5_4}	D_{Q5_3}	D_{Q5_2}	D_{Q5_1}	D_{Q5_0}
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
6 DUTY1_Q5	**free**	**free**	**DUTY1_Q5**								
			$DU1_{Q5\_8}$	$DU1_{Q5\_7}$	$DU1_{Q5\_6}$	$DU1_{Q5\_5}$	$DU1_{Q5\_4}$	$DU1_{Q5\_3}$	$DU1_{Q5\_2}$	$DU1_{Q5\_1}$	$DU1_{Q5\_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
7 DUTY2_Q5	**free**	**free**	**DUTY2_Q5**								
			$DU2_{Q5\_8}$	$DU2_{Q5\_7}$	$DU2_{Q5\_6}$	$DU2_{Q5\_5}$	$DU2_{Q5\_4}$	$DU2_{Q5\_3}$	$DU2_{Q5\_2}$	$DU2_{Q5\_1}$	$DU2_{Q5\_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
8 DUTY1_Q6	**free**	**free**	**DUTY1_Q6**								
			$DU1_{Q6\_8}$	$DU1_{Q6\_7}$	$DU1_{Q6\_6}$	$DU1_{Q6\_5}$	$DU1_{Q6\_4}$	$DU1_{Q6\_3}$	$DU1_{Q6\_2}$	$DU1_{Q6\_1}$	$DU1_{Q6\_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0

Table 50. Overview input register block (continued)

address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
9 DUTY2_Q6	**free**	**free**	**DUTY2_Q6**								
			DU2$_{Q6_8}$	DU2$_{Q6_7}$	DU2$_{Q6_6}$	DU2$_{Q6_5}$	DU2$_{Q6_4}$	DU2$_{Q6_3}$	DU2$_{Q6_2}$	DU2$_{Q6_1}$	DU2$_{Q6_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
10 DUTY1_Q7	**free**	**free**	**DUTY1_Q7**								
			CU1$_{Q7_8}$	CU1$_{Q7_7}$	CU1$_{Q7_6}$	CU1$_{Q7_5}$	CU1$_{Q7_4}$	CU1$_{Q7_3}$	CU1$_{Q7_2}$	CU1$_{Q7_1}$	CU1$_{Q7_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
11 DUTY2_Q7	**free**	**free**	**DUTY2_Q7**								
			CU2$_{Q7_8}$	CU2$_{Q7_7}$	CU2$_{Q7_6}$	CU2$_{Q7_5}$	CU2$_{Q7_4}$	CU2$_{Q7_3}$	CU2$_{Q7_2}$	CU2$_{Q7_1}$	CU2$_{Q7_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
12 DUTY1_Q8	**free**	**free**	**DUTY1_Q8**								
			CU1$_{Q8_8}$	CU1$_{Q8_7}$	CU1$_{Q8_6}$	CU1$_{Q8_5}$	CU1$_{Q8_4}$	CU1$_{Q8_3}$	CU1$_{Q8_2}$	CU1$_{Q8_1}$	CU1$_{Q8_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
13 DUTY2_Q8	**free**	**free**	**DUTY2_Q8**								
			CU2$_{Q8_8}$	CU2$_{Q8_7}$	CU2$_{Q8_6}$	CU2$_{Q8_5}$	CU2$_{Q8_4}$	CU2$_{Q8_3}$	CU2$_{Q8_2}$	CU2$_{Q8_1}$	CU2$_{Q8_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
14 Duration Q7/Q8	**free**	**D_Q8**					**D_Q7**				
		D$_{Q8_4}$	D$_{Q8_3}$	D$_{Q8_2}$	D$_{Q8_1}$	D$_{Q8_0}$	D$_{Q7_4}$	D$_{Q7_3}$	D$_{Q7_2}$	D$_{Q7_1}$	D$_{Q7_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
15 Duration Q3/Q4	**free**	**D_Q4**					**D_Q3**				
		D$_{Q4_4}$	D$_{Q4_3}$	D$_{Q4_2}$	D$_{Q4_1}$	D$_{Q4_0}$	D$_{Q3_4}$	D$_{Q3_3}$	D$_{Q3_2}$	D$_{Q3_1}$	D$_{Q3_0}$
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0

6.1.1 Status register block overview (MISO data)

Note: Note: without address-bits and parity

Table 51. Overview answer register block

Address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0 G_INFO	**free**	**SGND_L**	**FSON_S**	**CLKIN_State**		**HW_EN**	**CLKIN_F**	**SYNC_F**	**Data_F**	**SPICLK_F**	**PARITY_F**
				CLKIN_S_1	CLKIN_S_0						
P.O.R. State	0	0	0	0	1	0	0	1	0	0	0
1 STATUS_Q1	**free**	**free**	**TW_1**	**Q1_OFF**	**Q1_ON**	**free**	**PGNDL_Q1**	**TEMP_Q1**	**OVER_Q1**	**UC_Q1**	**OL_Q1**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
2 STATUS_Q2	**free**	**free**	**TW_2**	**Q2_OFF**	**Q2_ON**	**free**	**PGNDL_Q2**	**TEMP_Q2**	**OVER_Q2**	**UC_Q2**	**OL_Q2**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
3 STATUS_Q5	**free**	**free**	**TW_5**	**Q5_OFF**	**Q5_ON**	**free**	**PGNDL_Q5**	**TEMP_Q5**	**OVER_Q5**	**UC_Q5**	**OL_Q5**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
4 STATUS_Q6	**free**	**free**	**TW_6**	**Q6_OFF**	**Q6_ON**	**free**	**PGNDL_Q6**	**TEMP_Q6**	**OVER_Q6**	**UC_Q6**	**OL_Q6**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
5 STATUS_Q3	**free**	**free**	**TW_3**	**Q3_OFF**	**Q3_ON**	**free**	**PGNDL_Q3**	**TEMP_Q3**	**OVER_Q3**	**UC_Q3**	**OL_Q3**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
6 STATUS_Q4	**free**	**free**	**TW_4**	**Q4_OFF**	**Q4_ON**	**free**	**PGNDL_Q4**	**TEMP_Q4**	**OVER_Q4**	**UC_Q4**	**OL_Q4**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
7 STATUS_Q7	**free**	**free**	**TW_7**	**Q7_OFF**	**Q7_ON**	**free**	**PGNDL_Q7**	**TEMP_Q7**	**OVER_Q7**	**UC_Q7**	**OL_Q7**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
8 STATUS_Q8	**free**	**free**	**TW_8**	**Q8_OFF**	**Q8_ON**	**free**	**PGNDL_Q8**	**TEMP_Q8**	**OVER_Q8**	**UC_Q8**	**OL_Q8**
P.O.R. State	0	0	0	0	0	0	0	0	0	0	0
9 - 15 RESERVED	**RESERVED**										
answer to access	0	0	0	0	0	0	0	0	0	0	0

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

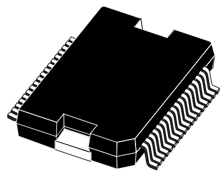
ECOPACK® is an ST trademark.

Figure 35. PowerSO-36 (slug down) mechanical data and package dimensions

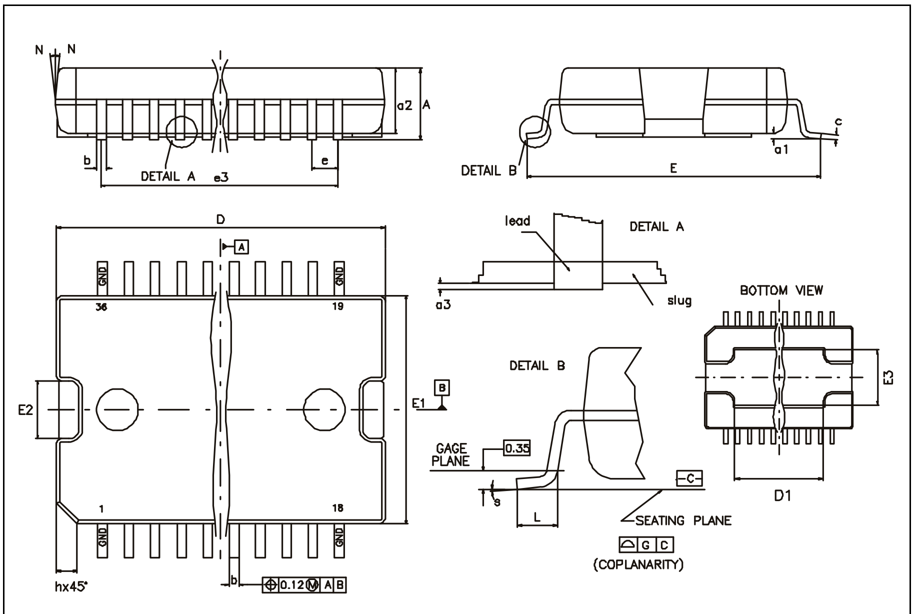
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10° (max)					
s	8° (max)					

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO-36



GAPGPS00191

8 Revision history

Table 52. Document revision history

Date	Revision	Changes
26-Mar-2014	1	Initial release.

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **"LifeElectronics" LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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- *Подбор аналогов.*
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- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru