

# 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input

## Features

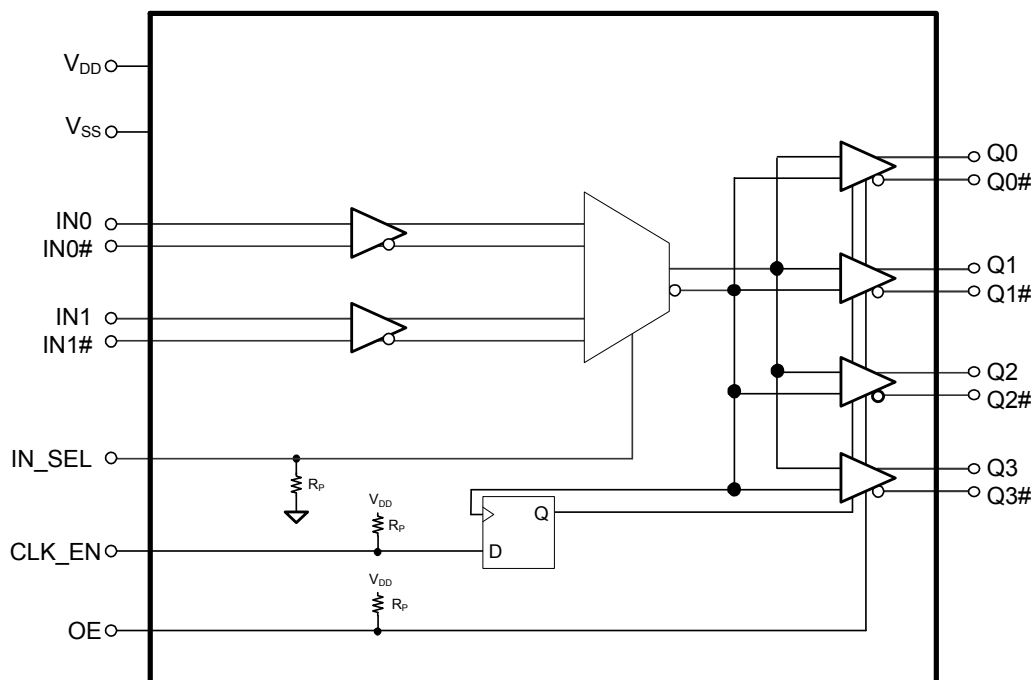
- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to four LVDS output pairs
- Translates any single-ended input signal to 3.3 V LVDS levels with resistor bias on INx# input
- 30 ps maximum output-to-output skew
- 480 ps maximum propagation delay
- 0.11 ps maximum additive RMS phase jitter at 156.25 MHz (12 kHz to 20 MHz offset)
- Up to 1.5 GHz operation
- Output enable and synchronous clock enable functions
- 20-pin TSSOP
- 2.5 V or 3.3 V operating voltage <sup>[1]</sup>
- Commercial and industrial operating temperature range

## Functional Description

The CY2DL1504 is an ultra-low noise, low-skew, low-propagation delay 1:4 differential LVDS fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DL1504 can select between two separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN\_SEL pin. The synchronous clock enable function ensures glitch-free output transitions during enable and disable periods. The output enable function allows the outputs to be asynchronously driven to a high-impedance state. The device has a fully differential internal architecture that is optimized to achieve low-additive jitter and low-skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

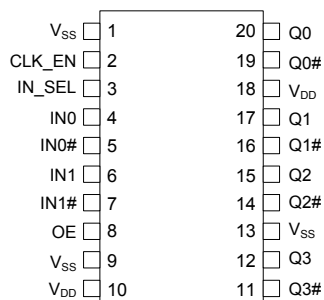
1. Input AC-coupling capacitors are required for voltage-translation applications.

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## Pinouts

**Figure 1. 20-pin TSSOP pinout**



## Pin Definitions

| Pin No.        | Pin Name        | Pin Type | Description                                                                                                                                                                      |
|----------------|-----------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 9, 13       | V <sub>SS</sub> | Power    | Ground                                                                                                                                                                           |
| 2              | CLK_EN          | Input    | Synchronous clock enable. LVCMOS/LVTTL;<br>When CLK_EN = Low, Q(0:3) outputs are held low and Q(0:3)# outputs are held high                                                      |
| 3              | IN_SEL          | Input    | Input clock select pin. LVCMOS/LVTTL;<br>When IN_SEL = Low, the IN0/IN0# differential input pair is active<br>When IN_SEL = High, the IN1/IN1# differential input pair is active |
| 4              | IN0             | Input    | Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = Low                                                                                                  |
| 5              | IN0#            | Input    | Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = Low                                                                                    |
| 6              | IN1             | Input    | Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = High                                                                                                 |
| 7              | IN1#            | Input    | Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = High                                                                                   |
| 8              | OE              | Input    | Output enable. LVCMOS/LVTTL;<br>When OE = Low, Q(0:3) and Q(0:3)# outputs are disabled (see I <sub>OZ</sub> )                                                                    |
| 10, 18         | V <sub>DD</sub> | Power    | Power supply                                                                                                                                                                     |
| 11, 14, 16, 19 | Q(0:3)#         | Output   | LVDS complementary output clocks                                                                                                                                                 |
| 12, 15, 17, 20 | Q(0:3)          | Output   | LVDS output clocks                                                                                                                                                               |

## Absolute Maximum Ratings

| Parameter       | Description                                                 | Condition           | Min                                                  | Max                             | Unit |
|-----------------|-------------------------------------------------------------|---------------------|------------------------------------------------------|---------------------------------|------|
| $V_{DD}$        | Supply voltage                                              | Nonfunctional       | -0.5                                                 | 4.6                             | V    |
| $V_{IN}^{[2]}$  | Input voltage, relative to $V_{SS}$                         | Nonfunctional       | -0.5                                                 | Lesser of 4.0 or $V_{DD} + 0.4$ | V    |
| $V_{OUT}^{[2]}$ | DC output or I/O voltage, relative to $V_{SS}$              | Nonfunctional       | -0.5                                                 | Lesser of 4.0 or $V_{DD} + 0.4$ | V    |
| $T_S$           | Storage temperature                                         | Nonfunctional       | -55                                                  | 150                             | °C   |
| $ESD_{HBM}$     | Electrostatic discharge (ESD) protection (Human body model) | JEDEC STD 22-A114-B | 2000                                                 | –                               | V    |
| $L_U$           | Latch up                                                    |                     | Meets or exceeds JEDEC Spec JESD78B IC latch up test |                                 |      |
| UL-94           | Flammability rating                                         | At 1/8 in.          | V-0                                                  |                                 |      |
| MSL             | Moisture sensitivity level                                  |                     | 3                                                    |                                 |      |

## Operating Conditions

| Parameter | Description                   | Condition                                                                                     | Min   | Max   | Unit |
|-----------|-------------------------------|-----------------------------------------------------------------------------------------------|-------|-------|------|
| $V_{DD}$  | Supply voltage                | 2.5 V supply                                                                                  | 2.375 | 2.625 | V    |
|           |                               | 3.3 V supply                                                                                  | 3.135 | 3.465 | V    |
| $T_A$     | Ambient operating temperature | Commercial                                                                                    | 0     | 70    | °C   |
|           |                               | Industrial                                                                                    | -40   | 85    | °C   |
| $t_{PU}$  | Power ramp time               | Power-up time for $V_{DD}$ to reach minimum specified voltage. (Power ramp must be monotonic) | 0.05  | 500   | ms   |

### Note

2. The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

## DC Electrical Specifications

( $V_{DD} = 3.3 \text{ V} \pm 5\%$  or  $2.5 \text{ V} \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Commercial) or  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  (Industrial))

| Parameter            | Description                                                             | Condition                                                                                           | Min   | Max            | Unit          |
|----------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|-------|----------------|---------------|
| $I_{DD}$             | Operating supply current                                                | All LVDS outputs terminated with a load of $100 \Omega$ [3, 4]                                      | –     | 61             | mA            |
| $V_{IH1}$            | Input high voltage, differential input clocks, IN0, IN0#, IN1, and IN1# |                                                                                                     | –     | $V_{DD} + 0.3$ | V             |
| $V_{IL1}$            | Input low voltage, differential input clocks, IN0, IN0#, IN1, and IN1#  |                                                                                                     | –0.3  | –              | V             |
| $V_{IH2}$            | Input high voltage, CLK_EN, IN_SEL, and OE                              | $V_{DD} = 3.3 \text{ V}$                                                                            | 2.0   | $V_{DD} + 0.3$ | V             |
| $V_{IL2}$            | Input low voltage, CLK_EN, IN_SEL, and OE                               | $V_{DD} = 3.3 \text{ V}$                                                                            | –0.3  | 0.8            | V             |
| $V_{IH3}$            | Input high voltage, CLK_EN, IN_SEL, and OE                              | $V_{DD} = 2.5 \text{ V}$                                                                            | 1.7   | $V_{DD} + 0.3$ | V             |
| $V_{IL3}$            | Input low voltage, CLK_EN, IN_SEL, and OE                               | $V_{DD} = 2.5 \text{ V}$                                                                            | –0.3  | 0.7            | V             |
| $V_{ID\_LVDS}$ [5]   | LVDS input differential amplitude                                       | See Figure 3 on page 8                                                                              | 0.4   | 0.8            | V             |
| $V_{ID\_LVPECL}$ [5] | LVPECL/CML/HCSL input differential amplitude                            | See Figure 3 on page 8                                                                              | 0.4   | 1.0            | V             |
| $V_{ICM}$            | Input common mode voltage                                               | See Figure 3 on page 8                                                                              | 0.2   | $V_{DD} - 0.2$ | V             |
| $I_{IH}$             | Input high current, All inputs                                          | Input = $V_{DD}$ [6]                                                                                | –     | 150            | $\mu\text{A}$ |
| $I_{IL}$             | Input low current, All inputs                                           | Input = $V_{SS}$ [6]                                                                                | –150  | –              | $\mu\text{A}$ |
| $V_{PP}$             | LVDS differential output voltage peak to Peak, Single-ended             | $V_{DD} = 3.3 \text{ V}$ or $2.5 \text{ V}$ , $R_{TERM} = 100 \Omega$ between Q and Q# pairs [3, 7] | 250   | 470            | mV            |
| $V_{OCM}$            | LVDS differential output common mode voltage                            | $V_{DD} = 3.3 \text{ V}$ or $2.5 \text{ V}$ , $R_{TERM} = 100 \Omega$ between Q and Q# pairs [3, 7] | 1.125 | 1.375          | V             |
| $\Delta V_{OCM}$     | Change in $V_{OCM}$ between complementary output states                 | $V_{DD} = 3.3 \text{ V}$ or $2.5 \text{ V}$ , $R_{TERM} = 100 \Omega$ between Q and Q# pairs [3, 7] | –     | 50             | mV            |
| $I_{OZ}$             | Output leakage current                                                  | OE = $V_{SS}$ , $V_{OUT} = 0.75 \text{ V} - 1.75 \text{ V}$                                         | –15   | 15             | $\mu\text{A}$ |
| $R_P$                | Internal pull-up/pull-down resistance, LVCMOS logic inputs              | CLK_EN has pull-up only<br>IN_SEL has pull-down only<br>OE has pull-up only                         | 60    | 165            | $k\Omega$     |
| $C_{IN}$             | Input capacitance                                                       | Measured at 10 MHz; per pin                                                                         | –     | 3              | pF            |

## Thermal Resistance

| Parameter [8] | Description                              | Test Conditions                                                                                                             | 20-pin TSSOP | Unit               |
|---------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|--------------|--------------------|
| $\theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 80           | $^\circ\text{C/W}$ |
| $\theta_{JC}$ | Thermal resistance (junction to case)    |                                                                                                                             | 16           | $^\circ\text{C/W}$ |

### Notes

- Refer to Figure 2 on page 8.
- $I_{DD}$  includes current that is dissipated externally in the output termination resistors.
- $V_{ID}$  minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with  $V_{ID}$  minimum of greater than 200 mV.
- Positive current flows into the input pin, negative current flows out of the input pin.
- Refer to Figure 4 on page 8.
- These parameters are guaranteed by design and are not tested.

## AC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$  (Commercial) or  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$  (Industrial))

| Parameter                  | Description                                                                                                                                               | Condition                                                                                                             | Min | Typ | Max  | Unit   |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----|-----|------|--------|
| $F_{IN}$                   | Input frequency                                                                                                                                           | Differential Input                                                                                                    | DC  | –   | 1.5  | GHz    |
|                            |                                                                                                                                                           | Single ended input <sup>[9]</sup>                                                                                     | DC  | –   | 250  | MHz    |
| $F_{OUT}$                  | Output frequency                                                                                                                                          | $F_{OUT} = F_{IN}$ , Differential Input                                                                               | DC  | –   | 1.5  | GHz    |
|                            |                                                                                                                                                           | $F_{OUT} = F_{IN}$ , Single ended input <sup>[9]</sup>                                                                | DC  | –   | 250  | MHz    |
| $t_{PD}$ <sup>[10]</sup>   | Propagation delay differential input pair to differential output pair                                                                                     | Input rise/fall time < 1.5 ns (20% to 80%)                                                                            | –   | –   | 480  | ps     |
| $t_{ODC}$ <sup>[11]</sup>  | Output duty cycle                                                                                                                                         | Diff input at 50% duty cycle<br>Frequency range up to 1 GHz                                                           | 48  | –   | 52   | %      |
|                            |                                                                                                                                                           | 50% duty cycle at input,<br>Frequency range up to 250MHz,<br>Single ended input <sup>[9]</sup>                        | 45  | –   | 55   | %      |
| $t_{SK1}$ <sup>[12]</sup>  | Output-to-output skew                                                                                                                                     | Any output to any output, with same load conditions at DUT                                                            | –   | –   | 30   | ps     |
| $t_{SK1D}$ <sup>[12]</sup> | Device-to-device output skew                                                                                                                              | Any output to any output between two or more devices. Devices must have the same input and have the same output load. | –   | –   | 150  | ps     |
| $PN_{ADD}$                 | Additive RMS phase noise<br>156.25 MHz Input<br>Rise/fall time < 150 ps (20% to 80%)<br>$V_{ID} > 400\text{ mV}$ or<br>Input Swing = 3.0 V <sup>[9]</sup> | Offset = 1 kHz                                                                                                        | –   | –   | –120 | dBc/Hz |
|                            |                                                                                                                                                           | Offset = 10 kHz                                                                                                       | –   | –   | –135 | dBc/Hz |
|                            |                                                                                                                                                           | Offset = 100 kHz                                                                                                      | –   | –   | –135 | dBc/Hz |
|                            |                                                                                                                                                           | Offset = 1 MHz                                                                                                        | –   | –   | –150 | dBc/Hz |
|                            |                                                                                                                                                           | Offset = 10 MHz                                                                                                       | –   | –   | –154 | dBc/Hz |
|                            |                                                                                                                                                           | Offset = 20 MHz                                                                                                       | –   | –   | –155 | dBc/Hz |

### Notes

9. Refer to [Application Information on page 10](#).
10. Refer to [Figure 5 on page 8](#).
11. Refer to [Figure 6 on page 8](#).
12. Refer to [Figure 7 on page 9](#).

## AC Electrical Specifications (continued)

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$  (Commercial) or  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$  (Industrial))

| Parameter         | Description                              | Condition                                                                                                                                      | Min | Typ | Max  | Unit |
|-------------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| $t_{JIT}^{[13]}$  | Additive RMS phase jitter (Random)       | 156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400\text{ mV}$                                      | —   | —   | 0.11 | ps   |
|                   |                                          | 156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V <sup>[14]</sup>                  | —   | —   | 0.11 | ps   |
| $t_R, t_F^{[15]}$ | Output rise/fall time, single-ended      | 50% duty cycle at input, 20% to 80% of full swing ( $V_{OL}$ to $V_{OH}$ )<br>Input rise/fall time < 1.5 ns (20% to 80%)<br>Measured at 1 GHz. | —   | —   | 300  | ps   |
| $t_{SOD}$         | Time from clock edge to outputs disabled | Synchronous clock enable (CLK_EN) switched low                                                                                                 | —   | —   | 700  | ps   |
| $t_{SOE}$         | Time from clock edge to outputs enabled  | Synchronous clock enable (CLK_EN) switched high                                                                                                | —   | —   | 700  | ps   |

### Notes

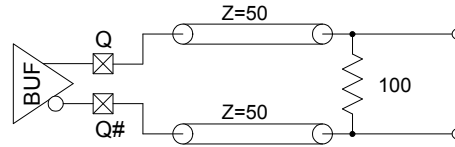
13. Refer to Figure 8 on page 9.

14. Refer to Application Information on page 10.

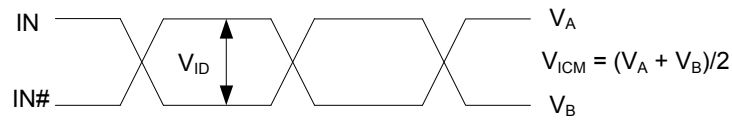
15. Refer to Figure 9 on page 9.

## Switching Waveforms

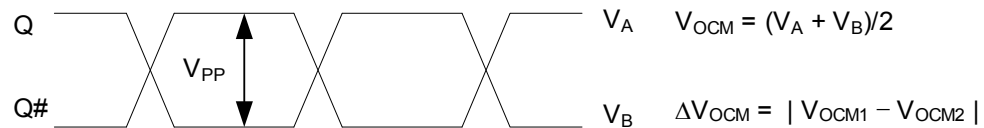
**Figure 2. LVDS Output Termination**



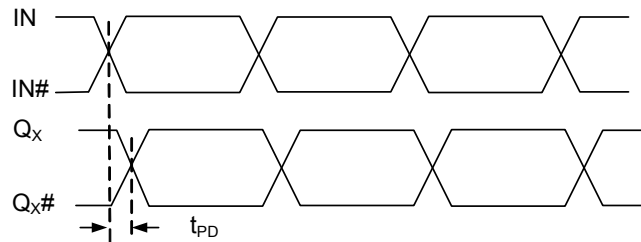
**Figure 3. Input Differential and Common Mode Voltages**



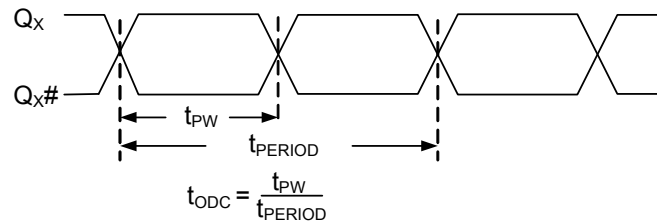
**Figure 4. Output Differential and Common Mode Voltages**



**Figure 5. Input to Any Output Pair Propagation Delay**



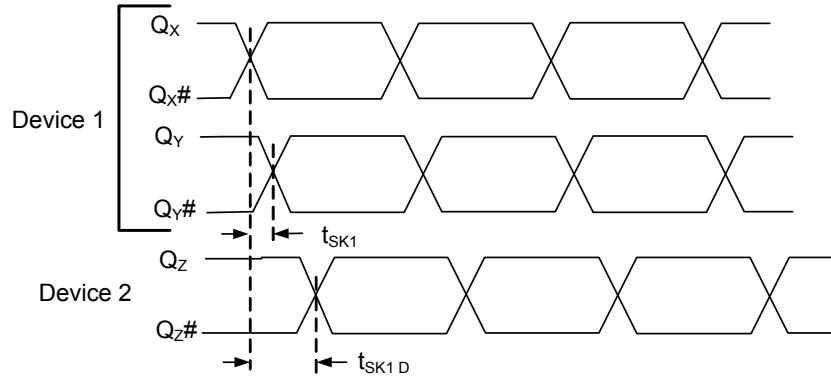
**Figure 6. Output Duty Cycle**



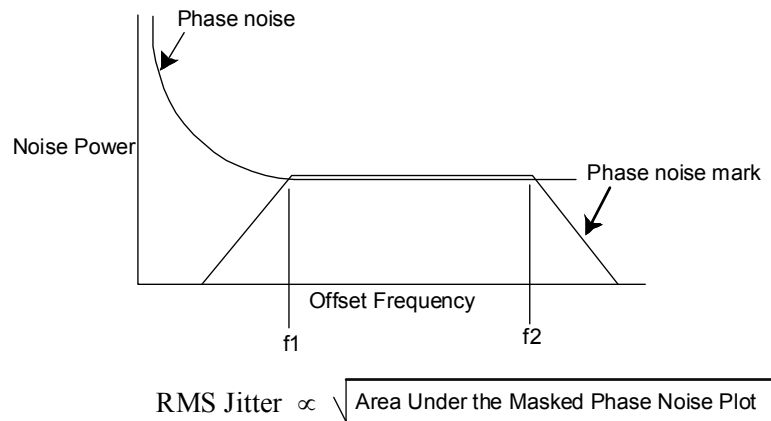


## Switching Waveforms (continued)

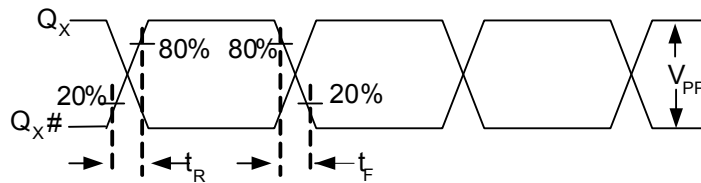
**Figure 7. Output-to-output and Device-to-device Skew**



**Figure 8. RMS Phase Jitter**

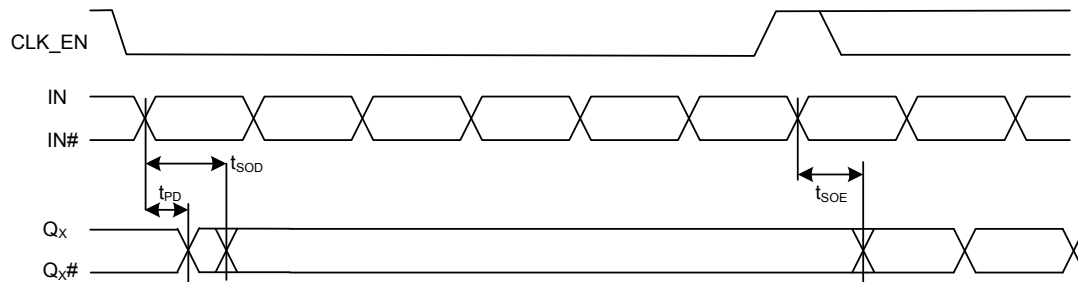


**Figure 9. Output Rise/Fall Time**



## Switching Waveforms (continued)

**Figure 10. Synchronous Clock Enable Timing**



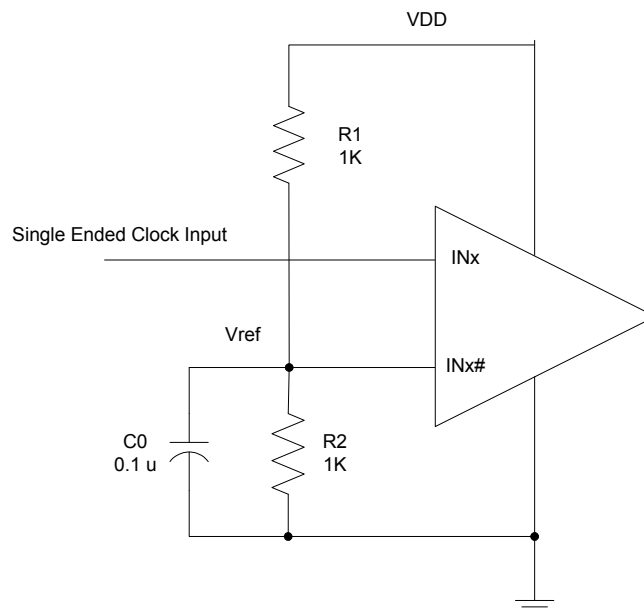
## Application Information

CY2DL1504 can be used with a single ended CMOS input by biasing the Complementary Input Clock (INx#). “True” input pins (INx) of differential input pair can be fed with a single ended CMOS input signal. The “complementary” input pin (INx#) of the same differential input pair can be biased with Vref.

Figure 11 shows the schematic which can be used to give single ended CMOS input to the CY2DL1504.

The reference voltage  $V_{ref} = VDD/2$  is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and  $VDD = 3.3$  V,  $V_{ref}$  should be 1.25 V and  $R2/R1 = 0.609$ .

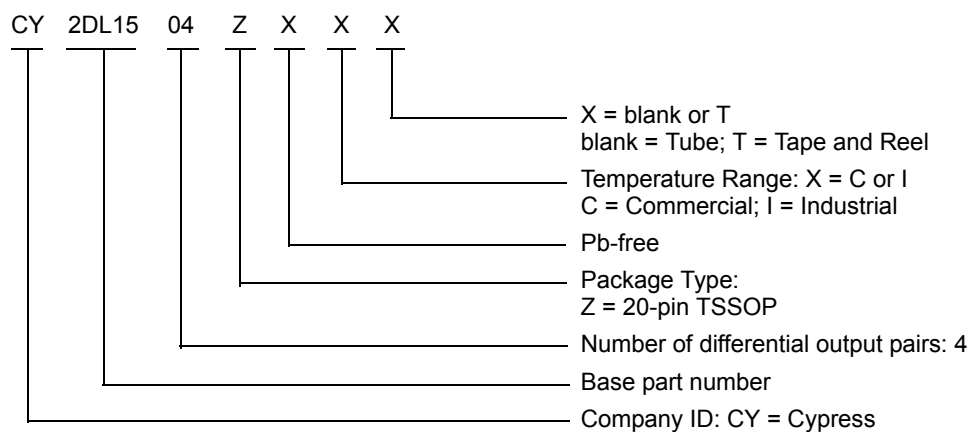
**Figure 11. Single ended CMOS input given to the CY2DL1504**



## Ordering Information

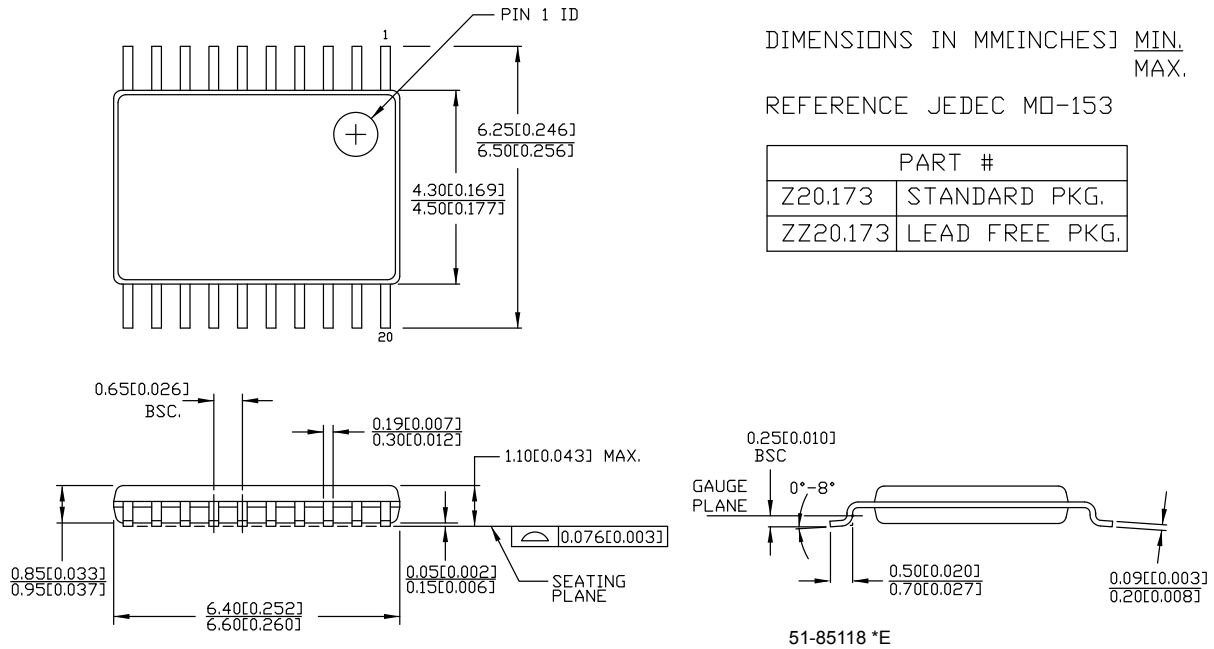
| Part Number    | Type         | Production Flow             |
|----------------|--------------|-----------------------------|
| <b>Pb-free</b> |              |                             |
| CY2DL1504ZXC   | 20-pin TSSOP | Commercial, 0 °C to 70 °C   |
| CY2DL1504ZXCT  | 20-pin TSSOP | Commercial, 0 °C to 70 °C   |
| CY2DL1504ZXI   | 20-pin TSSOP | Industrial, -40 °C to 85 °C |
| CY2DL1504ZXIT  | 20-pin TSSOP | Industrial, -40 °C to 85 °C |

## Ordering Code Definitions



## Package Diagram

Figure 12. 20-pin TSSOP (4.40 mm Body) Z20.173/ZZ20.173 Package Outline, 51-85118



## Acronyms

| Acronym | Description                                         |
|---------|-----------------------------------------------------|
| ESD     | electrostatic discharge                             |
| HBM     | human body model                                    |
| HCSL    | high-speed current steering logic                   |
| JEDEC   | joint electron devices engineering council          |
| LVDS    | low-voltage differential signal                     |
| LVC MOS | low-voltage complementary metal oxide semiconductor |
| LVPECL  | low-voltage positive emitter-coupled logic          |
| LV TTL  | low-voltage transistor-transistor logic             |
| OE      | output enable                                       |
| RMS     | root mean square                                    |
| TSSOP   | thin shrunk small outline package                   |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure                  |
|--------|----------------------------------|
| °C     | degree Celsius                   |
| dBc    | decibels relative to the carrier |
| GHz    | gigahertz                        |
| Hz     | hertz                            |
| kΩ     | kilohm                           |
| MHz    | megahertz                        |
| μA     | microampere                      |
| μF     | microfarad                       |
| μs     | microsecond                      |
| mA     | milliampere                      |
| ms     | millisecond                      |
| mV     | millivolt                        |
| ns     | nanosecond                       |
| Ω      | ohm                              |
| pF     | picofarad                        |
| ps     | picosecond                       |
| V      | volt                             |
| W      | watt                             |

## Document History Page

| Document Title: CY2DL1504, 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input<br>Document Number: 001-56312 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                 | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| **                                                                                                                       | 2782891 | CXQ             | 10/09/09        | New data sheet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| *A                                                                                                                       | 2838613 | CXQ             | 01/05/2010      | <p>Changed status from Advance to Preliminary.</p> <p>Changed from 0.34 ps to 0.25 ps maximum additive jitter in "Features" on page 1 and in <math>t_{JIT}</math> in the AC Electrical Specs table on page 5.</p> <p>Added <math>t_{PU}</math> spec to the Operating Conditions table on page 3.</p> <p>Changed max <math>I_{DD}</math> spec in the DC Electrical Specs table on page 4 from 60 mA to 61 mA.</p> <p>Removed <math>V_{OD}</math> and <math>\Delta V_{OD}</math> specs from the DC Electrical Specs table on page 4.</p> <p>Changed <math>I_{OZ}</math> in the DC Electrical Specs table on page 4 from min of -10 uA to -15 uA and from max of 10 uA to 15 uA.</p> <p>Added <math>R_P</math> spec in the DC Electrical Specs table on page 4. Min = 60 k<math>\Omega</math>, Max = 140 k<math>\Omega</math>.</p> <p>Added a measurement definition for <math>C_{IN}</math> in the DC Electrical Specs table on page 4.</p> <p>Added <math>V_{PP}</math> and <math>\Delta V_{PP}</math> specs to the AC Electrical Specs table on page 5. <math>V_{PP}</math> min = 250 mV and max = 470 mV; <math>\Delta V_{PP}</math> max = 50 mV.</p> <p>Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS.</p> <p>Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5.</p> <p>Added condition to <math>t_R</math> and <math>t_F</math> specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%).</p> <p>Changed letter case and some names of all the timing parameters in Figures 4, 5, 6, 7 and 9, to be consistent with EROS. Updated Figure 4 with definition for <math>V_{PP}</math> and <math>\Delta V_{PP}</math>.</p> |
| *B                                                                                                                       | 3010332 | CXQ             | 08/18/2010      | <p>Changed from 0.25 ps to 0.11 ps maximum additive jitter in "Features" on page 1 and in <math>t_{JIT}</math> in the AC Electrical Specs table on page 5.</p> <p>Added "Functional equivalent to ICS8543i" to the "Features" section.</p> <p>Changed pin 13 in Figure 1 and Table 1 from <math>V_{DD}</math> to <math>V_{SS}</math>.</p> <p>Changed pin 8 description in Table 1 from "high impedance" to "disabled".</p> <p>Added note 6 to describe <math>I_{IH}</math> and <math>I_{IL}</math> specs.</p> <p>Removed reference to data distribution from "Functional Description".</p> <p>Changed <math>R_P</math> for diff inputs from 100 k<math>\Omega</math> to 150 k<math>\Omega</math> in the Logic Block Diagram and from 60 k<math>\Omega</math> min / 140 k<math>\Omega</math> max to 90 k<math>\Omega</math> min / 210 k<math>\Omega</math> max in the DC Electrical Specs table.</p> <p>Split <math>V_{ID}</math> into separate specs in DC Electrical Specs table: 0.4 V min and 0.8 V max for LVDS, 0.4 V min and 1.0 V max for LVPECL.</p> <p>Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table.</p> <p>Added "Frequency range up to 1 GHz" condition to <math>t_{ODC}</math> spec.</p> <p>Changed <math>t_{OD}</math> in the AC Electrical Specs table from 3 ns max to 5 ns max.</p> <p>Added Acronyms and Ordering Code Definition.</p>                                                                                                                                                                                                                                                                                                                                                  |

**Document History Page** (continued)

| Document Title: CY2DL1504, 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input<br>Document Number: 001-56312 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                 | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *C                                                                                                                       | 3090644 | CXQ             | 11/19/2010      | Changed $V_{IN}$ and $V_{OUT}$ specs from 4.0V to "lesser of 4.0 or $V_{DD} + 0.4$ "<br>Removed 200mA min LU spec, replaced with "Meets or exceeds JEDEC Spec JESD78B IC Latchup Test"<br>Added " $V_{OUT} = 0.75V - 1.75V$ " to $I_{OZ}$ comments.<br>Moved $V_{PP}$ from AC spec table to DC spec table, removed $\Delta V_{PP}$ .<br>Removed $R_P$ spec for differential input clock pins $IN_X$ and $IN_{X\#}$ .<br>Changed $C_{IN}$ condition to "Measured at 10 MHz".<br>Changed $PN_{ADD}$ specs for 10kHz, 10MHz, and 20MHz offsets.<br>Added "Measured at 1 GHz" to $t_R$ , $t_F$ spec condition.<br>Removed specs $t_S$ , $t_H$ , $t_{OD}$ , and $t_{OE}$ from AC spec table.<br>Removed $\Delta V_{PP}$ reference from Figure 4.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| *D                                                                                                                       | 3135189 | CXQ             | 01/12/2011      | Changed status from Preliminary to Final.<br>Removed "Functional equivalent" bullet on page 1.<br>Added "(see $I_{OZ}$ )" note to pin 8 description in <a href="#">Pin Definitions</a> .<br>Fixed typo and removed resistors from $IN_X/IN_{X\#}$ in <a href="#">Logic Block Diagram</a> .<br>Added <a href="#">Figure 10</a> to describe $T_{SOE}$ and $T_{SOD}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *E                                                                                                                       | 3090938 | CXQ             | 02/25/11        | Post to external web.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *F                                                                                                                       | 3208968 | CXQ             | 03/29/2011      | Changed $R_P$ max from 140 k $\Omega$ to 165 k $\Omega$ and updated $R_P$ in <a href="#">Logic Block Diagram</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *G                                                                                                                       | 3308039 | CXQ             | 07/11/2011      | Updated supported differential input clock types to include CML in Features, Functional Description, Pin Definitions, and DC specs table sections.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *H                                                                                                                       | 3395868 | PURU            | 10/05/11        | Updated supported differential input clock types to include HCSL in <a href="#">Features</a> , <a href="#">Pinouts</a> , and <a href="#">DC Electrical Specifications</a> table.<br>Changed Min value of $V_{ICM}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| *I                                                                                                                       | 3892255 | PURU            | 02/01/2013      | Updated <a href="#">Features</a> (Added "Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on $IN_{X\#}$ input").<br>Updated <a href="#">AC Electrical Specifications</a> :<br>Added Note 9 and Note 14.<br>Added $F_{IN}$ parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz).<br>Added $F_{OUT}$ parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz).<br>Added $t_{ODC}$ parameter values for "Single Ended Input" condition (Minimum value = 45%, Maximum value = 55%).<br>Updated Description of $PN_{ADD}$ parameter (Replaced "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400$ mV" with "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400$ mV or Input Swing = 3.0 V <sup>[9]</sup> ").<br>Added $t_{JIT}$ parameter values for the Condition "156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V <sup>[14]</sup> " (Maximum value = 0.11 ps).<br>Added <a href="#">Application Information</a> .<br>Updated to new template. |
| *J                                                                                                                       | 4587249 | PURU            | 12/04/2014      | Updated <a href="#">Functional Description</a> :<br>Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end.<br>Updated <a href="#">Package Diagram</a> :<br>spec 51-85118 – Changed revision from *D to *E.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *K                                                                                                                       | 5267558 | PSR             | 05/13/2016      | Added <a href="#">Thermal Resistance</a> .<br>Updated to new template.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *L                                                                                                                       | 5962077 | AESATMP8        | 11/09/2017      | Updated logo and Copyright.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

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