EFM32®

... the world's most energy friendly microcontrollers

EFM32TG108 DATASHEET

F32/F16/F8/F4

- **ARM Cortex-M3 CPU platform**
  - High Performance 32-bit processor @ up to 32 MHz
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 1.0 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 51 µA/MHz @ 3 V Sleep Mode
  - 150 µA/MHz @ 3 V Run Mode, with code executed from flash
- **32/16/8/4 KB Flash**
- **4/4/2/2 KB RAM**
- **17 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 11 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Timers/Counters**
  - 2× 16-bit Timer/Counter
    - 2×3 Compare/Capture/PWM channels
  - 16-bit Low Energy Timer
  - 1× 24-bit Real-Time Counter
  - 1× 16-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Communication interfaces**
  - Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 2× Analog Comparator
    - Capacitive sensing with up to 4 inputs
  - Supply Voltage Comparator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
  - 1-pin Serial Wire Viewer
- **Pre-Programmed UART Bootloader**
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.98 to 3.8 V**
- **QFN24 package**

32-bit ARM Cortex-M0+, Cortex-M3 and Cortex-M4 microcontrollers for:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32TG108 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32TG108F4-QFN24	4	2	32	1.98 - 3.8	-40 - 85	QFN24
EFM32TG108F8-QFN24	8	2	32	1.98 - 3.8	-40 - 85	QFN24
EFM32TG108F16-QFN24	16	4	32	1.98 - 3.8	-40 - 85	QFN24
EFM32TG108F32-QFN24	32	4	32	1.98 - 3.8	-40 - 85	QFN24

Visit **www.silabs.com** for information on global distributors and representatives.

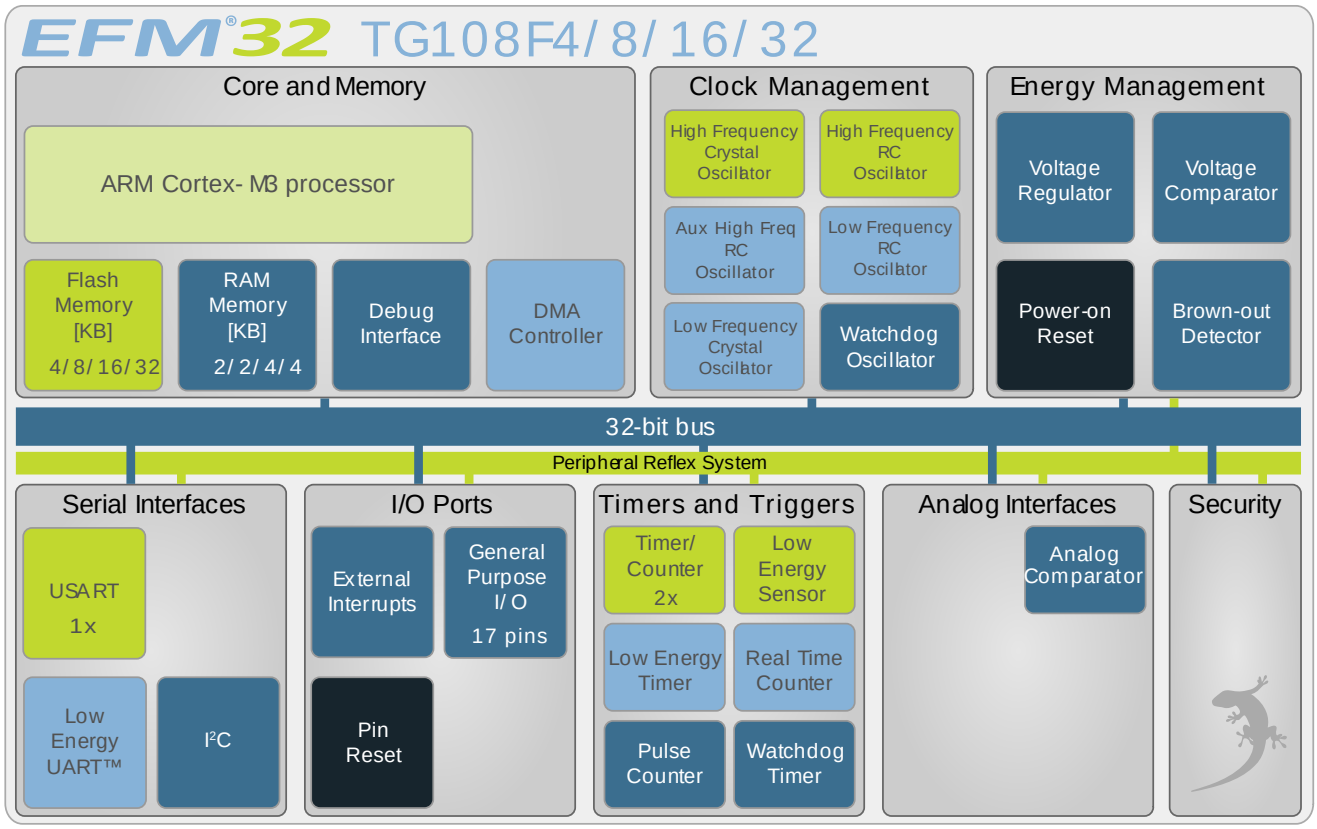
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG108 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32TG Reference Manual*.

A block diagram of the EFM32TG108 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32TG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32TG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32TG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.20 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE), is a highly configurable sensor interface with support for up to 4 individually configurable sensors. By controlling the analog comparators, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure resistive and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.21 General Purpose Input/Output (GPIO)

In the EFM32TG108, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 11 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32TG108 is a subset of the feature set described in the EFM32TG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

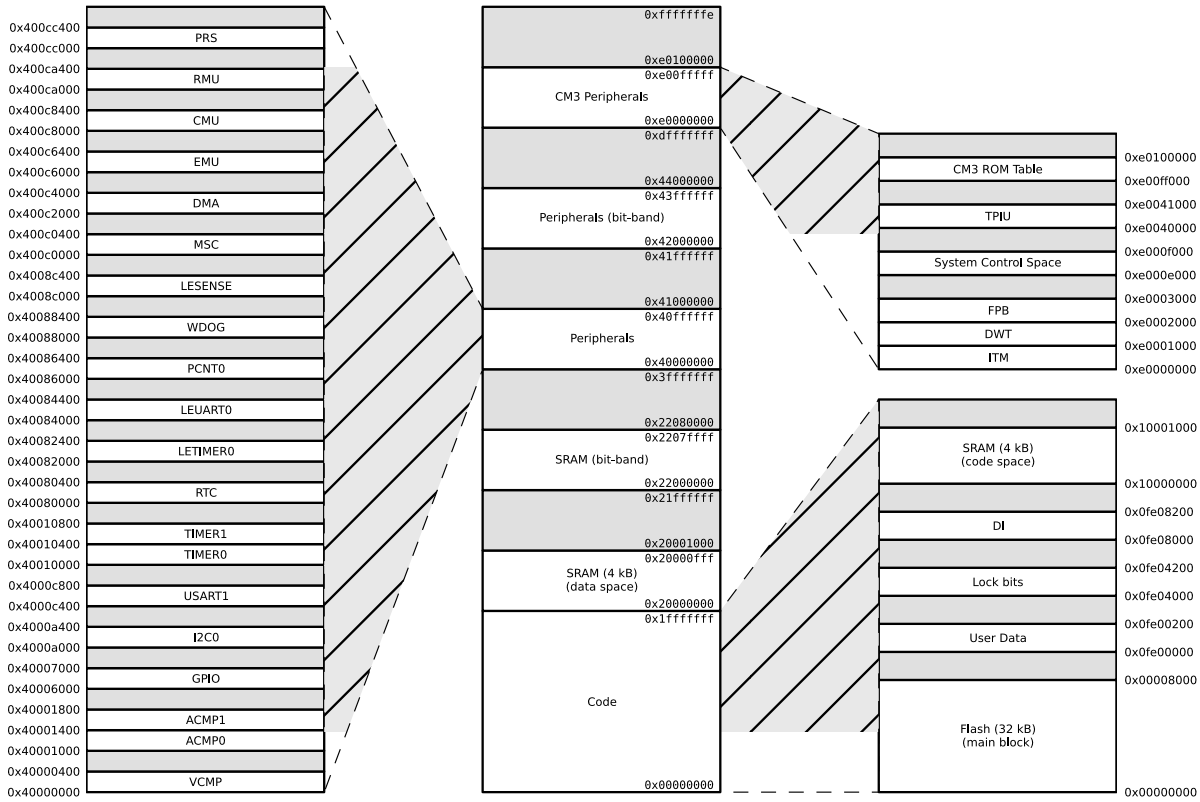
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA

Module	Configuration	Pin Connections
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[1:0], ACMP1_O
VCMP	Full configuration	NA
GPIO	17 pins	Available pins are shown in Table 4.3 (p. 33)

2.3 Memory Map

The *EFM32TG108* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32TG108 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		157		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		150	170	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		153	172	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		155	175	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		157	178	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		162	183	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		200	240	µA/MHz
I_{EM1}	EM1 current (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		53		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		51	57	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		55	59	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		56	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		58	63	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		63	68	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V		100	122	µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		1.0	1.2	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		2.4	5.0	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.59	1.0	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.0	4.5	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02	0.055	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.25	0.70	µA

Figure 3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.

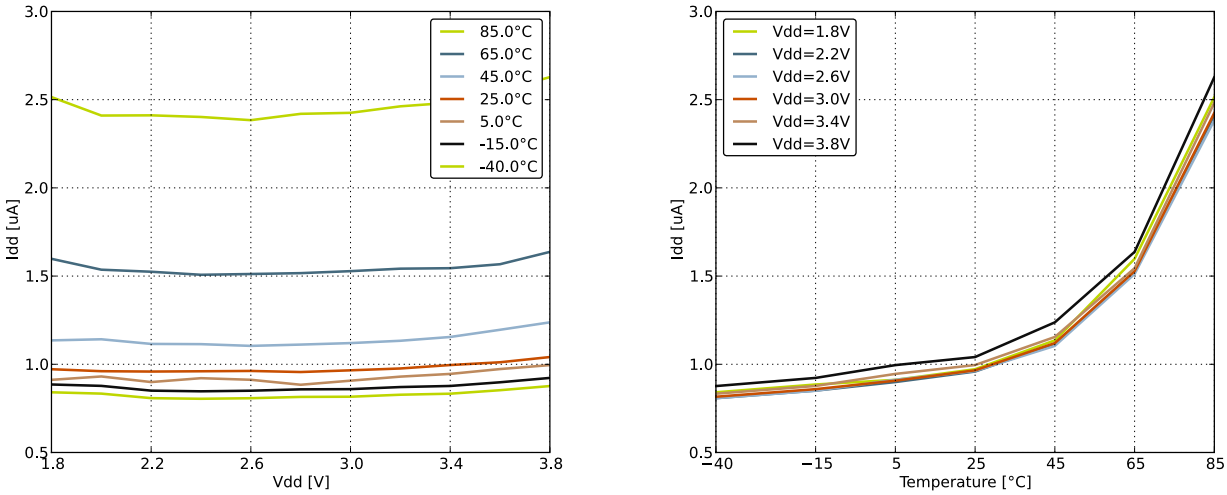


Figure 3.2. EM3 current consumption.

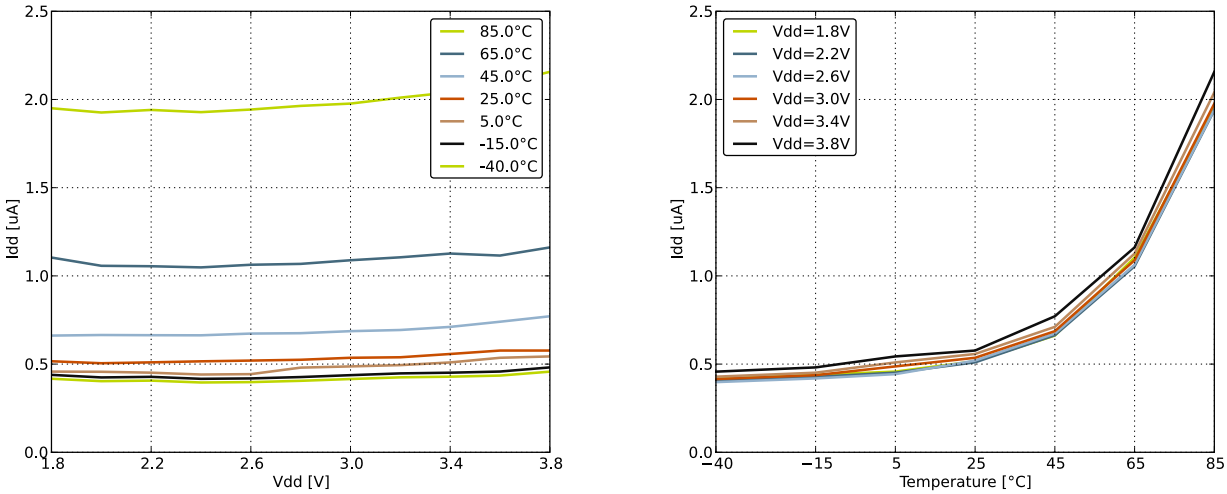
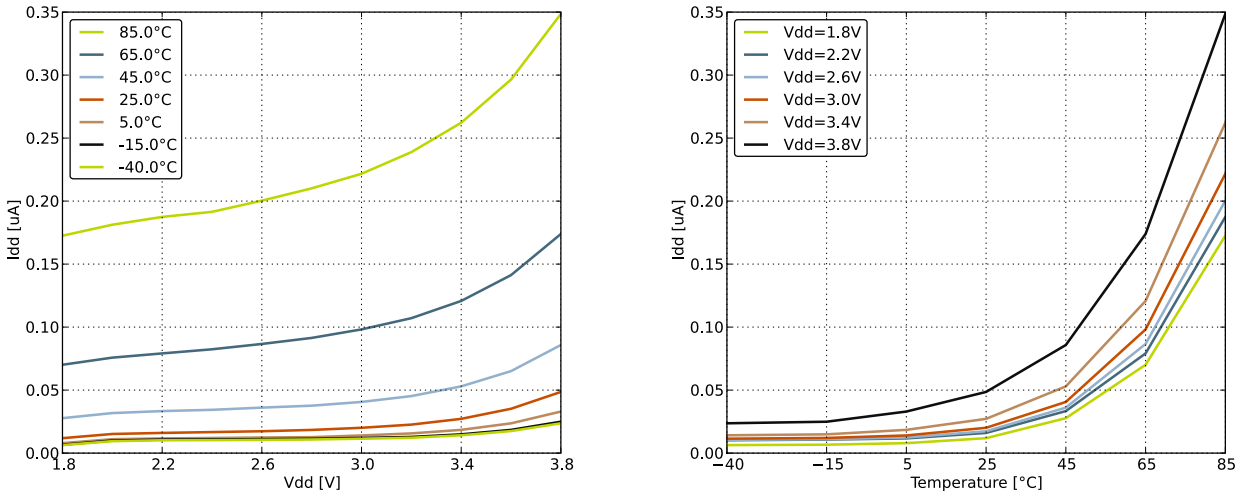


Figure 3.3. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

3.6 Power Management

The EFM32TG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{P_ERASE}	Page erase time		20	20.4	20.8	ms
t_{D_ERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

[1]Measured at 25°C

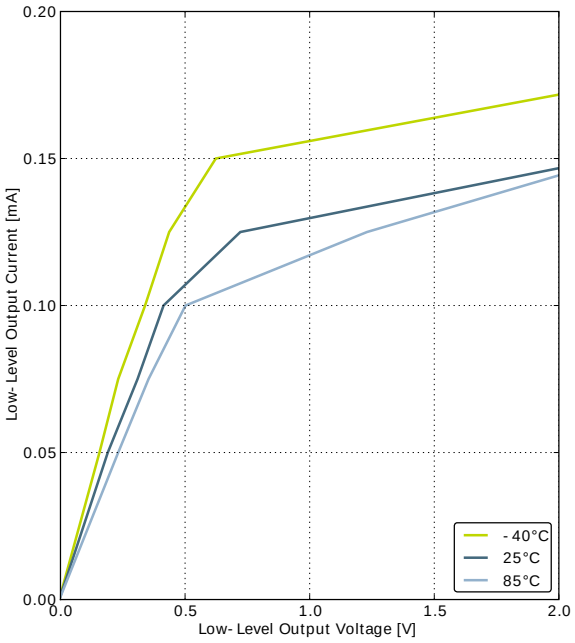
3.8 General Purpose Input Output

Table 3.7. GPIO

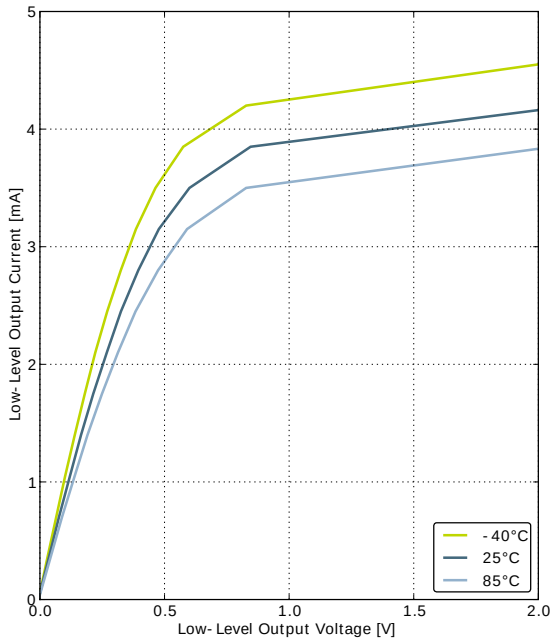
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				$0.30V_{DD}$	V
V_{IOIH}	Input high voltage		$0.70V_{DD}$			V
V_{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.80V_{DD}$		V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.90V_{DD}$		V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.85V_{DD}$		V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.90V_{DD}$		V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75V_{DD}$			V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85V_{DD}$			V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60V_{DD}$			V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V_{DD}			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V_{DD}		V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V_{DD}		V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.20V_{DD}	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V_{DD}		±0.1	±100	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.98 - 3.8 V	0.1V_{DD}			V

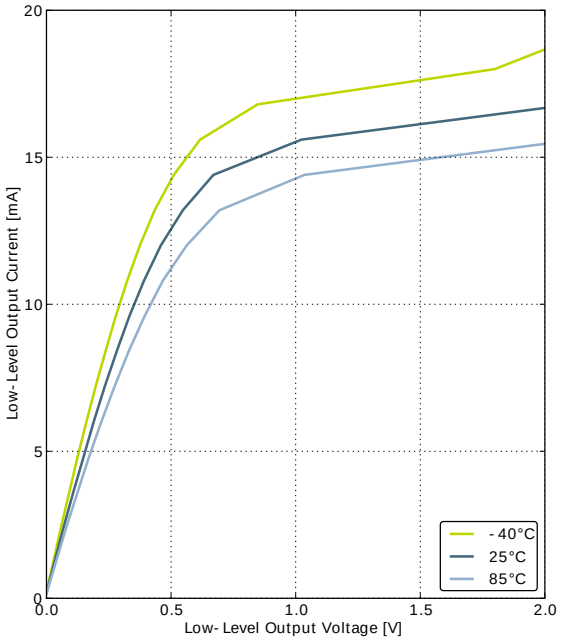
Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage



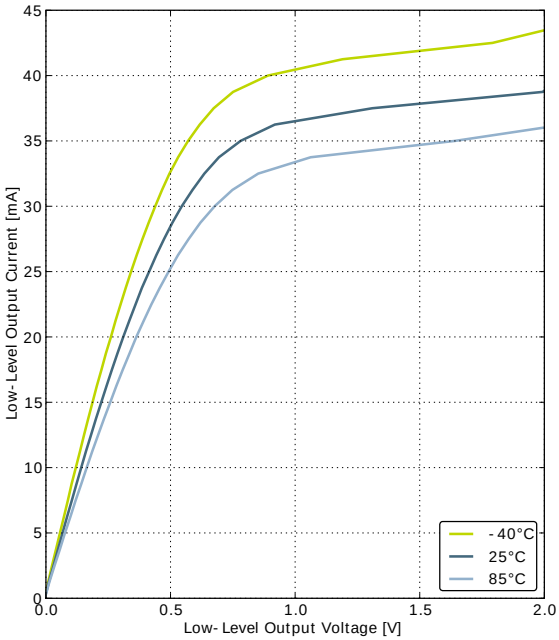
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

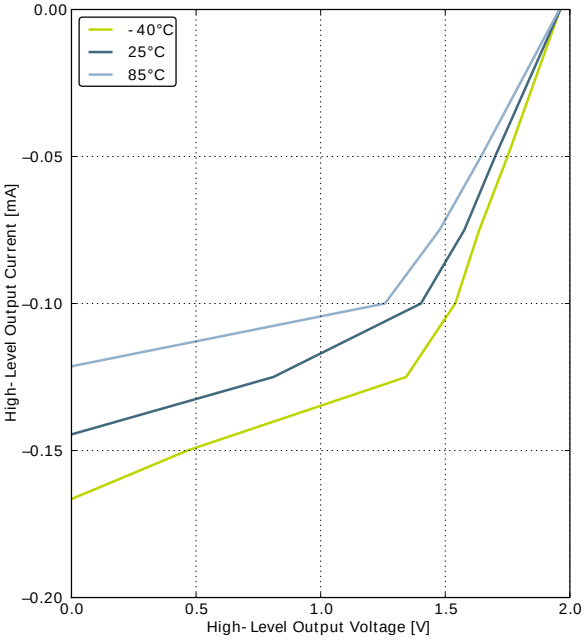


GPIO_Px_CTRL DRIVEMODE = STANDARD

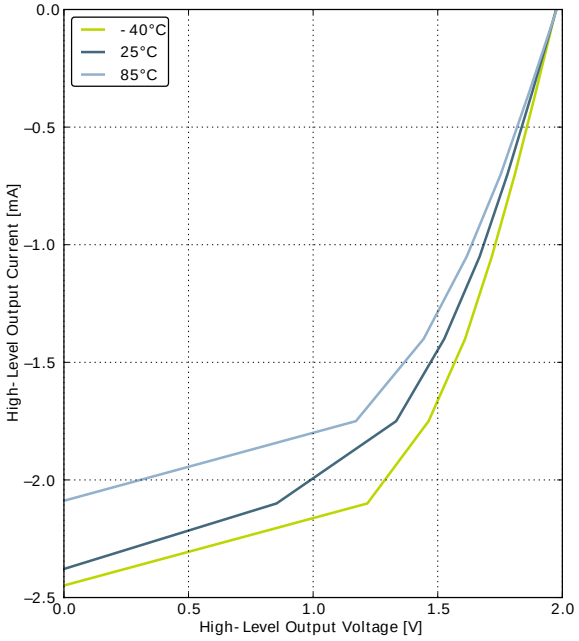


GPIO_Px_CTRL DRIVEMODE = HIGH

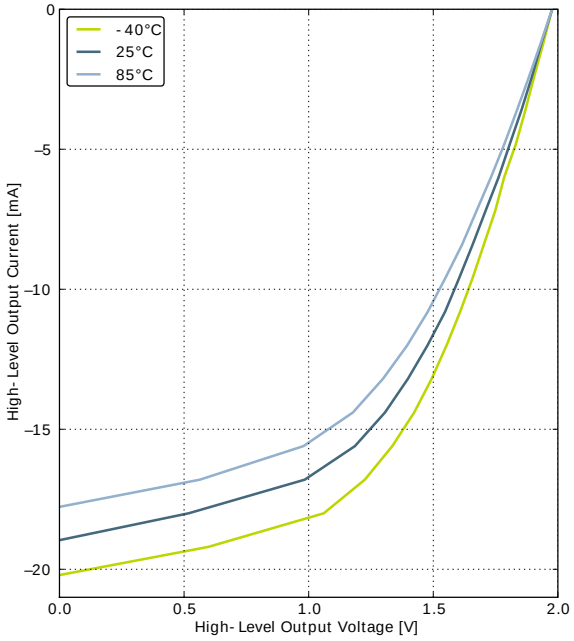
Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



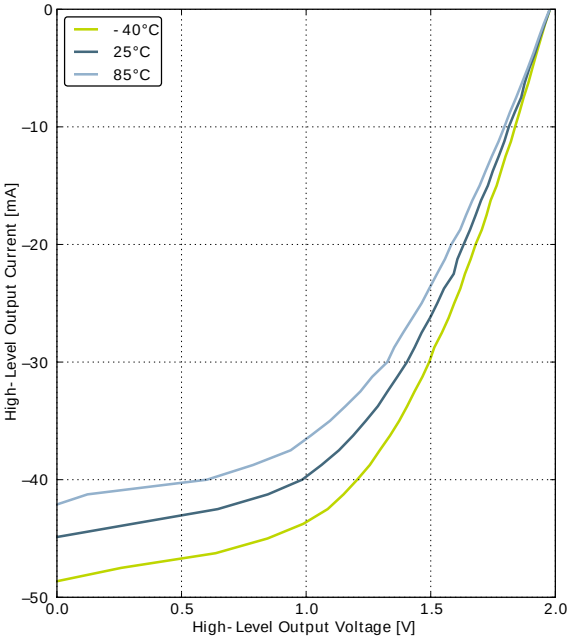
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

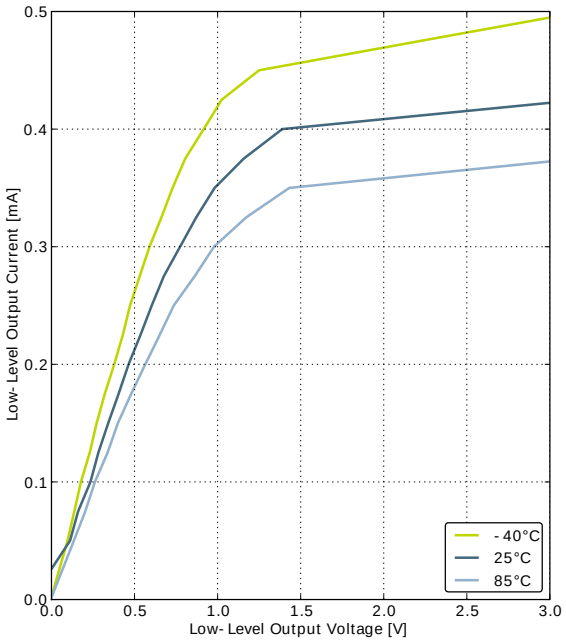


GPIO_Px_CTRL DRIVEMODE = STANDARD

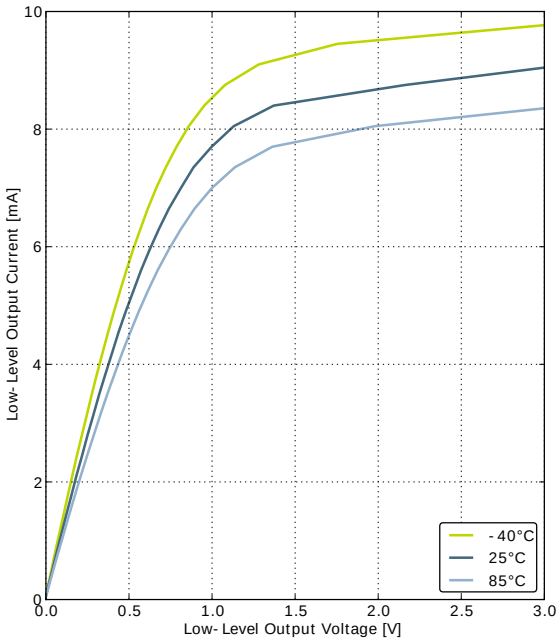


GPIO_Px_CTRL DRIVEMODE = HIGH

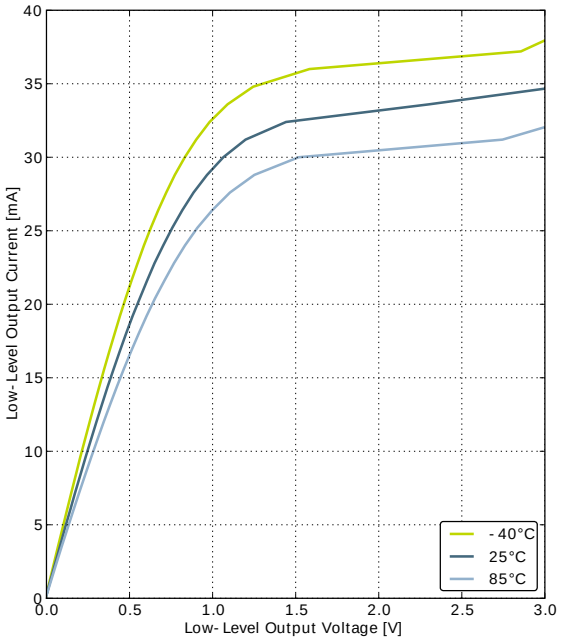
Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



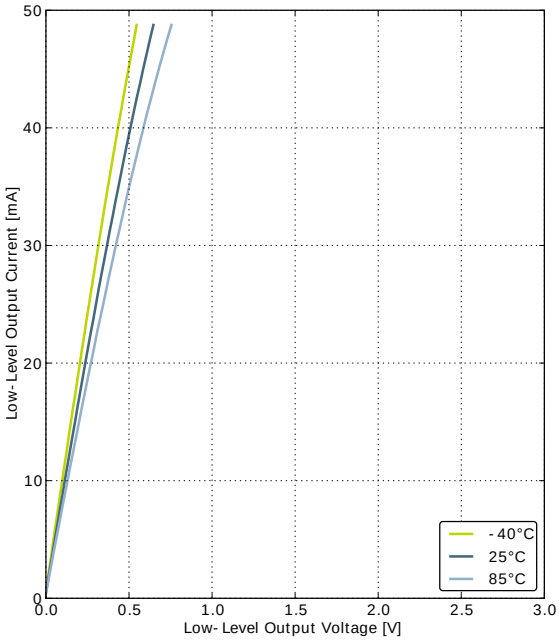
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

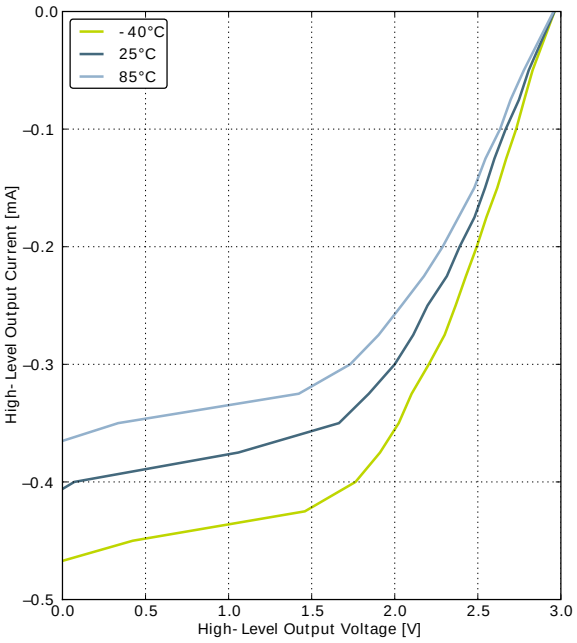


GPIO_Px_CTRL DRIVEMODE = STANDARD

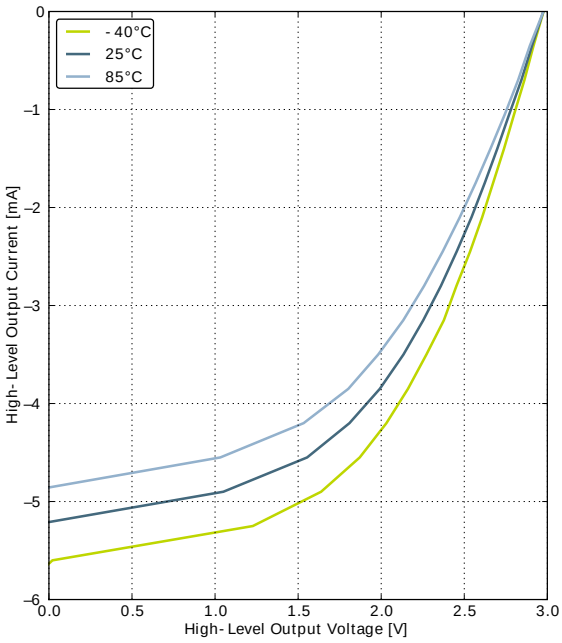


GPIO_Px_CTRL DRIVEMODE = HIGH

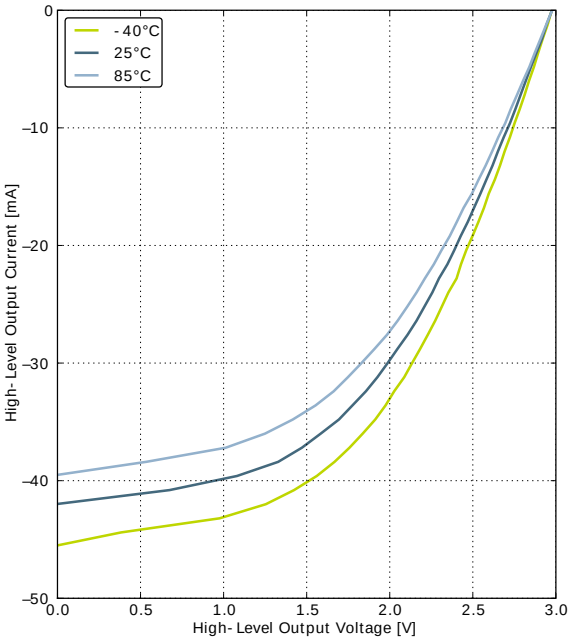
Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage



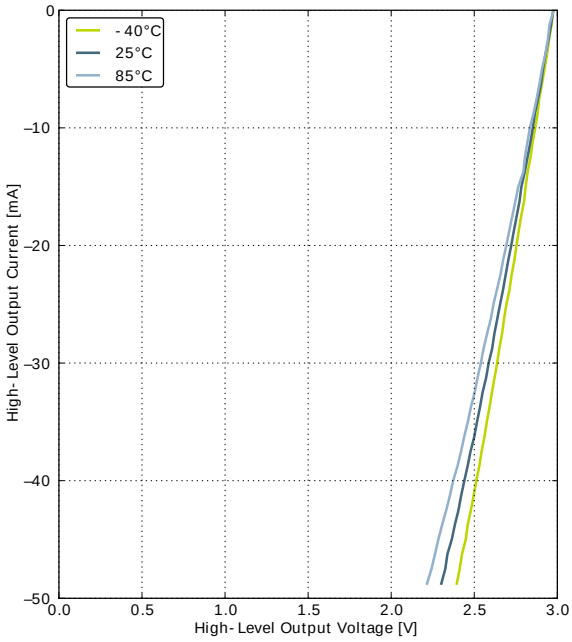
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

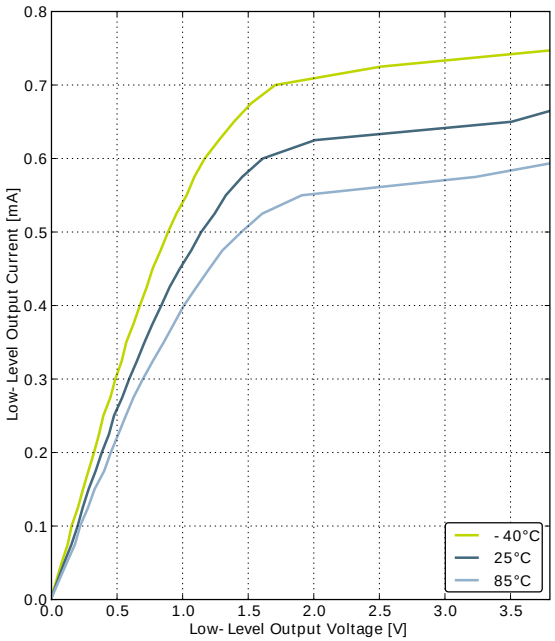


GPIO_Px_CTRL DRIVEMODE = STANDARD

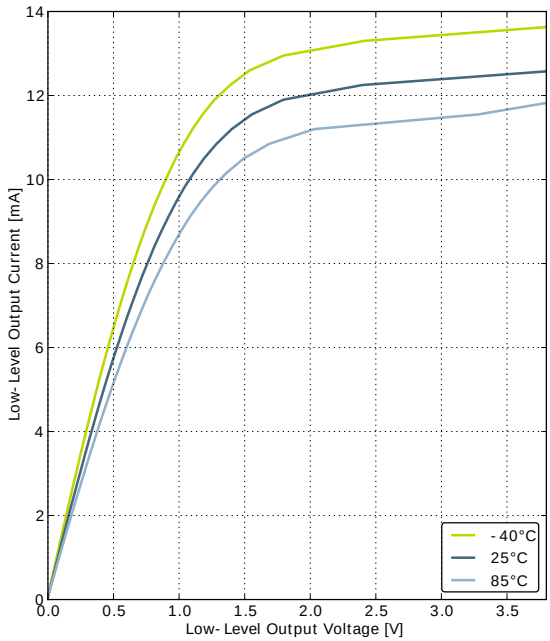


GPIO_Px_CTRL DRIVEMODE = HIGH

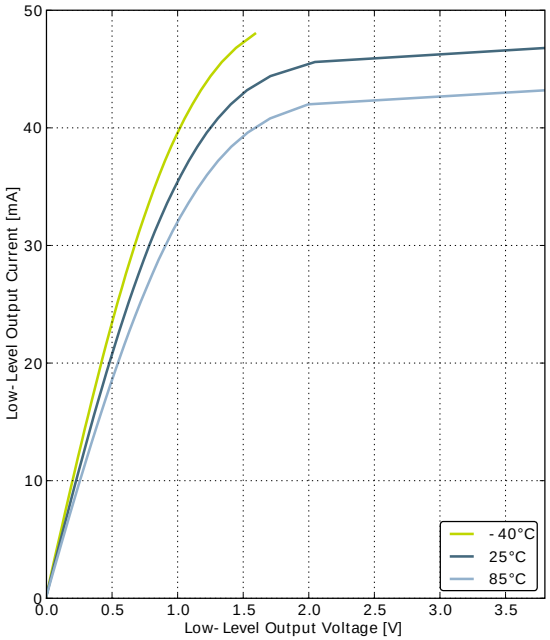
Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



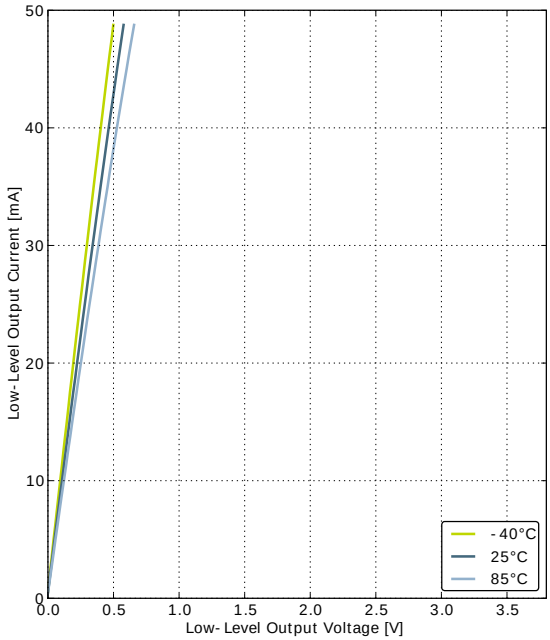
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

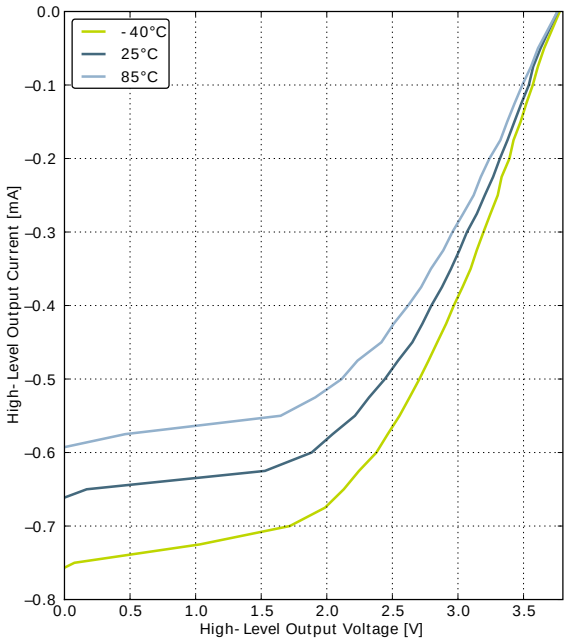


GPIO_Px_CTRL DRIVEMODE = STANDARD

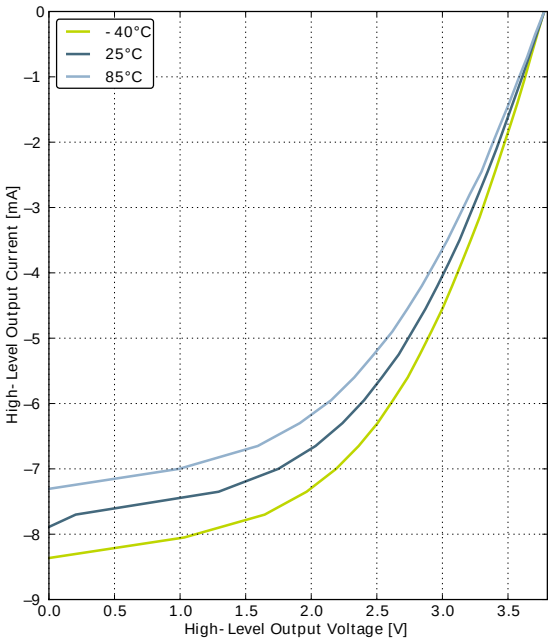


GPIO_Px_CTRL DRIVEMODE = HIGH

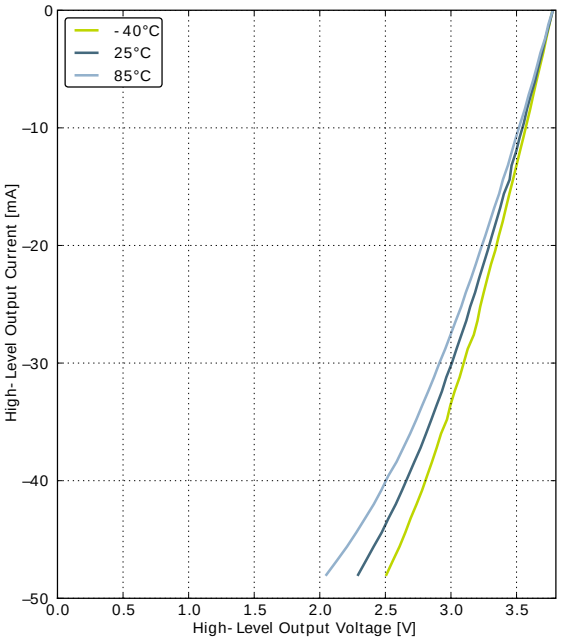
Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



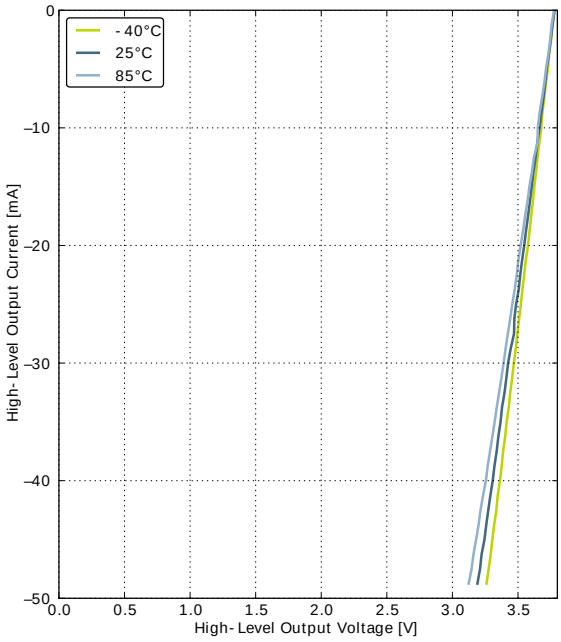
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1]See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

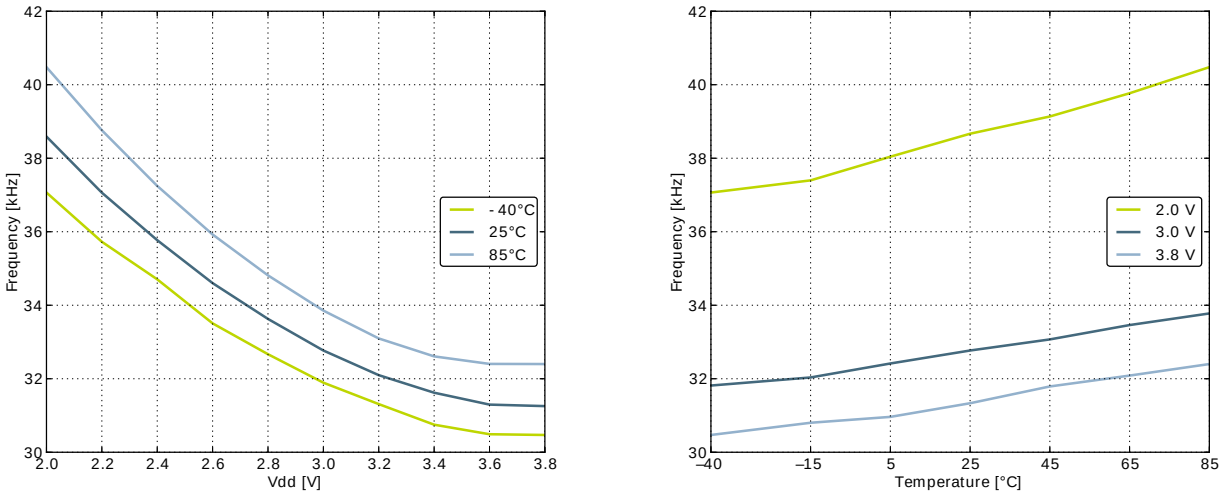
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.29	32.768	34.24	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			210	380	nA
$TUNESTEP_{LFRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	28 MHz frequency band	27.16	28.0	28.84	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40[1]	6.60[1]	6.80[1]	MHz
		1 MHz frequency band	1.16[2]	1.20[2]	1.24[2]	MHz
$t_{HFRCO_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption (Production test condition = 14 MHz)	f_{HFRCO} = 28 MHz		160	190	µA
		f_{HFRCO} = 21 MHz		125	155	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		f_{HFRCO} = 14 MHz		104	120	µA
		f_{HFRCO} = 11 MHz		94	110	µA
		f_{HFRCO} = 6.6 MHz		63	90	µA
		f_{HFRCO} = 1.2 MHz		22	32	µA
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value			0.3[3]		%

[1]For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2]For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

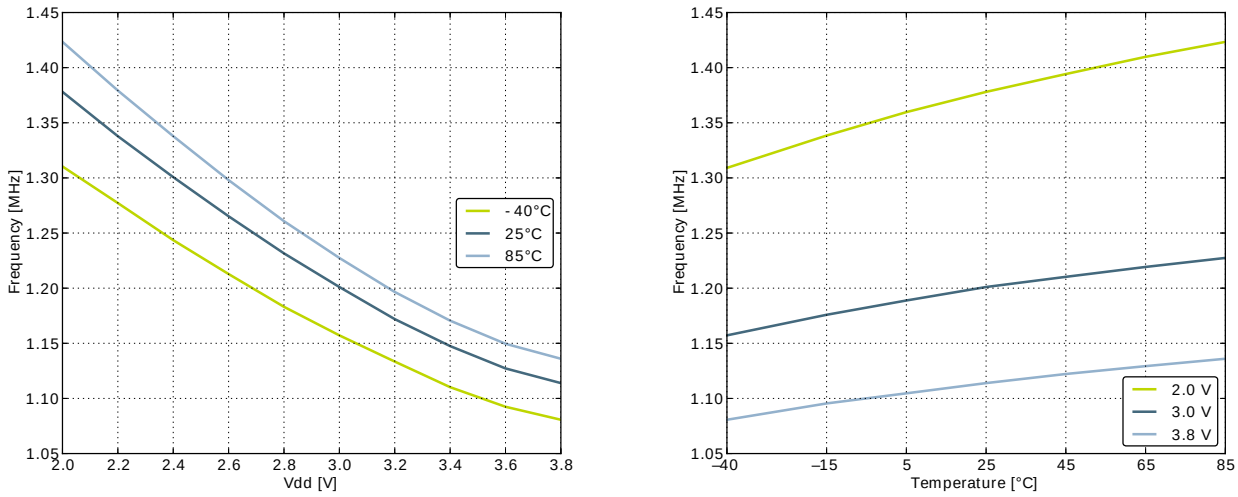


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

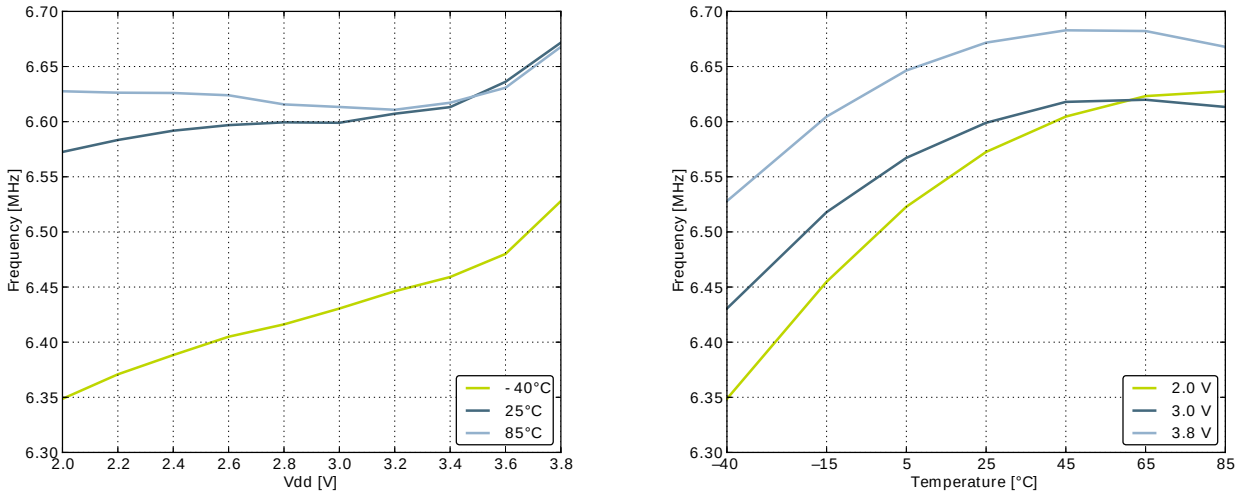


Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

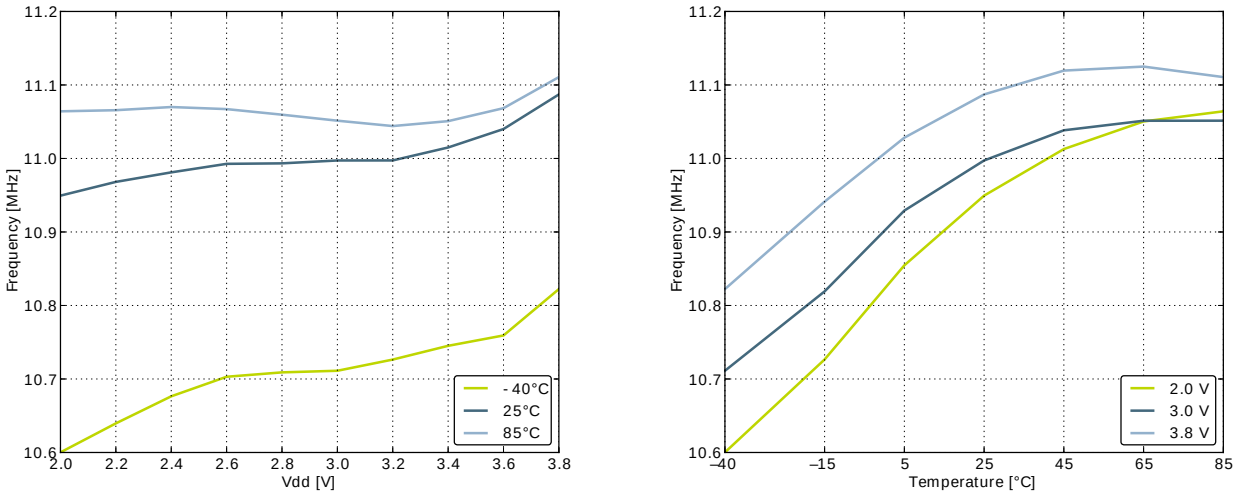


Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

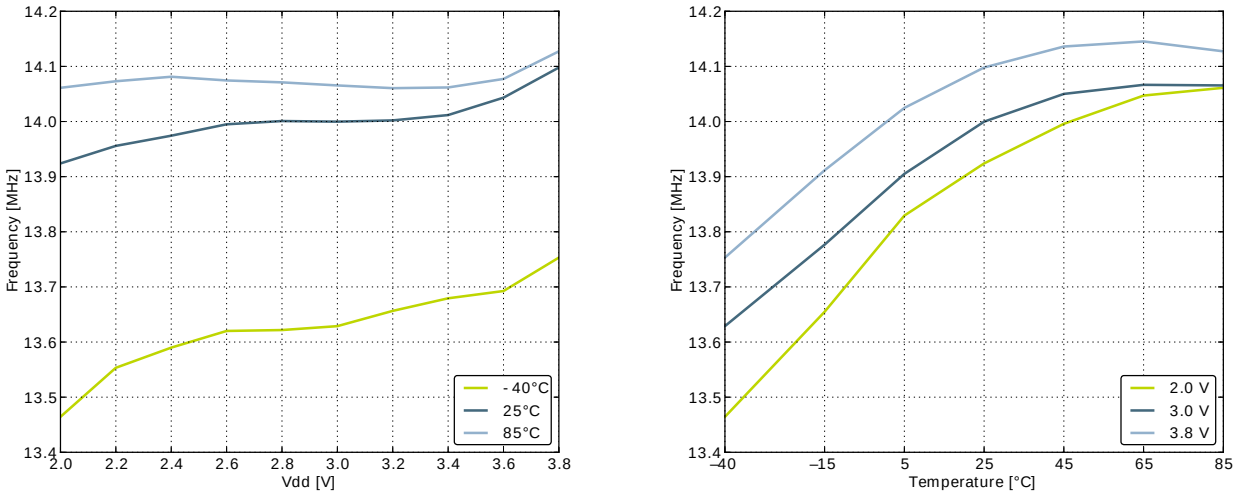


Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

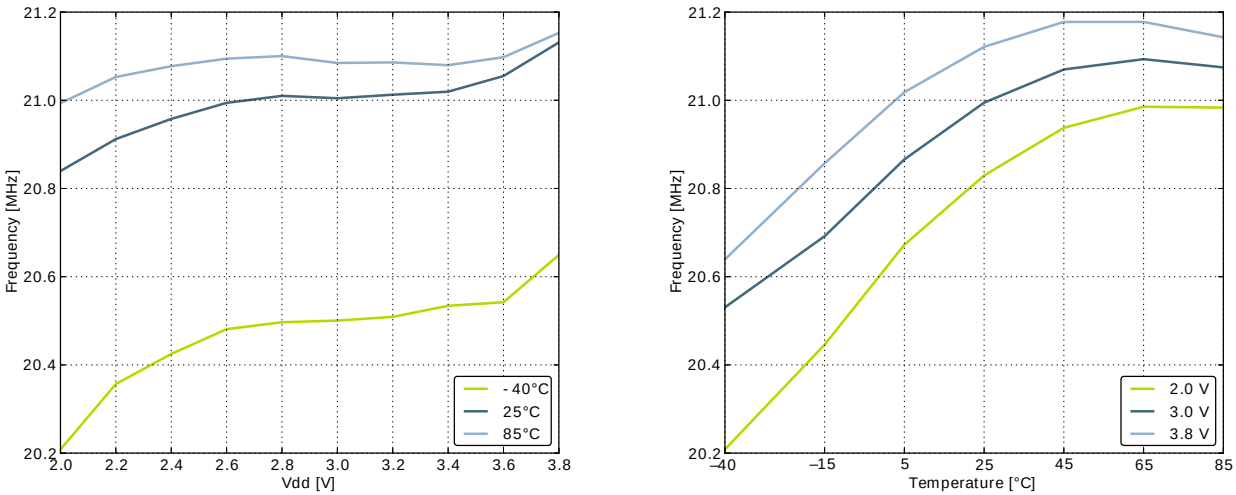
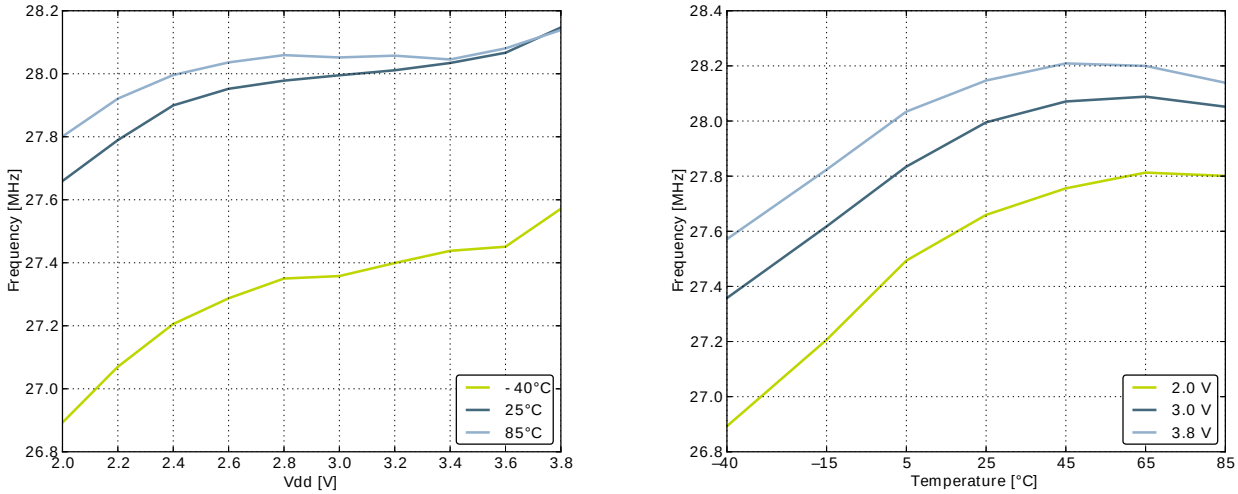


Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature



3.9.5 AUXHFRCO

Table 3.12. AUXHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{AUXHFRCO}$	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	28 MHz frequency band	27.16	28.0	28.84	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40[1]	6.60[1]	6.80[1]	MHz
		1 MHz frequency band	1.16[2]	1.20[2]	1.24[2]	MHz
$t_{AUXHFRCO_settling}$	Settling time after start-up	$f_{AUXHFRCO}$ = 14 MHz		0.6		Cycles
$TUNESTEP_{AUX-HFRCO}$	Frequency step for LSB change in TUNING value			0.3[3]		%

[1]For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2]For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3]The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

3.9.6 ULFRCO

Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Comparator (ACMP)

Table 3.14. ACMP

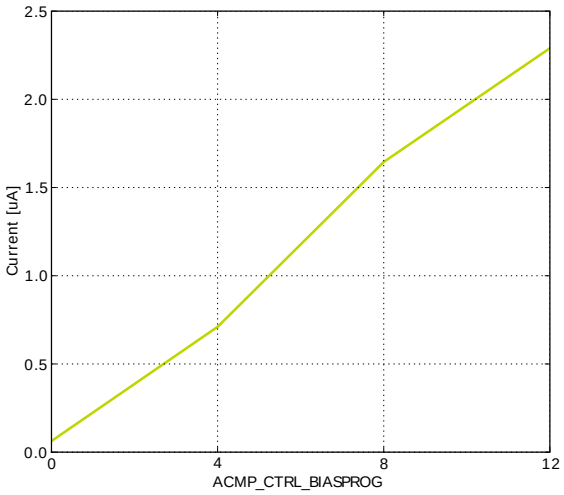
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.6	µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	12	µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0.0	0.5	µA
		Internal voltage reference		2.15	3.00	µA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	µs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 25) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

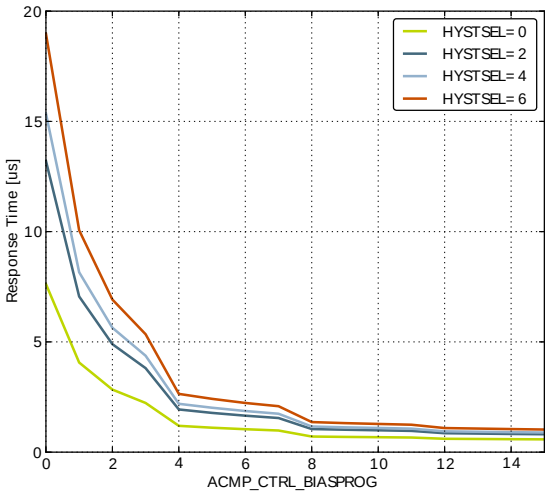
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

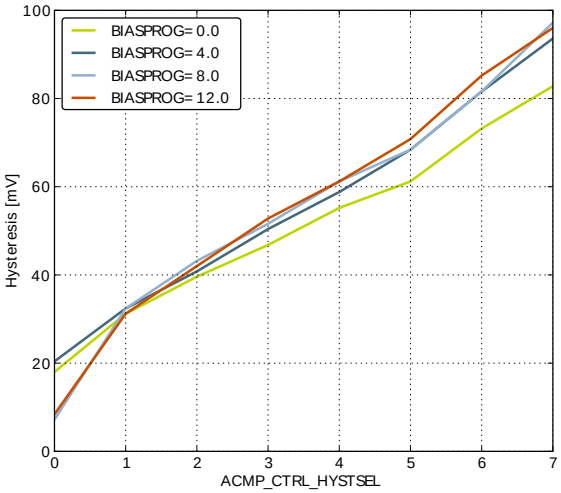
Figure 3.17. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time , V_{cm} = 1.25V, CP+ to CP- = 100mV



Hysteresis

3.11 Voltage Comparator (VCMP)

Table 3.15. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	30	µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV
$t_{VCMPSTART}$	Startup time				10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.12 I2C

Table 3.16. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		100[1]	kHz
t_{LOW}	SCL clock low time	4.7			µs
t_{HIGH}	SCL clock high time	4.0			µs
$t_{SU,DAT}$	SDA set-up time	250			ns
$t_{HD,DAT}$	SDA hold time	8		3450[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	4.7			µs
$t_{HD,STA}$	(Repeated) START condition hold time	4.0			µs
$t_{SU,STO}$	STOP condition set-up time	4.0			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32TG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 3.17. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400[1]	kHz
t_{LOW}	SCL clock low time	1.3			µs
t_{HIGH}	SCL clock high time	0.6			µs
$t_{SU,DAT}$	SDA set-up time	100			ns
$t_{HD,DAT}$	SDA hold time	8		900[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	0.6			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.6			µs
$t_{SU,STO}$	STOP condition set-up time	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32TG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 3.18. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32TG Reference Manual.

3.13 Digital Peripherals

Table 3.19. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		75		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		60		nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{RTC}	RTC current	RTC idle current, clock enabled		40		nA
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/MHz
I_{PRS}	PRS current	PRS idle current		2.81		µA/MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32TG108.

4.1 Pinout

The *EFM32TG108* pinout is shown in Figure 4.1 (p. 30) and Table 4.1 (p. 30). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32TG108 Pinout (top view, not to scale)

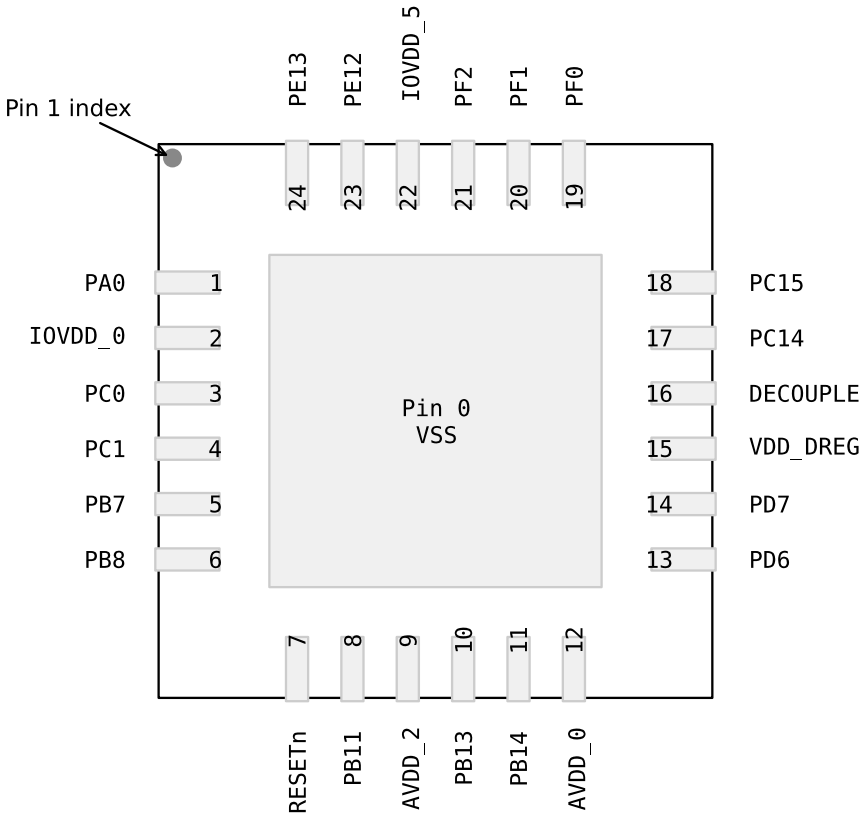


Table 4.1. Device Pinout

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
2	IOVDD_0	Digital IO power supply 0.			
3	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
4	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
5	PB7	LFXTAL_P	TIM1_CC0 #3	US1_CLK #0	
6	PB8	LFXTAL_N	TIM1_CC1 #3	US1_CS #0	
7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
8	PB11		TIM1_CC2 #3 LETIM0_OUT0 #1		
9	AVDD_2	Analog power supply 2.			
10	PB13	HFXTAL_P		LEU0_TX #1	
11	PB14	HFXTAL_N		LEU0_RX #1	
12	AVDD_0	Analog power supply 0.			
13	PD6		TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2
14	PD7		TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2
15	VDD_DREG	Power supply for on-chip voltage regulator.			
16	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
17	PC14	ACMP1_CH6	TIM1_CC1 #0 PCNT0_S1IN #0		LES_CH14 #0
18	PC15	ACMP1_CH7	TIM1_CC2 #0		LES_CH15 #0 DBG_SWO #1
19	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1 BOOT_TX
20	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1 GPIO_EM4WU3 BOOT_RX
21	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
22	IOVDD_5	Digital IO power supply 5.			
23	PE12		TIM1_CC2 #1	I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
24	PE13			I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 32). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0			PD7					Clock Management Unit, clock output number 0.
CMU_CLK1			PE12					Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0	PF0						Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1						Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15						Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL		PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0					Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1					Low Energy Timer LETIM0, output channel 1.
LEU0_RX		PB14		PF1	PA0			LEUART0 Receive input.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LEU0_TX		PB13		PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN			PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH2	PC0							Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1							Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1					PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2					PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0				PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14			PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
US1_CLK	PB7		PF0					USART1 clock input / output.
US1_CS	PB8		PF1					USART1 chip select input / output.
US1_RX	PC1		PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0		PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

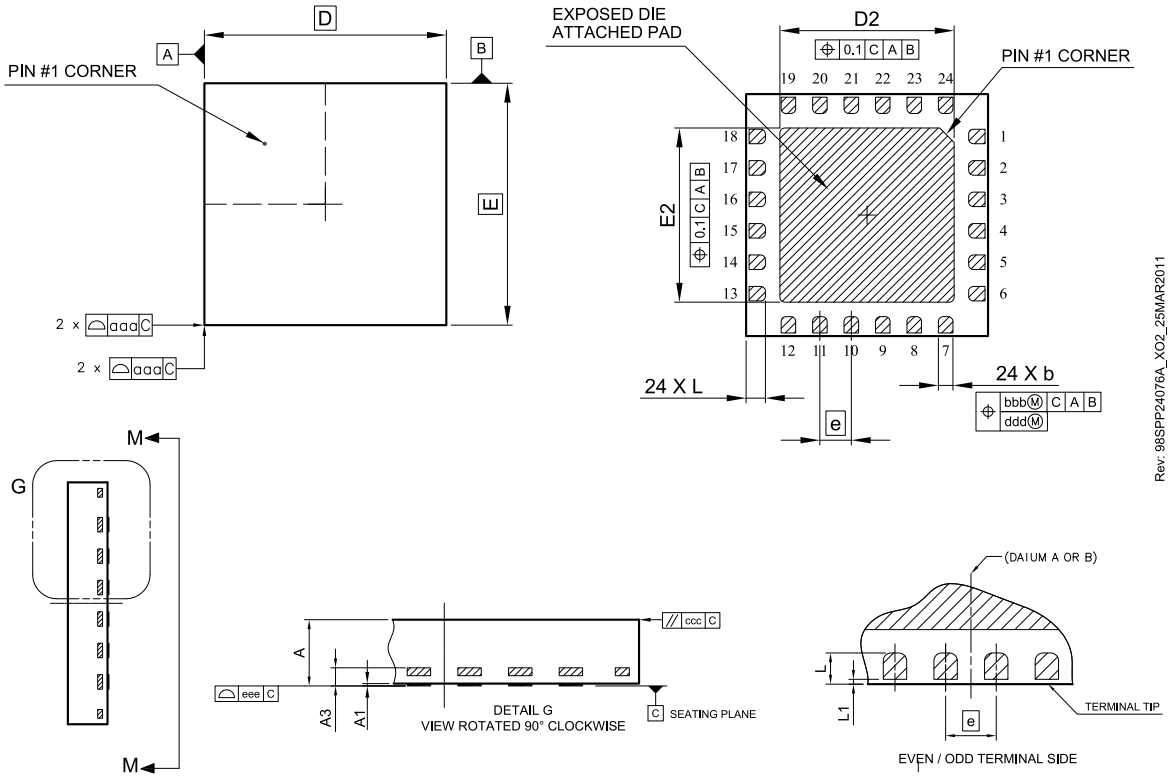
The specific GPIO pins available in *EFM32TG108* is shown in Table 4.3 (p. 33). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

4.4 QFN24 Package

Figure 4.2. QFN24



Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Table 4.4. QFN24 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	5.00 BSC	5.00 BSC	3.50	3.50	0.65 BSC	0.35	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	-		0.30			3.60	3.60		0.40						
Max	0.90	0.05		0.35			3.70	3.70		0.45	0.10					

The QFN24 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN24 PCB Land Pattern

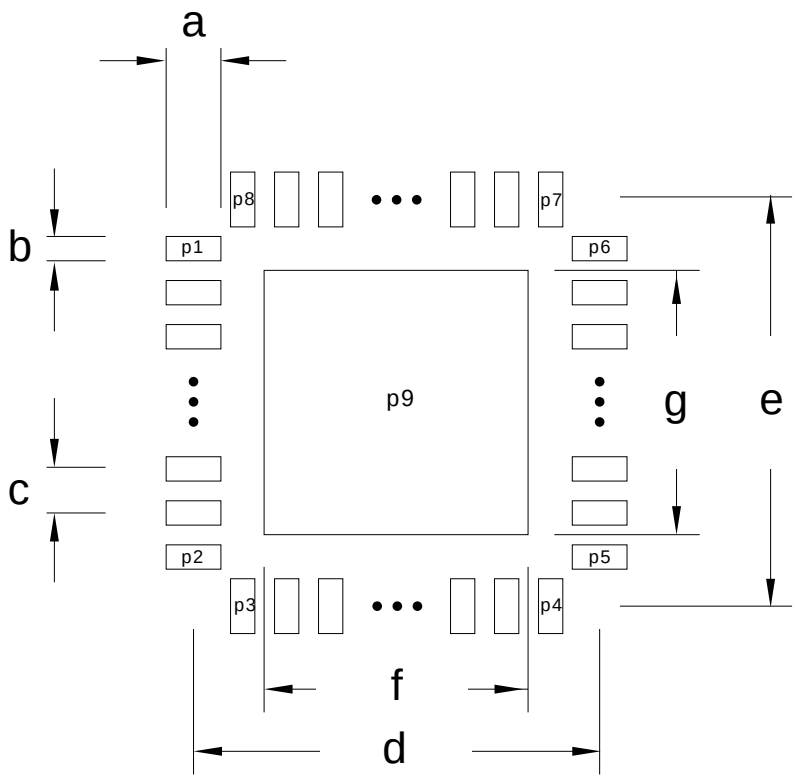


Table 5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.80	P1	1	P8	24
b	0.30	P2	6	P9	25
c	0.65	P3	7	-	-
d	5.00	P4	12	-	-
e	5.00	P5	13	-	-
f	3.60	P6	18	-	-
g	3.60	P7	19	-	-

Figure 5.2. QFN24 PCB Solder Mask

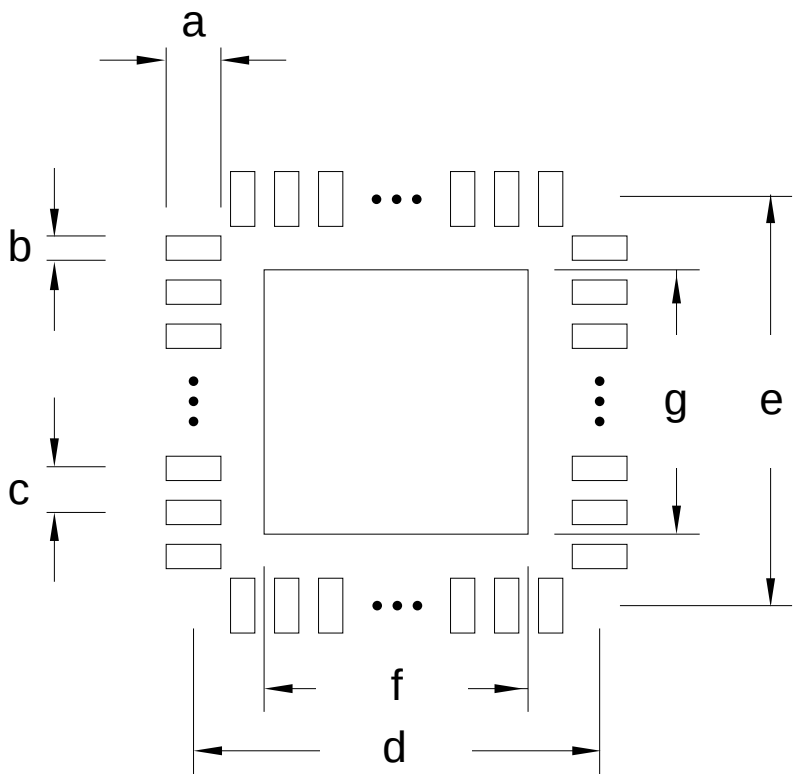


Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.92	e	5.00
b	0.42	f	3.72
c	0.65	g	3.72
d	5.00	-	-

Figure 5.3. QFN24 PCB Stencil Design

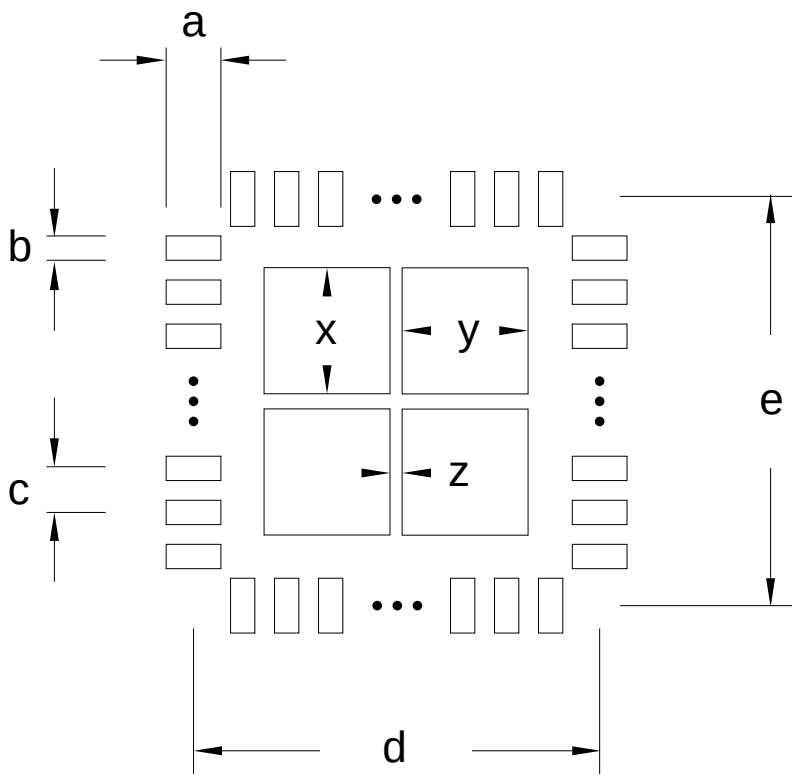


Table 5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.60	e	5.00
b	0.25	x	1.00
c	0.65	y	1.00
d	5.00	z	0.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 34) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

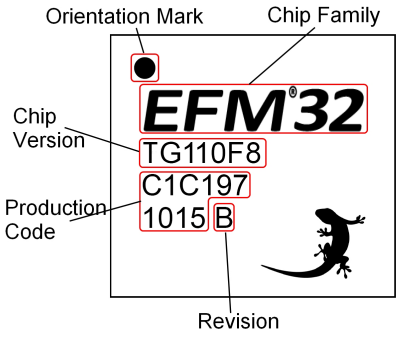
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions. Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 38) .

6.3 Errata

Please see the errata document for EFM32TG108 for description and resolution of device erratas. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

7 Revision History

7.1 Revision 1.40

March 6th, 2015

Updated Block Diagram.

Updated Energy Modes current consumption.

Updated Power Management section.

Updated LFRCO and HFRCO sections.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Corrected unit to kHz on LFRCO plots y-axis.

Updated ACMP section and the response time graph.

Updated VCMP section.

Updated Package dimensions table.

Updated Digital Peripherals section.

7.2 Revision 1.30

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ACMP data.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Document changed status from "Preliminary".

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.5 Revision 1.10

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Added GPIO_EM4WU3, GPIO_EM4WU4 and GPIO_EM4WU5 pins and removed GPIO_EM4WU1 in the Alternate functionality overview table.

Other minor corrections.

7.7 Revision 0.96

May 4th, 2012

Corrected PCB footprint figures and tables.

7.8 Revision 0.95

February 27th, 2012

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level and corrected Thermometer output gradient in Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added reference to errata document.

7.9 Revision 0.92

July 22nd, 2011

Updated current consumption numbers from latest device characterization data.

7.10 Revision 0.91

February 4th, 2011

Corrected max DAC sampling rate.

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

7.11 Revision 0.90

December 1st, 2010

New peripherals added to pinout, including LESENSE and OpAmps.

7.12 Revision 0.50

May 25th, 2010

Block diagram update.

7.13 Revision 0.40

March 26th, 2010

Initial preliminary release.

A Disclaimer and Trademarks

A.1 Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

A.2 Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

B Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
http://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

Table of Contents

1. Ordering Information 2
2. System Summary 3
    2.1. System Introduction 3
    2.2. Configuration Summary 6
    2.3. Memory Map 7
3. Electrical Characteristics 8
    3.1. Test Conditions 8
    3.2. Absolute Maximum Ratings 8
    3.3. General Operating Conditions 8
    3.4. Current Consumption 9
    3.5. Transition between Energy Modes 11
    3.6. Power Management 11
    3.7. Flash 12
    3.8. General Purpose Input Output 12
    3.9. Oscillators 20
    3.10. Analog Comparator (ACMP) 25
    3.11. Voltage Comparator (VCMP) 27
    3.12. I2C 27
    3.13. Digital Peripherals 28
4. Pinout and Package 30
    4.1. Pinout 30
    4.2. Alternate Functionality Pinout 31
    4.3. GPIO Pinout Overview 33
    4.4. QFN24 Package 34
5. PCB Layout and Soldering 35
    5.1. Recommended PCB Layout 35
    5.2. Soldering Information 37
6. Chip Marking, Revision and Errata 38
    6.1. Chip Marking 38
    6.2. Revision 38
    6.3. Errata 38
7. Revision History 39
    7.1. Revision 1.40 39
    7.2. Revision 1.30 39
    7.3. Revision 1.21 39
    7.4. Revision 1.20 40
    7.5. Revision 1.10 40
    7.6. Revision 1.00 40
    7.7. Revision 0.96 40
    7.8. Revision 0.95 40
    7.9. Revision 0.92 41
    7.10. Revision 0.91 41
    7.11. Revision 0.90 41
    7.12. Revision 0.50 41
    7.13. Revision 0.40 41
A. Disclaimer and Trademarks 42
    A.1. Disclaimer 42
    A.2. Trademark Information 42
B. Contact Information 43
    B.1. 43

List of Figures

2.1. Block Diagram 3
2.2. *EFM32TG108* Memory Map with largest RAM and Flash sizes 7
3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO. 10
3.2. EM3 current consumption. 10
3.3. EM4 current consumption. 10
3.4. Typical Low-Level Output Current, 2V Supply Voltage 14
3.5. Typical High-Level Output Current, 2V Supply Voltage 15
3.6. Typical Low-Level Output Current, 3V Supply Voltage 16
3.7. Typical High-Level Output Current, 3V Supply Voltage 17
3.8. Typical Low-Level Output Current, 3.8V Supply Voltage 18
3.9. Typical High-Level Output Current, 3.8V Supply Voltage 19
3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage 21
3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature 22
3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature 22
3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature 23
3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature 23
3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature 23
3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature 24
3.17. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1 26
4.1. *EFM32TG108* Pinout (top view, not to scale) 30
4.2. QFN24 34
5.1. QFN24 PCB Land Pattern 35
5.2. QFN24 PCB Solder Mask 36
5.3. QFN24 PCB Stencil Design 37
6.1. Example Chip Marking (top view) 38

List of Tables

1.1. Ordering Information 2
2.1. Configuration Summary 6
3.1. Absolute Maximum Ratings 8
3.2. General Operating Conditions 8
3.3. Current Consumption 9
3.4. Energy Modes Transitions 11
3.5. Power Management 11
3.6. Flash 12
3.7. GPIO 12
3.8. LFXO 20
3.9. HFXO 20
3.10. LFRCO 21
3.11. HFRCO 21
3.12. AUXHFRCO 24
3.13. ULFRCO 24
3.14. ACMP 25
3.15. VCMP 27
3.16. I2C Standard-mode (Sm) 27
3.17. I2C Fast-mode (Fm) 28
3.18. I2C Fast-mode Plus (Fm+) 28
3.19. Digital Peripherals 28
4.1. Device Pinout 30
4.2. Alternate functionality overview 32
4.3. GPIO Pinout 33
4.4. QFN24 (Dimensions in mm) 34
5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm) 35
5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm) 36
5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm) 37

List of Equations

3.1. Total ACMP Active Current 25
3.2. VCMP Trigger Level as a Function of Level Setting 27

silabs.com

ZERO
ARM Cortex-M0+
TINY
ARM Cortex-M3
GECKO
ARM Cortex-M3
LEOPARD
ARM Cortex-M3
GIANT
ARM Cortex-M3
WONDER
ARM Cortex-M4

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru